QUAD CHANNEL, 14 BIT, 125/105 MSPS ADC WITH SERIAL LVDS OUTPUTS

Check for Samples: ADS6445-EP, ADS6444-EP

FEATURES

- **Maximum Sample Rate: 125 MSPS**
- **14-Bit Resolution with No Missing Codes**
- **Simultaneous Sample and Hold**
- **3.5-dB Coarse Gain and up to 6-dB Programmable Fine Gain for SFDR/SNR Trade-Off**
- **Serialized LVDS Outputs with Programmable Internal Termination Option**
- **Supports Sine, LVCMOS, LVPECL, LVDS Clock Inputs and Amplitude Down to 400 mV_{PP}**
- **Internal Reference with External Reference Support**
- **No External Decoupling Required for References**
- **3.3-V Analog and Digital Supply**
- **64-pin QFN Package (9 mm × 9 mm)**
- **Feature Compatible Dual Channel Family**

APPLICATIONS

- **Base-Station IF Receivers**
- **Diversity Receivers**
- **Medical Imaging**
- **Test Equipment**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C to 125°C) Temperature Range**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

Table 1. ADS644X Quad Channel Family(1)

	125 MSPS	105 MSPS
ADS644X 14 Bit	ADS6445	ADS6444

(1) Product Preview for ADS6444

Table 2. Performance Summary

		ADS6445	ADS6444
SFDR, dBc	Fin = 10 MHz (0 dB gain)	87	91
	Fin = 170 MHz (3.5 dB gain)	79	83
SINAD, dBFS	Fin = 10 MHz (0 dB gain)	73.4	73.4
	Fin = 170 MHz (3.5 dB gain)	68.3	69.3
Power, per channel, mW		420	340

DESCRIPTION

The ADS6445/ADS6444 is a high performance 14 bit 125/105 MSPS quad channel A-D converter. Serial LVDS data outputs reduce the number of interface lines, resulting in a compact 64-pin QFN package (9 mm × 9 mm) that allows for high system integration density. The device includes 3.5 dB coarse gain option that can be used to improve SFDR performance with little degradation in SNR. In addition to the coarse gain, fine gain options also exist, programmable in 1 dB steps up to 6 dB.

The output interface is 2-wire, where each ADC data is serialized and output over two LVDS pairs. This makes it possible to halve the serial data rate (compared to a 1-wire interface) and restrict it to less than 1 Gbps easing receiver design. The ADS644X also includes the traditional 1-wire interface that can be used at lower sampling frequencies.

An internal phase lock loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock. The bit clock is used to serialize the 14 bit data from each channel. In addition to the serial data streams, the frame and bit clocks also are transmitted as LVDS outputs.

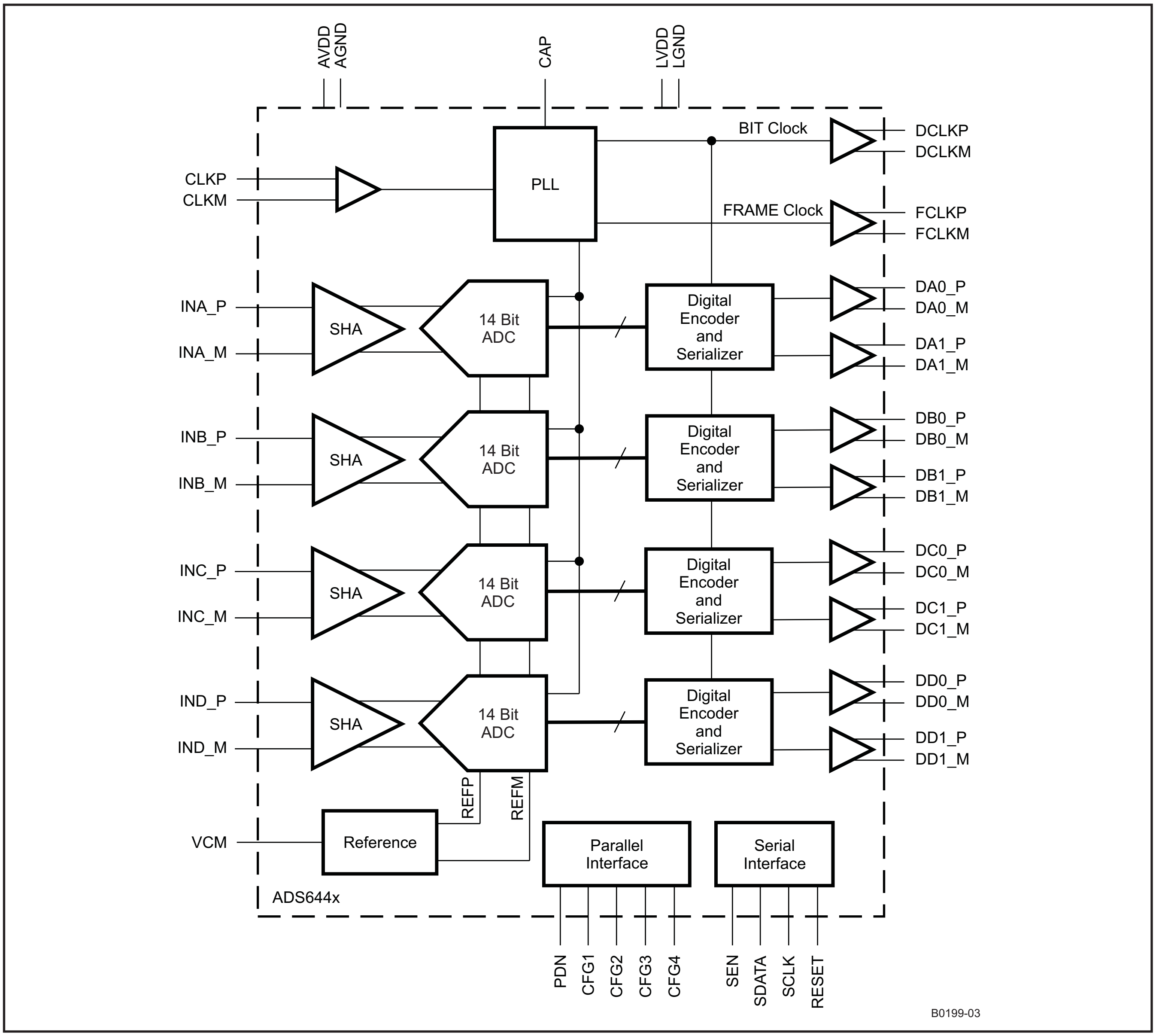
The LVDS output buffers have features such as programmable LVDS currents, current doubling modes and internal termination options. These can be used to widen eye openings and improve signal integrity, easing capture by the receiver.

The ADC channel outputs can be transmitted either as MSB or LSB first and 2s complement or straight binary.

The ADS644X has internal references, but also can support an external reference mode. The device is specified over –55°C to 125°C operating junction temperature range.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



ORDERING INFORMATION(1)

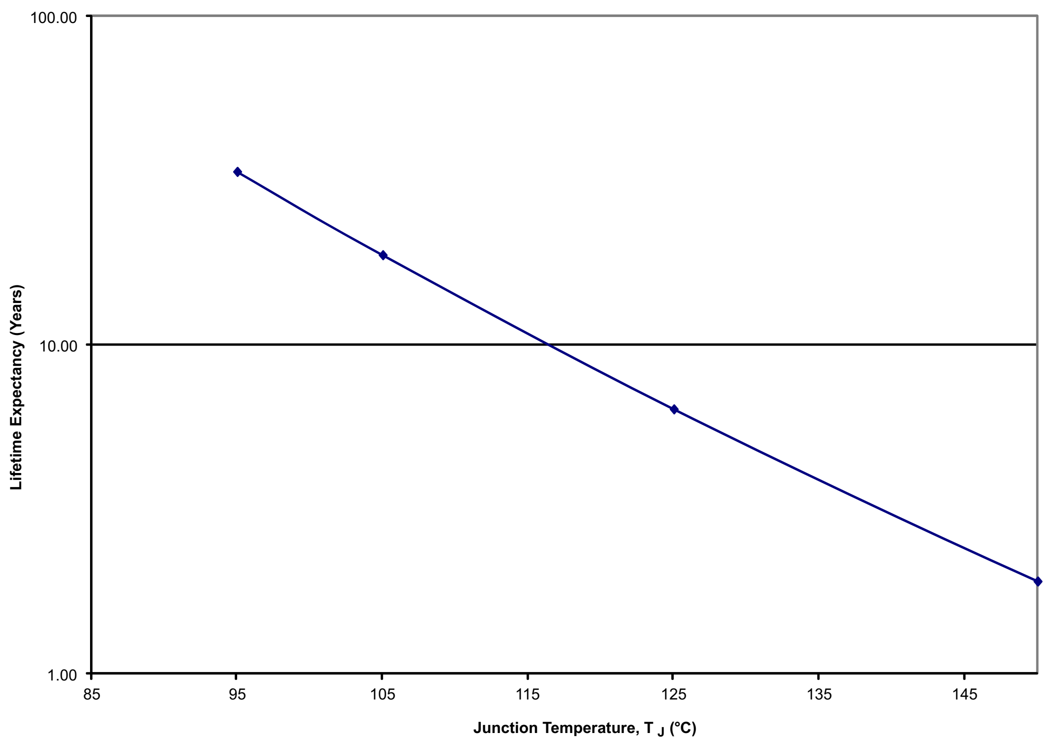
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(2)	SPECIFIED JUNCTION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY	VID NUMBER
ADS6445	QFN-64(3)	RGC	–55°C to 125°C	6445EP	ADS6445MRGCTEP	250, Tape/reel	V62/08628-01XE
ADS6444				6444EP	ADS6444MRGCTEP		V62/08628-02XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) For thermal pad size on the package, see the mechanical drawings at the end of this data sheet. θ_{JA} = 23.17 °C/W (0 LFM air flow), θ_{JC} = 22.1 °C/W when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in. x 3 in. PCB.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
AVDD	Supply voltage range	–0.3 to 3.9	V
LVDD	Supply voltage range	–0.3 to 3.9	V
	Voltage between AGND and DGND	–0.3 to 0.3	V
	Voltage between AVDD to LVDD	–0.3 to 3.3	V
	Voltage applied to external pin, VCM	–0.3 to 2.0	V
	Voltage applied to analog input pins	–0.3 V to minimum (3.6, AVDD + 0.3 V)	V
T_J	Operating junction temperature	150	°C
T_{stg}	Storage temperature range	–65 to 150	°C
	Lead temperature 1,6 mm (1/16") from the case for 10 seconds	220	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

Figure 1. Lifetime Expectancy Graph at Elevated Temperature

THERMAL INFORMATION

THERMAL METRIC[1]		ADS644x-EP RGC 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	23.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	7.7	
θ_{JB}	Junction-to-board thermal resistance[4]	3	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.1	
ψ_{JB}	Junction-to-board characterization parameter[6]	3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		3.0	3.3	3.6	V
LVDD	LVDS Buffer supply voltage		3.0	3.3	3.6	V
ANALOG INPUTS						
	Differential input voltage range			2		V_{pp}
	Input common-mode voltage			1.5±0.1		V
	Voltage applied on VCM in external reference mode		1.45	1.50	1.55	V
CLOCK INPUT						
	Input clock sample rate, F_{srated}	ADS6445	5		125	MSPS
		ADS6444	5		105	
	Input clock amplitude differential ($V_{CLKP} - V_{CLKM}$)	Sine wave, ac coupled	0.4	1.5		V_{pp}
		LVPECL, ac coupled		± 0.8		
		LVDS, ac coupled		± 0.35		
		LVCMOS, ac coupled		3.3		
	Input Clock duty cycle		35	50	65	%
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DGND	Without internal termination		5		pF
		With internal termination		10		
R_{LOAD}	Differential load resistance (external) between the LVDS output pairs			100		Ω

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full junction temperature range $T_{J,MIN}$ = –55°C to $T_{J,MAX}$ = 125°C, AVDD = LVDD = 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode (unless otherwise noted).

PARAMETER		ADS6445 F_s = 125 MSPS			ADS6444 F_s = 105 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			14			14		Bits
ANALOG INPUT								
	Differential input voltage range		2.0			2.0		V_{PP}
	Differential input capacitance		7			7		pF
	Analog input bandwidth		500			500		MHz
	Analog input common mode current (per input pin of each ADC)		155			130		µA
REFERENCE VOLTAGES								
VREFB	Internal reference bottom voltage		1.0			1.0		V
VREFT	Internal reference top voltage		2.0			2.0		V
ΔV_{REF}	Internal reference error (VREFT–VREFB)	0.985	1	1.015	0.985	1	1.015	V
VCM	Common mode output voltage		1.5			1.5		V
	VCM output current capability		±4			±4		mA
DC ACCURACY								
	No missing codes		Assured			Assured		
E_O	Offset error, across devices and across channels within a device	–15	±2	15	–15	±2	15	mV
	Offset error temperature coefficient, across devices and across channels within a device		0.05			0.05		mV/°C
	There are two sources of gain error - internal reference inaccuracy and channel gain error							
E_{GREF}	Gain error due to internal reference inaccuracy alone, (ΔV_{REF} /2.0) %	-0.75	0.1	0.75	-0.75	0.1	0.75	% FS
	Reference gain error temperature coefficient		0.0125			0.0125		Δ%/°C
E_{GCHAN}	Gain error of channel alone, across devices and across channels within a device		±0.3			±0.3		% FS
	Channel gain error temperature coefficient, across devices and across channels within a device		0.005			0.005		Δ%/°C
DNL	Differential nonlinearity, Fin = 50 MHz	–0.99	±0.6	2.0	–0.99	±0.6	2.0	LSB
INL	Integral nonlinearity, Fin = 50 MHz	-5	±3	5	-5	±3	5	LSB
PSRR	DC power supply rejection ratio		0.5			0.5		mV/V
POWER SUPPLY								
I_{CC}	Total supply current		502			410		mA
I_{AVDD}	Analog supply current		410			322		mA
I_{LVDD}	LVDS supply current		92			88		mA
	Total power		1.65	1.8		1.35	1.5	W
	Power down (with input clock stopped)		77	150		77	150	mW

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full junction temperature range $T_{J,MIN}$ = –55°C to $T_{J,MAX}$ = 125°C, AVDD = LVDD = 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode (unless otherwise noted).

PARAMETER	TEST CONDITIONS		ADS6445 F_s = 125 MSPS			ADS6444 F_s = 105 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR Signal to noise ratio	Fin = 10 MHz			73.7			73.8		dBFS
	Fin = 50 MHz		68.5	73.1			73.2		
	Fin = 70 MHz			72.7		69	73		
	Fin = 100 MHz			72.1			72.2		
	Fin = 170 MHz	0 dB gain		69.9			70.2		
		3.5 dB Coarse gain		69.4			69.7		
	Fin = 230 MHz	0 dB gain		68.7			68.8		
		3.5 dB Coarse gain		68.1			68.2		
SINAD Signal to noise and distortion ratio	Fin = 10 MHz			73.4			73.4		dBFS
	Fin = 50 MHz		67.75	72.3			71.7		
	Fin = 70 MHz			71.2		68.5	72		
	Fin = 100 MHz			71.8			72		
	Fin = 170 MHz	0 dB gain		67.9			69.8		
		3.5 dB Coarse gain		68.3			69.3		
	Fin = 230 MHz	0 dB gain		67.8			67.7		
		3.5 dB Coarse gain		67.9			67.6		
RMS Output noise	Inputs tied to common-mode			1.05			1.05		LSB
SFDR Spurious free dynamic range	Fin = 10 MHz			87			91		dBc
	Fin = 50 MHz		69	81			80		
	Fin = 70 MHz			78		74	81		
	Fin = 100 MHz			86			88		
	Fin = 170 MHz	0 dB gain		76			79		
		3.5 dB Coarse gain		79			83		
	Fin = 230 MHz	0 dB gain		77			77		
		3.5 dB Coarse gain		80			80		
HD2 Second harmonic	Fin = 10 MHz			93			94		dBc
	Fin = 50 MHz		69	87			88		
	Fin = 70 MHz			87		74	88		
	Fin = 100 MHz			89			90		
	Fin = 170 MHz	0 dB gain		83			84		
		3.5 dB Coarse gain		85			86		
	Fin = 230 MHz	0 dB gain		80			81		
		3.5 dB Coarse gain		82			83		
HD3 Third harmonic	Fin = 10 MHz			87			91		dBc
	Fin = 50 MHz		69	81			80		
	Fin = 70 MHz			78		74	81		
	Fin = 100 MHz			86			88		
	Fin = 170 MHz	0 dB gain		76			79		
		3.5 dB Coarse gain		79			83		
	Fin = 230 MHz	0 dB gain		77			77		
		3.5 dB Coarse gain		80			80		

ELECTRICAL CHARACTERISTICS (continued)

Typical values are at 25°C, min and max values are across the full junction temperature range $T_{J,MIN}$ = –55°C to $T_{J,MAX}$ = 125°C, AVDD = LVDD = 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode (unless otherwise noted).

PARAMETER	TEST CONDITIONS	ADS6445 F_s = 125 MSPS			ADS6444 F_s = 105 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Worst harmonic (other than HD2, HD3)	Fin = 10 MHz		91			91		dBc
	Fin = 50 MHz		87			87		
	Fin = 100 MHz		90			91		
	Fin = 170 MHz		88			88		
	Fin = 230 MHz		87			87		
THD Total harmonic distortion	Fin = 10 MHz		86			89.5		dBc
	Fin = 50 MHz	69	80			80		
	Fin = 100 MHz		84.5		72	79		
	Fin = 170 MHz		73.5			86		
	Fin = 230 MHz		74			77		
ENOB Effective number of bits	Fin = 50 MHz	10.95	11.7					Bits
	Fin = 70 MHz				11.3	11.7		
IMD 2-Tone inter-modulation distortion	F1= 46.09 MHz, F2 = 50.09 MHz		88			90		dBFS
	F1= 185.09 MHz, F2 = 190.09 MHz		86			88		
Cross-talk	Near channel Cross-talk signal frequency = 10 MHz		90			92		dBc
	Far channel Cross-talk signal frequency = 10 MHz		103			105		
Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine wave input		1			1		Clock cycles
AC PSRR Power supply rejection ratio	< 100 MHz signal, 100 mV_{PP} on AVDD supply		35			35		dBc

DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1 AVDD = LVDD = 3.3 V, I_O = 3.5 mA, R_{LOAD} = 100 Ω(1).

All LVDS specifications are characterized, but not tested at production.

PARAMETER	TEST CONDITIONS	ASD6445/ADS6444			UNIT
		MIN	TYP	MAX	
DIGITAL INPUTS					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current			10		μA
Low-level input current			10		μA
Input capacitance			4		pF
DIGITAL OUTPUTS					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage $\|V_{OD}\|$		250	350	450	mV
Output offset voltage V_{OS}	Common-mode voltage of OUTP and OUTM		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) I_O refers to the LVDS buffer current setting, R_{LOAD} is the external differential load resistance between the LVDS output pair.

TIMING SPECIFICATIONS(1)

Typical values are at 25°C, min and max values are across the full junction temperature range $T_{J,MIN}$ = –55°C to $T_{J,MAX}$ = 125°C, AVDD = LVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} clock amplitude, C_L = 5 pF (2), I_O = 3.5 mA, R_L = 100 Ω (3), no internal termination, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	ADS6445 F_s = 125 MSPS			ADS6444 F_s = 105 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_J	Aperture jitter	Uncertainty in the sampling instant		250			250		fs rms
INTERFACE: 2-wire, DDR bit clock, 14x serialization									
t_{su}	Data setup time(4) (5) (6)	From data cross-over to bit clock cross-over		0.55			0.65		ns
t_h	Data hold time(4) (5) (6)	From bit clock cross-over to data cross-over		0.58			0.7		ns
t_{pd_clk}	Clock propagation delay (6)	Input clock rising edge cross-over to frame clock rising edge cross-over		4.4			4.4		ns
	Bit clock cycle-cycle jitter (5)			350			350		ps pp
	Frame clock cycle-cycle jitter (5)			75			75		ps pp
The following specifications apply for 5 MSPS ≤ Fs ≤ 125 MSPS and all interface options.									
t_A	Aperture delay	Delay from input clock rising edge to the actual sampling instant		2			2		ns
	Aperture delay variation	Channel-channel within same device		±80			±80		ps
	ADC Latency (7)	Time for a sample to propagate to ADC outputs, see Figure 2		12			12		Clock cycles
	Wake up time	Time to valid data after coming out of global power down		100			100		µs
		Time to valid data after input clock is re-started		100			100		µs
		Time to valid data after coming out of channel standby		200			200		Clock cycles
t_{RISE}	Data rise time	From –100 mV to +100 mV		100			100		ps
t_{FALL}	Data fall time	From +100 mV to –100 mV		100			100		ps
t_{RISE}	Bit clock and frame clock rise time	From –100 mV to +100 mV		100			100		ps
t_{FALL}	Bit clock and frame clock fall time	From +100 mV to –100 mV		100			100		ps
	LVDS Bit clock duty cycle			50%			50%		
	LVDS Frame clock duty cycle			50%			50%		

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) C_L is the external single-ended load capacitance between each output pin and ground.
(3) I_o refers to the LVDS buffer current setting; R_L is the external differential load resistance between the LVDS output pair.
(4) Timing parameters are measured at the end of a 2 inch PCB trace (100 Ω characteristic impedance) terminated by R_L and C_L.
(5) Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Refer to Output Timings in application section for timings at lower sampling frequencies and other interface options.
(7) Note that the total latency = ADC latency + internal serializer latency. The serializer latency depends on the interface option selected as shown in Table 27.

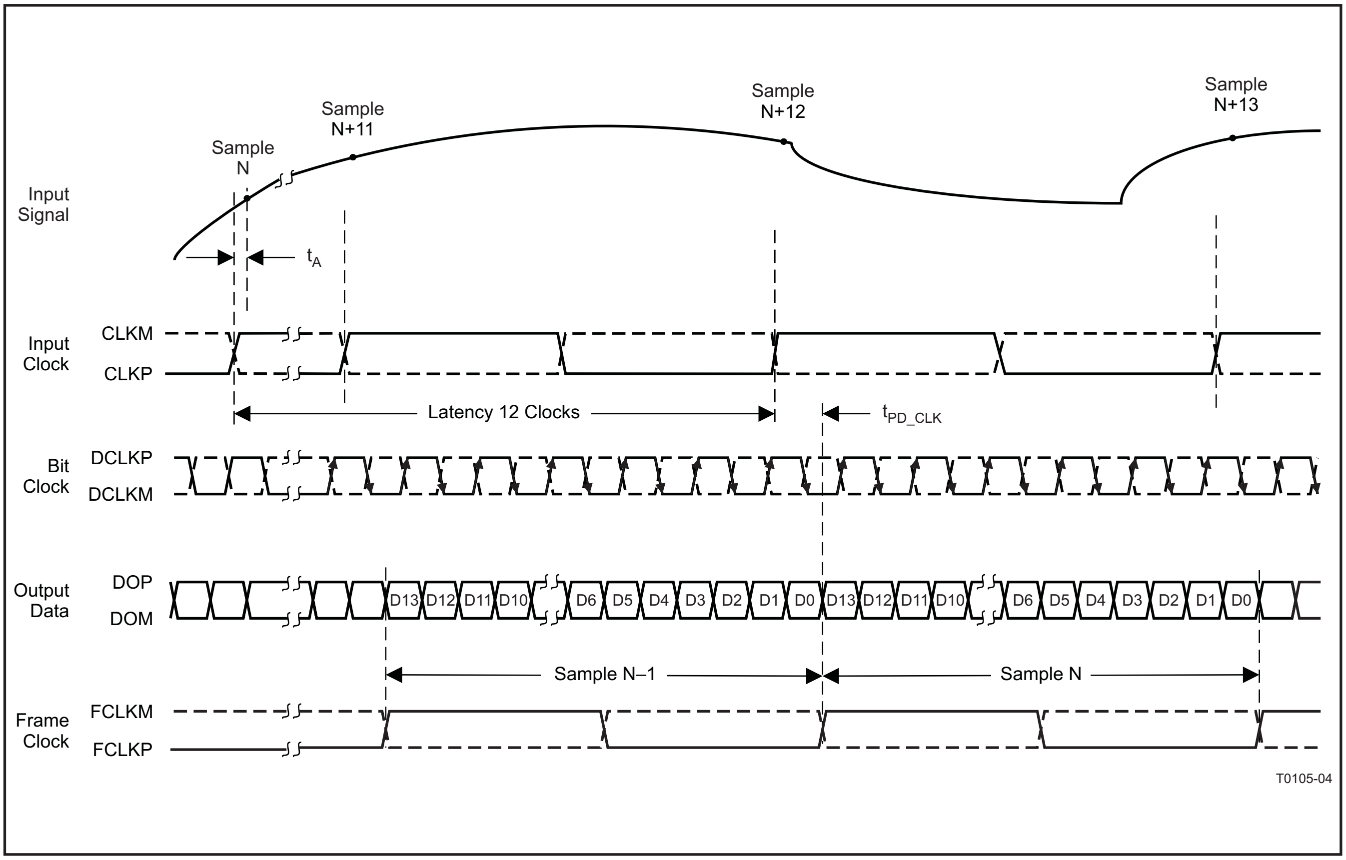


Figure 2. Latency

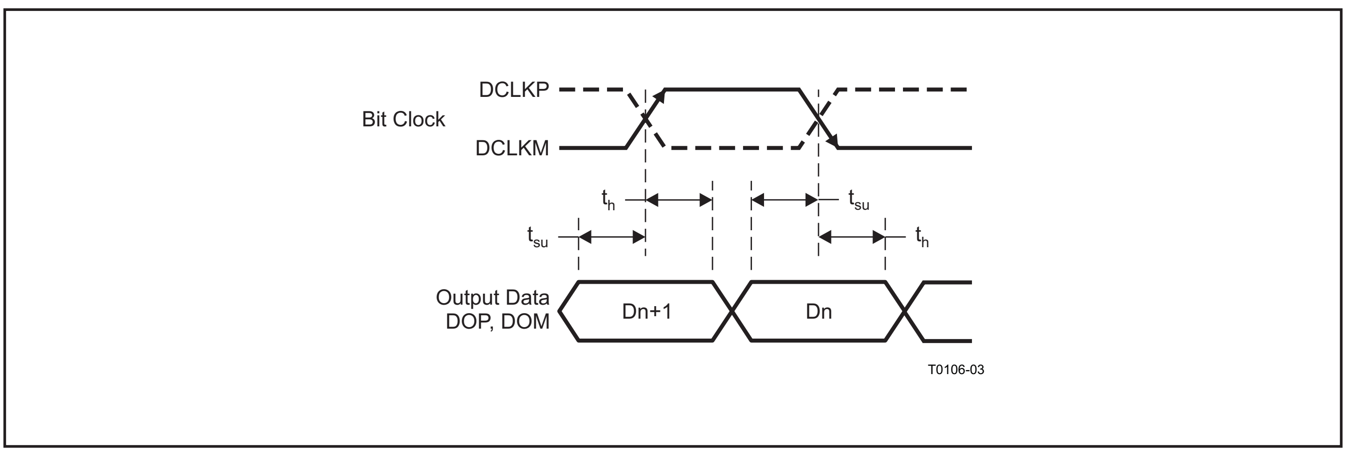


Figure 3. LVDS Timing

DEVICE PROGRAMMING MODES

ADS644X offers flexibility with several programmable features that are easily configured.

The device can be configured independently using either parallel interface control or serial interface programming.

In addition, the device supports a third configuration mode, where both the parallel interface and the serial control registers are used. In this mode, the priority between the parallel and serial interfaces is determined by a priority table (refer to Table 4). If this additional level of flexibility is not required, the user can select either the serial interface programming or the parallel interface control.

USING PARALLEL INTERFACE CONTROL ONLY

To control the device using parallel interface, keep RESET tied to ***high*** (LVDD). Pins CFG1, CFG2, CFG3, CFG4, PDN, SEN, SCLK, and SDATA are used to directly control certain functions of the ADC. After power-up, the device is automatically configured as per the parallel pin voltage settings (refer to Table 5 to Table 8) and no reset is required. In this mode, SEN, SCLK, and SDATA function as parallel interface control pins.

Frequently used functions are controlled in this mode—output data interface and format, power down modes, coarse gain and internal/external reference. The parallel pins can be configured using a simple resistor string as illustrated in Figure 4.

Table 3 has a description of the modes controlled by the parallel pins.

Table 3. Parallel Pin Definition

PIN	CONTROL FUNCTIONS
SEN	Coarse gain and internal/external reference.
SCLK, SDATA	Sync, deskew patterns and global power down.
PDN	Dedicated pin for global power down
CFG1	1-wire/2-wire and DDR/SDR bit clock
CFG2	14x/16x serialization and SDR bit clock capture edge
CFG3	Reserved function. **Tie CFG3 to Ground.**
CFG4	MSB/LSB first and data format.

USING SERIAL INTERFACE PROGRAMMING ONLY

In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers must first be reset to their default values either by applying a pulse on RESET pin or by a ***high*** setting on the <RST> bit (in register). After reset, the RESET pin must be kept **low.**

The serial interface section describes the register programming and register reset in more detail.

Because the parallel pins (CFG1-4 and PDN) are not used in this mode, they must be tied to ground. The register override bit <OVRD> - D10 in register 0x0D has to be set ***high*** to disable the control of parallel interface pins in this serial interface control ONLY mode.

USING BOTH THE SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CFG1-4 and PDN) also can be used to configure the device.

The parallel interface control pins CFG1 to CFG4 and PDN are available. After power-up, the device is automatically configured as per the parallel pin voltage settings (refer to Table 5 through Table 11) and no reset is required. A simple resistor string can be used as illustrated in Figure 4.

SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers must first be reset to their default values either by applying a pulse on RESET pin or by a ***high*** setting on the <RST> bit (in register). After reset, the RESET pin must be kept **low.**

The Serial Interface section describes the register programming and register reset in more detail.

Since some functions are controlled using both the parallel pins and serial registers, the priority between the two is determined by a priority table (refer to Table 4).

Table 4. Priority Between Parallel Pins and Serial Registers

PIN	FUNCTIONS SUPPORTED	PRIORITY
CFG1 to CFG4	As described in Table 8 through Table 11	Register bits can control the modes ***only*** if the register bit **<OVRD>** is ***high***. If **<OVRD>** bit is ***low***, then the control voltage on these parallel pins determines the function.
PDN	Global power down	Register bit **<PDN GLOBAL>** controls global power down ***only*** if PDN pin is ***low***. If PDN is ***high***, device is in global power down.
SEN	Serial interface enable	Coarse gain is controlled by register bit **<COARSE GAIN>** ***only*** if the **<OVRD>** bit is ***high***. Else, device has 0 dB coarse gain.
		Internal/external reference setting is determined by register bit **<REF>**.
SCLK, SDATA	Serial interface clock and serial interface data pins	Register bits **<PATTERNS>** control the sync and deskew output patterns.
		Power down is determined by bit **<PDN GLOBAL>**

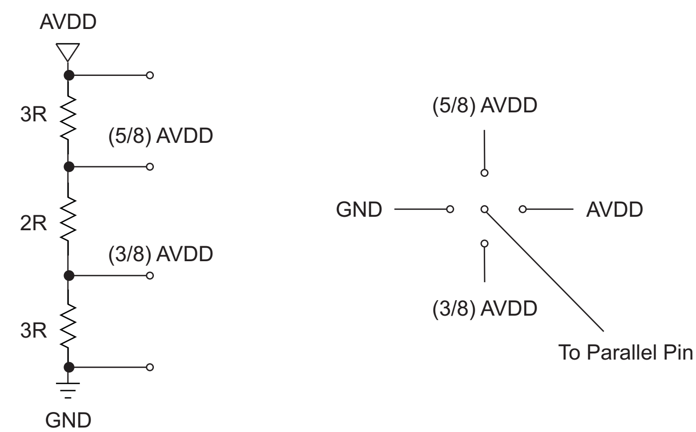


Figure 4. Simple Scheme to Configure Parallel Pins

DESCRIPTION OF PARALLEL PINS

Table 5. SCLK, SDATA Control Pins

SCLK	SDATA	DESCRIPTION
LOW	LOW	NORMAL conversion.
LOW	HIGH	SYNC – ADC outputs sync pattern on all channels. This pattern can be used by the receiver to align the deserialized data to the frame boundary. See Capture Test Patterns for details.
HIGH	LOW	POWER DOWN – Global power down, all channels of the ADC are powered down, including internal references, PLL and output buffers.
HIGH	HIGH	DESKEW – ADC outputs deskew pattern on all channels. This pattern can be used by the receiver to ensure deserializer uses the right clock edge. See Capture Test Patterns for details.

Table 6. SEN Control Pin

SEN	DESCRIPTION
0	External reference and 0 dB coarse gain (full-scale = 2 V_{PP})
(3/8)LVDD	External reference and 3.5 dB coarse gain (full-scale = 1.34 V_{PP})
(5/8)LVDD	Internal reference and 3.5 dB coarse gain (full-scale = 1.34 V_{PP})
LVDD	Internal reference and 0 dB coarse gain (full-scale = 2 V_{PP})

Independent of the programming mode used, after power-up the parallel pins PDN, CFG1 to CFG4 automatically configure the device as per the voltage applied (refer to Table 7 to Table 11).

Table 7. PDN Control Pin

PDN	DESCRIPTION
0	Normal operation
AVDD	Power down global

Table 8. CFG1 Control Pin

CFG1	DESCRIPTION
0	DDR Bit clock and 1-wire interface
(3/8)LVDD	Not used
(5/8)LVDD	SDR Bit clock and 2-wire interface
LVDD	DDR Bit clock and 2-wire interface

Table 9. CFG2 Control Pin

CFG2	DESCRIPTION
0	14x Serialization and capture at falling edge of bit clock (only in 2-wire SDR bit clock mode)
(3/8)LVDD	16x Serialization and capture at falling edge of bit clock (only in 2-wire SDR bit clock mode)
(5/8)LVDD	16x Serialization and capture at rising edge of bit clock (only in 2-wire SDR bit clock mode)
LVDD	14x Serialization and capture at rising edge of bit clock (only in 2-wire SDR bit clock mode)

Table 10. CFG3 Control Pin

CFG3	RESERVED - TIE TO GROUND

Table 11. CFG4 Control Pin

CFG4	DESCRIPTION
0	MSB First and 2s complement
(3/8)LVDD	MSB First and offset binary
(5/8)LVDD	LSB First and offset binary
LVDD	LSB First and 2s complement

SERIAL INTERFACE

The ADC has a serial interface formed by pins SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and RESET. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiple of 16 bit words within a single active SEN pulse. The interface can work with SCLK frequency from 20 MHz down to very low speeds (few hertz) and even with non-50% duty cycle SCLK.

The first 5 bits of the 16 bit word are the address of the register while the next 11 bits are the register data.

Register Reset

After power-up, the internal registers ***must*** be reset to their default values. This can be done in one of two ways:

1. Either by applying a high-going pulse on RESET (of width greater than 10 ns) **OR**
2. By applying software reset. Using the serial interface, set the **<RST>** bit in register 0x00 to ***high*** – this resets the registers to their default values and then self-resets the **<RST>** bit to LOW.

When RESET pin is not used, it must be tied to LOW.

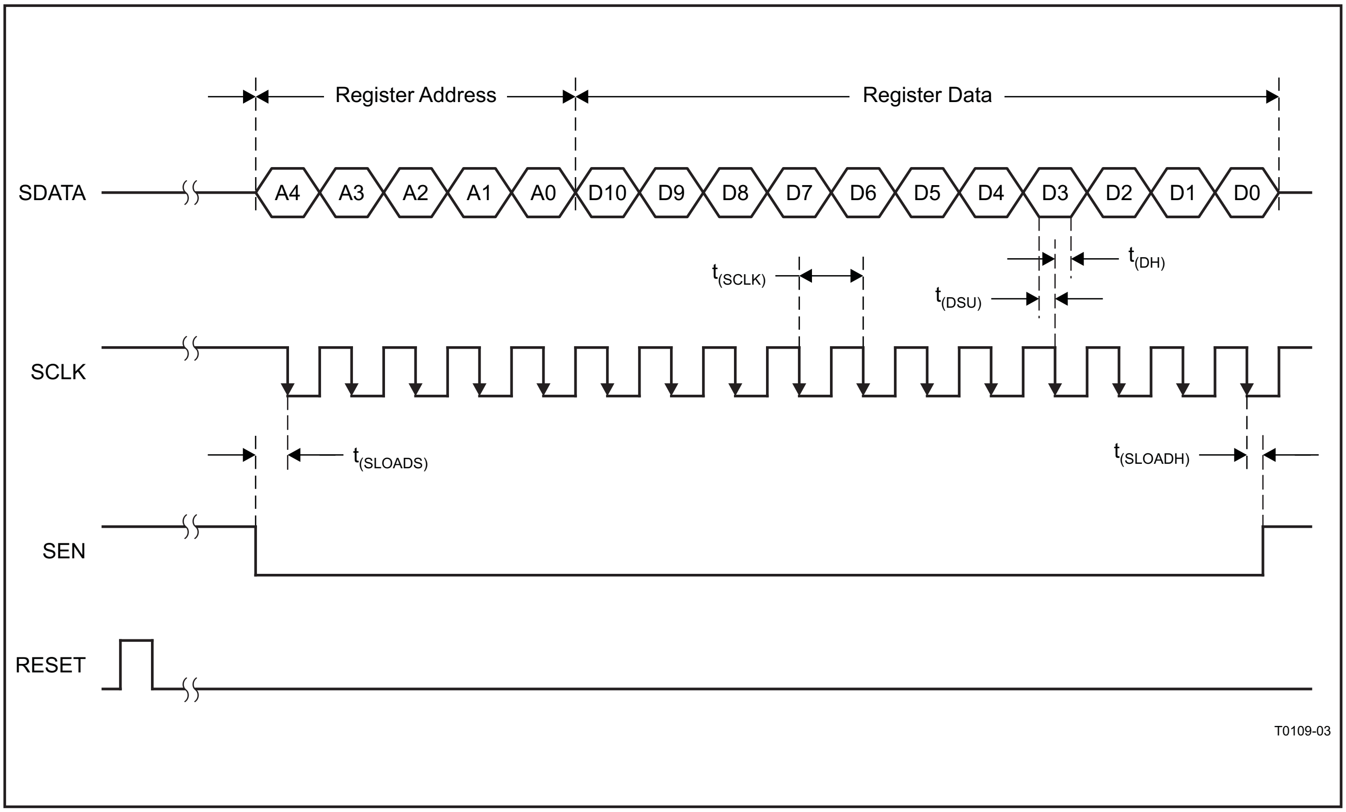


Figure 5. Serial Interface Timing

SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25°C, min and max values across the full junction temperature range $T_{J,MIN}$ = –55°C to $T_{J,MAX}$ = 125°C, AVDD = LVDD = 3.3 V, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK Frequency, f_{SCLK} = 1/t_{SCLK}	> DC		20	MHz
t_{SLOADS}	SEN to SCLK Setup time		25		ns
t_{SLOADH}	SCLK to SEN Hold time		25		ns
t_{DSU}	SDATA Setup time		25		ns
t_{DH}	SDATA Hold time		25		ns
	Time taken for register write to take effect after 16th SCLK falling edge		100		ns

RESET TIMING

Typical values at 25°C, min and max values across the full junction temperature range $T_{J,MIN}$ = –55°C to $T_{J,MAX}$ = 125°C, AVDD = LVDD = 3.3 V, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay time	Delay from power-up of AVDD and LVDD to RESET pulse active		5		ms
t_2	Reset pulse width	Pulse width of active RESET signal		10		ns
t_3	Register write delay time	Delay from RESET disable to SEN active		25		ns
t_{PO}	Power-up delay time	Delay from power-up of AVDD and LVDD to output stable		6.5		ms

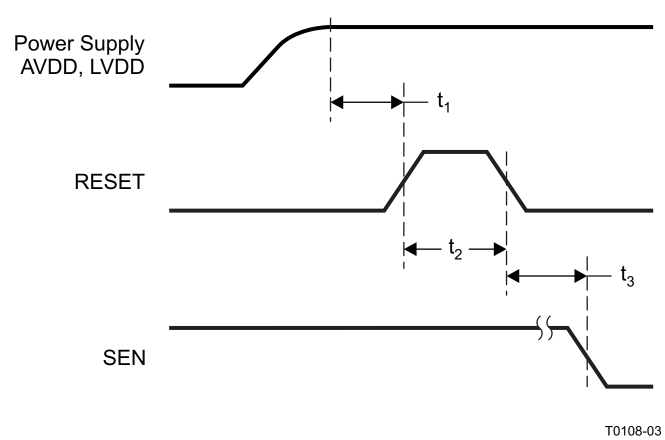


Figure 6. Reset Timing

SERIAL REGISTER MAP

Table 12. Summary of Functions Supported By Serial Interface

<table>
<tr><th>REGISTER ADDRESS</th><th colspan="11">REGISTER FUNCTIONS(1) (2)</th></tr>
<tr><th>A4 - A0</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>00</td><td>**<RST>** S/W RESET</td><td>0</td><td>0</td><td>0</td><td>0</td><td>**<REF>** INTERNAL OR EXTERNAL</td><td>**<PDN CHD>** POWER DOWN CH D</td><td>**<PDN CHC>** POWER DOWN CHC</td><td>**<PDN CHB>** POWER DOWN CH B</td><td>**<PDN CHA>** POWER DOWN CH A</td><td>**<PDN GLOBAL>** GLOBAL POWER DOWN</td></tr>
<tr><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="5">**<CLKIN GAIN>** INPUT CLOCK BUFFER GAIN CONTROL</td><td>0</td><td>0</td></tr>
<tr><td>0A</td><td>0</td><td>**<DF>** DATA FORMAT 2S COMP OR STRAIGHT BINARY</td><td>0</td><td colspan="3">**<PATTERNS>** TEST PATTERNS</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0B</td><td colspan="11">**<CUSTOM A>** CUSTOM PATTERN (LOWER 11 BITS)</td></tr>
<tr><td>0C</td><td colspan="3">**<FINE GAIN>** FINE GAIN CONTROL (1 dB to 6 dB)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">**<CUSTOM B>** CUSTOM PATTERN (UPPER 3 BITS)</td></tr>
<tr><td>0D</td><td>**<OVRD>** OVERRIDE BIT</td><td>0</td><td>0</td><td>BYTE-WISE OR BIT-WISE</td><td>MSB OR LSB FIRST</td><td>**<COARSE GAIN>** COURSE GAIN ENABLE</td><td>FALLING OR RISING BIT CLOCK CAPTURE EDGE</td><td>0</td><td>14 BIT OR 16 BIT SERIALIZE</td><td>DDR OR SDR BIT CLOCK</td><td>1-WIRE OR 2-WIRE INTERFACE</td></tr>
<tr><td>10</td><td colspan="5">**<TERM CLK>** LVDS INTERNAL TERMINATION BIT AND WORD CLOCKS</td><td colspan="4">**<LVDS CURR>** LVDS CURRENT SETTINGS</td><td colspan="2">**<CURR DOUBLE>** LVDS CURRENT DOUBLE</td></tr>
<tr><td>11</td><td colspan="2">WORD-WISE CONTROL</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="5">**<TERM DATA>** LVDS INTERNAL TERMINATION - DATA OUTPUTS</td></tr>
</table>

(1) The unused bits in each register (shown by blank cells in above table) must be programmed as 0.
(2) Multiple functions in a register can be programmed in a single write operation.

DESCRIPTION OF SERIAL REGISTERS

Table 13. Serial Register A

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	**<RST>** S/W RESET	0	0	0	0	**<REF>** INTERNAL OR EXTERNAL	**<PDN CHD>** POWER DOWN CH D	**<PDN CHC>** POWER DOWN CHC	**<PDN CHB>** POWER DOWN CH B	**<PDN CHA>** POWER DOWN CH A	**<PDN>** GLOBAL POWER DOWN

D0 - D4	**Power down modes**
D0	**<PDN GLOBAL>**
0	Normal operation
1	Global power down, including all channels ADCs, internal references, internal PLL and output buffers
D1	**<PDN CHA>**
0	CH A Powered up
1	CH A ADC Powered down
D2	**<PDN CHB>**
0	CH B Powered up
1	CH B ADC Powered down
D3	**<PDN CHC>**
0	CH C Powered up
1	CH C ADC Powered down
D4	**<PDN CHD>**
0	CH D Powered up
1	CH D ADC Powered down
D5	**<REF>** Reference
0	Internal reference enabled
1	External reference enabled
D10	**<RST>**
1	Software reset applied – resets all internal registers and self-clears to 0

Table 14. Serial Register B

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
04	0	0	0	0	**<CLKIN GAIN>** INPUT CLOCK BUFFER GAIN CONTROL					0	0

D6 - D2	**<CLKIN GAIN>** Input clock buffer gain control
11000	Gain 0, minimum gain
00000	Gain 1, default gain after reset
01100	Gain 2
01010	Gain 3
01001	Gain 4
01000	Gain 5, maximum gain

Table 15. Serial Register C

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	0	**<DF>** DATA DORMAT 2S COMP OR STRAIGHT BINARY	0	**<PATTERNS>** TEST PATTERNS			0	0	0	0	0

D7 - D5	**<PATTERNS>** Capture test patterns
000	Normal ADC operation
001	Output all zeros
010	Output all ones
011	Output toggle pattern
100	Unused
101	Output custom pattern (contents of CUSTOM pattern registers 0x0B and 0x0C)
110	Output DESKEW pattern (serial stream of 1010..)
111	Output SYNC pattern

D9	**<DF>** Data format selection
0	2s Complement format
1	Straight binary format

Table 16. Serial Register D

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0B	<CUSTOM A> CUSTOM PATTERN (LOWER 11 BITS)										

D10 - D0 **<CUSTOM A>** Lower 11 bits of custom pattern <D10>…<D0>

Table 17. Serial Register E

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0C	<FINE GAIN> FINE GAIN CONTROL (1 dB to 6 dB)			0	0	0	0	0	<CUSTOM B> CUSTOM PATTERN (UPPER 3 BITS)		

D4 - D0 **<CUSTOM B>** Upper 3 bits of custom pattern <D13>…<D11>

D10-D8	**<FINE GAIN>** Fine gain control
000	0 dB Gain (full-scale range = 2.00 V_{PP})
001	1 dB Gain (full-scale range = 1.78 V_{PP})
010	2 dB Gain (full-scale range = 1.59 V_{PP})
011	3 dB Gain (full-scale range = 1.42 V_{PP})
100	4 dB Gain (full-scale range = 1.26 V_{PP})
101	5 dB Gain (full-scale range = 1.12 V_{PP})
110	6 dB Gain (full-scale range = 1.00 V_{PP})

Table 18. Serial Register F

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0D	<OVRD> OVER-RIDE BITE	0	0	BYTE-WISE OR BIT-WISE	MSB OR LSB FIRST	<COARSE GAIN> COURSE GAIN ENABLE	FALLING OR RISING BIT CLOCK CAPTURE EDGE	0	14 BIT OR 16 BIT SERIALIZE	DDR OR SDR BIT CLOCK	1-WIRE OR 2- WIRE INTERFACE

D0	**Interface selection**
0	1-Wire interface
1	2-Wire interface

D1	**Bit clock selection** (only in 2-wire interface)
0	DDR Bit clock
1	SDR Bit clock

D2	**Serialization factor selection**
0	14X Serialization
1	16X Serialization

D4	**Bit clock capture edge** (only when SDR bit clock is selected, D1 = 1)
0	Capture data with falling edge of bit clock
1	Capture data with rising edge of bit clock

D5	**<COARSE GAIN> Coarse gain control**
0	0 dB Coarse gain (full-scale range = 2.0 V_{PP})

1	3.5 dB Coarse gain (full-scale range = 1.34 V_{PP})
D6	**MSB or LSB First selection**
0	MSB First
1	LSB First
D7	**Byte/bit wise outputs** (only when 2-wire is selected)
0	Byte wise
1	Bit wise
D10	**<OVRD>** Over-ride bit. All the functions in register 0x0D also can be controlled using the parallel control pins. By setting bit <OVRD> = 1, the contents of register 0x0D will over-ride the settings of the parallel pins.
0	Disable over-ride
1	Enable over-ride

Table 19. Serial Register G

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
10	<TERM CLK> LVDS INTERNAL TERMINATION BIT AND WORD CLOCKS					<LVDS CURR> LVDS CURRENT SETTINGS				<LVDS DOUBLE> LVDS CURRENT DOUBLE	

D0	**<CURR DOUBLE>** LVDS current double for data outputs
0	Nominal LVDS current, as set by <D5…D2>
1	Double the nominal value
D1	**<CURR DOUBLE>** LVDS current double for bit and word clock outputs
0	Nominal LVDS current, as set by <D5…D2>
1	Double the nominal value
D3-D2	**<LVDS CURR>** LVDS current setting for data outputs
00	3.5 mA
01	4 mA
10	2.5 mA
11	3 mA
D5-D4	**<LVDS CURR>** LVDS current setting for bit and word clock outputs
00	3.5 mA
01	4 mA
10	2.5 mA
11	3 mA
D10-D6	**<TERM CLK>** LVDS internal termination for bit and word clock outputs
00000	No internal termination
00001	166 Ω
00010	200 Ω
00100	250 Ω
01000	333 Ω

10000	500 Ω
	Any combination of above bits also can be programmed, resulting in a parallel combination of the selected values. For example, 00101 is the parallel combination of 166‖250 = 100 Ω
00101	100 Ω

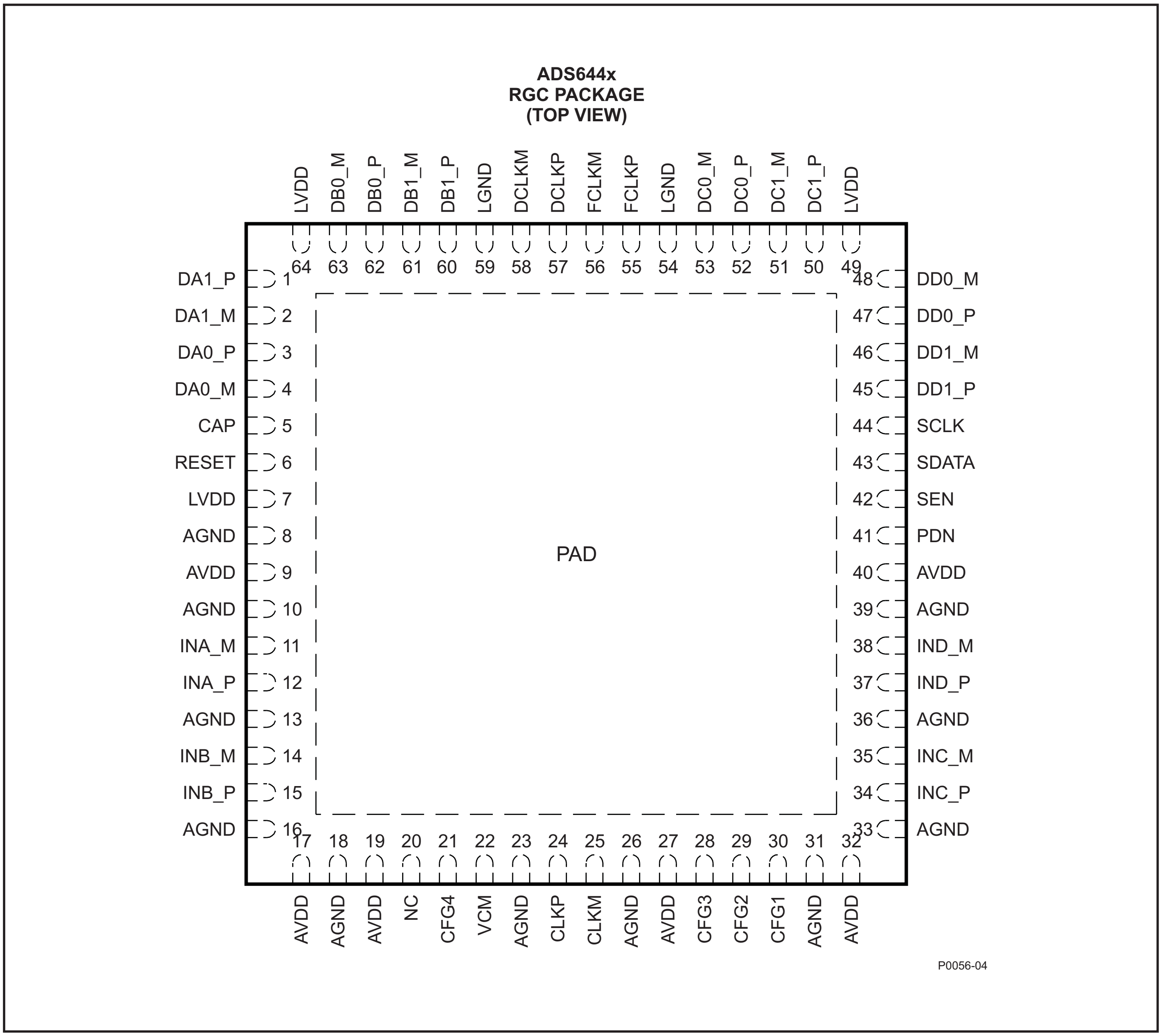
Table 20. Serial Register H

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
11	WORD-WISE CONTROL		0	0	0	0	<TERM DATA> LVDS INTERNAL TERMINATION - DATA OUTPUTS				

D4-D0	**<TERM DATA>** LVDS internal termination for data outputs
00000	No internal termination
00001	166 Ω
00010	200 Ω
00100	250 Ω
01000	333 Ω
10000	500 Ω
	Any combination of above bits can also be programmed, resulting in a parallel combination of the selected values. For example, 00101 is the parallel combination of 166‖250 = 100 Ω
00101	100 Ω

D10-D9	**Only when 2-wire interface is selected**
00	Byte-wise or bit-wise output, 1x frame clock
11	Word-wise output enabled, 0.5x frame clock
01,10	Do not use

PIN CONFIGURATION (2-WIRE INTERFACE)



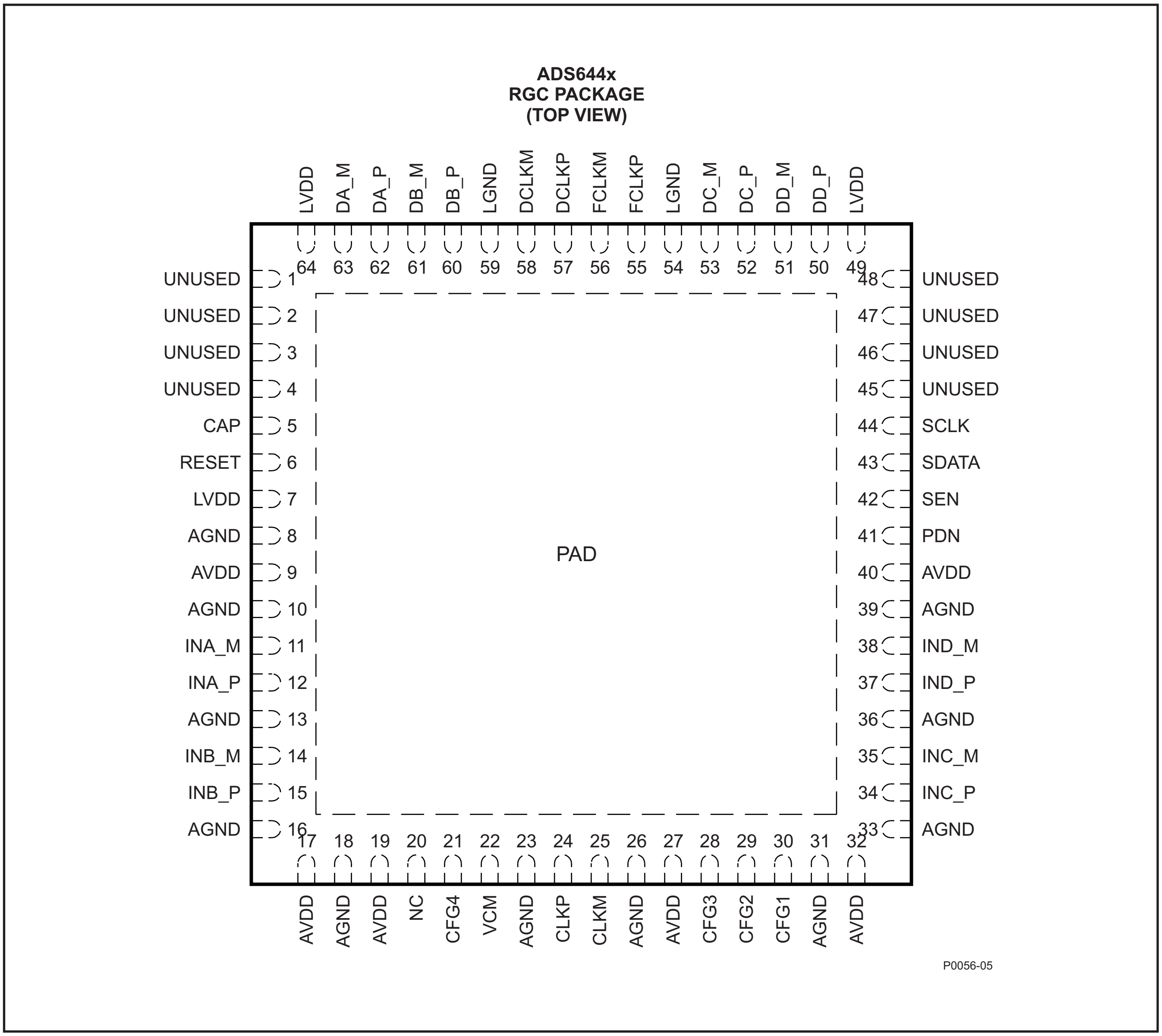
PIN ASSIGNMENTS (2-WIRE INTERFACE)

PINS		I/O	NO. OF PINS	DESCRIPTION
NAME	NO.			
SUPPLY AND GROUND PINS				
AVDD	9, 17, 19, 27, 32, 40		6	Analog power supply
AGND	8, 10, 13, 16, 18, 23, 26, 31, 33, 36, 39		11	Analog ground
LVDD	7, 49, 64		3	Digital power supply
LGND	54, 59		2	Digital ground
INPUT PINS				
CLKP, CLKM	24, 25	I	2	Differential input clock pair
INA_P, INA_M	12, 11	I	2	Differential input signal pair, channel A. If unused, the pins should be tied to VCM. Do not float.

PIN ASSIGNMENTS (2-WIRE INTERFACE) (continued)

PINS		I/O	NO. OF PINS	DESCRIPTION
NAME	NO.			
INB_P, INB_M	15, 14	I	2	Differential input signal pair, channel B. If unused, the pins should be tied to VCM. Do not float.
INC_P, INC_M	34, 35	I	2	Differential input signal pair, channel C If unused, the pins should be tied to VCM. Do not float.
IND_P, IND_M	37, 38	I	2	Differential input signal pair, channel D. If unused, the pins should be tied to VCM. Do not float.
CAP	5		1	Connect 2-nF capacitor from pin to ground
SCLK	44	I	1	This pin functions as serial interface clock input when RESET is low. When RESET is ***high***, it controls DESKEW, SYNC and global POWER DOWN modes (along with SDATA). Refer to Table 5 for description. This pin has an internal pull-down resistor.
SDATA	43	I	1	This pin functions as serial interface data input when RESET is low. When RESET is ***high***, it controls DESKEW, SYNC and global POWER DOWN modes (along with SCLK). Refer to Table 5 for description. This pin has an internal pull-down resistor.
SEN	42	I	1	This pin functions as serial interface enable input when RESET is low. When RESET is ***high***, it controls coarse gain and internal/external reference modes. Refer to Table 6 for description. This pin has an internal pull-up resistor.
RESET	6	I	1	Serial interface reset input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to the Serial Interface section. In parallel interface mode, tie RESET permanently ***high***. (SCLK, SDATA and SEN function as parallel control pins in this mode). The pin has an internal pull-down resistor to ground.
PDN	41	I	1	Global power down control pin.
CFG1	30	I	1	Parallel input pin. It controls 1-wire or 2-wire interface and DDR or SDR bit clock selection. Refer to Table 8 for description. Tie to AVDD for 2-wire interface with DDR bit clock.
CFG2	29	I	1	Parallel input pin. It controls 14x or 16x serialization and SDR bit clock capture edge. Refer to Table 9 for description. For 14x serialization with DDR bit clock, tie to ground or AVDD.
CFG3	28	I	1	RESERVED pin - **Tie to ground.**
CFG4	21	I	1	Parallel input pin. It controls data format and MSB or LSB first modes. Refer to Table 11 for description.
VCM	22	I/O	1	Internal reference mode – common-mode voltage output External reference mode – reference input. The voltage forced on this pin sets the internal reference.
OUTPUT PINS				
DA0_P,DA0_M	3, 4	O	2	Channel A differential LVDS data output pair, wire 0
DA1_P,DA1_M	1, 2	O	2	Channel A differential LVDS data output pair, wire 1
DB0_P,DB0_M	62, 63	O	2	Channel B differential LVDS data output pair, wire 0
DB1_P,DB1_M	60, 61	O	2	Channel B differential LVDS data output pair, wire 1
DC0_P,DC0_M	52, 53	O	2	Channel C differential LVDS data output pair, wire 0
DC1_P,DC1_M	50, 51	O	2	Channel C differential LVDS data output pair, wire 1
DD0_P,DD0_M	47, 48	O	2	Channel D differential LVDS data output pair, wire 0
DD1_P,DD1_M	45, 46	O	2	Channel D differential LVDS data output pair, wire 1
DCLKP,DCLKM	57, 58	O	2	Differential bit clock output pair
FCLKP,FCLKM	55, 56	O	2	Differential frame clock output pair
NC	20		1	Do Not Connect
PAD	0		1	Connect to ground plane using multiple vias. Refer to Board Design Considerations section.

PIN CONFIGURATION (1-WIRE INTERFACE)



PIN ASSIGNMENTS (1-WIRE INTERFACE)

PINS		I/O	NO. OF PINS	DESCRIPTION
NAME	NO.			
SUPPLY AND GROUND PINS				
AVDD	9, 17, 19, 27, 32, 40		6	Analog power supply
AGND	8, 10, 13, 16, 18, 23, 26, 31, 33, 36, 39		11	Analog ground
LVDD	7, 49, 64		3	Digital power supply
LGND	54, 59		2	Digital ground
INPUT PINS				
CLKP, CLKM	24, 25	I	2	Differential input clock pair
INA_P, INA_M	12, 11	I	2	Differential input signal pair, channel A. If unused, the pins should be tied to VCM. Do not float.
INB_P, INB_M	15, 14	I	2	Differential input signal pair, channel B. If unused, the pins should be tied to VCM. Do not float.

PIN ASSIGNMENTS (1-WIRE INTERFACE) (continued)

PINS		I/O	NO. OF PINS	DESCRIPTION
NAME	**NO.**			
INC_P, INC_M	34, 35	I	2	Differential input signal pair, channel C. If unused, the pins should be tied to VCM. Do not float.
IND_P, IND_M	37, 38	I	2	Differential input signal pair, channel D. If unused, the pins should be tied to VCM. Do not float.
CAP	5		1	Connect 2 nF capacitance from pin to ground
SCLK	44	I	1	This pin functions as serial interface clock input when RESET is ***low***. When RESET is ***high***, it controls DESKEW, SYNC and global POWER DOWN modes (along with SDATA). Refer to Table 5 for description. This pin has an internal pull-down resistor.
SDATA	43	I	1	This pin functions as serial interface data input when RESET is ***low***. When RESET is ***high***, it controls DESKEW, SYNC and global POWER DOWN modes (along with SCLK). Refer to Table 5 for description. This pin has an internal pull-down resistor.
SEN	42	I	1	This pin functions as serial interface enable input when RESET is ***low***. When RESET is ***high***, it controls coarse gain and internal/external reference modes. Refer to Table 6 for description. This pin has an internal pull-up resistor.
RESET	6	I	1	Serial interface reset input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to the Serial Interface section. In parallel interface mode, tie RESET permanently ***high***. (SCLK, SDATA and SEN function as parallel control pins in this mode). The pin has an internal pull-down resistor to ground.
PDN	41	I	1	Global power down control pin.
CFG1	30	I	1	Parallel input pin. It controls 1-wire or 2-wire interface and DDR or SDR bit clock selection. Refer to Table 8 for description. Tie to ground for 1-wire interface with DDR bit clock.
CFG2	29	I	1	Parallel input pin. It controls 14x or 16x serialization and SDR bit clock capture edge. Refer to Table 9 for description. For 14x serialization with DDR bit clock, tie to ground or AVDD.
CFG3	28	I	1	RESERVED pin - **Tie to ground**.
CFG4	21	I	1	Parallel input pin. It controls data format and MSB or LSB first modes. Refer to Table 11 for description.
VCM	22	I/O	1	Internal reference mode – common-mode voltage output External reference mode – reference input. The voltage forced on this pin sets the internal reference.
OUTPUT PINS				
DA_P,DA_M	62, 63	O	2	Channel A differential LVDS data output pair
DB_P,DB_M	60, 61	O	2	Channel B differential LVDS data output pair
DC_P,DC_M	52, 53	O	2	Channel C differential LVDS data output pair
DD_P,DD_M	50, 51	O	2	Channel D differential LVDS data output pair
DCLKP,DCLKM	57, 58	O	2	Differential bit clock output pair
FCLKP,FCLKM	55, 56	O	2	Differential frame clock output pair
UNUSED	1–4, 45–48		8	These pins are unused in the 1-wire interface. Do not connect
NC	20		1	Do not connect
PAD	0		1	Connect to ground plane using multiple vias. Refer to Board Design Considerations in the application section.

TYPICAL CHARACTERISTICS

All plots are at 25°C, AVDD = LVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain (unless otherwise noted)

ADS6445 (F_{srated} = 125 MSPS)

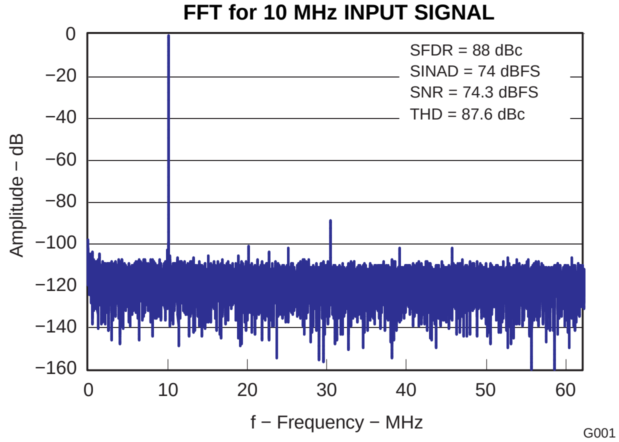


Figure 7.

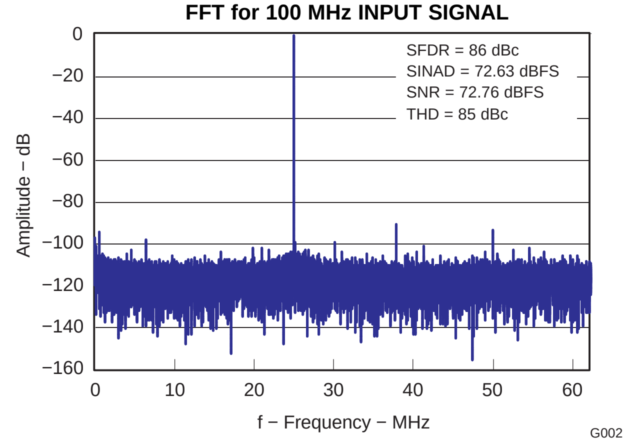


Figure 8.

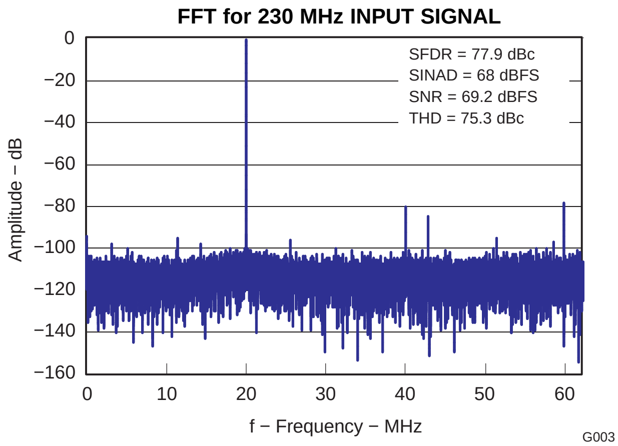
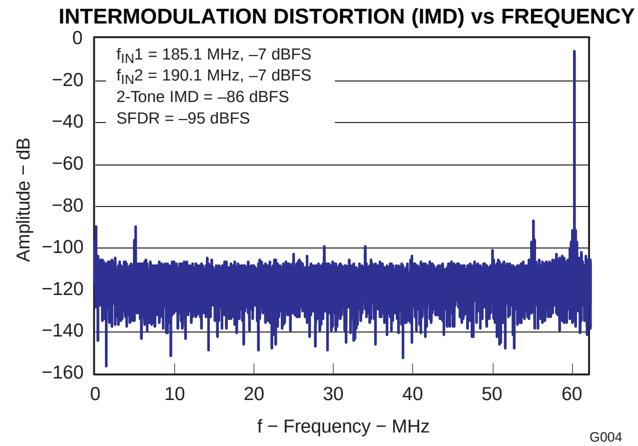


Figure 9.



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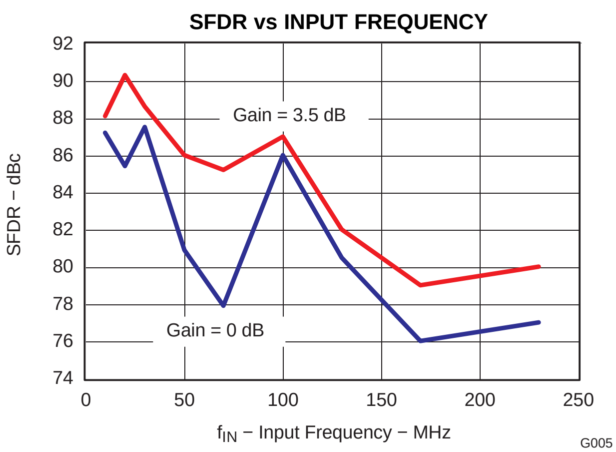


Figure 11.

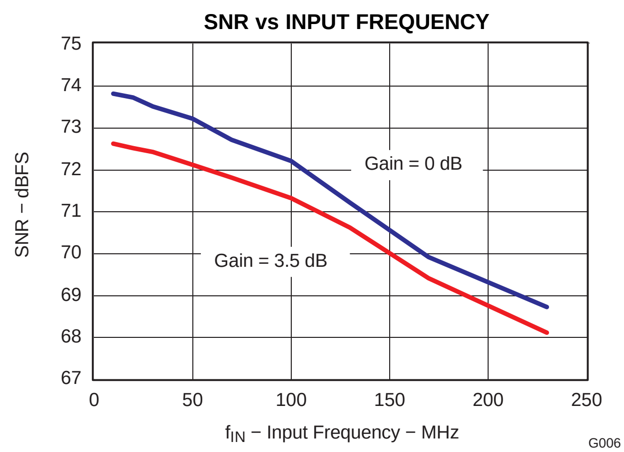


Figure 12.

ADS6445 (F_{srated} = 125 MSPS) (continued)

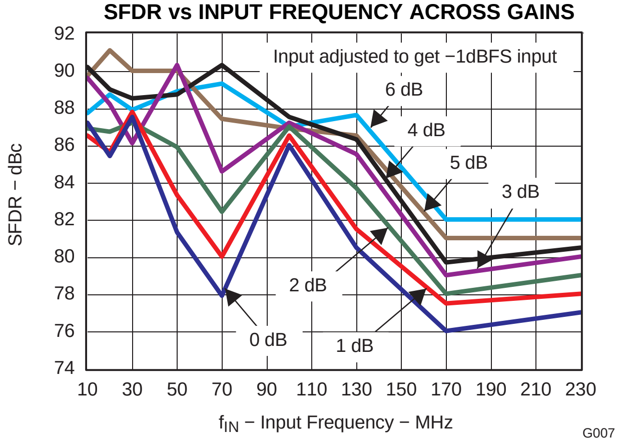
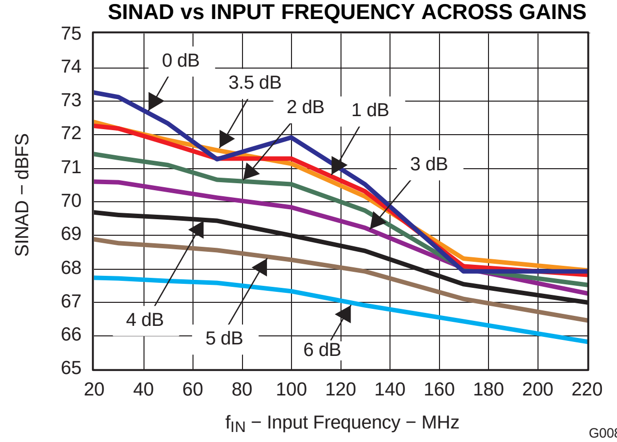


Figure 13.



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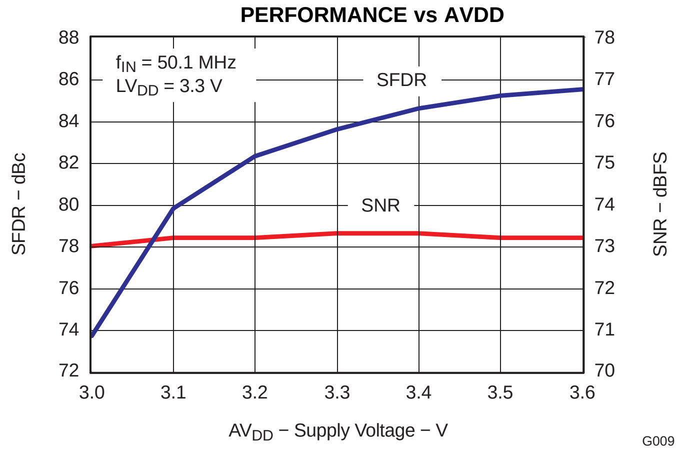

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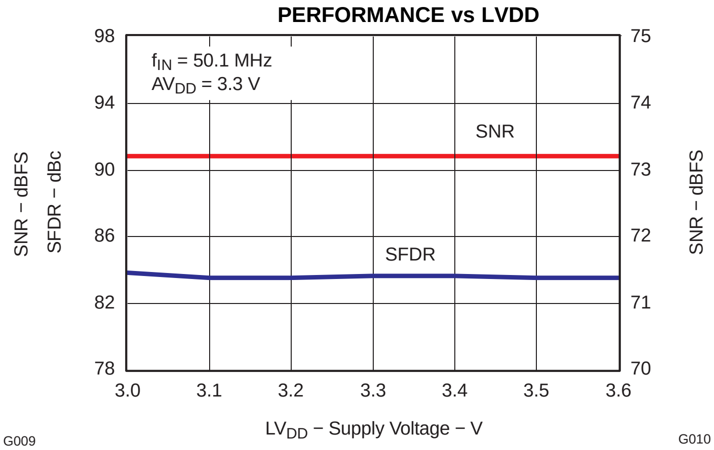

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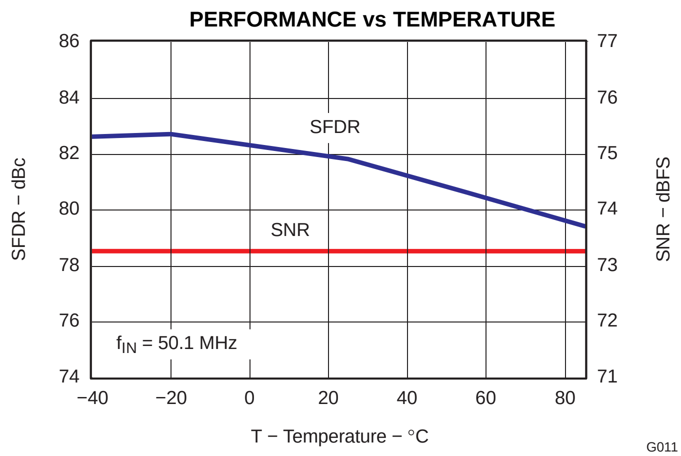


Figure 17.

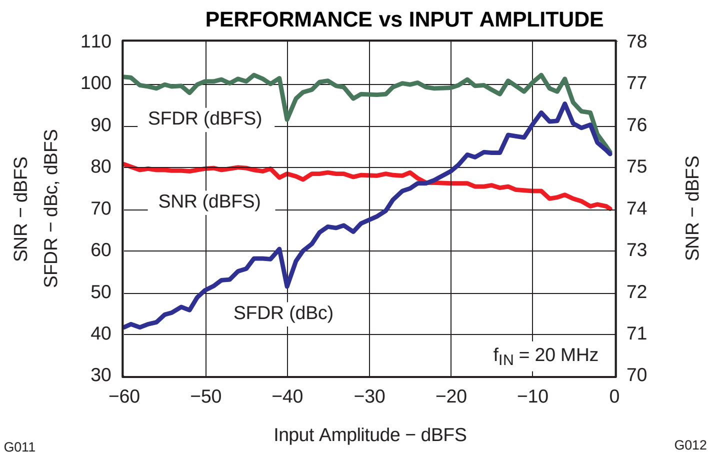


Figure 18.

ADS6445 (F_{srated} = 125 MSPS) (continued)

PERFORMANCE vs CLOCK AMPLITUDE (differential)

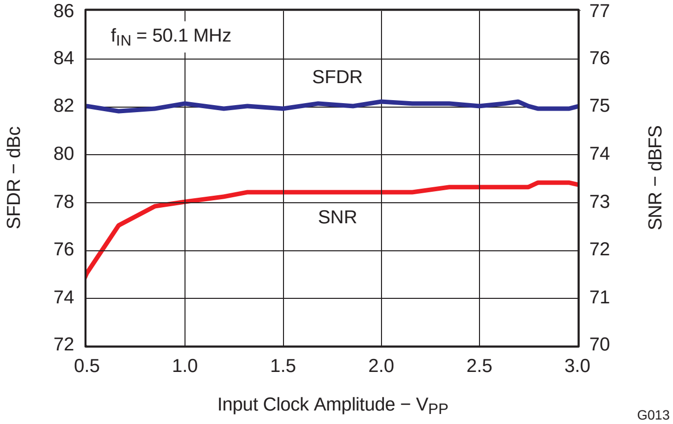


Figure 19.

PERFORMANCE vs CLOCK DUTY CYCLE

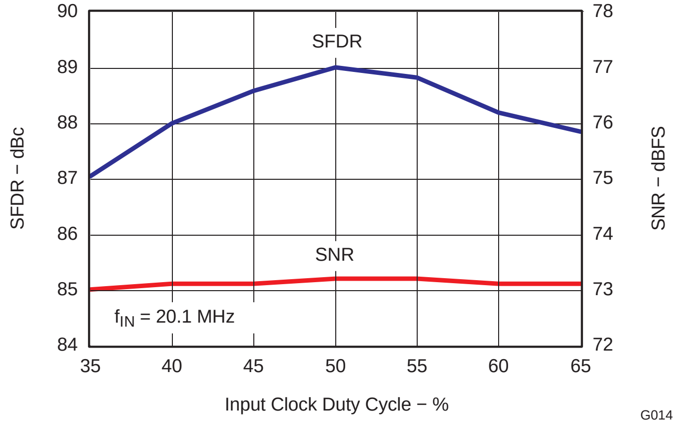


Figure 20.

POWER DISSIPATION vs SAMPLING FREQUENCY

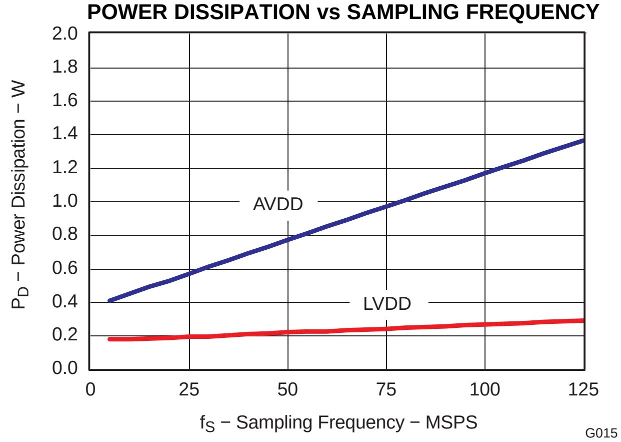


Figure 21.

OUTPUT NOISE HISTOGRAM WITH INPUTS TIED TO COMMON-MODE

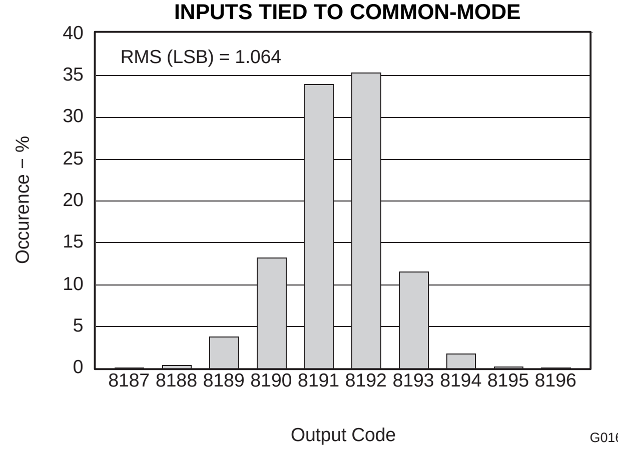


Figure 22.

PERFORMANCE IN EXTERNAL REFERENCE MODE

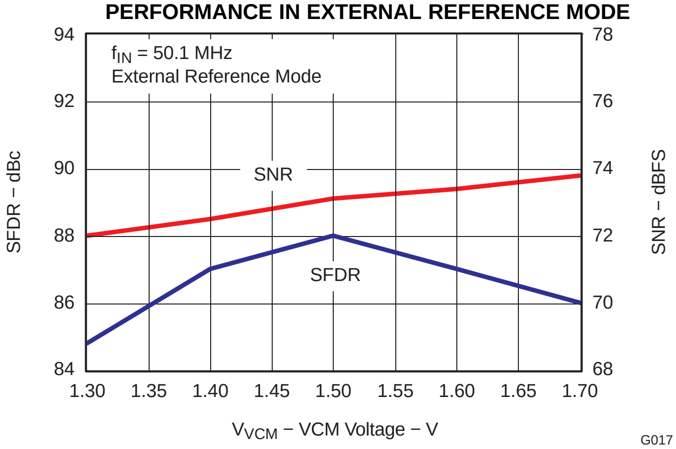


Figure 23.

CMRR vs FREQUENCY

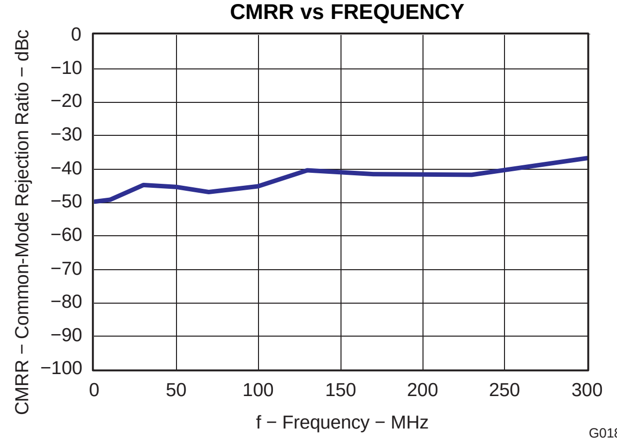
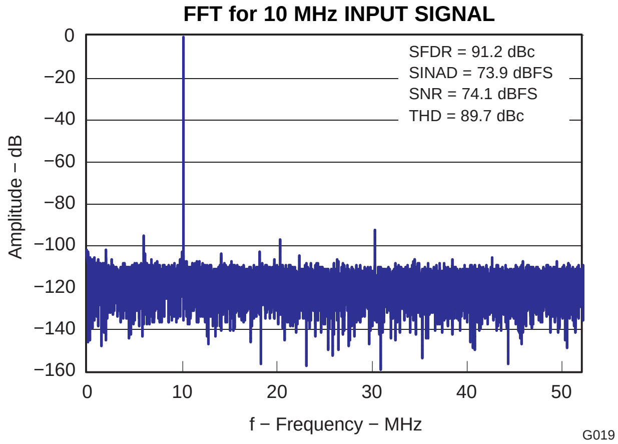


Figure 24.

ADS6444 (F_{srated} = 105 MSPS)



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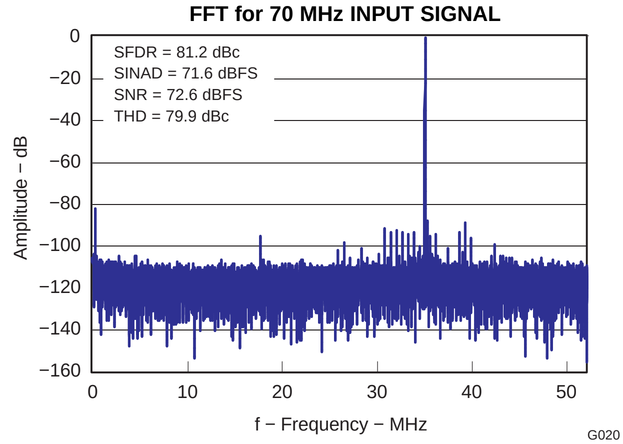


Figure 26.

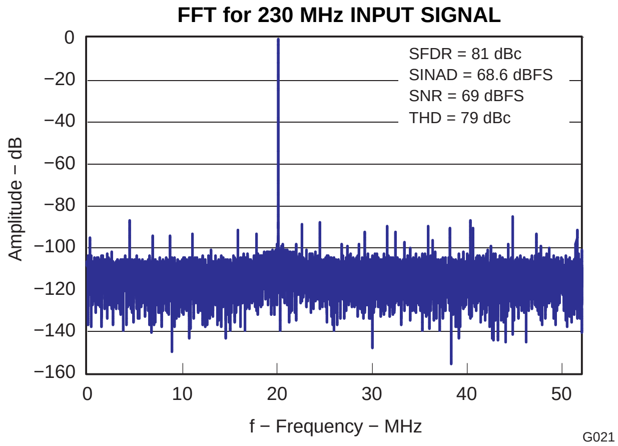
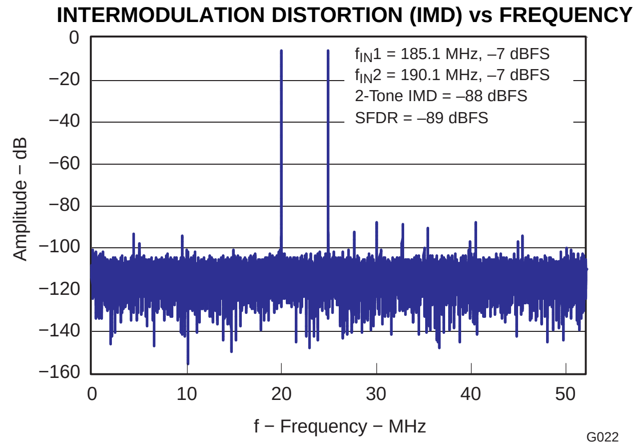


Figure 27.



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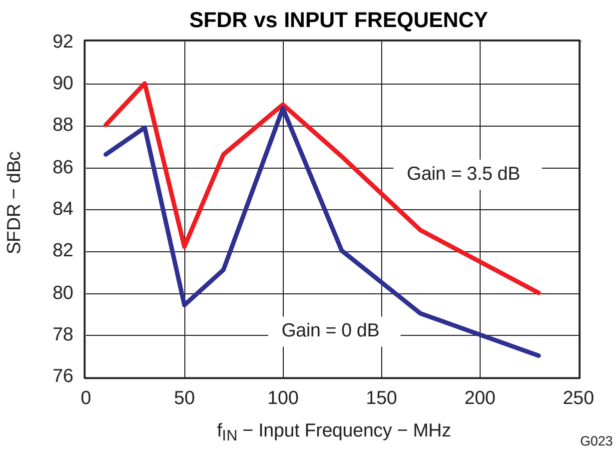


Figure 29.

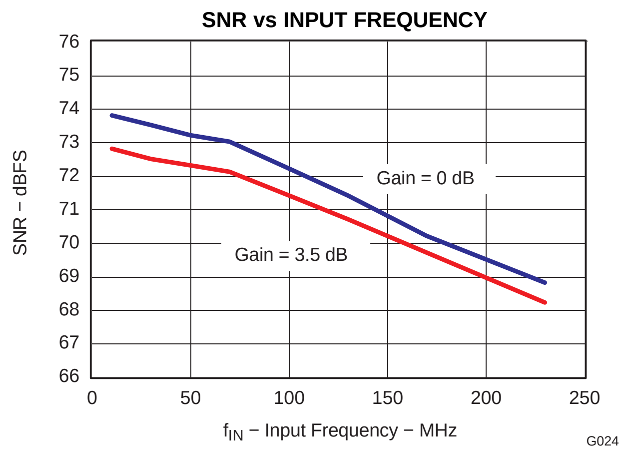


Figure 30.

ADS6444 (F_{srated} = 105 MSPS) (continued)

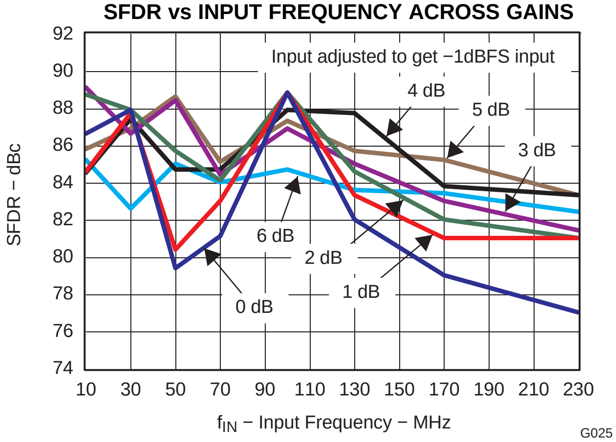


Figure 31.

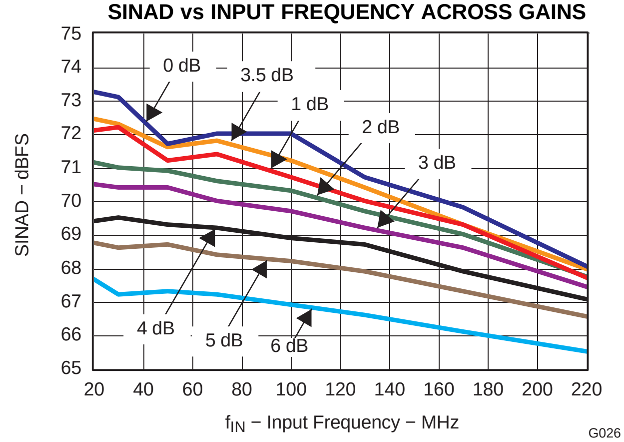


Figure 32.

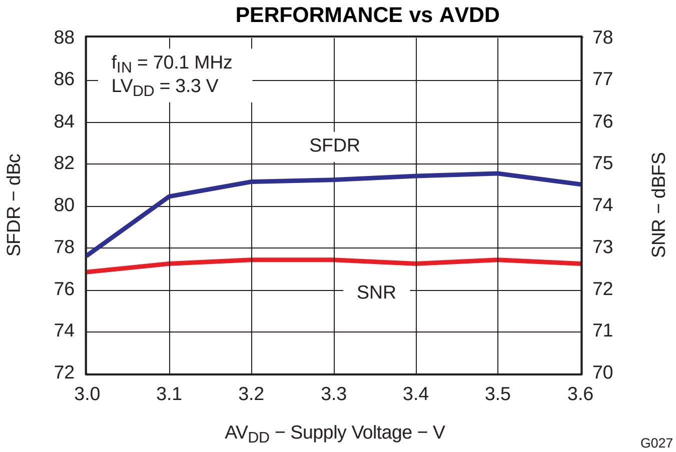


Figure 33.

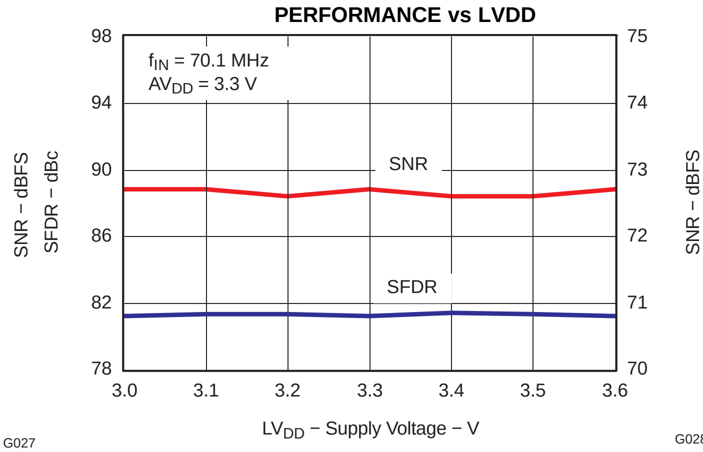


Figure 34.

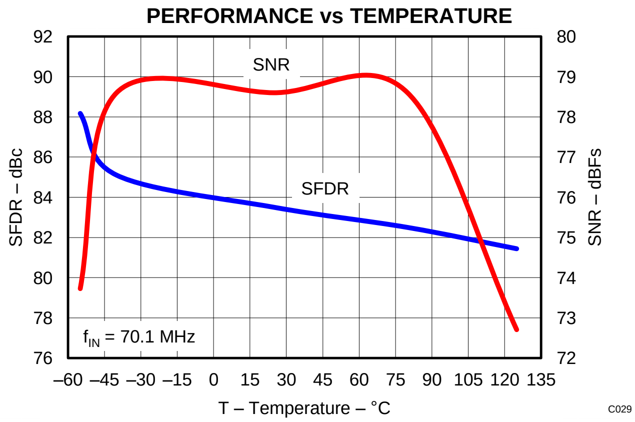


Figure 35.

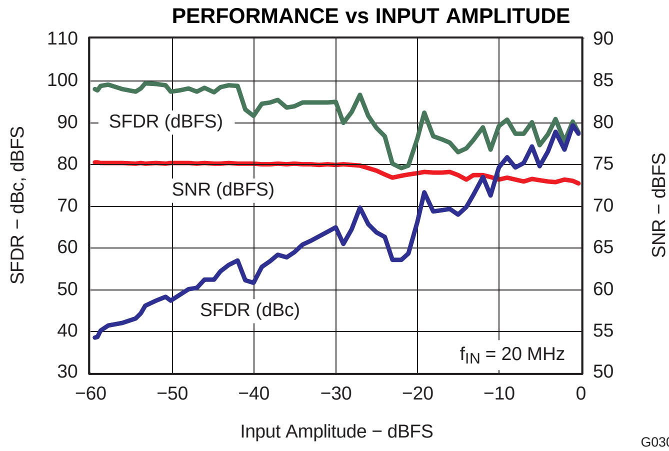


Figure 36.

ADS6444 (F_{srated} = 105 MSPS) (continued)

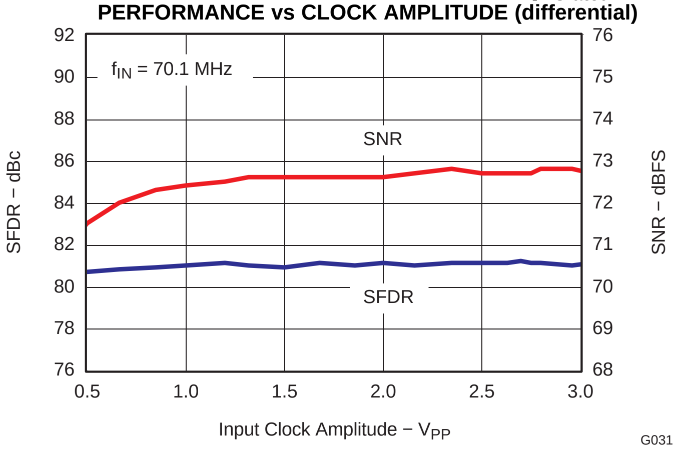


Figure 37.

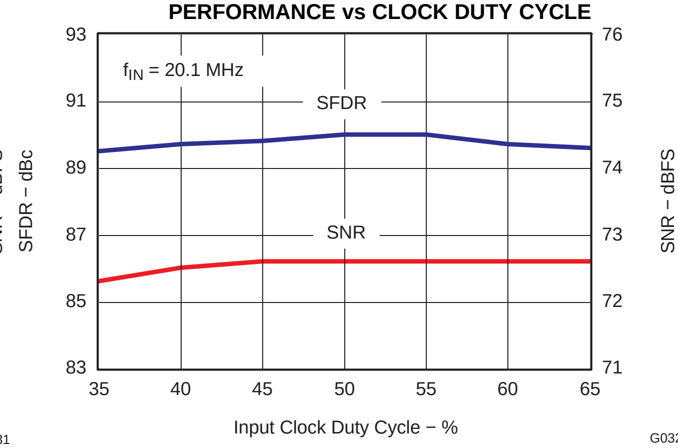


Figure 38.

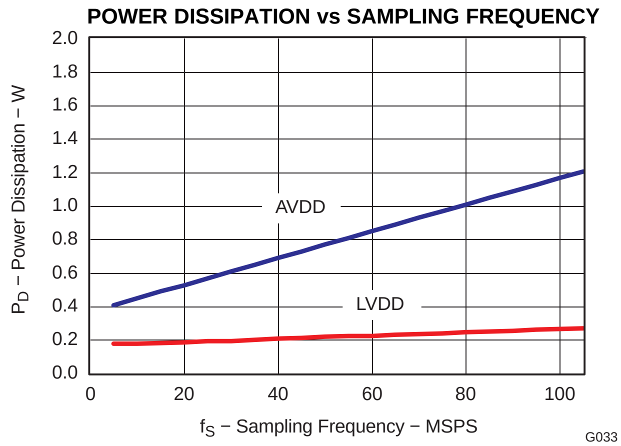


Figure 39.

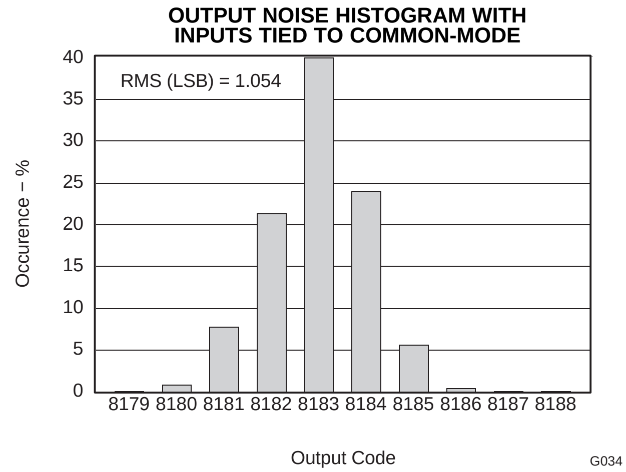


Figure 40.

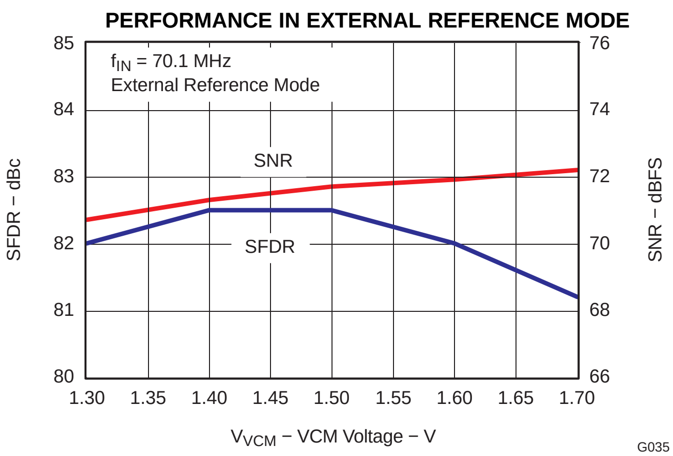


Figure 41.

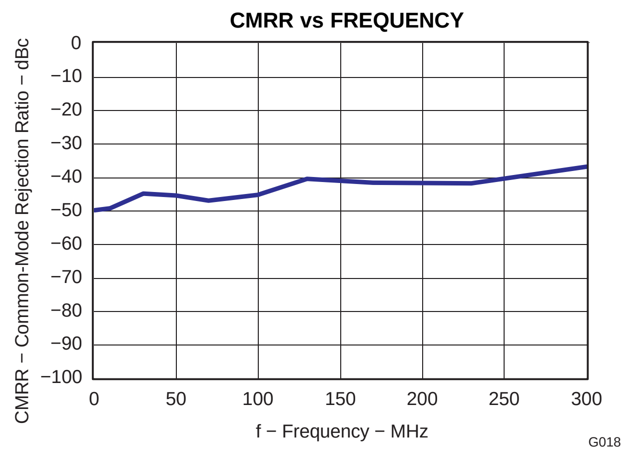


Figure 42.

Contour Plots across Input and Sampling Frequencies

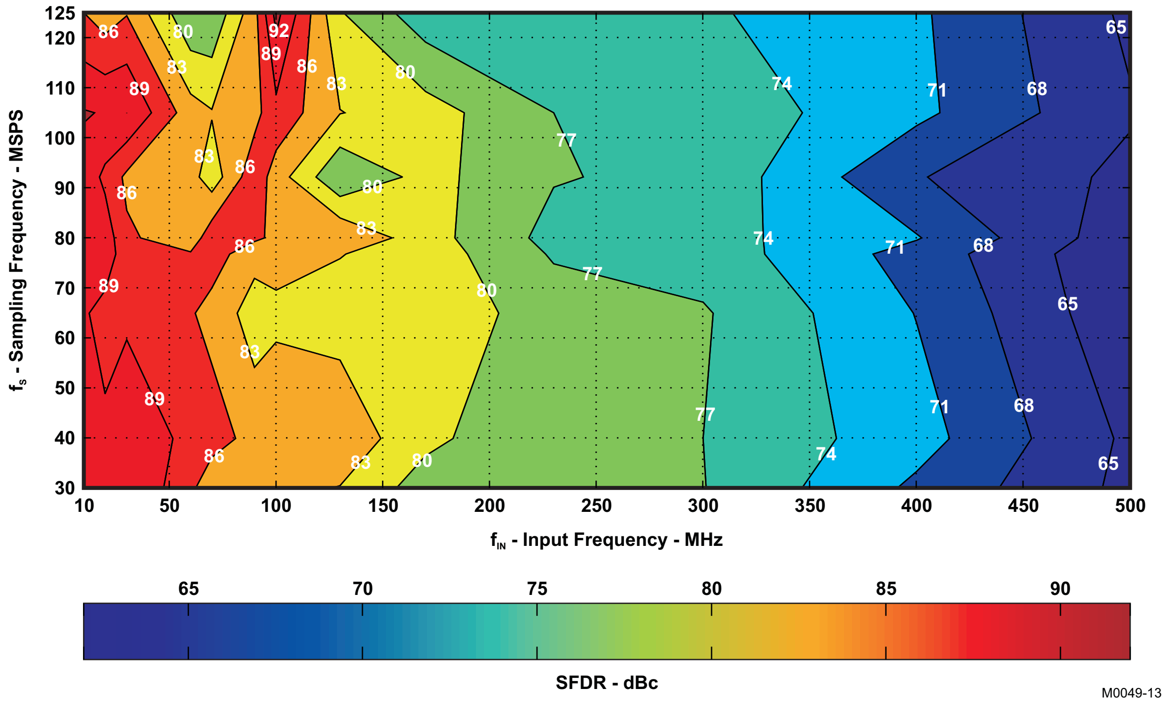


Figure 43. SFDR Contour (no gain)

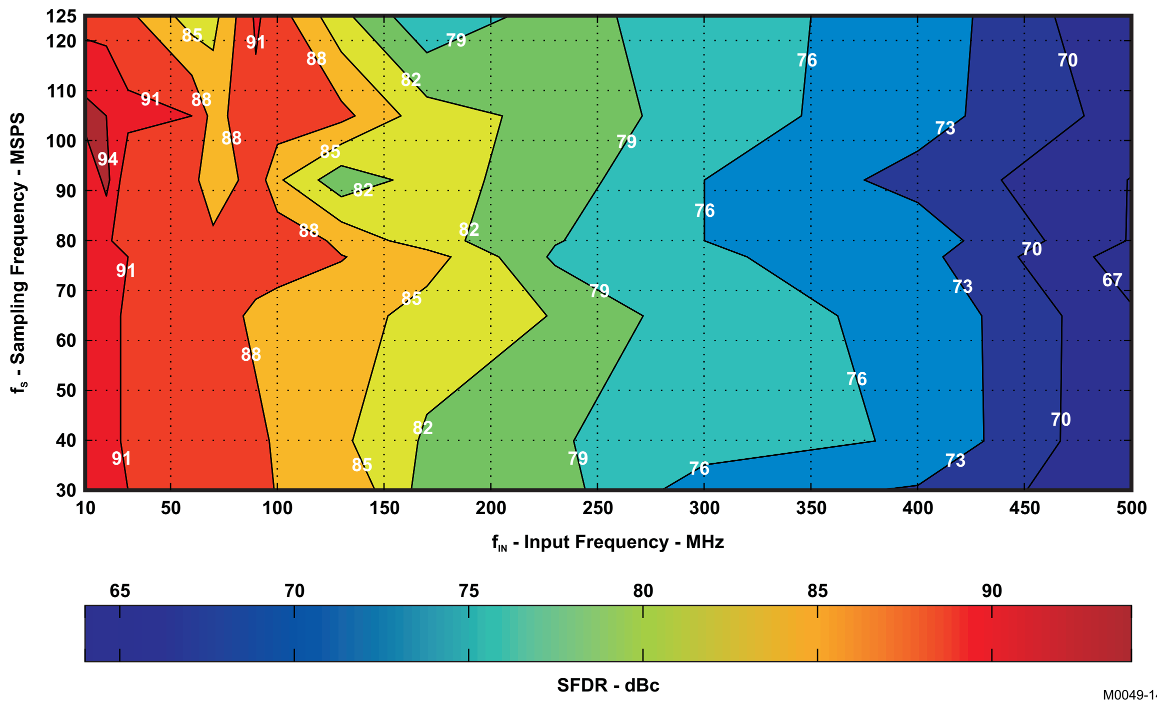


Figure 44. SFDR Contour (3.5 dB coarse gain)

Contour Plots across Input and Sampling Frequencies (continued)

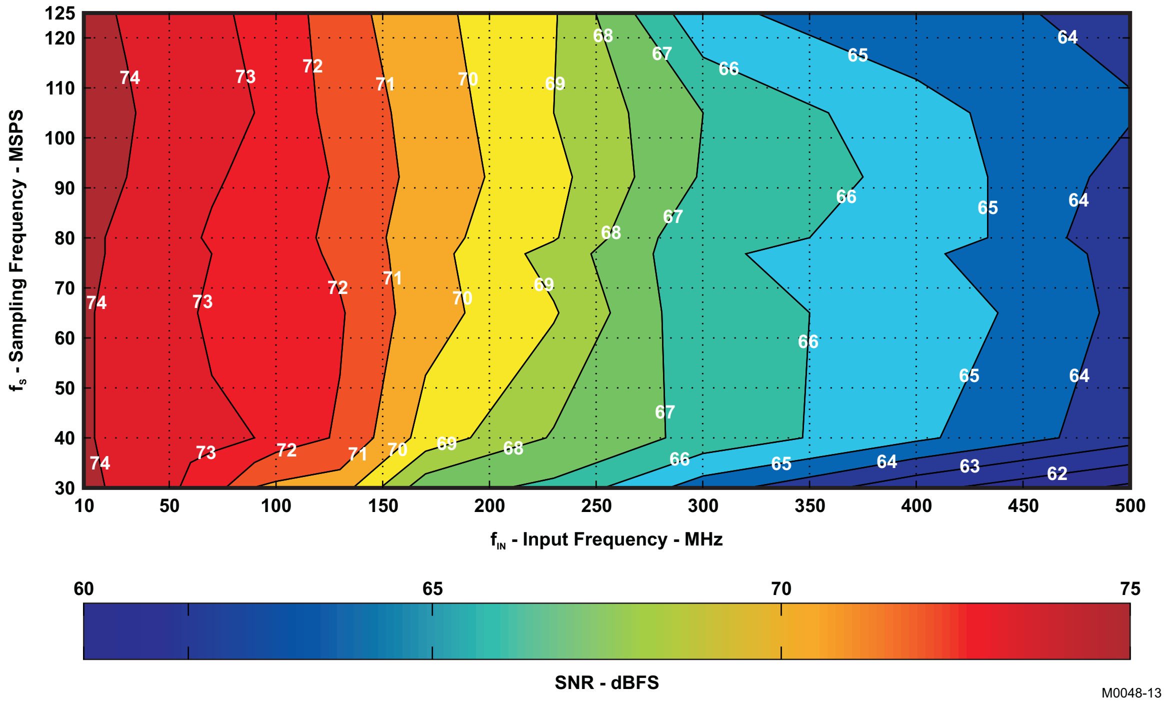


Figure 45. SNR Contour (no gain)

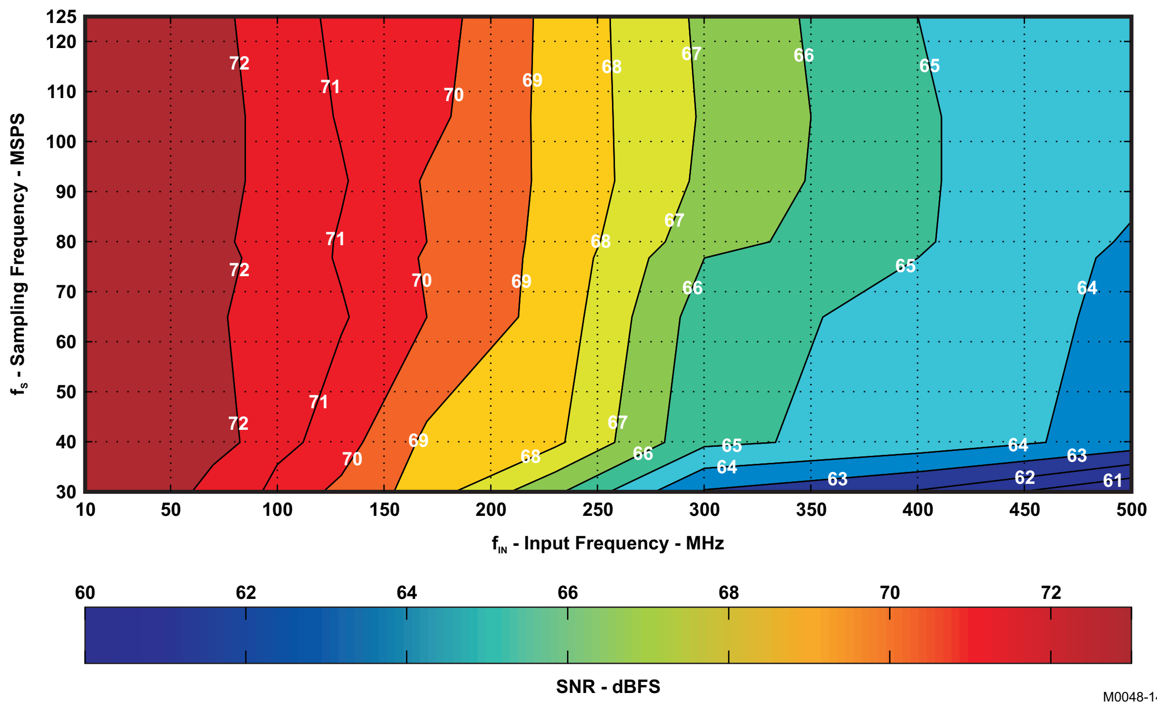


Figure 46. SNR Contour (3.5 dB coarse gain)

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS6445/ADS6444 is a quad channel, 14 bit pipeline ADC based on switched capacitor architecture in CMOS technology.

The conversion is initiated simultaneously by all the four channels at the rising edge of the external input clock. After the input signals are captured by the sample and hold circuit of each channel, the samples are sequentially converted by a series of low resolution stages. The stage outputs are combined in a digital correction logic block to form the final 14 bit word with a latency of 12 clock cycles. The 14 bit word of each channel is serialized and output as LVDS levels. In addition to the data streams, a bit clock and frame clock also are output. The frame clock is aligned with the 14 bit word boundary.

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture, shown in Figure 47. This differential topology results in very good AC performance even for high input frequencies. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5 V, available on VCM pin 13. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2 V_{PP} differential input swing. The maximum swing is determined by the internal reference voltages REFP (2.0 V nominal) and REFM (1.0 V, nominal). The sampling circuit has a 3 dB bandwidth that extends up to 500 MHz (see Figure 48, shown by the transfer function from the analog input pins to the voltage across the sampling capacitors, TF_ADC).

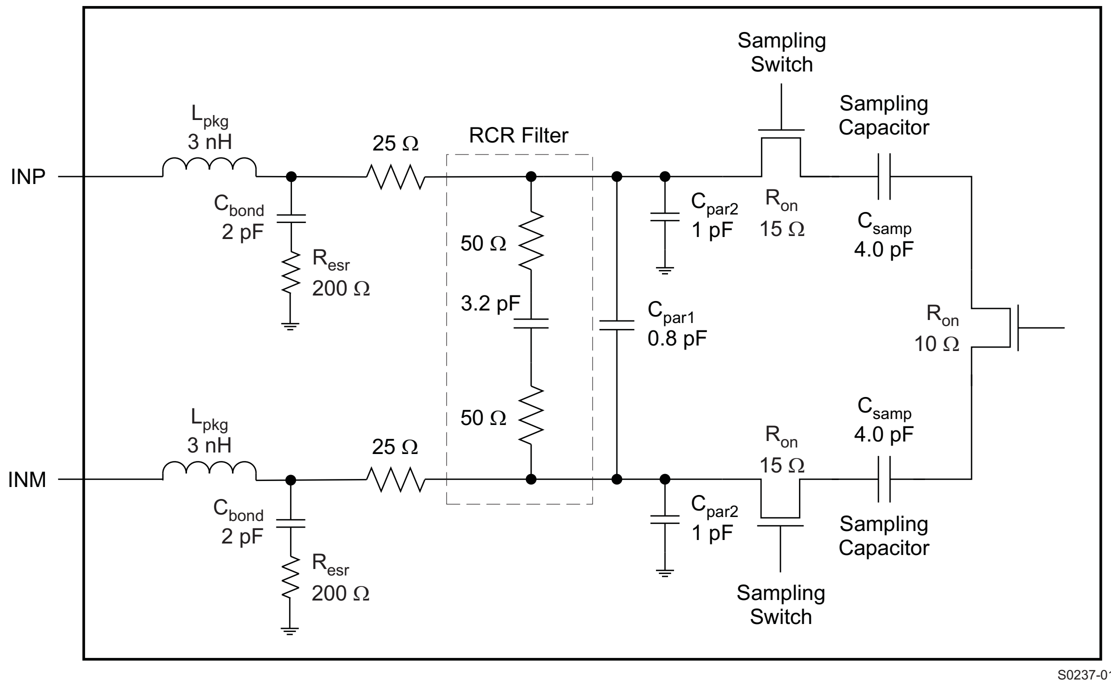


Figure 47. Input Sampling Circuit

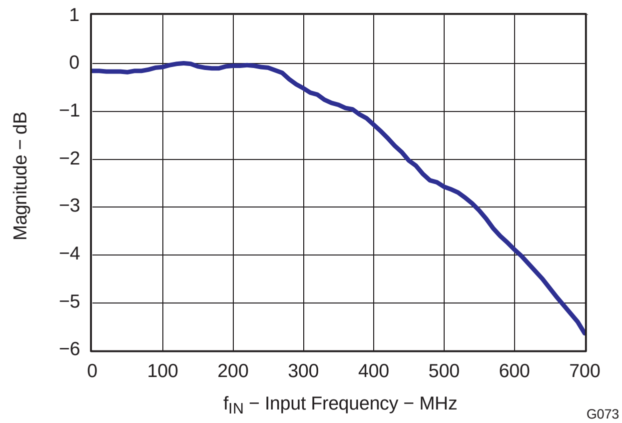


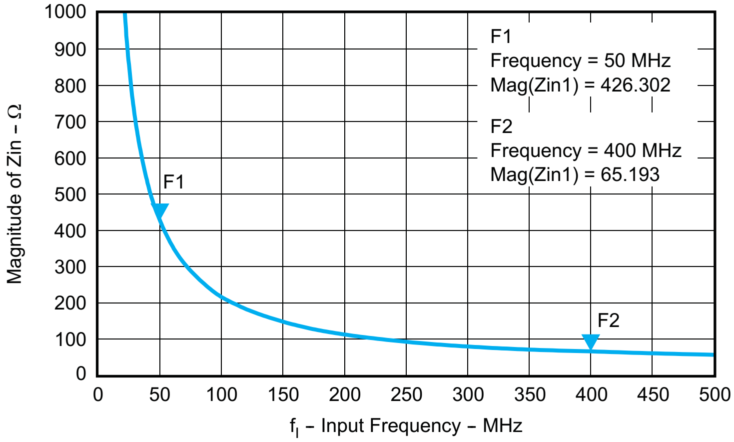
Figure 48. Analog Input Bandwidth (represented by magnitude of TF_ADC, see Figure 50)

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection.

A 5 Ω resistor in series with each input pin is recommended to damp out ringing caused by the package parasitics. It is also necessary to present low impedance (< 50 Ω) for the common mode switching currents. For example, this is achieved by using two resistors from each input terminated to the common mode voltage (VCM).

In addition to the above, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance has to be taken into account. Figure 49 shows that the impedance (Zin, looking into the ADC input pins) decreases at high input frequencies. The Smith chart shows that the input impedance is capacitive and can be approximated by a series R-C up to 500 MHz.



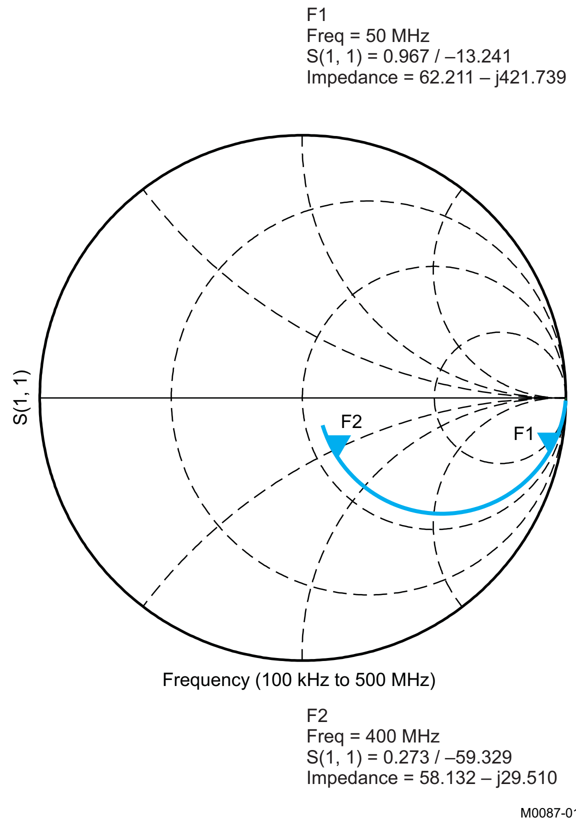


Figure 49. ADC Input Impedance, Zin

Using RF-Transformers Based Drive Circuits

Figure 50 shows a configuration using a single 1:1 turns ratio transformer (for example, Coilcraft WBC1-1) that can be used for low input frequencies up to 100 MHz.

The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated on the secondary side. Putting the termination on the secondary side helps to shield the kickbacks caused by the sampling circuit from the RF transformer's leakage inductances. The termination is accomplished by two resistors connected in series, with the center point connected to the 1.5 V common mode (VCM pin). The value of the termination resistors (connected to common mode) has to be low (< 100 Ω) to provide a low-impedance path for the ADC common-mode switching current.

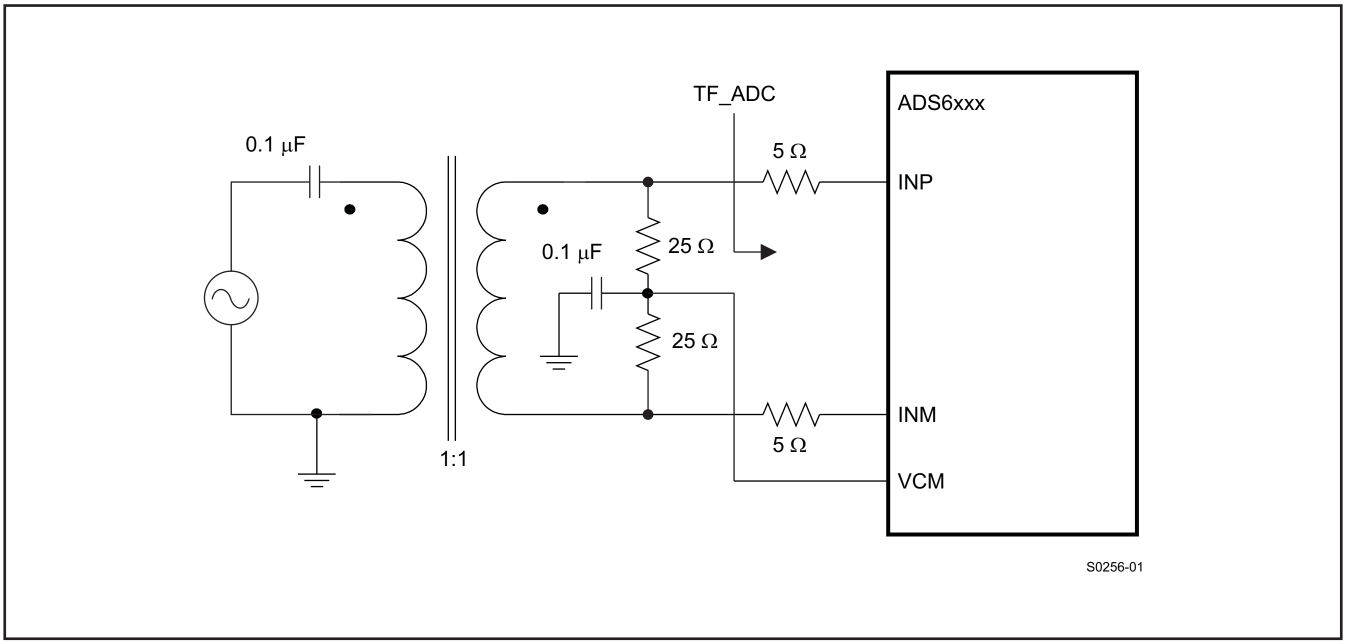


Figure 50. Single Transformer Drive Circuit

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch, and good performance is obtained for high frequency input signals. Figure 51 shows an example using two transformers (like Coilcraft WBC1-1). An additional termination resistor pair (enclosed within the shaded box in Figure 51) may be required between the two transformers to improve the balance between the P and M sides. The center point of this termination must be connected to ground.

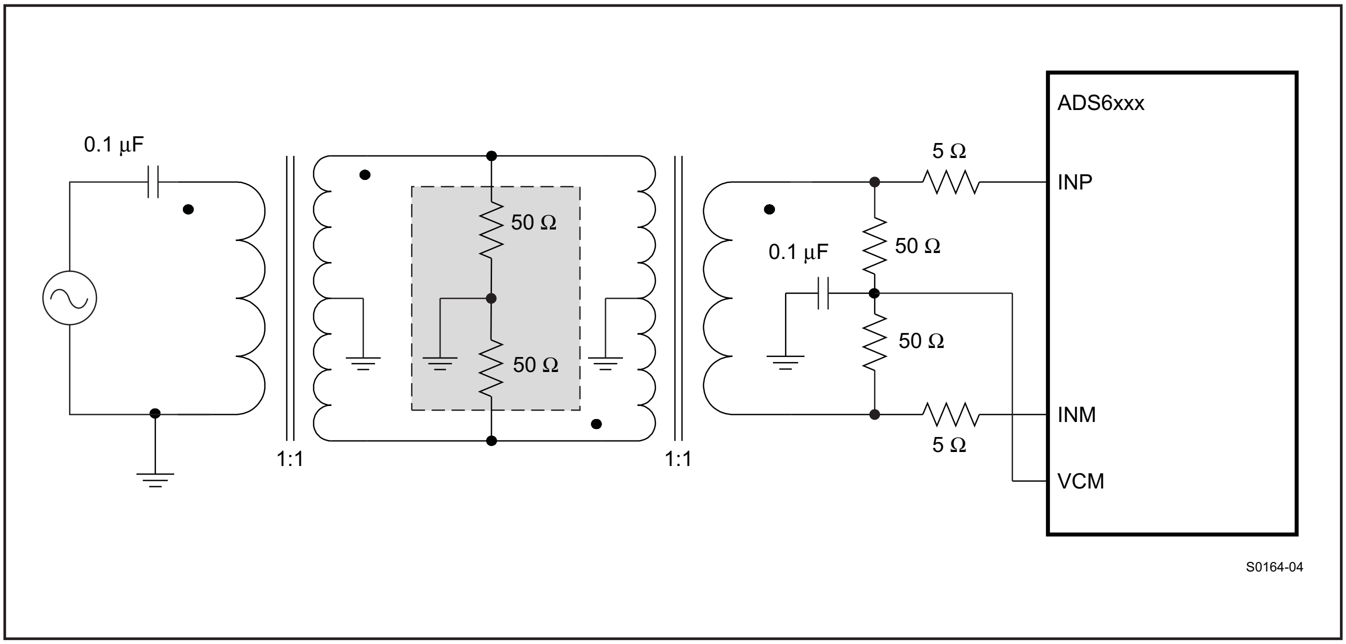


Figure 51. Two Transformer Drive Circuit

Using Differential Amplifier Drive Circuits

Figure 52 shows a drive circuit using a differential amplifier (TI's THS4509) to convert a single-ended input to differential output that can be interfaced to the ADC input pins. In addition to the single-ended to differential conversion, the amplifier also provides gain (10 dB in Figure 52). As shown in the figure, R_{FIL} helps to isolate the amplifier output from the switching inputs of the ADC. Together with C_{FIL}, it also forms a low-pass filter that bandlimits the noise (and signal) at the ADC input. As the amplifier outputs are ac-coupled, the common-mode voltage of the ADC input spins is set using two resistors connected to VCM.

The amplifier outputs also can be dc-coupled. Using the output common-mode control of the THS4509, the ADC input pins can be biased to 1.5 V. In this case, use +4 V and -1 V supplies for the THS4509 to ensure that it's output common-mode voltage (1.5 V) is at mid-supply.

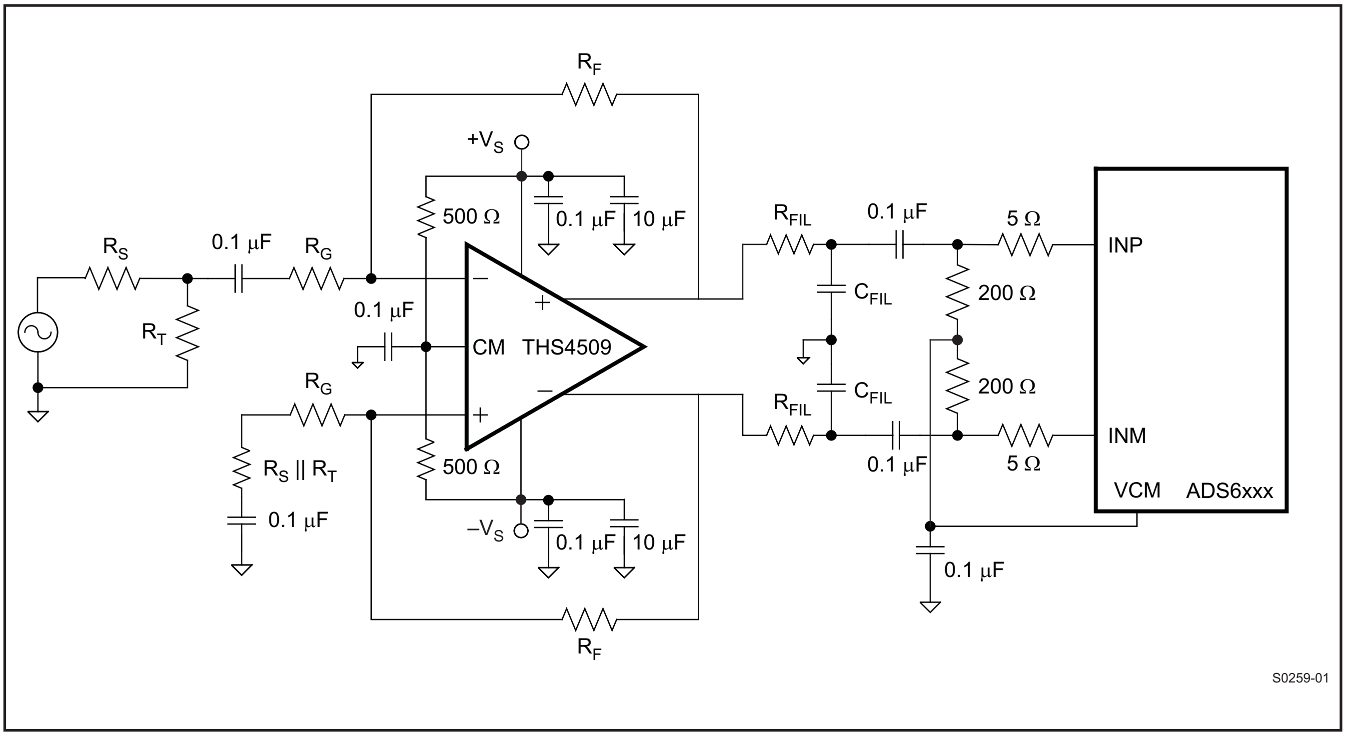


Figure 52. Drive Circuit Using THS4509

Refer to the EVM User Guide (SLAU196) for more information.

INPUT COMMON MODE

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1 μF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 155 μA at 125 MSPS (per input pin). Equation 1 describes the dependency of the common-mode current and the sampling frequency.

$$\frac{155\ \mu A x Fs}{125\ MSPS} \quad (1)$$

This equation helps to design the output capability and impedance of the CM driving circuit accordingly.

REFERENCE

The ADS644X has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the on-chip integration of the requisite reference capacitors eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by programming the register bit **<REF>** (refer to Table 13).

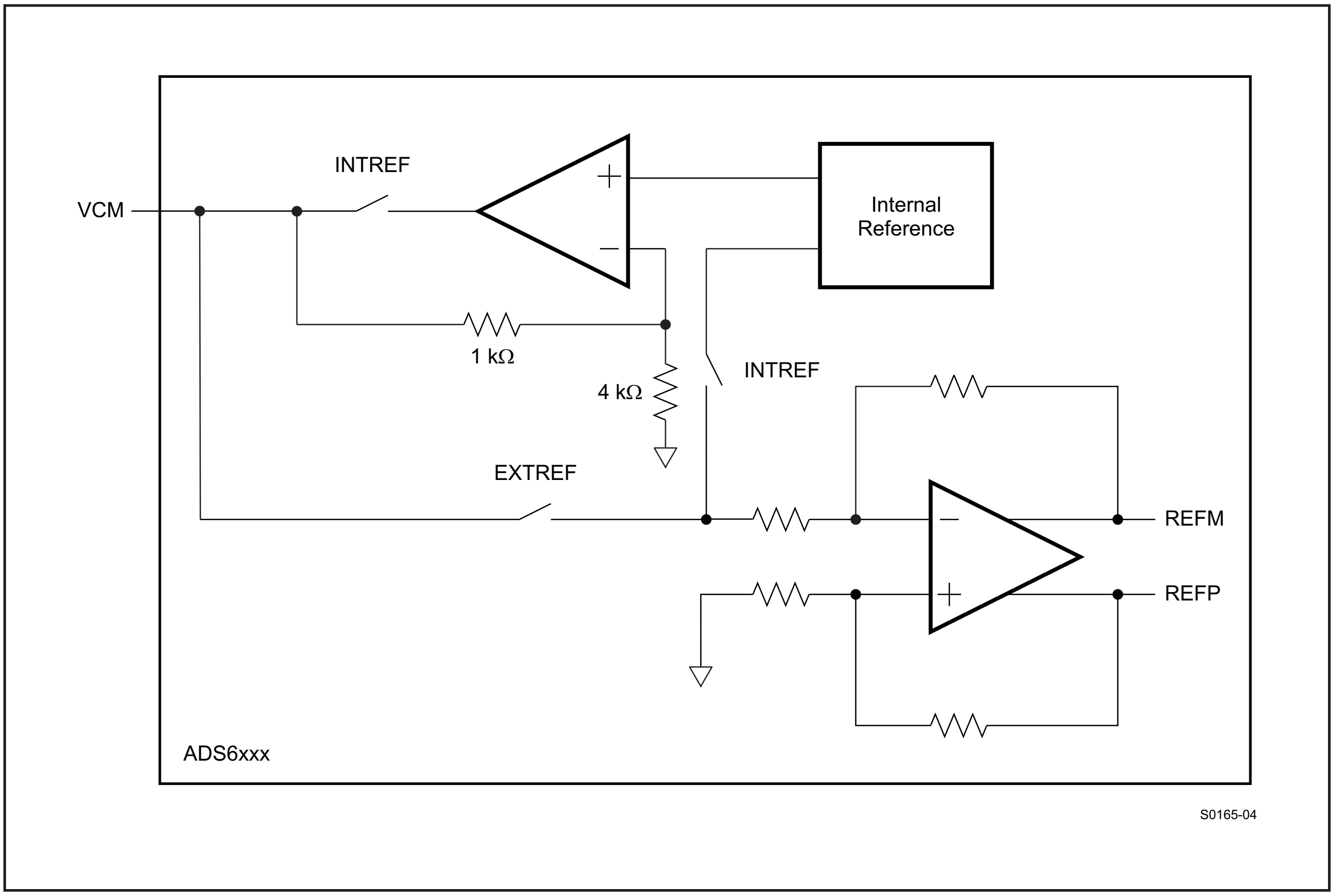


Figure 53. Reference Section

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5 V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

External Reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by Equation 2.

$$\text{Full-scale differential input pp} = (\text{Voltage forced on VCM}) \times 1.33 \quad (2)$$

In this mode, the range of voltage applied on VCM should be 1.45 V to 1.55 V. The 1.5-V common-mode voltage to bias the input pins has to be generated externally.

COARSE GAIN AND PROGRAMMABLE FINE GAIN

ADS644X includes gain settings that can be used to get improved SFDR performance (compared to 0 dB gain mode). The gain settings are 3.5 dB coarse gain and programmable fine gain from 0 dB to 6 dB. For each gain setting, the analog input full-scale range scales proportionally, as listed in Table 21.

The coarse gain is a fixed setting of 3.5 dB and is designed to improve SFDR with little degradation in SNR (as seen in Figure 11 and Figure 12). The fine gain is programmable in 1 dB steps from 0 to 6 dB. With fine gain also, SFDR improvement is achieved, but at the expense of SNR (there is about 1 dB SNR degradation for every 1 dB of fine gain).

So, the fine gain can be used to trade-off between SFDR and SNR. The coarse gain makes it possible to get best SFDR but without losing SNR significantly. At high input frequencies, the gains are especially useful as the SFDR improvement is significant with marginal degradation in SINAD.

The gains can be programmed using the register bits **<COARSE GAIN>** (refer to Table 18) and **<FINE GAIN>** (refer to Table 17). Note that the default gain after reset is 0 dB.

Table 21. Full-Scale Range Across Gains

GAIN, dB	TYPE	FULL-SCALE, V_{PP}
0	Default (after reset)	2
3.5	Coarse setting (fixed)	1.34
1	Fine setting (programmable)	1.78
2		1.59
3		1.42
4		1.26
5		1.12
6		1.00

CLOCK INPUT

The ADS644X clock inputs can be driven differentially (SINE, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5 kΩ resistors as shown in Figure 54. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS clock sources (see Figure 55 and Figure 57).

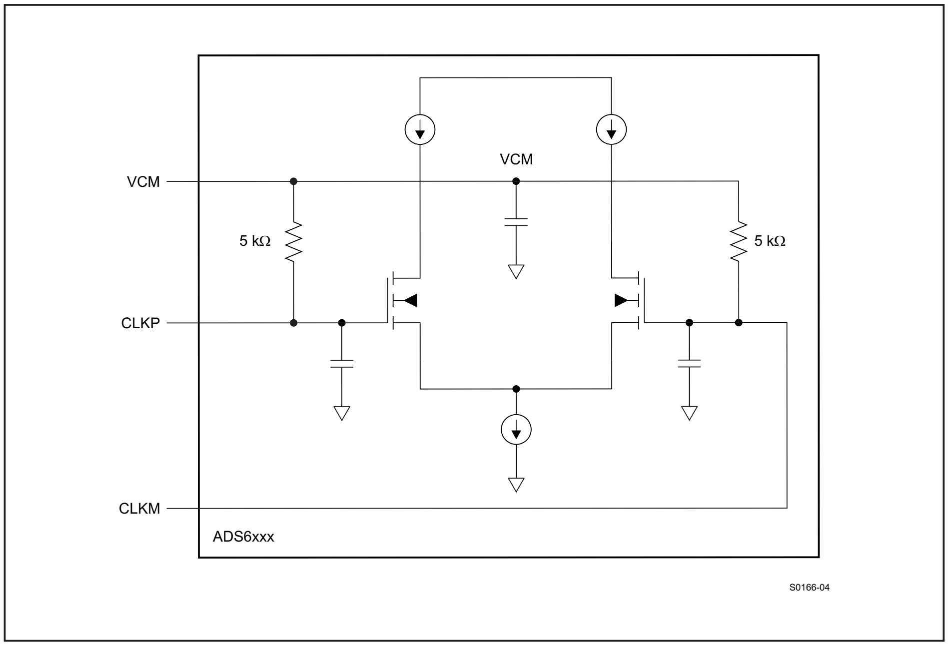


Figure 54. Internal Clock Buffer

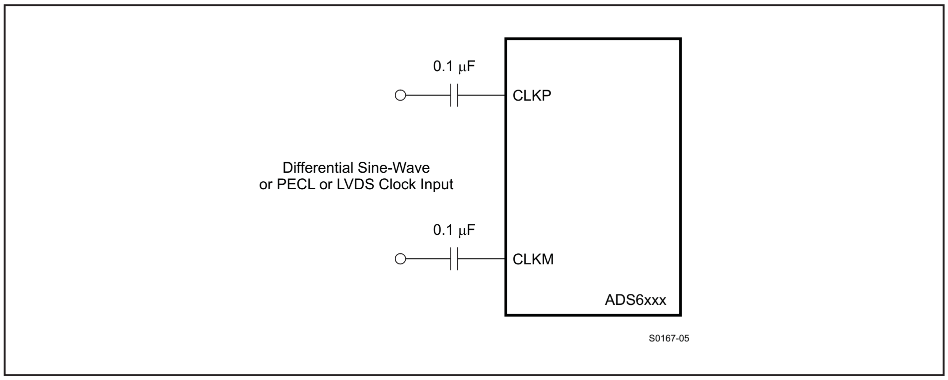


Figure 55. Differential Clock Driving Circuit

Figure 56 shows a typical scheme using PECL clock drive from a CDCM7005 clock driver. SNR performance with this scheme is comparable with that of a low jitter sine wave clock source.

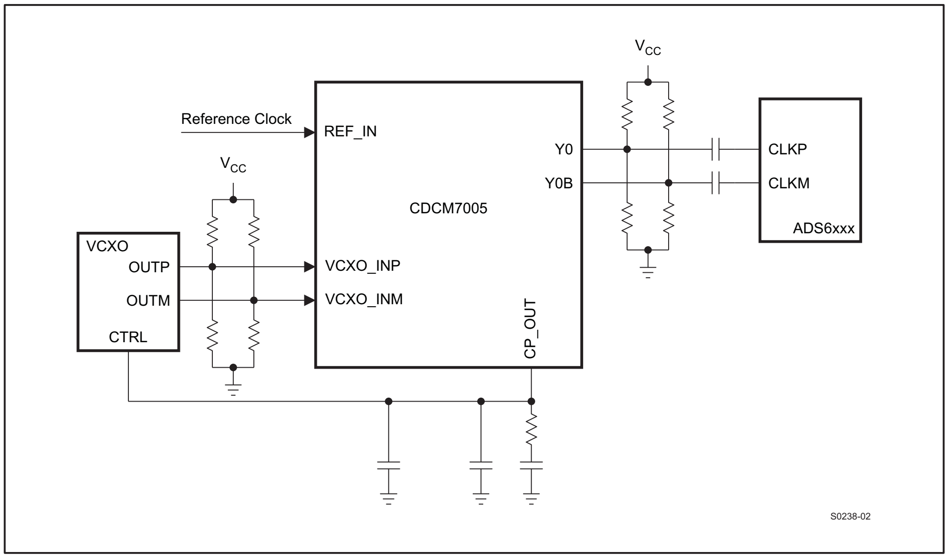


Figure 56. PECL Clock Drive Using CDCM7005

Single-ended CMOS clock can be ac coupled to the CLKP input, with CLKM (pin) connected to ground with a 0.1-μF capacitor, as shown in Figure 57.

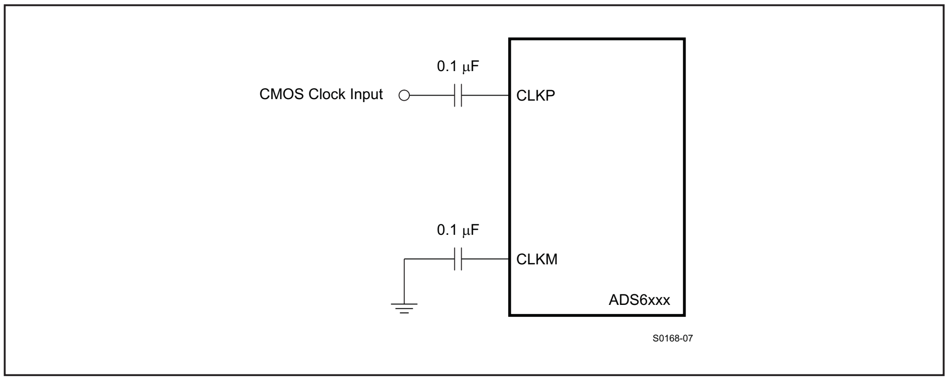


Figure 57. Single-Ended Clock Driving Circuit

For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

CLOCK BUFFER GAIN

When using a sinusoidal clock input, the noise contributed by clock jitter improves as the clock amplitude is increased. Hence, it is recommended to use large clock amplitude. As shown by Figure 19, use clock amplitude greater than 1 V_{PP} to avoid performance degradation.

In addition, the clock buffer has programmable gain to amplify the input clock to support very low clock amplitude. The gain can be set by programming the register bits **<CLKIN GAIN>** (refer to Table 14) and increases monotonically from Gain 0 to Gain 4 settings. Table 22 lists the minimum clock amplitude supported for each gain setting.

Table 22. Minimum Clock Amplitude across gains

CLOCK BUFFER GAIN	MINIMUM CLOCK AMPLITUDE SUPPORTED mV_{PP} differential
Gain 0 (minimum gain)	800
Gain 1 (default gain)	400
Gain 2	300
Gain 3	200
Gain 4 (highest gain)	150

POWER DOWN MODES

The ADS644X has three power-down modes – global power down, channel standby and input clock stop.

Global Power Down

This is a global power-down mode in which almost the entire chip is powered down, including the four ADCs, internal references, PLL and LVDS buffers. As a result, the total power dissipation falls to about 77 mW typical (with input clock running). This mode can be initiated by setting the register bit **<PDN GLOBAL>** (refer to Table 13). The output data and clock buffers are in high-impedance state.

The wake-up time from this mode to data becoming valid in normal mode is 100 µs.

Channel Standby

In this mode, only the ADC of each channel is powered down and this helps to get very fast wake-up times. Each of the four ADCs can be powered down independently using the register bits **<PDN CH>** (refer to Table 13). The output LVDS buffers remain powered up.

The wake-up time from this mode to data becoming valid in normal mode is 200 clock cycles.

Input Clock Stop

The converter enters this mode:

- If the input clock frequency falls below 1 MSPS or
- If the input clock amplitude is less than 400 mV_{PP}, differential with default clock buffer gain setting) at any sampling frequency.

All ADCs and LVDS buffers are powered down and the power dissipation is about 235 mW. The wake-up time from this mode to data becoming valid in normal mode is 100 µs.

Table 23. Power-Down Mode Summary

POWER-DOWN MODE	AVDD POWER (mW)	LVDD POWER (mW)	WAKE-UP TIME
In power-up	1360	297	–

Table 23. Power-Down Mode Summary (continued)

POWER-DOWN MODE	AVDD POWER (mW)	LVDD POWER (mW)	WAKE-UP TIME
Global power down	65	12	100 µs
1 Channel in standby	1115 (1)	297 (1)	200 Clocks
2 Channels in standby	825 (1)	297 (1)	200 Clocks
3 Channels in standby	532 (1)	297 (1)	200 Clocks
4 Channels in standby	245 (1)	297 (1)	200 Clocks
Input clock stop	200	35	100 µs

(1) Sampling frequency = 125 MSPS.

POWER SUPPLY SEQUENCING

During power-up, the AVDD and LVDD supplies can come up in any sequence. The two supplies are separated inside the device. Externally, they can be driven from separate supplies or from a single supply.

DIGITAL OUTPUT INTERFACE

The ADS644X offers several flexible output options making it easy to interface to an ASIC or an FPGA. Each of these options can be easily programmed using either parallel pins or the serial interface.

The output interface options are:

- 1-Wire, 1× frame clock, 14× and 16× serialization with DDR bit clock
- 2-Wire, 1× frame clock, 16× serialization, with DDR and SDR bit clock, byte wise/bit wise/word wise
- 2-Wire, 1× frame clock, 14× serialization, with SDR bit clock, byte wise/bit wise/word wise
- 2-Wire, (0.5 x) frame clock, 14× serialization, with DDR bit clock, byte wise/bit wise/word wise

The maximum sampling frequency, bit clock frequency and output data rate will vary depending on the interface options selected (refer to Table 12).

Table 24. Maximum Recommended Sampling Frequency for Different Output Interface Options

INTERFACE OPTIONS			MAXIMUM RECOMMENDED SAMPLING FREQUENCY, MSPS	BIT CLOCK FREQUENCY, MHZ	FRAME CLOCK FREQUENCY, MHZ	SERIAL DATA RATE, Mbps
1-Wire	DDR Bit clock	14× Serialization	65	455	65	910
		16× Serialization	65	520	65	1040
2-Wire	DDR Bit clock	14× Serialization	125	437.5	62.5	875
		16× Serialization	125	500	125	1000
2-Wire	SDR Bit clock	14× Serialization	65	455	65	910
		16× Serialization	65	520	65	1040

Each interface option is described in detail in the following sections.

1-WIRE INTERFACE - 14× AND 16× SERIALIZATION WITH DDR BIT CLOCK

Here the device outputs the data of each ADC serially on a single LVDS pair (1 wire). The data is available at the rising and falling edges of the bit clock (DDR bit clock). The ADC outputs a new word at the rising edge of every frame clock, starting with the MSB. Optionally, it can also be programmed to output the LSB first. The data rate is 14 × sample frequency (14× serialization) and 16 × sample frequency (16× serialization).

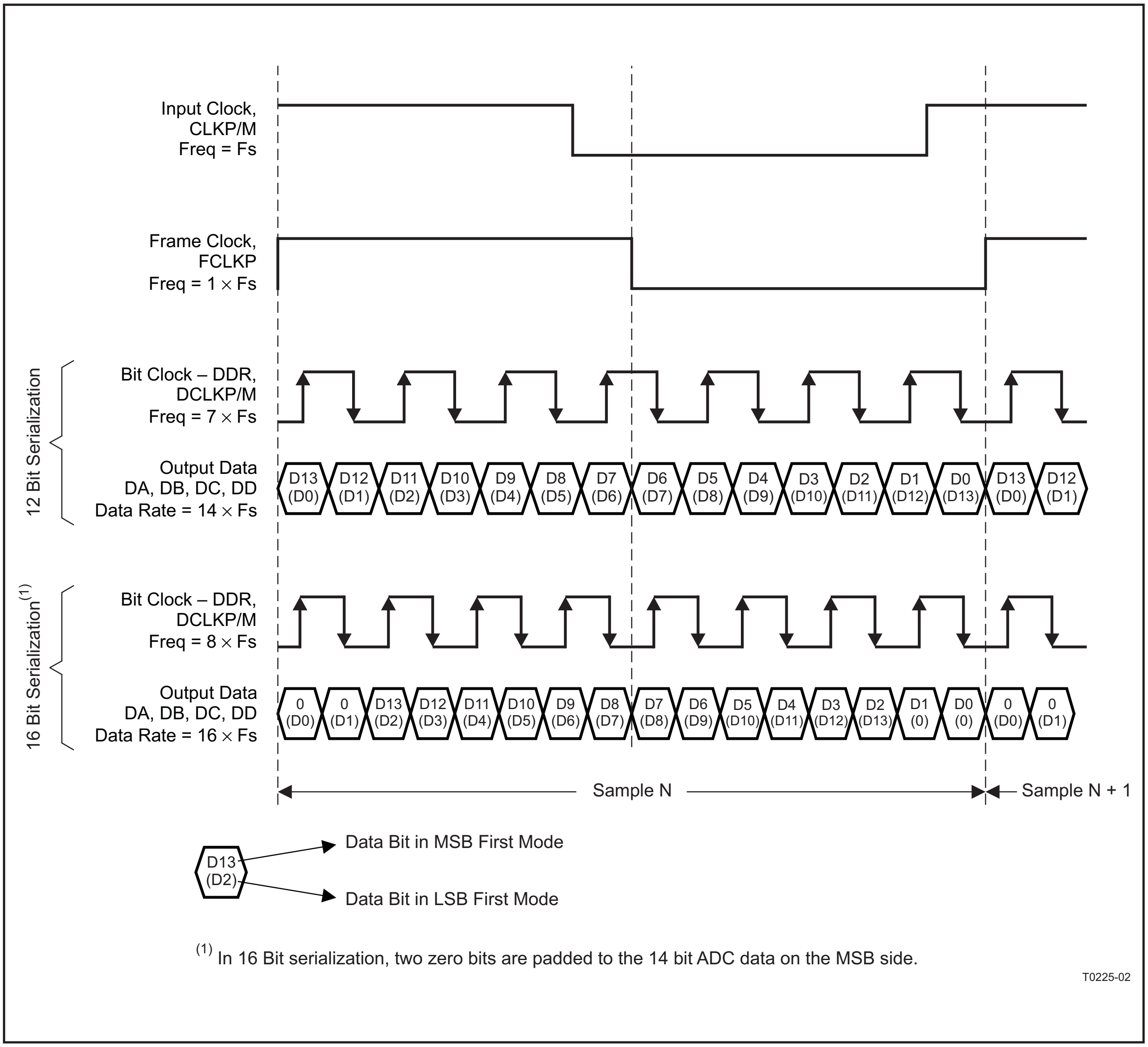


Figure 58. 1-Wire Interface

2-WIRE INTERFACE - 16× SERIALIZATION WITH DDR/SDR BIT CLOCK

The 2-wire interface is recommended for sampling frequencies above 65 MSPS. In 16× serialization, two zero bits are padded to the 14 bit ADC data on the MSB side and the combined 16 bit data is serialized and output over two LVDS pairs. The data rate is 8 × Sample frequency since 8 bits are sent on each wire every clock cycle. The data is available along with DDR bit clock or optionally with SDR bit clock. Each ADC sample is sent over the 2 wires as byte-wise or bit-wise or word-wise.

Using the 16× serialization makes it possible to upgrade to a 16-bit ADC in the future seamlessly, without requiring any modification to the receiver capture logic design.

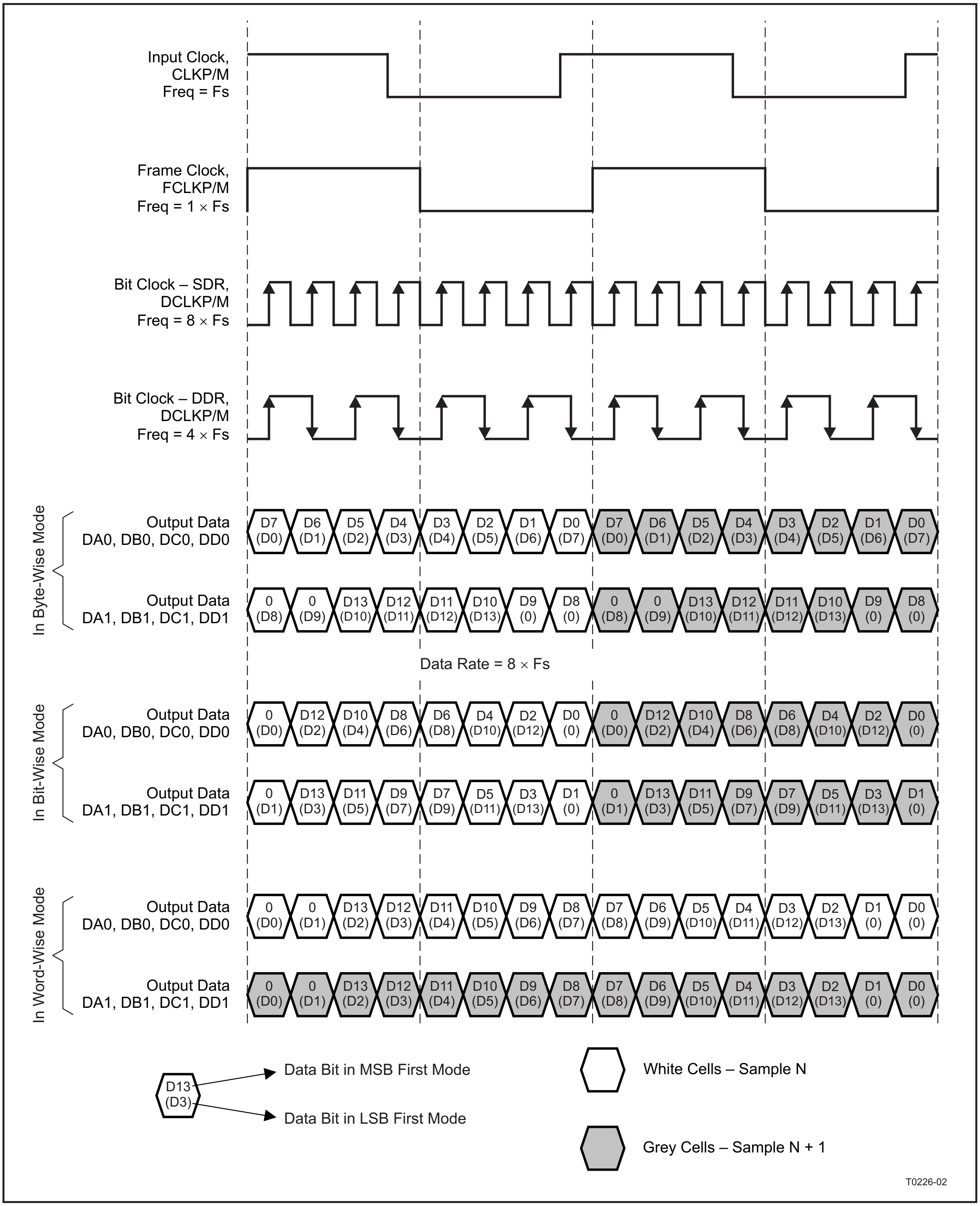


Figure 59. 2-Wire Interface 16× Serialization

2-WIRE INTERFACE - 14× SERIALIZATION

The 14 bit ADC data is serialized and output over two LVDS pairs. A frame clock at 1× sample frequency is also available with an SDR bit clock. With DDR bit clock option, the frame clock frequency is 0.5× sample frequency.

The output data rate will be 7 × sample frequency as 7 data bits are output every clock cycle on each wire. Each ADC sample is sent over the 2 wires as byte-wise or bit-wise or word-wise.

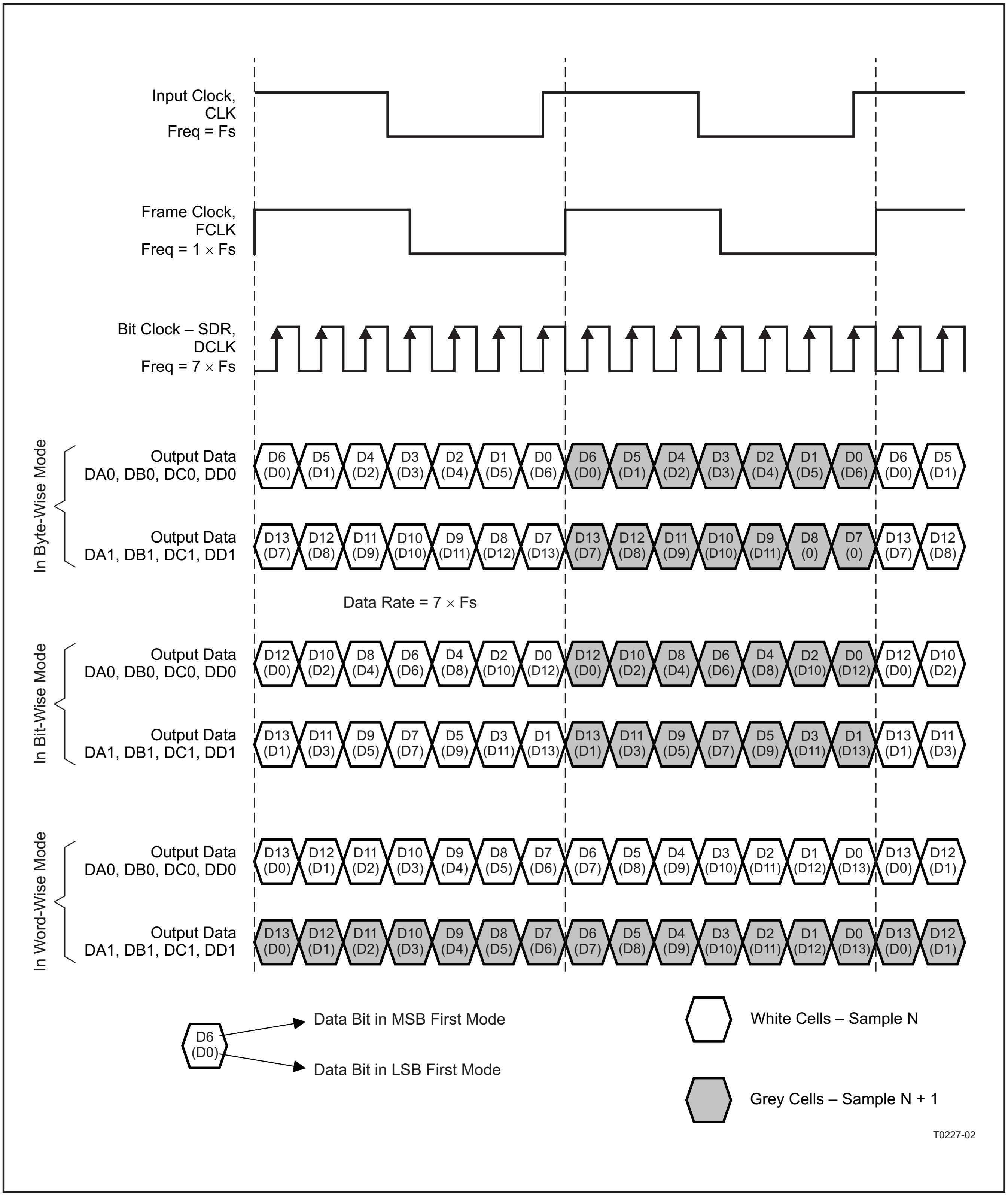


Figure 60. 2-Wire Interface 14× Serialization - SDR Bit Clock

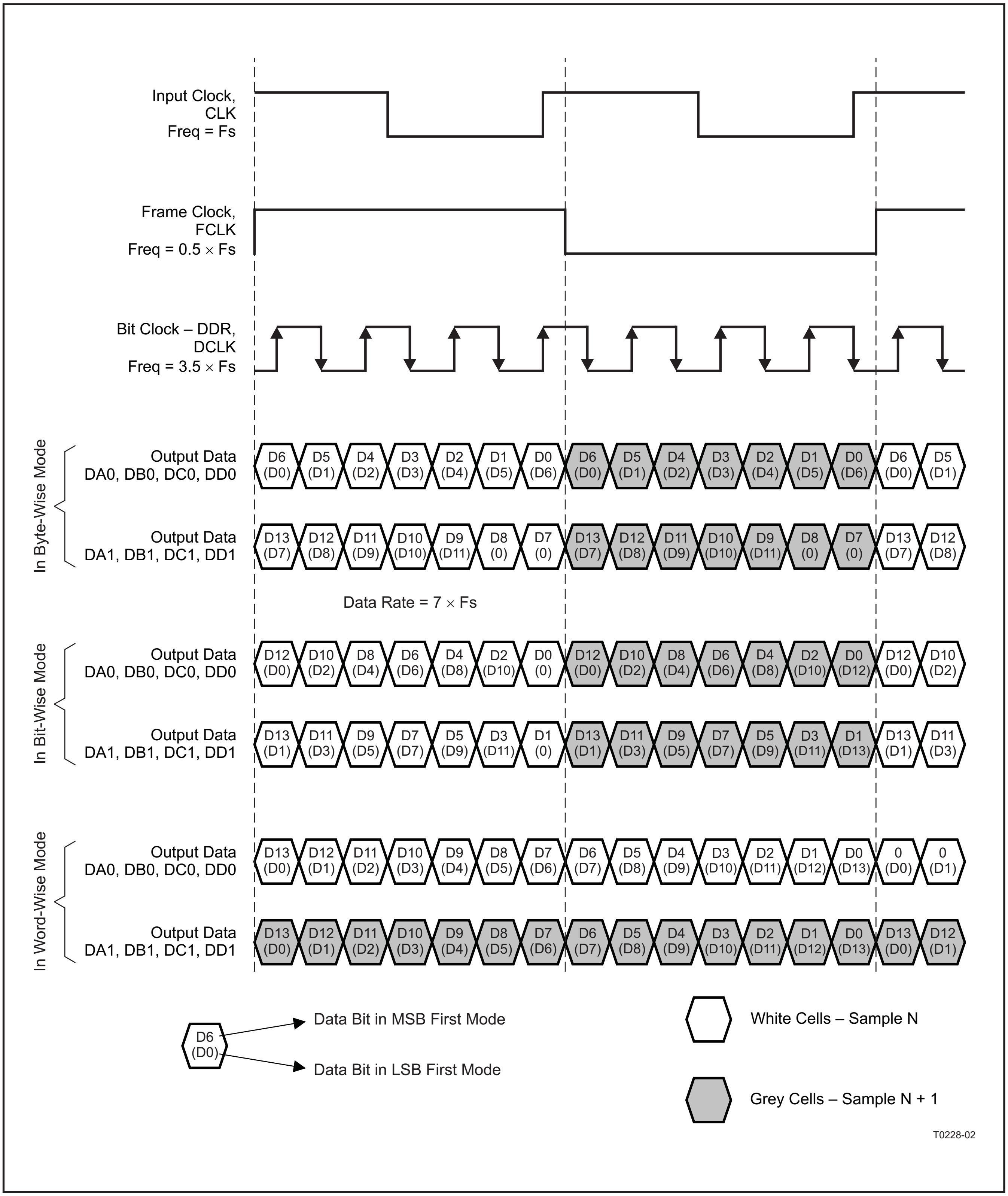


Figure 61. 2-Wire interface 14× Serialization - DDR Bit Clock

OUTPUT BIT ORDER

In the 2-wire interface, three types of bit order are supported - byte-wise, bit-wise and word-wise.

Byte-wise: Each 14 bit sample is split across the 2 wires. Wires DA0, DB0, DC0, and DD0 carry the 7 LSB bits D6 - D0 and wires DA1, DB1, DC1, and DD1 carry the 7 MSB bits.

Bit-wise: Each 14 bit sample is split across the 2 wires. Wires DA0, DB0, DC0 and DD0 carry the 7 even bits (D0, D2, D4...) and wires DA1, DB1, DC1 and DD1 carry the 7 odd bits (D1, D3, D5...).

Word-wise: In this case, all 14 bits of a sample are sent over a single wire. Successive samples are sent over the 2 wires. For example sample N is sent on wires DA0, DB0, DC0 and DD0, while sample N+1 is sent over wires DA1, DB1, DC1 and DD1. The frame clock frequency is 0.5x sampling frequency, with the rising edge aligned with the start of each word.

MSB/LSB FIRST

By default after reset, the 14 bit ADC data is output serially with the MSB first (D13, D12, D11,...D1, D0). The data can be output LSB first also by programming the register bit **<MSB_LSB_First>**. In the 2-wire mode, the bit order in each wire is flipped in the LSB first mode.

OUTPUT DATA FORMATS

Two output data formats are supported – 2s complement (default after reset) and offset binary. They can be selected using the serial interface register bit **<DF>**. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 0x3FFF in offset binary output format, and 0x1FFF in 2s complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x2000 in 2s complement output format.

LVDS CURRENT CONTROL

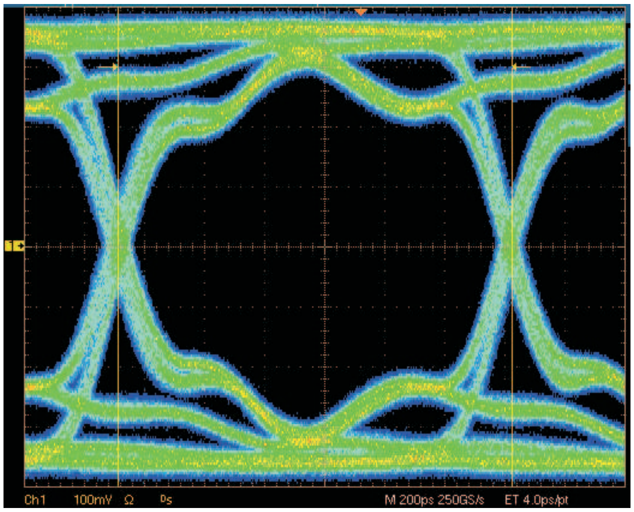
The default LVDS buffer current is 3.5 mA. With an external 100 Ω termination resistance, this develops ±350 mV logic levels at the receiver. The LVDS buffer currents also can be programmed to 2.5 mA, 3.0 mA, and 4.5 mA using the register bits **<LVDS CURR>**. In addition, there exists a current double mode, where the LVDS nominal current is doubled (register bits **<CURR DOUBLE>**, refer to Table 19).

LVDS INTERNAL TERMINATION

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. Five termination resistances are available – 166, 200, 250, 333, and 500 Ω (nominal with ±20% variation). Any combination of these terminations can be programmed; the effective termination is the parallel combination of the selected resistances. The terminations can be programmed separately for the clock and data buffers (bits **<TERM CLK>** and **<TERM DATA>**, refer to Table 20).

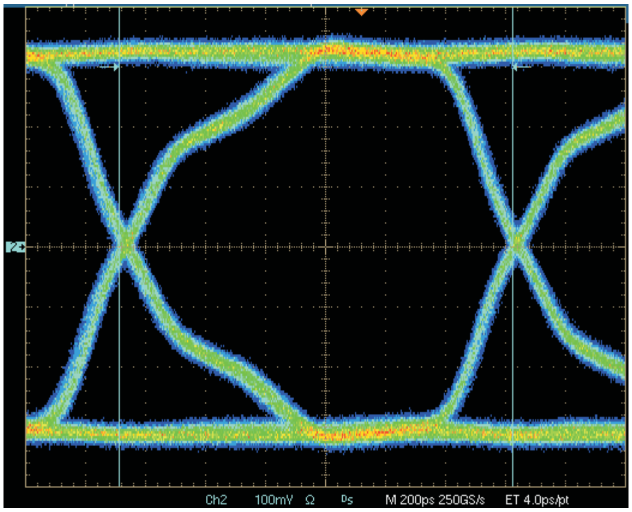
The internal termination helps to absorb any reflections from the receiver end, improving the signal integrity. This makes it possible to drive up to 10 pF of load capacitance, compared to only 5 pF without the internal termination. Figure 62 and Figure 63 show the eye diagram with 5 pF and 10 pF load capacitors (connected from each output pin to ground).

With 100 Ω internal and 100 Ω external termination, the voltage swing at the receiver end will be halved (compared to no internal termination). The voltage swing can be restored by using the LVDS current double mode (bits **<CURR DOUBLE>**, refer to Table 19).



C001

Figure 62. LVDS Data Eye Diagram With 5 pF Load Capacitance (No Internal Termination)



C002

Figure 63. LVDS Data Eye Diagram With 10 pF Load Capacitance (100 Ω Internal Termination)

CAPTURE TEST PATTERNS

ADS644X outputs the bit clock (DCLK), positioned nearly at the center of the data transitions. It is recommended to route the bit clock, frame clock and output data lines with minimum relative skew on the PCB. This ensures sufficient setup/hold times for a reliable capture by the receiver.

The DESKEW is a 1010... or 0101... pattern output on the serial data lines that can be used to verify if the receiver capture clock edge is positioned correctly. This may be useful in case there is some skew between DCLK and serial data inside the receiver. Once deserialized, it is required to ensure that the parallel data is aligned to the frame boundary. The SYNC test pattern can be used for this. For example, in the 1-wire interface, the SYNC pattern is 7 '1's followed by 7 '0's (from MSB to LSB). This information can be used by the receiver logic to shift the deserialized data until it matches the SYNC pattern.

In addition to DESKEW and SYNC, the ADS644X includes other test patterns to verify correctness of the capture by the receiver such as all zeros, all ones and toggle. These patterns are output on all four channel data lines simultaneously. Some patterns like custom and sync are affected by the type of interface selected, serialization and bit order.

Table 25. Test Patterns

PATTERN	DESCRIPTION
All zeros	Outputs logic low.
All ones	Outputs logic high.
Toggle	Outputs toggle pattern - <D13 – D0> alternates between 10101010101010 and 01010101010101 every clock cycle.
Custom	Outputs a 14 bit custom pattern. The 14 bit custom pattern can be specified into two serial interface registers. In the 2-wire interface, each code is sent over the 2 wires depending on the serialization and bit order.
Sync	Outputs a sync pattern.
Deskew	Outputs deskew pattern. Either <D13 – D0> = 10101010101010 or <D11 – D0> = 01010101010101 every clock cycle.

Table 26. SYNC Pattern

INTERFACE OPTION	SERIALIZATION	SYNC PATTERN ON EACH WIRE
1-Wire	14 X	**MSB**-11111110000000-**LSB**
	16 X	**MSB**-1111111100000000-**LSB**
2-Wire	14 X	**MSB**-1111000-**LSB**
	16 X	**MSB**-11110000-**LSB**

OUTPUT TIMINGS AT LOWER SAMPLING FREQUENCIES

Setup, hold, and other timing parameters are specified across sampling frequencies and for each type of output interface in the following tables.

Table 28 to Table 31: Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = LVDD = 3.3 V, C_L = 5 pF, I_O = 3.5 mA, R_L = 100 Ω, no internal termination, unless otherwise noted.

Timing parameters are ensured by design and characterization and not tested in production.

Ts = 1/ Sampling frequency = 1/Fs

Table 27. Clock Propagation Delay for Different Interface Options

INTERFACE	SERIALIZATION	CLOCK PROPAGATION DELAY, t_{pd_clk}	SERIALIZER LATENCY (1) clock cycles
1-Wire with DDR bit clock	14x	$t_{pd\_clk} = 0.428 \times T_s + t_{delay}$	0
	16x	$t_{pd\_clk} = 0.375 \times T_s + t_{delay}$	
2-Wire with DDR bit clock	14x	$t_{pd\_clk} = 0.857 \times T_s + t_{delay}$	2 (when $t_{pd\_clk} \geq T_s$)
			1 (when $t_{pd\_clk} < T_s$)
2-Wire with SDR bit clock		$t_{pd\_clk} = 0.428 \times T_s + t_{delay}$	0
2-Wire with DDR bit clock	16x	$t_{pd\_clk} = 0.75 \times T_s + t_{delay}$	1 (when $t_{pd\_clk} \geq T_s$)
			0 (when $t_{pd\_clk} < T_s$)
2-Wire with SDR bit clock		$t_{pd\_clk} = 0.375 \times T_s + t_{delay}$	0

(1) Note that the total latency = ADC latency + internal serializer latency. The ADC latency is 12 clock cycles.

Table 28. Timing for 1-Wire Interface

SERIALIZATION	SAMPLING FREQUENCY MSPS	DATA SETUP TIME, t_{su} ns			DATA HOLD TIME, t_h ns			t_{delay} ns		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
14×	65	0.3	0.5		0.4	0.6			$F_s \geq 40$ MSPS	
	40	0.65	0.85		0.7	0.9		3	4	5
	20	1.3	1.65		1.6	1.9			$F_s < 40$ MSPS	
	10	3.2	3.5		3.2	3.6		3	4.5	6
16×	65	0.22	0.42		0.35	0.55			$F_s \geq 40$ MSPS	
								3	4	5
									$F_s < 40$ MSPS	
								3	4.5	6

Table 29. Timing for 2-Wire Interface, DDR Bit Clock

SERIALIZATION	SAMPLING FREQUENCY MSPS	DATA SETUP TIME, t_{su} ns			DATA HOLD TIME, t_h ns			t_{delay} ns		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
14×	105	0.45	0.65		0.5	0.7			$F_s \geq 45$ MSPS	
	92	0.55	0.75		0.6	0.8		3.4	4.4	5.4
	80	0.65	0.85		0.7	0.9				
	65	0.8	1.1		0.8	1.1			$F_s < 45$ MSPS	
	40	1.4	1.7		1.5	1.9		3.7	5.2	6.7
16×	105	0.35	0.55		0.4	0.6			$F_s \geq 45$ MSPS	
	92	0.45	0.65		0.5	0.7		3.4	4.4	5.4
	80	0.55	0.75		0.6	0.8				
	65	0.6	0.9		0.7	1			$F_s < 45$ MSPS	
	40	1.1	1.4		1.3	1.7		3.7	5.2	6.7

Table 30. Timing for 2-Wire Interface, SDR Bit Clock

SERIALIZATION	SAMPLING FREQUENCY MSPS	DATA SETUP TIME, t_{su} ns			DATA HOLD TIME, t_h ns			t_{delay} ns		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
14×	65	0.8	1		1	1.2			**F_s ≥ 40 MSPS**	
	40	1.5	1.7		1.6	1.8		3.4	4.4	5.4
	20	3.4	3.6		3.3	3.5			**F_s < 40 MSPS**	
	10	6.9	7.2		6.6	6.9		3.7	5.2	6.7
16×	65	0.65	0.85		0.8	1.0			**F_s ≥ 40 MSPS**	
	40	1.3	1.5		1.4	1.6		3.4	4.4	5.4
	20	2.8	3.0		2.8	3.0			**F_s < 40 MSPS**	
	10	6.0	6.3		5.8	6.1		3.7	5.2	6.7

Table 31. Output Jitter (applies to all interface options)

SAMPLING FREQUENCY MSPS	BIT CLOCK JITTER, CYCLE-CYCLE ps, peak-peak			FRAME CLOCK JITTER, CYCLE-CYCLE ps, peak-peak		
	MIN	TYP	MAX	MIN	TYP	MAX
≥ 65		350			75	

BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give optimum performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. Refer to the EVM User Guide (SLAU196) for board layout schemes.

Supply Decoupling

As the ADS644X already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that the decoupling capacitors can help to filter external power supply noise, so the optimum number of decoupling capacitors would depend on actual application.

It is recommended to use separate supplies for the analog and digital supply pins to isolate digital switching noise from sensitive analog circuitry. In case only a single 3.3 V supply is available, it should be routed first to AVDD. It can then be tapped and isolated with a ferrite bead (or inductor) with decoupling capacitor, before being routed to LVDD.

Exposed Thermal Pad

It is necessary to solder the exposed pad at the bottom of the package to a ground plane for best thermal performance. For detailed information, see application notes QFN Layout Guidelines(SLOA122A) and QFN/SON PCB Attachment (SLUA271A).

DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay will be different across channels. The maximum variation is specified as aperture delay variation (channel-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. The gain error does not include the error caused by the internal reference deviation from ideal value. This is specified separately as internal reference error. The maximum variation of the gain error across devices and across channels within a device is specified separately.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference T_{MAX}–T_{MIN}.

Signal-to-Noise Ratio(SNR) is the ratio of the power of the fundamental (PS) to the noise floor power (PN), excluding the power at DC and the first nine harmonics.

$$\text{SNR} = 10\text{Log}10\frac{P_S}{P_N} \tag{3}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$\text{SINAD} = 10\text{Log}10\frac{P_S}{PN + PD} \tag{4}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB) – The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{5}$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (PD).

$$\mathrm{THD} = 10\mathrm{Log}10\frac{P_S}{PD} \quad (6)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1 – f2 or 2f2 – f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter’s full-scale range.

DC Power Supply Rejection Ratio (DC PSRR) – The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

AC Power Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔVsup is the change in supply voltage and ΔVout is the resultant change of the ADC output code (referred to the input), then

$$\mathrm{PSRR} = 20\mathrm{Log}10\frac{\Delta\mathrm{Vout}}{\Delta\mathrm{Vsup}},\ \text{expressed in dBc} \quad (7)$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6-dB positive and negative overload. The deviation of the first few samples after the overload (from their expected values) is noted.

Common Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔVcm_in is the change in the common-mode voltage of the input pins and ΔVout is the resultant change of the ADC output code (referred to the input), then

$$\mathrm{CMRR} = 20\mathrm{Log}10\frac{\Delta\mathrm{Vout}}{\Delta\mathrm{Vcm\_in}},\ \text{expressed in dBc} \quad (8)$$

Cross-Talk (only for multi-channel ADC)– This is a measure of the internal coupling of a signal from adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Cross-talk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS6444MRGCTEP	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	6444EP	Samples
ADS6445MRGCTEP	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	6445EP	Samples
V62/08628-01XE	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	6445EP	Samples
V62/08628-02XE	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	6444EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ADS6444-EP, ADS6445-EP :

- Catalog: ADS6444, ADS6445

NOTE: Qualified Version Definitions:

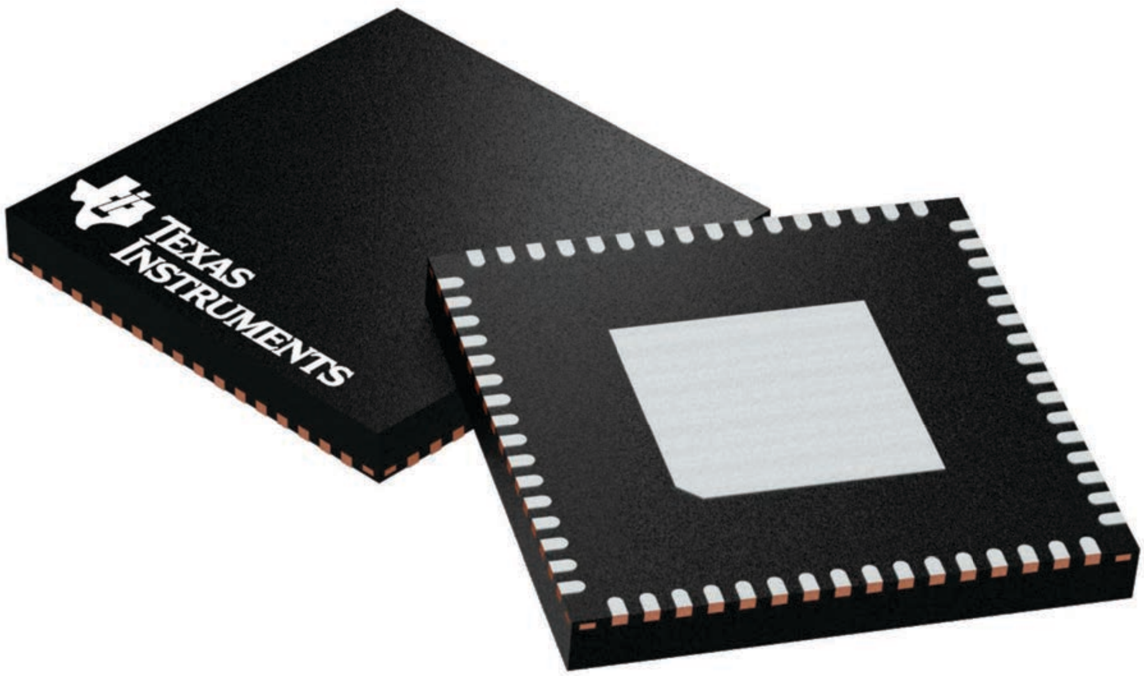
- Catalog - TI's standard catalog product

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

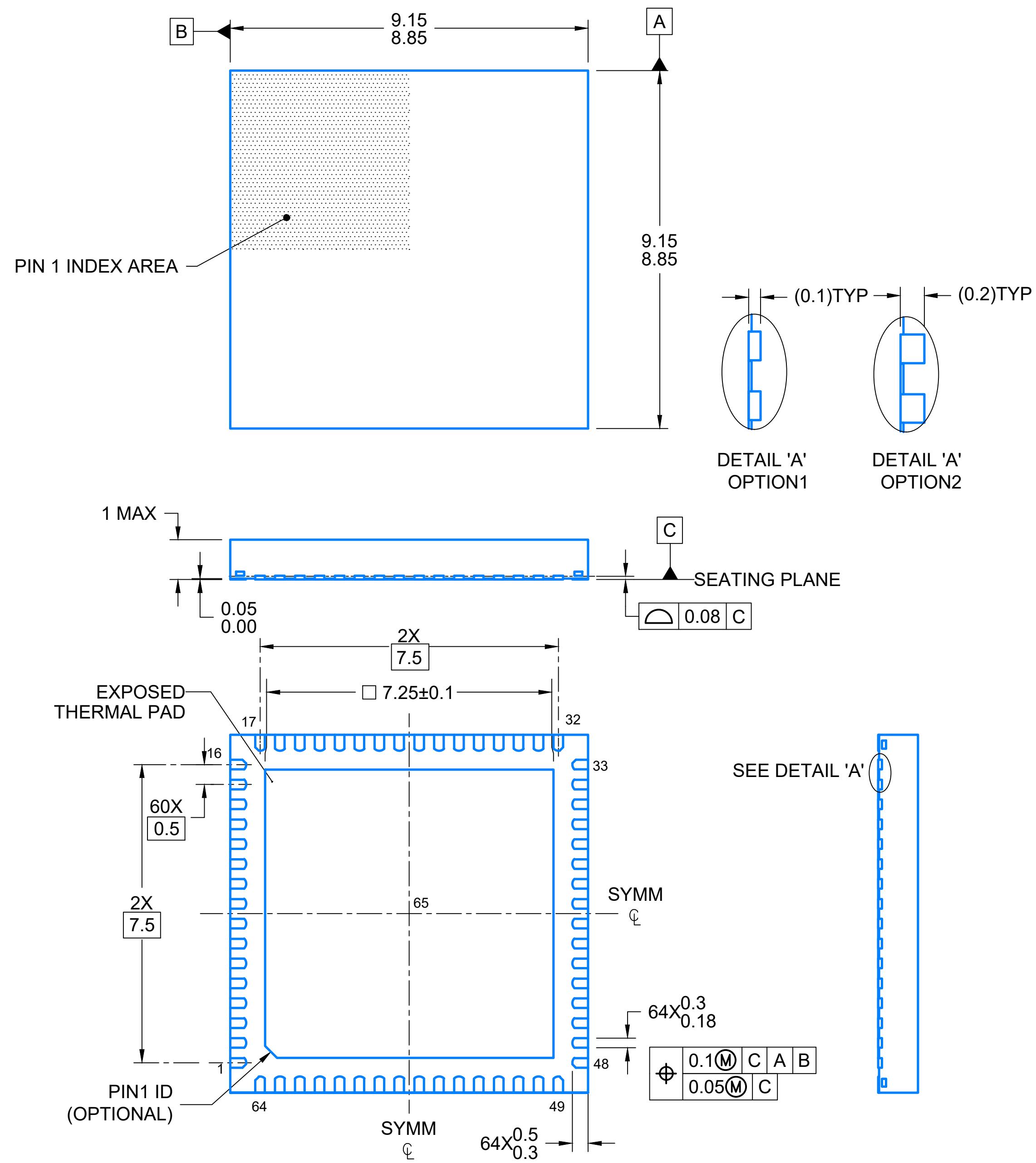
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A

PLASTIC QUADFLAT PACK- NO LEAD



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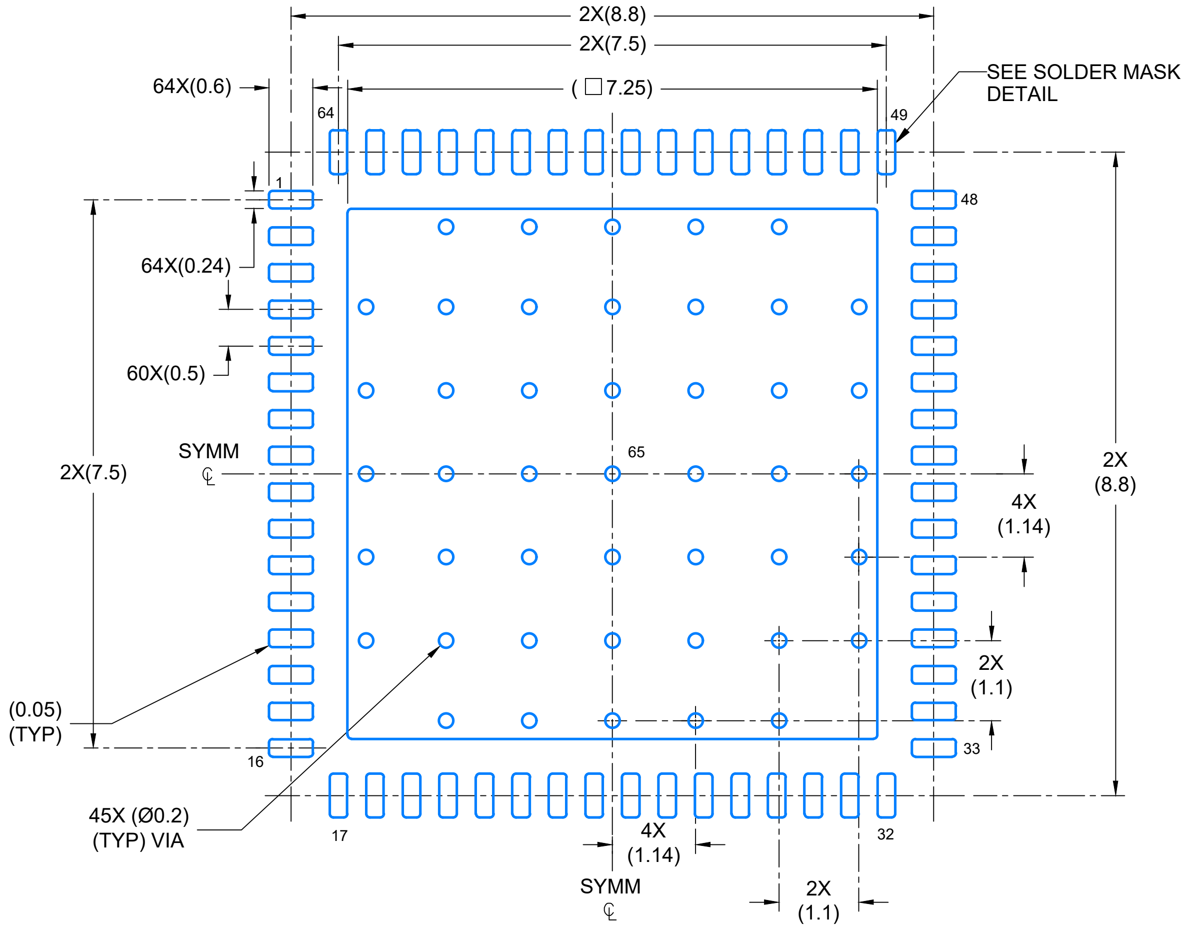
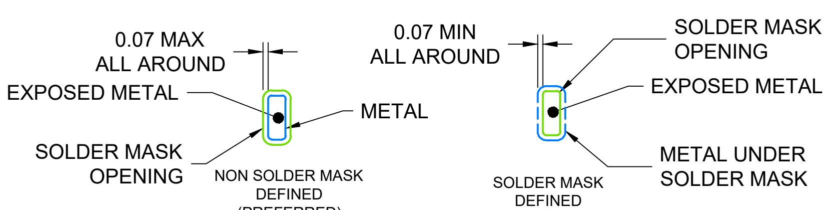
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 10X



SOLDER MASK DETAILS

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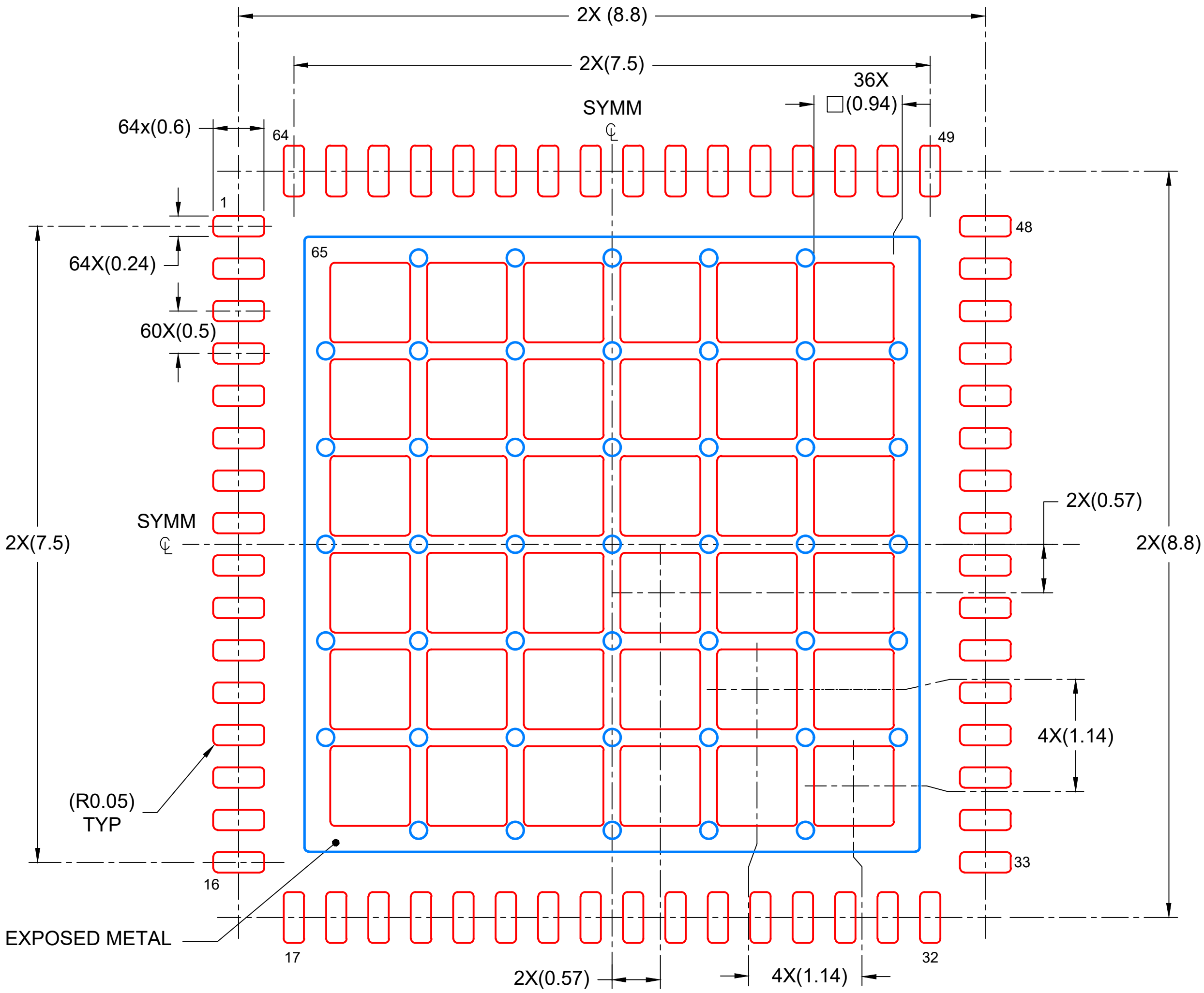
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.