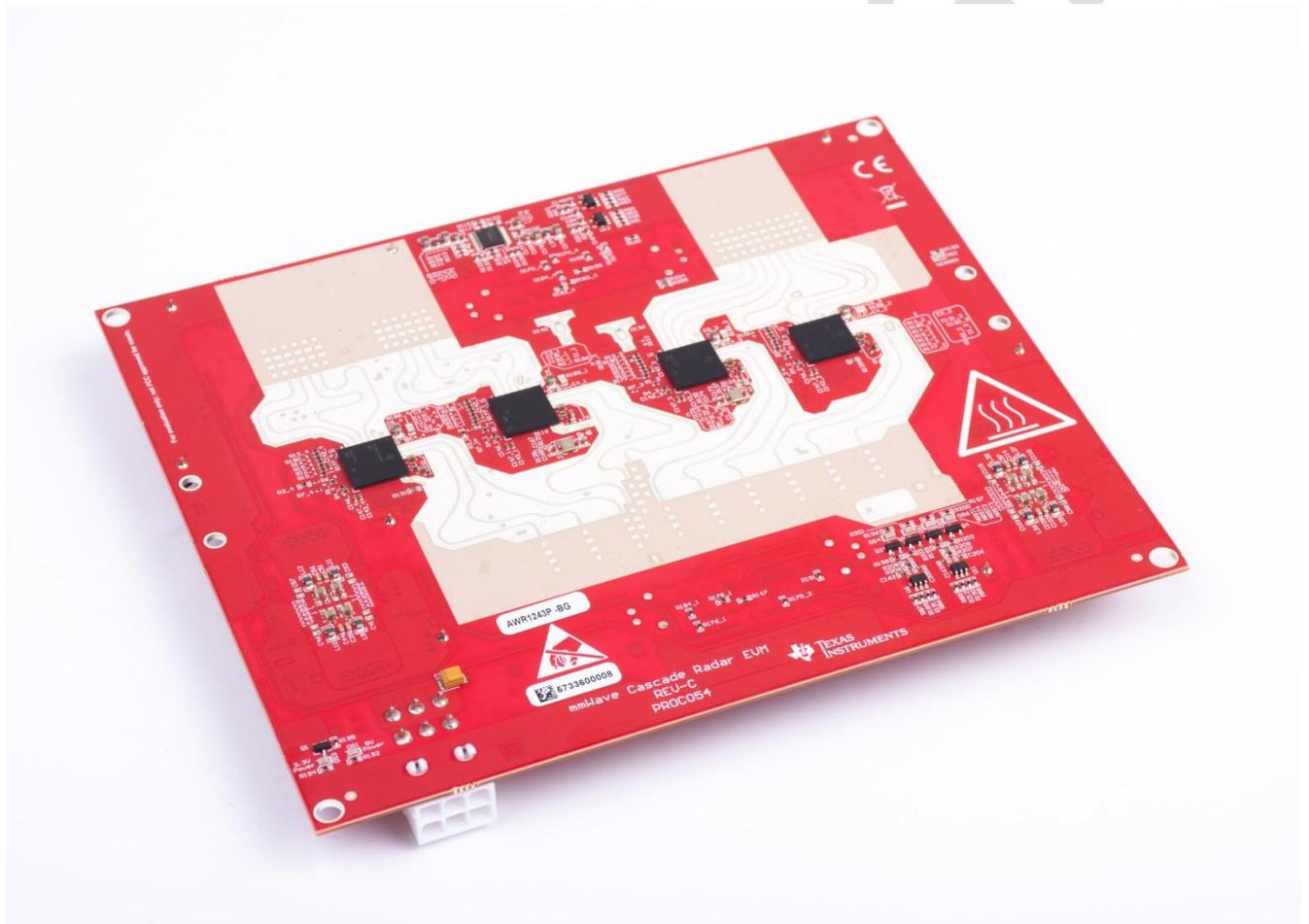


MMWCAS-RF-EVM (PROC054C) – Fabrication Test Plan

1 Summary

This production test document describes the different tests which shall be expected to be performed on each Cascade RF board (TI PROC054, MMWCAS-RF-EVM). This document outlines tests to be performed by the selected PCB fabricator, tests to be performed by the selected PCB assembler and prior to the assembled system being accepted by Texas Instruments. This documented shall be updated with newly defined or modified tests as required.

This document shall be referenced in PCB CAD fabrication drawings. This document must be discussed and agreed upon by the selected PCB fabricator and assembler used for this design as part of the formal statement of work process to ensure yield and quality of the TI EVM.



2 Table of Contents

1	SUMMARY	1
2	TABLE OF CONTENTS	2
3	GLOSSARY	3
4	INTRODUCTION	4
5	HARDWARE FABRICATION, ASSEMBLY AND TEST SPECIFICATIONS.....	5
5.1	HARDWARE FABRICATION TEST SPECIFICATIONS.....	5
5.1.1	<i>Pre-Fabrication Accuracy Testing and Iterations</i>	5
5.1.1.1	Critical RF Etch Regions.....	5
5.1.1.2	Etching Accuracy.....	9
5.1.1.3	Stack-Up, Via and Etch Profile Height Accuracy / Cross-Section Measurements.....	13
5.1.1.4	Drill Location and Size Accuracy.....	21
5.1.1.5	Etch and Mask Registration Accuracy Relative to Drills.....	21
5.1.2	<i>Post-Fabrication Accuracy Inspections</i>	21
5.2	HARDWARE ASSEMBLY TEST SPECIFICATIONS.....	22
5.2.1	<i>Pre-Assembly Test Specifications</i>	22
5.2.2	<i>Post-Assembly Test Specifications</i>	22
5.3	SYSTEM TEST SPECIFICATIONS.....	ERROR! BOOKMARK NOT DEFINED.
5.3.1	<i>Basic Radar Functionality Test</i>	Error! Bookmark not defined.
5.3.2	<i>Basic Radar Performance Test (TBD – NOT YET REQUIRED)</i>	Error! Bookmark not defined.
6	CRITICAL DOCUMENT REFERENCES.....	23
7	REVISION HISTORY	23

3 Glossary

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Preliminary

4 Introduction

The AWR1243P Cascade RF Board is the RF portion of the TI Cascade Radar evaluation kit. The full cascade radar system solution consists of an AWR1243P RF Board mated to a TDA2x Host Processor Board.

Compared to the single device Boosterpack EVM, with only 3TX and 4RX channels, this solution enables the evaluation of a 12 TX, 16 RX antenna array which provides for higher angular resolution MIMO and longer range beamforming performance.

The Cascade RF design is based on the cascade radar solution which the TI ADAS processor and Automotive Radar teams have developed. This design in turn was based on the TDA2/Vayu EVM and the AWR1243 Boosterpack and RF Characterization (CZ) board designs.

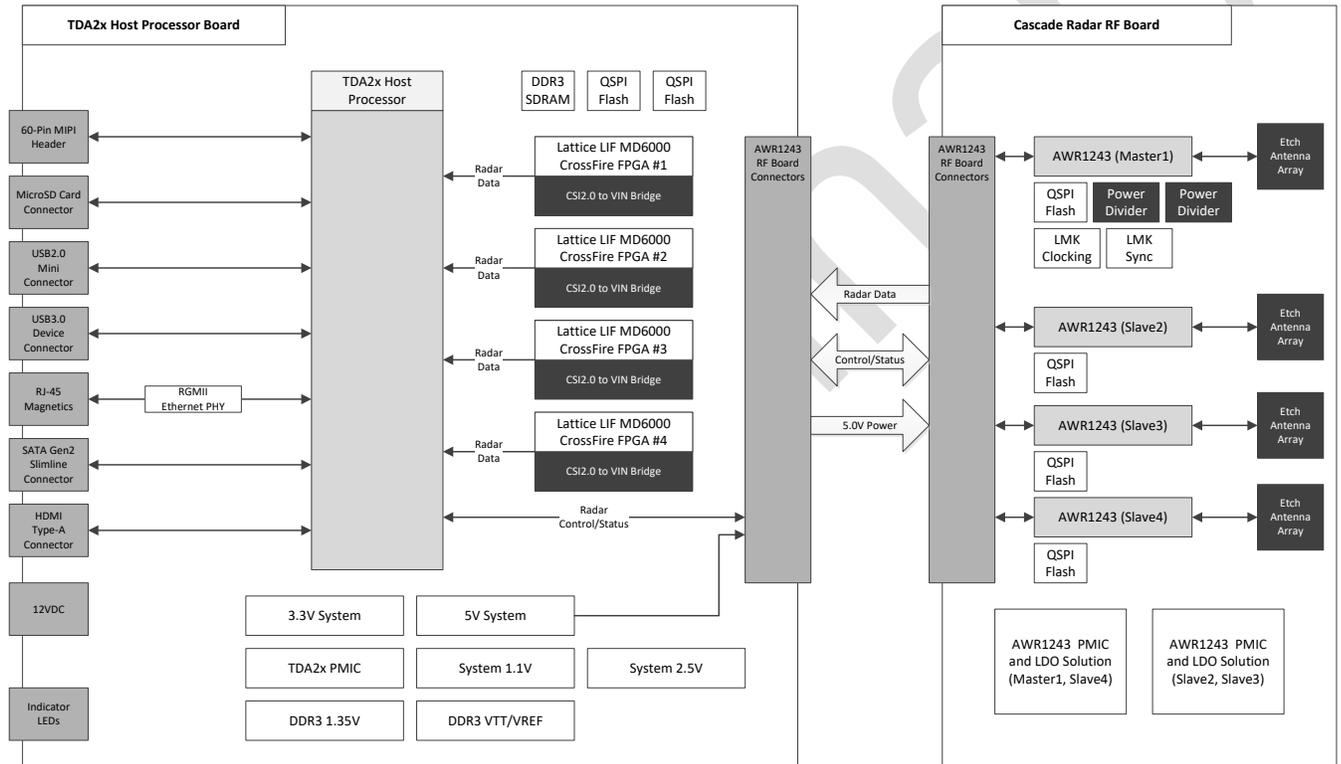


Figure 1 - TI Cascade Radar Evaluation System. TDA2x Host Board (left) Shown Attached to RF Cascade Board (right)

5 Hardware Fabrication, Assembly and Test Specifications

This section describes the fabrication, assembly and post-assembly test specifications for the Cascade Radar RF Board. The Host Board and Cascade RF Board integrated testing is described.

5.1 Hardware Fabrication Test Specifications

This section describes the inspections and tests to be performed during the initial PCB stack fabrication process.

5.1.1 Pre-Fabrication Accuracy Testing and Iterations

This section describes pre-fabrication, iterative fabrication testing that is needed to establish accuracy limits of a PCB fabricators process steps. These steps will also be used to establish any necessary adjustments required to a PCB fabricators process steps needed to ensure RF structure accuracy.

This process consists of the following steps:

1. Running a number of panels through the entire fabrication process and inspecting the result prior to any full lot run.
2. Each test panel run shall be used to gauge the accuracy of of the etching process, mask registration and drill registration.
3. Design dimensions shall be compared to the achieved fabricated dimensions.
4. Based on this comparison process modifications shall be implemented (etch times, mask offsets, drill offsets, additional registration fiducials or any additional tooling required).
5. These steps are then repeated until design to fabrication differences are under required minimums.

5.1.1.1 Critical RF Etch Regions

This section calls out the critical RF structure regions.

This PCB has multiple etched antenna arrays on the metal layer 1 (top) which require high etching tolerance to achieve expected RF performance.

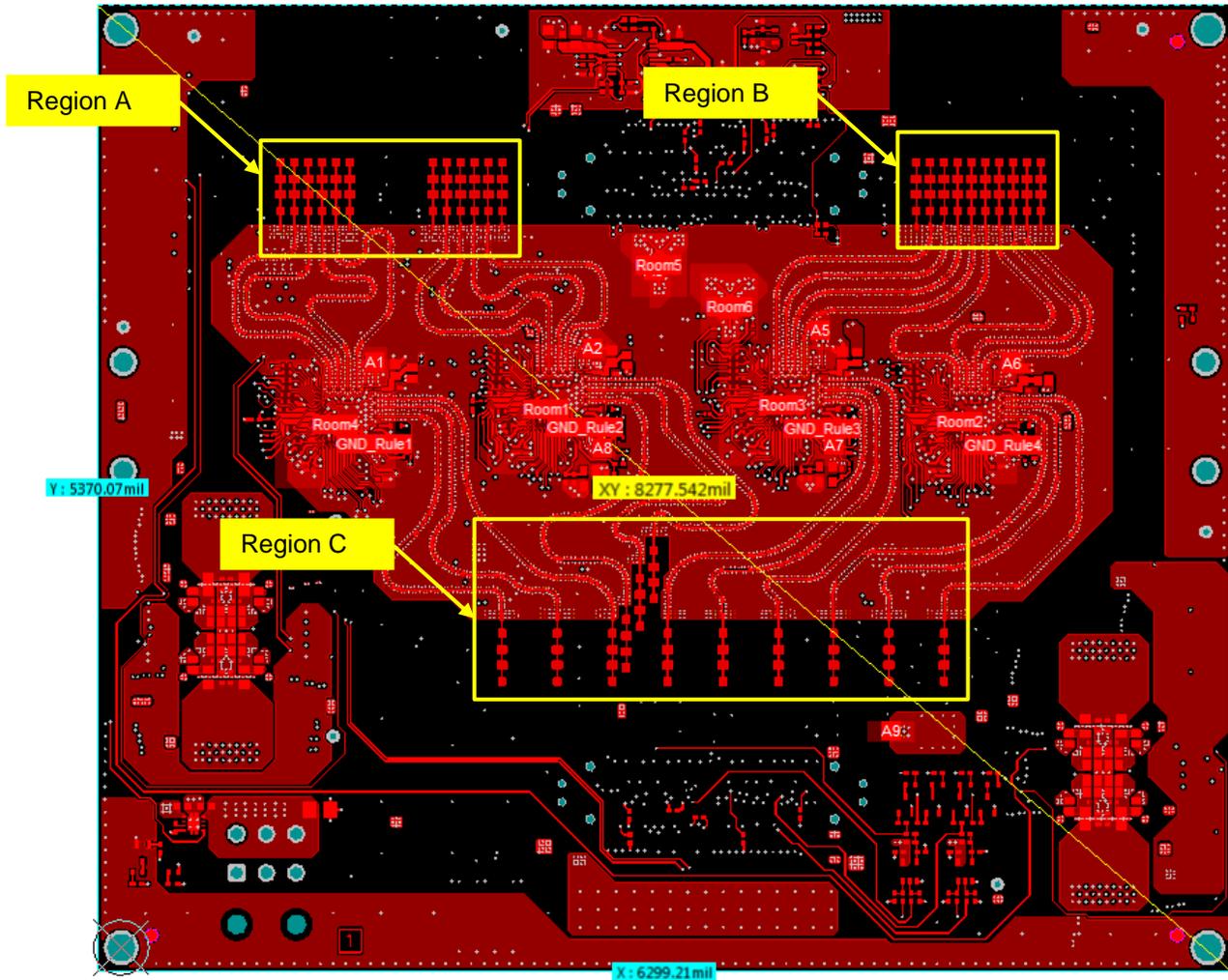


Figure 2 - Antenna Etching Critical Areas. Excerpted from Cascade RF Revision, Metal Layer 1 (top), C Altium Database (SVN revision 579)

PRELIMINARY

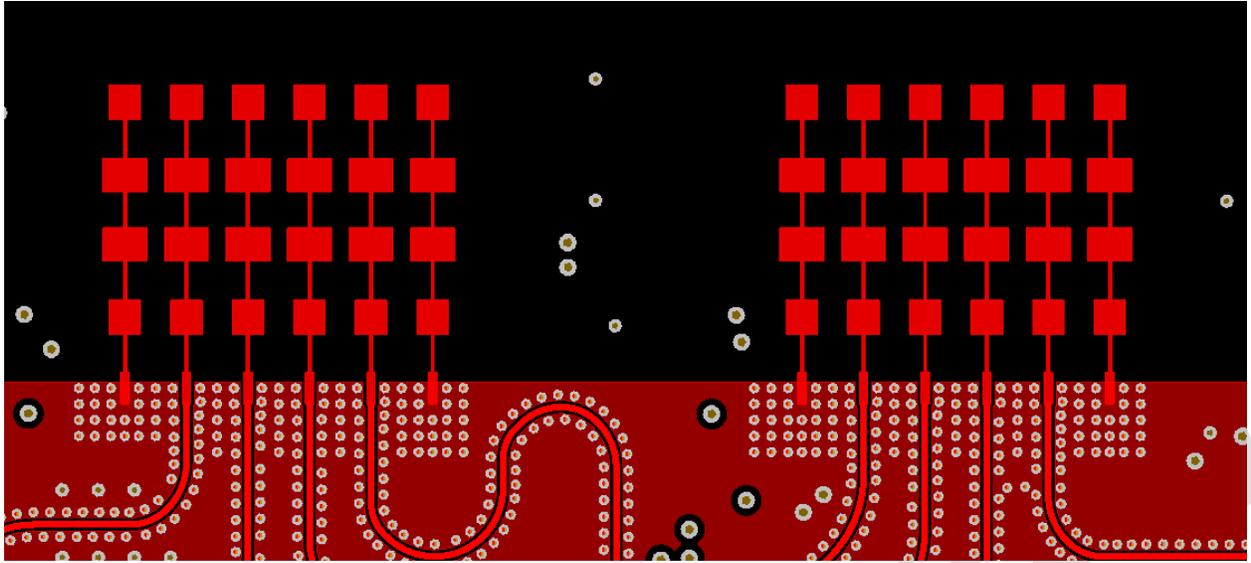


Figure 3 - Antenna Etching Critical Area – Region A. Excerpted from Cascade RF Revision, Metal Layer 1 (top), C Altium Database (SVN revision 579)

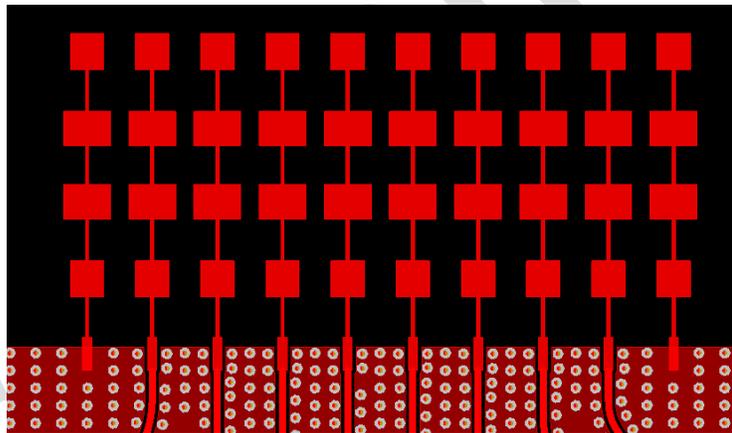


Figure 4 - Antenna Etching Critical Areas – Region B. Excerpted from Cascade RF Revision, Metal Layer 1 (top), C Altium Database (SVN revision 579)

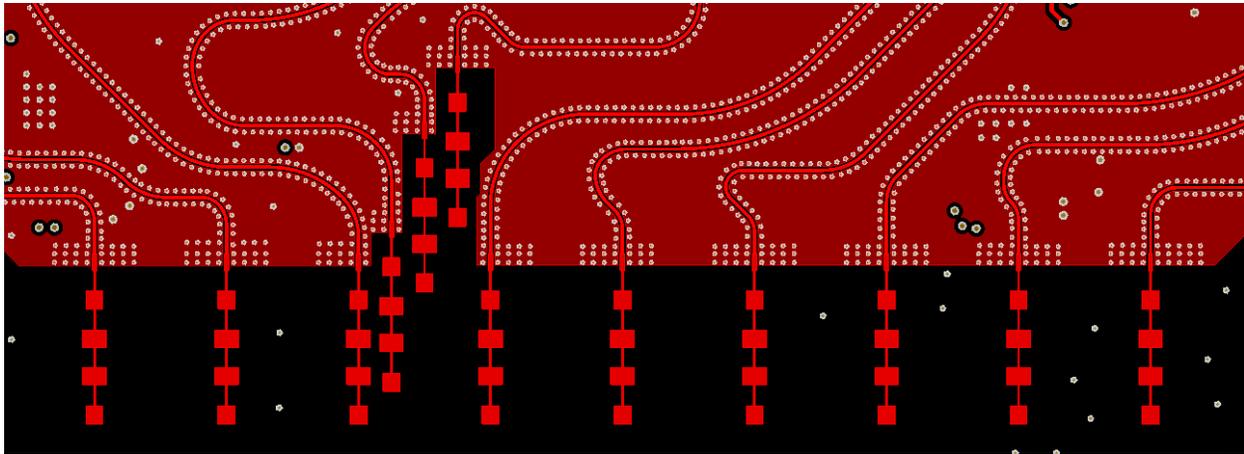


Figure 5 - Antenna Etching Critical Areas – Region C

Excerpted from Cascade RF Revision, Metal Layer 1 (top), C Altium Database (SVN revision 579)

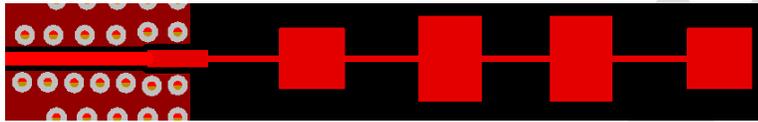


Figure 6 - Antenna Etching Critical Areas – Single Antenna Element

Excerpted from Cascade RF Revision, Metal Layer 1 (top), C Altium Database (SVN revision 579)

5.1.1.2 Etching Accuracy

This section defines critical antenna etching dimensions for the regions identified in the previous section.

In all chemical etching processes, the “top” of the copper structure will be over-etched relative to the bottom of the structure, resulting in a non-uniform trace width or side-wall profile to the copper shapes.

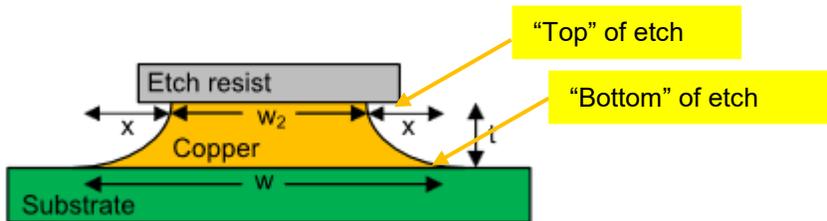


Figure 7 – Example of typical side-wall, etching profile seen in all PCB chemical etching processes

For the antenna structures called out here, for best performance, the target design dimensions must be the achieved as close as possible on the “top” of the resulting etched copper shapes. The etching process must be adjusted to meet the design dimensions on the “top” of the resulting copper shapes.

Tolerance of all etching must stay within +/- 20um (+/- 0.787mils)

Each of these dimensions shall be verified by the fabricator post-fabrication to ensure that all critical dimensions are achieved prior to the PCB being accepted for assembly and test. Each critical region is composed of an array of etched antenna elements. Each etched antenna element are themselves composed of rectangular patches and small width traces of varying dimension.

5.1.1.2.1 Antenna Etching

This section defines critical antenna etching dimensions for the regions identified in the previous section.

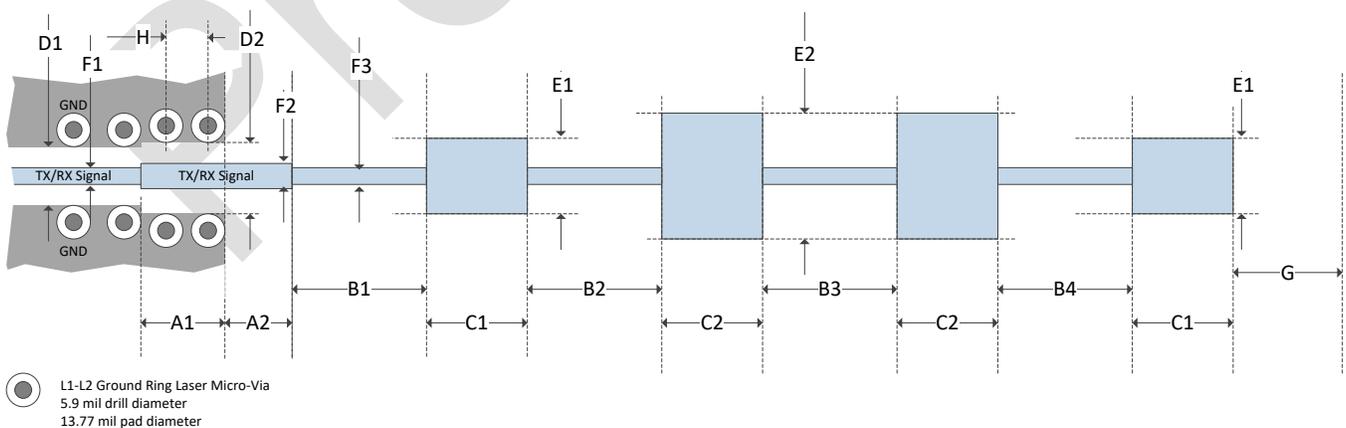


Figure 8 - Single Antenna Element Dimensions

Table 1 - Single Antenna Element Dimensions – Reference Associated Artwork For All Design Dimensions. Extracted dimensions provided here for reference only.

Dimension	Nominal Value (mils)	Error(+/-) (mils)	Min Value (mils)	Max Value (mils)
A1	27.568	0.787	26.781	28.355
A2	11.802	0.787	11.015	12.589
B1	47.24	0.787	46.453	48.027
B2	49.21	0.787	48.423	49.997
B3	45.27	0.787	44.483	46.057
B4	49.21	0.787	48.423	49.997
C1	42.52	0.787	41.733	43.307
C2	40.95	0.787	40.163	41.737
D1	16.722	0.787	15.935	17.509
D2	20.002	0.787	19.215	20.789
E1	39.38	0.787	38.593	40.167
E2	55.12	0.787	54.333	55.907
F1	8.4	0.787	7.613	9.187
F2	10.62	0.787	9.833	11.407
F3	3.94	0.787	3.153	4.727
G	78.7402	0.787	77.9532	79.5272
H	20.67	0.787	19.883	21.457

Table 1, Note 1 - Dimension G denotes the minimum distance the edge of the patch elements shall come to the edge of the continuous ground reference plane. This may be the edge of the PCB (as in the case of the BoosterPack EVM) or an internal edge.

Table 1, Note 2 - Dimension H denotes the minimum ground stitch via center-to-center distance.

5.1.1.2.2 RF and LO BGA Fan-Out Etching

This section defines critical RF and LO BGA fan-out etching dimensions. This applies to each AWRx device BGA footprint for the RF and LO BGA positions.

RF TX BGA: B4, B6, B8

RF RX BGA: M2, K2, H2, F2

LO BGA: B1, D1, B15

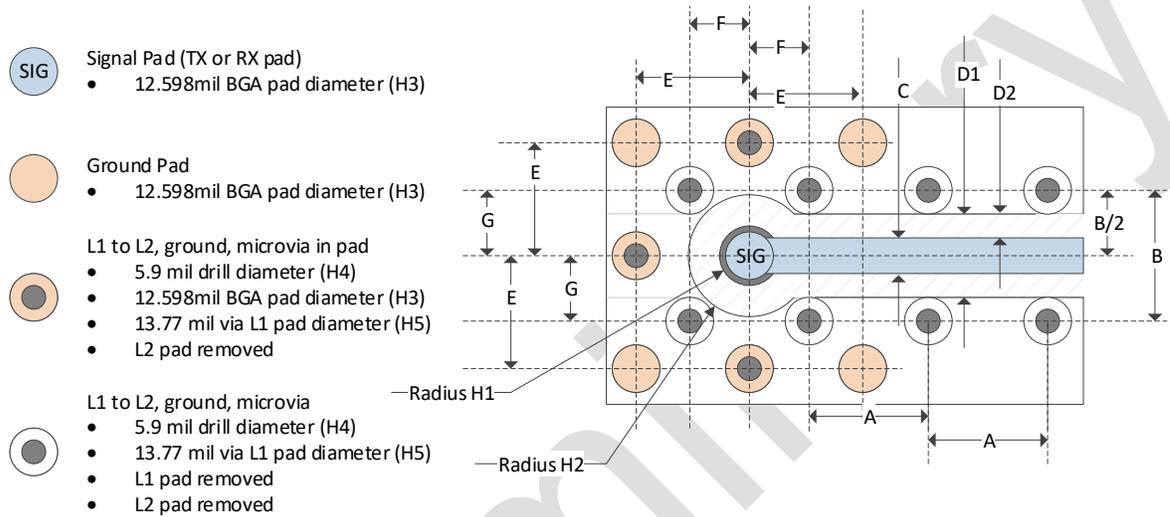


Figure 9 – RF and LO BGA Fan-Out Dimensions

Table 2 - RF and LO BGA Fan-Out Dimensions – Reference Associated Artwork For All Design Dimensions. Extracted dimensions provided here for reference only.

Dimension	Nominal Value (mils)	Error(+/-) (mils)	Min Value (mils)	Max Value (mils)
A	20.67	0.787	19.883	21.457
B	30.68	0.787	29.893	31.467
C	8.4	0.787	7.613	9.187
D1	16.722	0.787	15.935	17.509
D2	4.161	0.787	3.374	4.948
E	25.589	0.787	24.802	26.376
F	17.72	0.787	16.933	18.507
G	15.35	0.787	14.563	16.137
H1	7.681	0.787	6.894	8.468
H2	16.3	0.787	15.513	17.087
H3	12.598	0.787	11.811	13.385
H4	5.9	0.787	5.113	6.687
H5	13.77	0.787	12.983	14.557

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5.1.1.3 Stack-Up, Via and Etch Profile Height Accuracy / Cross-Section Measurements

Final stack-up height, via profiles and RF/LO path etches shall be measured during initial pre-fabrication accuracy testing iteration cycles and the measurements provided to TI for review prior to proceeding to full fabrication. The following sections detail the locations on the PCB where TI would like the fabricator to cross-section the design.

This process is currently states no requirements. It is only specifying required data from the fabricated PCB stack. The resulting data is needed for simulation baselining and gauging future design requirements for critical RF structures.

5.1.1.3.1 Layer 1 RF TX/RX GCPW

A single sample cross-section should be taken across the x and y-axis of the identified RF GCPW regions shown below. This will serve as a representative sample of the etch properties for all of the similarly constructed regions shown below. Cuts should be made to include via structures adjacent to signal paths where present.

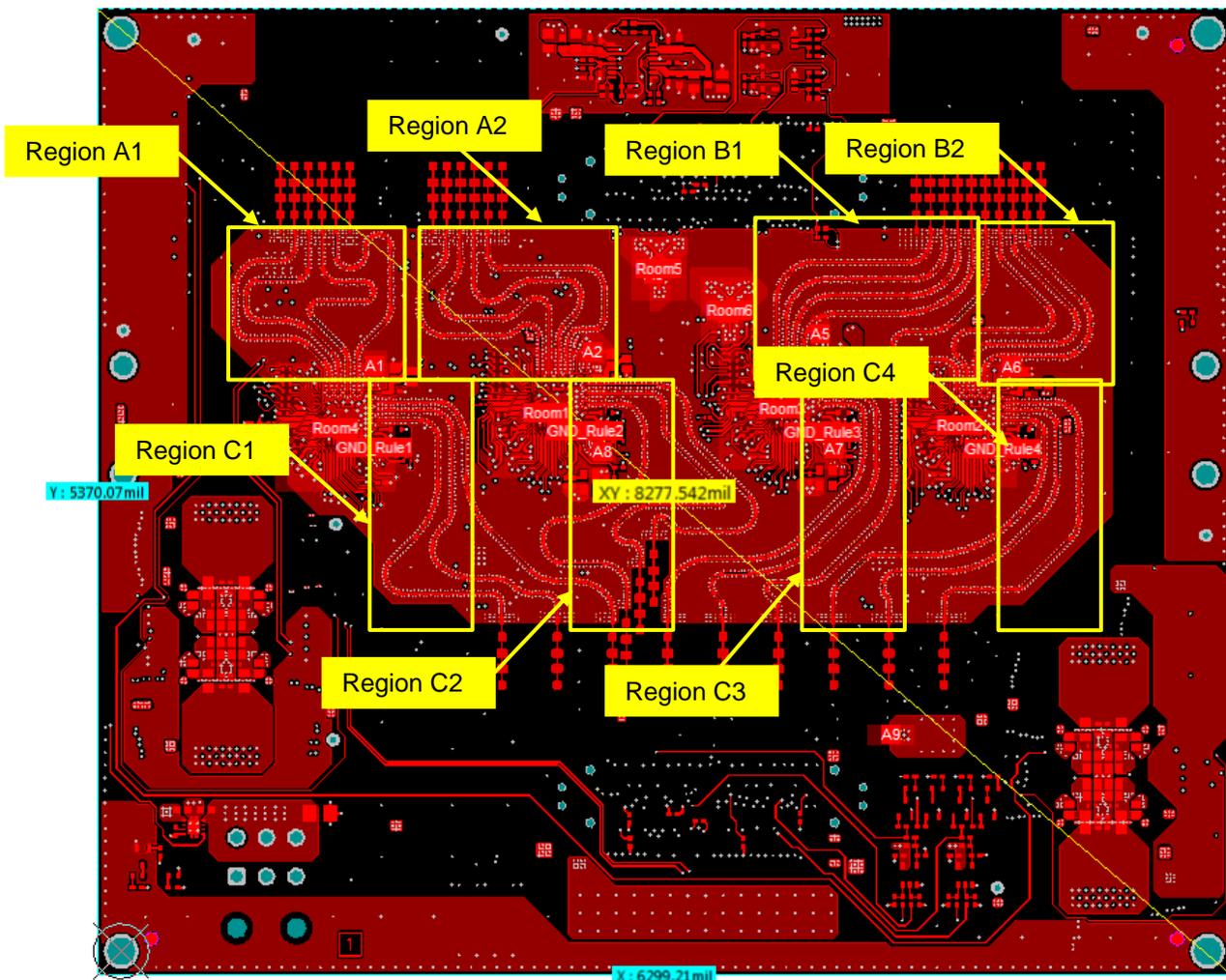


Figure 10 – RF GCPW Regions

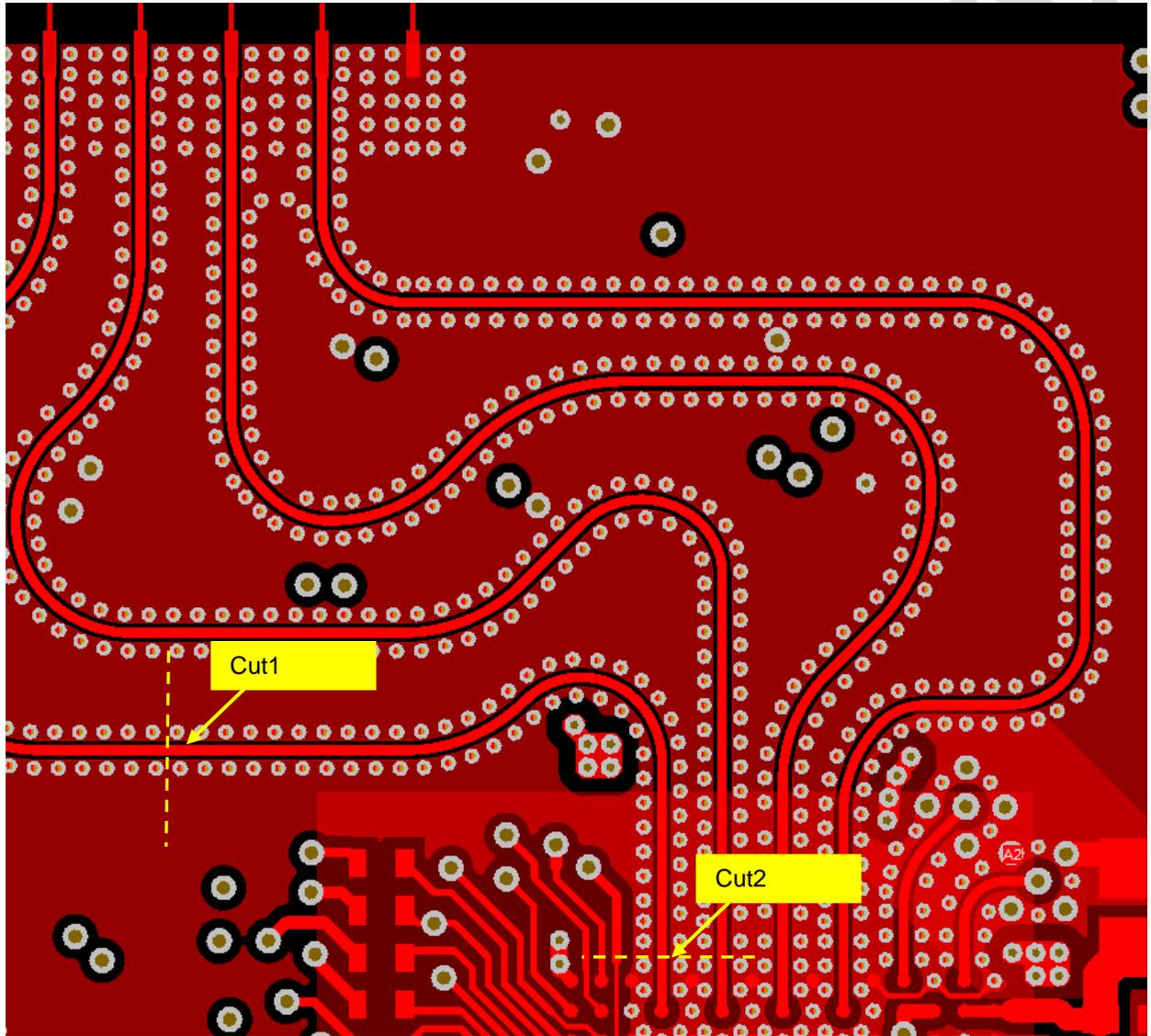


Figure 11 – Region A2 – RX RF GCPW Cuts

5.1.1.3.2 Layer 1 RF TX/RX Patch Antenna

A single sample cross-section should be taken across the x and y-axis of the identified RF patch antenna regions shown below. This will serve as a representative sample of the etch properties for all of the similarly constructed regions shown below. Cuts should be made to include via structures adjacent to signal paths where present.

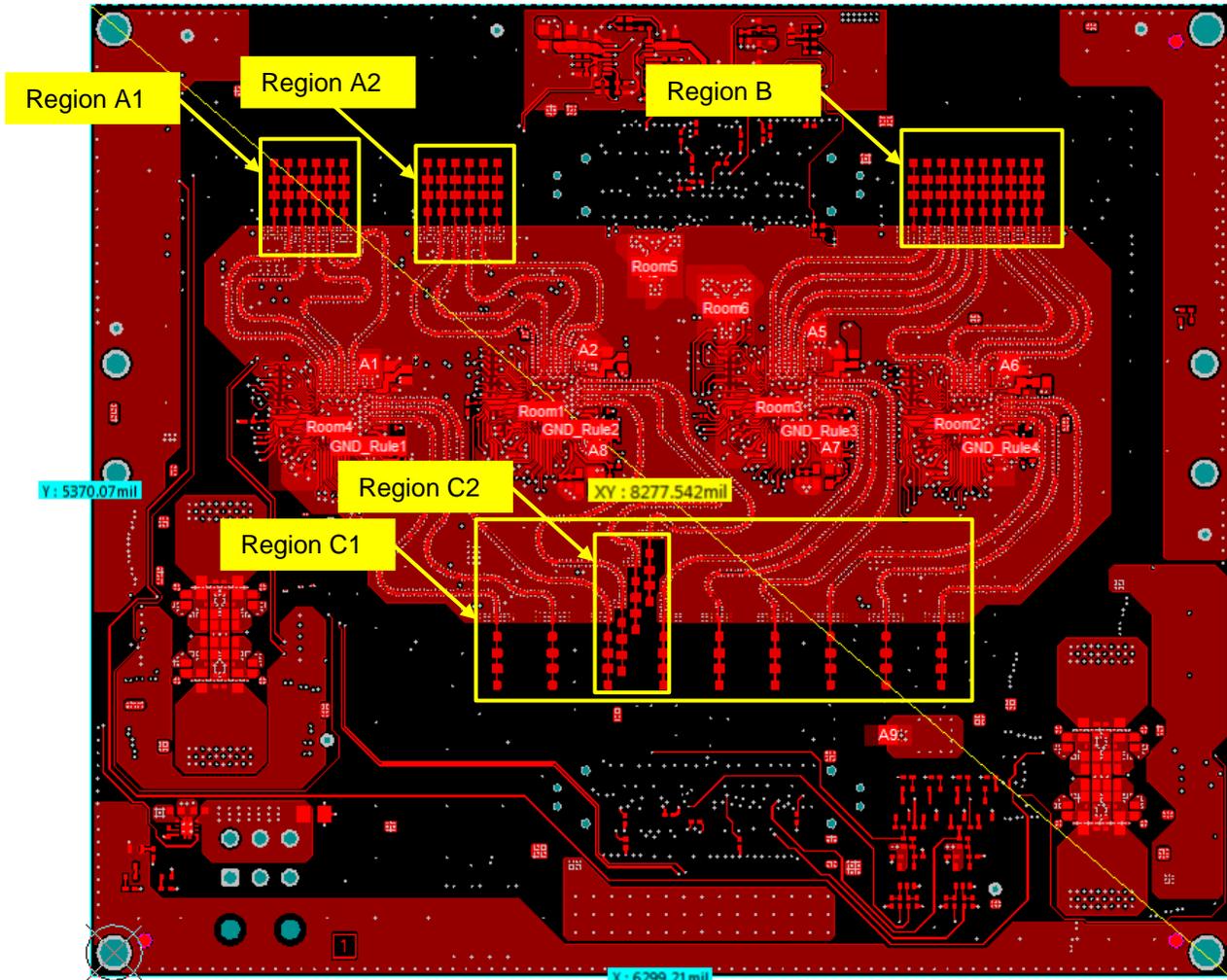


Figure 12 – RF Patch Antenna Regions

Cuts shall look at a few different regions of the antenna.

- Antenna Quarter-wave Stub
- Antenna Controlled Phase Stub
- Antenna Patch

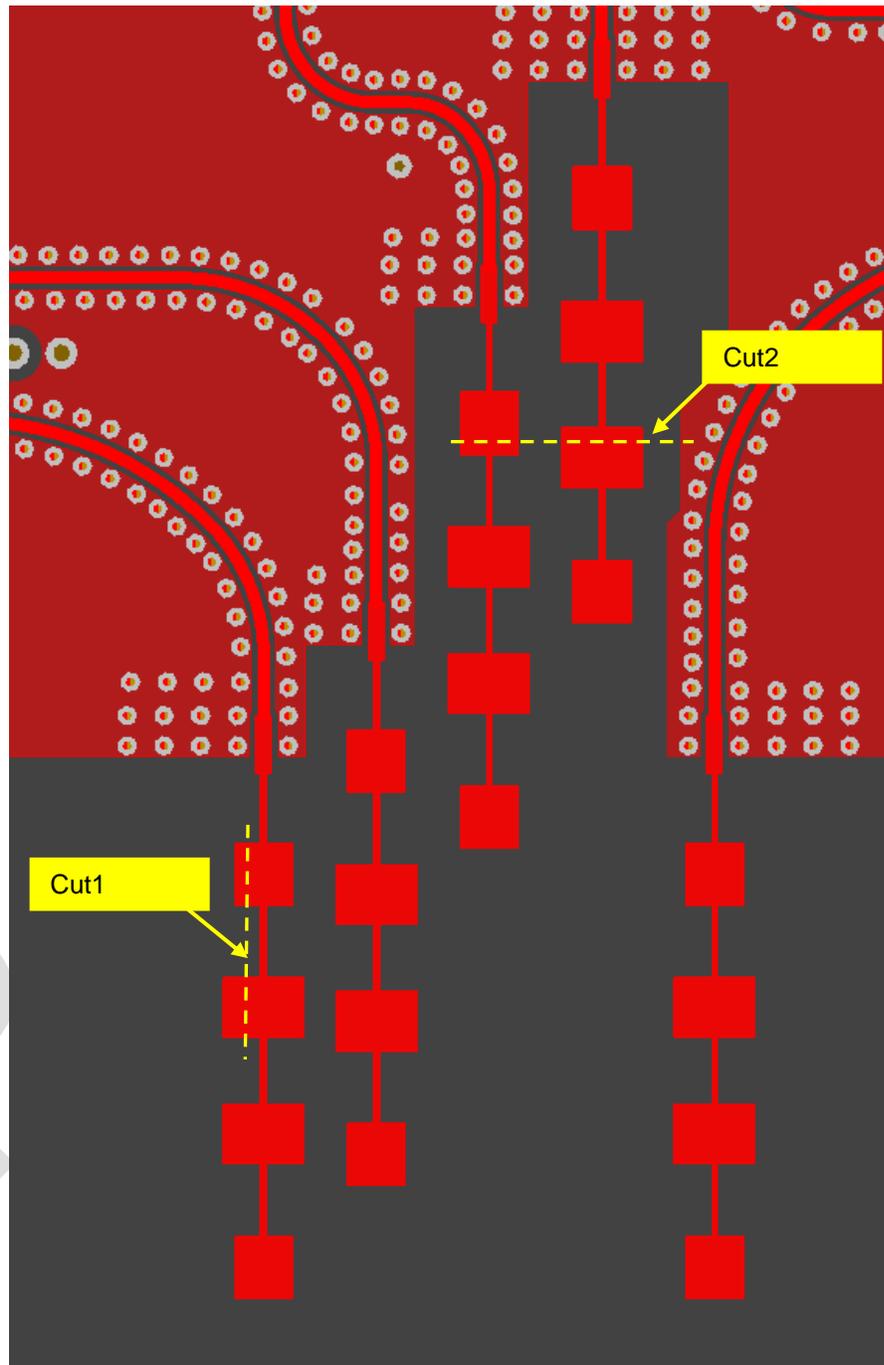


Figure 13 - RF Patch Antenna Cuts

5.1.1.3.3 Layer 1 20 GHz LO GCPW

A sample cross-section should be taken for each of the identified GCPW Regions shown below. Cuts should be made to include via structures adjacent to signal paths where present.

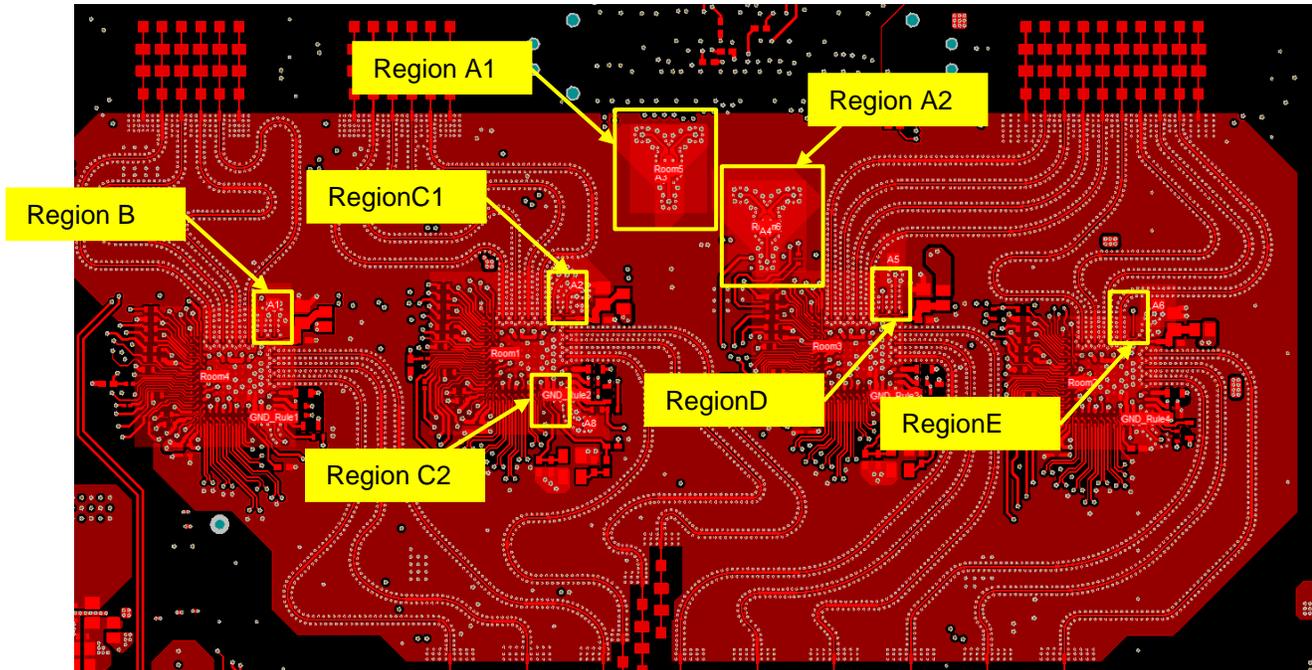


Figure 14 – 20GHz GCPW Regions

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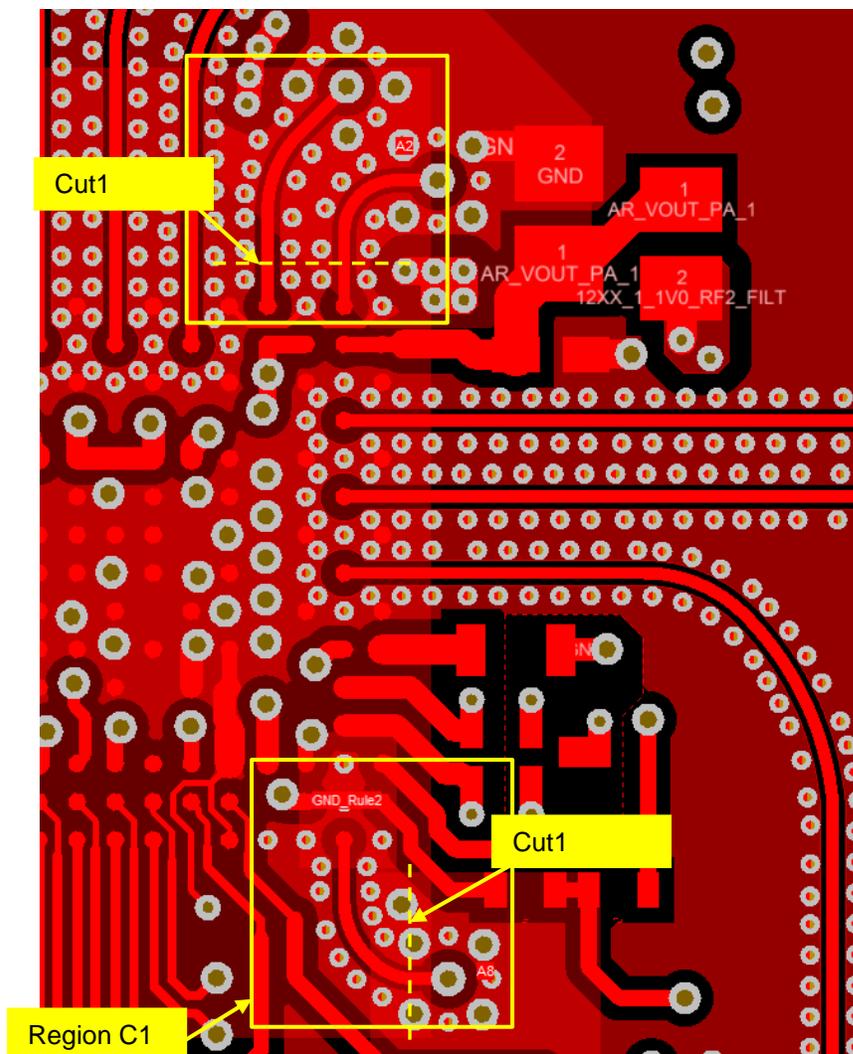


Figure 15 – 20 GHz GCPW Region C1 and C2

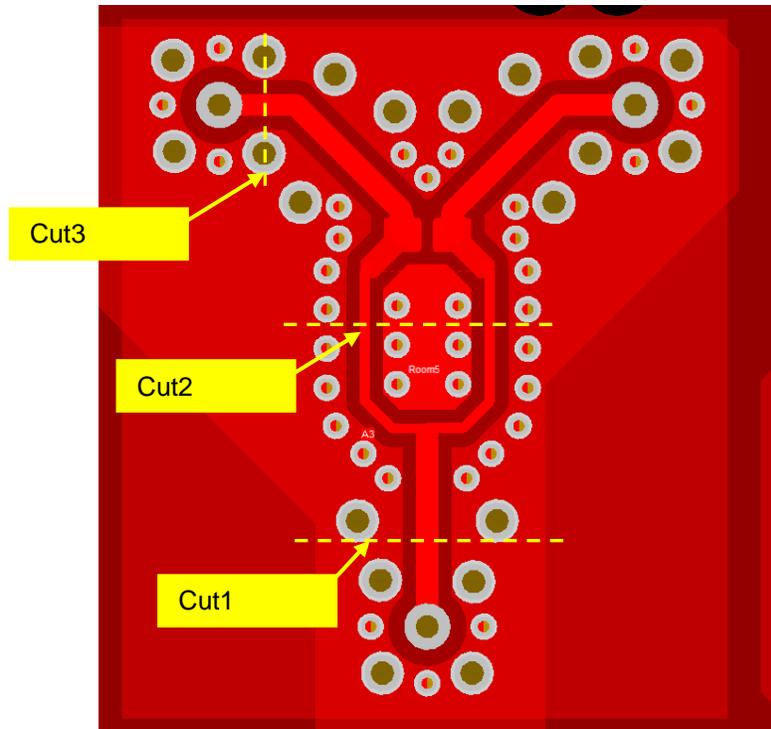


Figure 16 – 20 GHz GCPW Near Wilkinson Power Divider Region A1

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5.1.1.3.4 Layer 3 20 GHz LO Stripline

A sample cross-section should be taken for each of the identified Stripline Regions shown below. Cuts should be made to include via structures adjacent to signal paths where present.

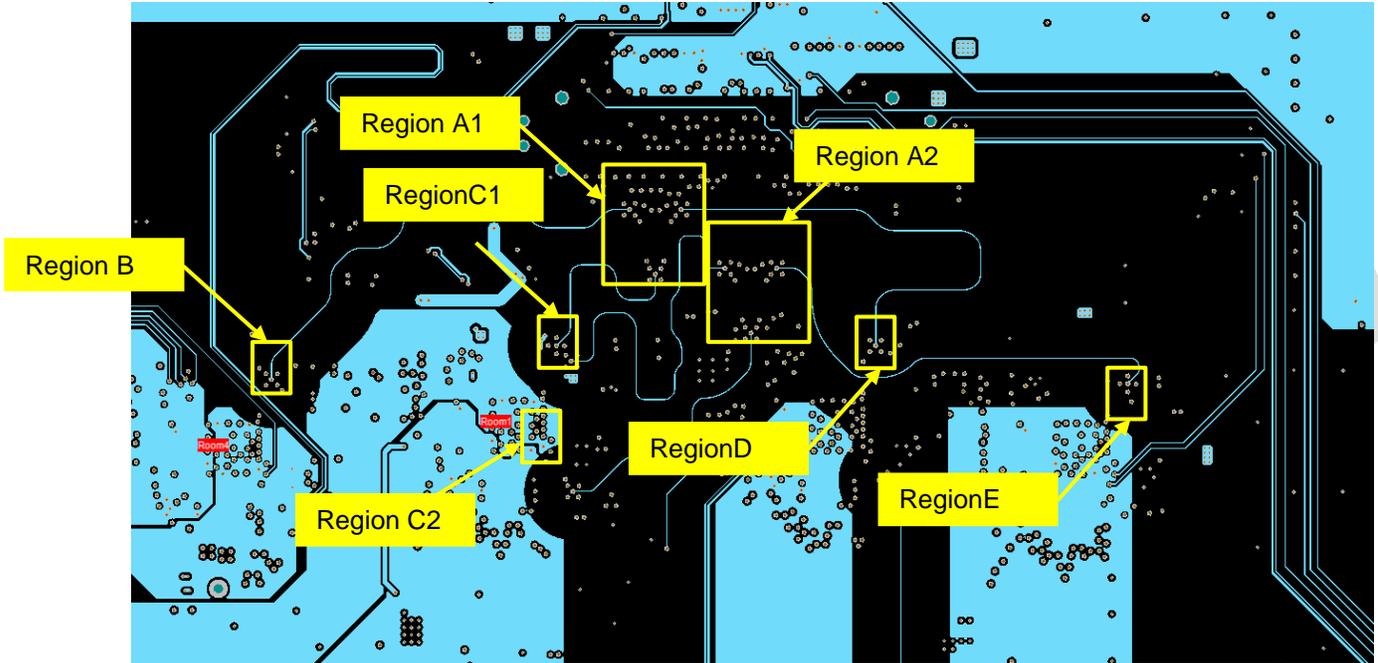


Figure 17 – 20GHz Stripline Regions

Pre

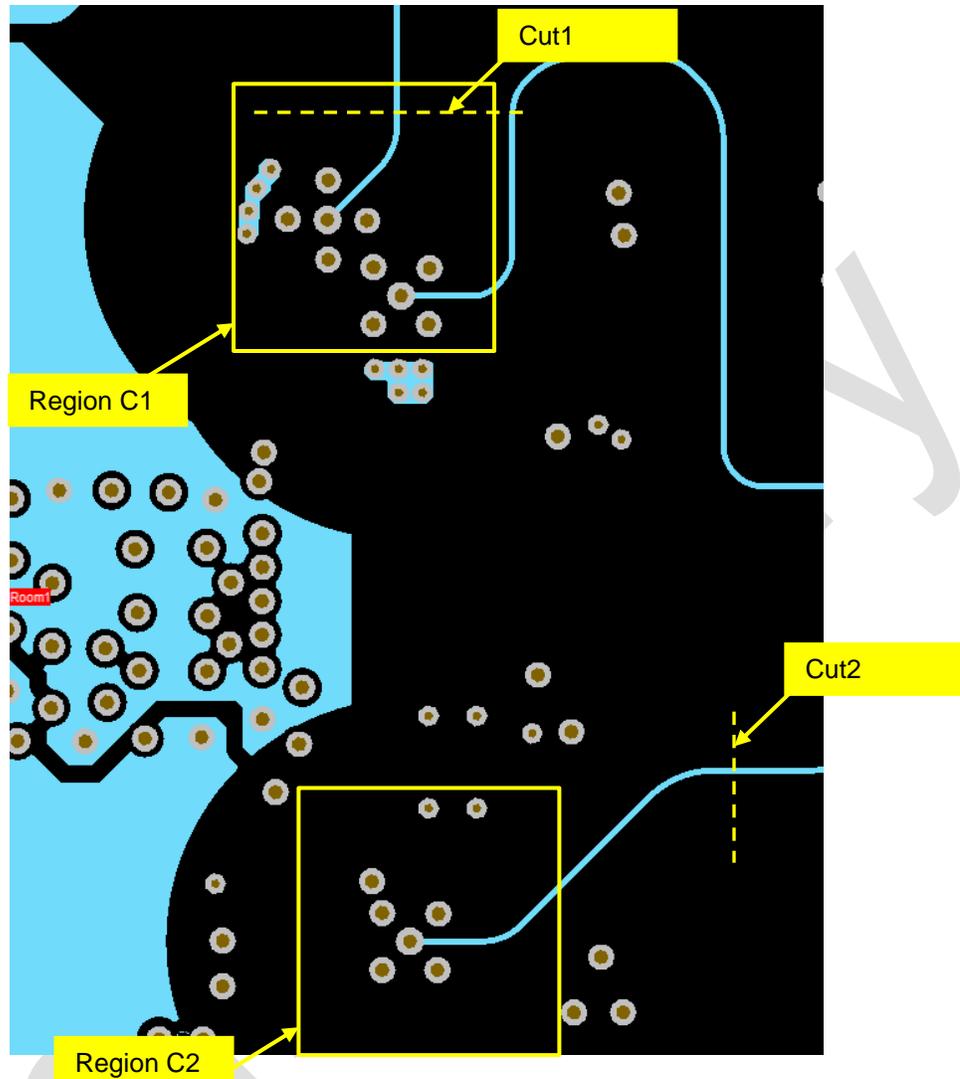


Figure 18 – 20 GHz Stripline Near AWR Region C1 and C2

5.1.1.4 Drill Location and Size Accuracy

All required drill location and size accuracies documented in fabrication drawing in CAM package.

5.1.1.5 Etch and Mask Registration Accuracy Relative to Drills

TI currently has no additional etch and mask registration requirements other than the standard metrics already used by the selected PCB fabricator.

5.1.2 Post-Fabrication Accuracy Inspections

During production runs of the PCB (after initial pre-fabrication accuracy testing) PCB that **do not meet** the established requirements should be considered scrap. Any yield loss and the specific failure mode resulting in

that loss shall be documented such that additional yield improvement actions can be taken by TI and the fabricator to reduce yield loss on future designs.

Ideally, these referenced requirements would be checked across each individual PCB in the panelization to understand how accuracies change across the panel PCB to PCB. However, sampling of one lead panel or some other sample method is acceptable as long as there is a check that the delivered material meets the requirements.

PCB that **meet** these TI fabrication requirements as well as any other standard quality metrics already used by the PCB fabricator shall be acceptable to proceed to assembly.

5.2 Hardware Assembly Test Specifications

This section describes the post-fabrication tests to be performed on each PCB prior to the

5.2.1 Pre-Assembly Test Specifications

TI currently has no additional pre-assembly testing requirements other than the standard metrics already used by the selected PCB assemblers such as:

- Open testing
- Shorts testing
- General post-fabrication delamination inspection/testing
- RF/Antenna post-fabrication delamination inspection/testing
- RF/LO transmission line post-fabrication delamination inspection/testing

5.2.2 Post-Assembly Test Specifications

TI currently has no additional post-assembly testing requirements other than the standard metrics already used by the selected PCB assemblers such as:

- Open testing
- Shorts testing
- General post-solder delamination inspection/testing
- RF/Antenna post-solder delamination inspection/testing
- RF/LO transmission line post-solder delamination inspection/testing

6 Critical Document References

1. AWR1243 TI.com product page can be referenced for more information:
<http://www.ti.com/product/awr1243>

7 Revision History

Rev 1 - 2018/07/20, R. Rosales (rosales.r@ti.com)

- Initial revision
- Added only the TDA2x Host Board functional post-assembly testing

Rev 2 - 2019/01/22, R. Rosales (rosales.r@ti.com)

- Made some small edits to intro, system description and hardware functional test description

Rev 3 - 2019/07/31, R. Rosales (rosales.r@ti.com)

- Merging in the Cascade_Radar_RF_Antenna_Etching document into the overall production test doc as Section 5.1 “Hardware Fabrication Test Specifications”

Rev 4 - 2019/08/01, R. Rosales (rosales.r@ti.com)

- Merging in the Cascade_Radar_RF_Cross_Section document into Section 5.1 “Hardware Fabrication Test Specifications”

Rev 5 - 2019/08/02, R. Rosales (rosales.r@ti.com)

- Removed section 5.3 dealing with post-assembly functional and performance testing
- Renamed this document to PROC054C_Fabrication_Test_Plan

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