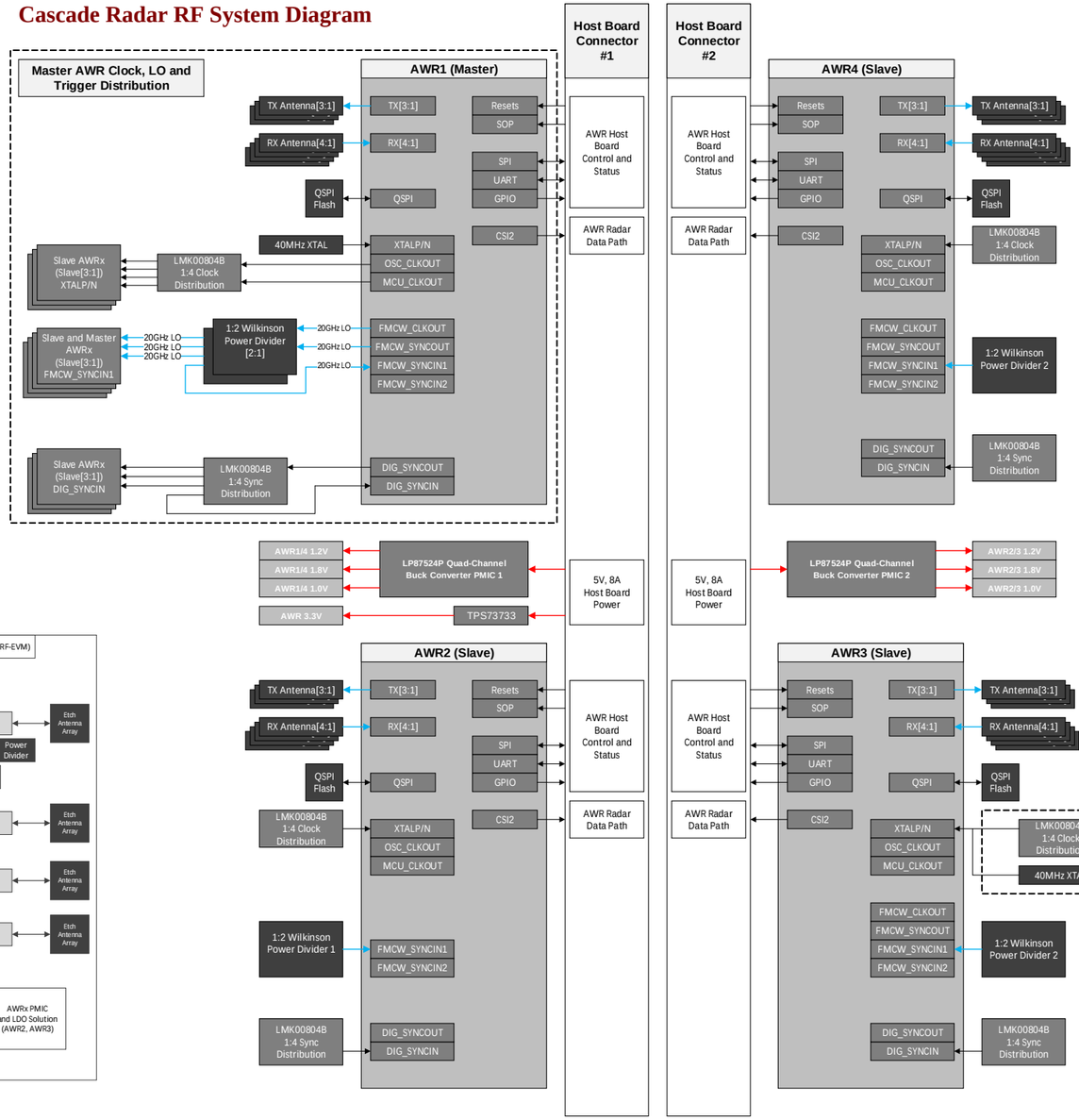
mmWave Cascade Radar RF Board (MMWCAS-RF-EVM)

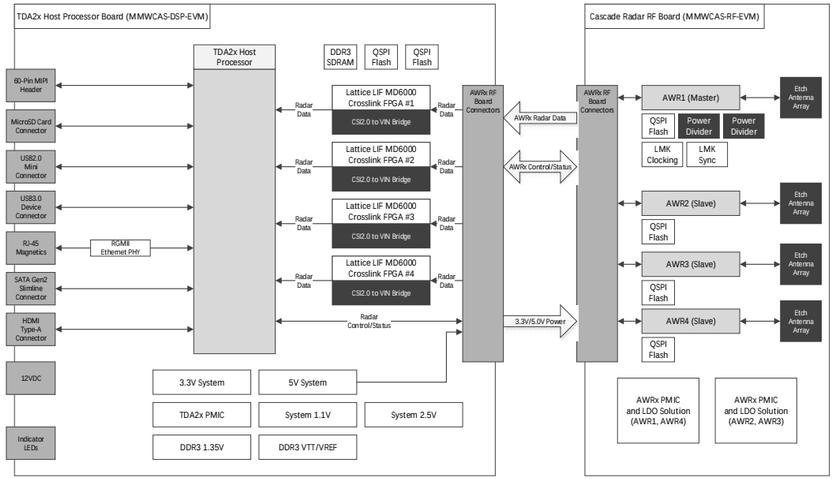
System Description

	Cascade Radar RF Board
4x AWRx 76-81GHz Radar SoC	Integrated VCO, LO distribution, PA, LNA, ADC, 3 TX and 4 RX ARM MCU R4 Controller
AWR RF Peripherals	
12x TX, 16x RX Antennas	12 total transmitters across all 4 AWRx devices 16 total receivers across all 4 AWRx devices
Embedded Antenna	4-element series-fed patch antenna
20 GHz LO Star Distribution	2x Wilkinson Power dividers fed by the Master AWRx device LO output to Slave AWRx devices
AWR Digital Peripherals	
CSI2.0 4-lane	600Mbps/Lane for 2.4Gbps ADC IF data per device
QSPI Flash	16Mbit QSPI flash for AWR firmware updates
Serial Peripherals	SPI, I2C, UART, GPIO
System Temperature	TMP112 I2C Temperature Sensors
Power	
Radar Power Management IC (PMIC) Solution	2x LP87524P Quad-Channel, Integrated FET, Buck Converters and LC filtering solution

Cascade Radar RF System Diagram



Cascade Radar Evaluation Kit Diagram



CASCADE_RF_BOARD
PROC054E_System_Top.SchDoc

EVM_HARDWARE
PROC054E_EVM_Hardware.SchDoc

REVISION_HISTORY
PROC054E_Revision_History.SchDoc

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 8/14/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: Coversheet	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:1 of 19
Drawn By:a0271760		File: PROC054E_Coversheet.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

TEXAS INSTRUMENTS
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Cascade Radar RF Board - Top Level Schematic

AWR_1 (Master)

AWR_1 — PROC054E_AWR_Interfaces.SchDoc

AWR_1_NRST, AWR_1_WARM_RST, AWR_1_XTAL_CLKP, AWR_1_XTAL_CLKM, AWR_1_OSC_CLKOUT, AWR_1_MCU_CLKOUT, AWR_1_PMIC_CLKOUT, AWR_1_UART_RX, AWR_1_UART_TX, AWR_1_SPI_CS1, AWR_1_SPI_CLK1, AWR_1_SPI_MISO1, AWR_1_SPI_MOSI1, AWR_1_SPI_HOST_INTR1, AWR_1_FMCW_CLKOUT, AWR_1_FMCW_SYNCOUT, AWR_1_FMCW_CLKOUT, AWR_1_SCL, AWR_1_SDA, AWR_1_BSS_LOGGER, AWR_1_MSS_LOGGER, AWR_1_1V0_RF2_FILT

CSI2_CLK_P/N, CSI2_TX0_P/N, CSI2_TX1_P/N, CSI2_TX2_P/N, CSI2_TX3_P/N, LVDS_VALID_P/N, LVDS_FRCLK_P/N, TCK, TMS, TDI, TDO, GPIO_0, GPIO_1, GPIO_2, NERROR_OUT, NERROR_IN, DIG_SYNCIN, DIG_SYNCOUT

AWR_1 — PROC054E_AWR_Pull_Resistors.SchDoc

AWR_1_WARM_RST, AWR_1_DIG_SYNCIN, AWR_1_UART_TX, AWR_1_UART_RX, AWR_1_SCL, AWR_1_SDA, AWR_1_SPI_CS1, AWR_1_SPI_CLK1, AWR_1_SPI_MISO1, AWR_1_SPI_MOSI1, AWR_1_SPI_HOST_INTR1, AWR_1_NERROR_IN

AWR_1 — PROC054E_AWR_Power_Decoupling.SchDoc

AWR_1V2, AWR_1V8, AWR_1V0_RF1, AWR_1V0_RF2

AWR_1_1V2_FILT, AWR_1_1V8_FILT, AWR_1_1V0_RF1_FILT, AWR_1_1V0_RF2_FILT

HOST_CONNECTORS

PROC054E_Host_Connector.SchDoc

AWR_1_NRST_HOST, AWR_1_WARM_RST, AWR_1_CSI2_CLK_P/N, AWR_1_CSI2_TX0_P/N, AWR_1_CSI2_TX1_P/N, AWR_1_CSI2_TX2_P/N, AWR_1_CSI2_TX3_P/N, AWR_1_LVDS_VALID_P/N, AWR_1_LVDS_FRCLK_P/N, AWR_1_TCK, AWR_1_TMS, AWR_1_TDI, AWR_1_TDO, AWR_1_GPIO_0, AWR_1_GPIO_1, AWR_1_GPIO_2, AWR_1_NERROR_OUT, AWR_1_NERROR_IN, AWR_1_DIG_SYNCIN, AWR_1_DIG_SYNCOUT, AWR_1_PMIC_CLKOUT, AWR_1_MCU_CLKOUT_CONN, AWR_1_UART_TX, AWR_1_UART_RX, AWR_1_SPI_CS1, AWR_1_SPI_CLK1, AWR_1_SPI_MISO1, AWR_1_SPI_MOSI1, AWR_1_SPI_HOST_INTR1, AWR_1_BSS_LOGGER, AWR_1_MSS_LOGGER

AWR_3_NRST_HOST, AWR_3_WARM_RST, AWR_3_CSI2_CLK_P/N, AWR_3_CSI2_TX0_P/N, AWR_3_CSI2_TX1_P/N, AWR_3_CSI2_TX2_P/N, AWR_3_CSI2_TX3_P/N, AWR_3_LVDS_VALID_P/N, AWR_3_LVDS_FRCLK_P/N, AWR_3_TCK, AWR_3_TMS, AWR_3_TDI, AWR_3_TDO, AWR_3_GPIO_0, AWR_3_GPIO_1, AWR_3_GPIO_2, AWR_3_NERROR_OUT, AWR_3_NERROR_IN, AWR_3_DIG_SYNCIN, AWR_3_DIG_SYNCOUT, AWR_3_PMIC_CLKOUT, AWR_3_UART_RX, AWR_3_UART_TX, AWR_3_SPI_CS1, AWR_3_SPI_CLK1, AWR_3_SPI_MISO1, AWR_3_SPI_MOSI1, AWR_3_SPI_HOST_INTR1, AWR_3_BSS_LOGGER, AWR_3_MSS_LOGGER

AWR_3 (Slave)

AWR_3 — PROC054E_AWR_Interfaces.SchDoc

AWR_3_NRST, AWR_3_WARM_RST, AWR_3_XTAL_CLKP, AWR_3_XTAL_CLKM, AWR_3_OSC_CLKOUT, AWR_3_MCU_CLKOUT, AWR_3_PMIC_CLKOUT, AWR_3_UART_RX, AWR_3_UART_TX, AWR_3_SPI_CS1, AWR_3_SPI_CLK1, AWR_3_SPI_MISO1, AWR_3_SPI_MOSI1, AWR_3_SPI_HOST_INTR1, AWR_3_FMCW_CLKOUT, AWR_3_FMCW_SYNCOUT, AWR_1_FMCW_SYNCOUT, AWR_3_SCL, AWR_3_SDA, AWR_3_BSS_LOGGER, AWR_3_MSS_LOGGER, AWR_3_1V0_RF2_FILT

AWR_3 — PROC054E_AWR_Power_Decoupling.SchDoc

AWR_3_1V2_FILT, AWR_3_1V8_FILT, AWR_3_1V0_RF1_FILT, AWR_3_1V0_RF2_FILT

AWR_3 — PROC054E_AWR_Pull_Resistors.SchDoc

AWR_3_WARM_RST, AWR_3_DIG_SYNCIN, AWR_3_UART_TX, AWR_3_UART_RX, AWR_3_SCL, AWR_3_SDA, AWR_3_SPI_CS1, AWR_3_SPI_CLK1, AWR_3_SPI_MISO1, AWR_3_SPI_MOSI1, AWR_3_SPI_HOST_INTR1, AWR_3_NERROR_IN

System Power/Reset

SYSTEM_POWER — PROC054E_System_Power.SchDoc

AWR_1_1V2_FILT, AWR_4_1V2_FILT, AWR_1_1V8_FILT, AWR_4_1V8_FILT, AWR_1_1V0_RF1_FILT, AWR_1_1V0_RF2_FILT, AWR_4_1V0_RF1_FILT, AWR_4_1V0_RF2_FILT, AWR_2_1V2_FILT, AWR_3_1V2_FILT, AWR_2_1V8_FILT, AWR_3_1V8_FILT, AWR_2_1V0_RF1_FILT, AWR_2_1V0_RF2_FILT, AWR_3_1V0_RF1_FILT, AWR_3_1V0_RF2_FILT

PMIC_NRST, PMIC_BUCK_EN, PMIC1_CLKIN, PMIC2_CLKIN, AWR_1_PMIC_CLKOUT, AWR_3_PMIC_CLKOUT

PMIC1_I2C: PMIC1_SCL, PMIC1_SDA

PMIC2_I2C: PMIC2_SCL, PMIC2_SDA

PMIC2_TMPSNS_SCL, PMIC2_TMPSNS_SDA, TMPSNS_ALERT

AWR_1_NRST, AWR_2_NRST, AWR_3_NRST, AWR_4_NRST, AWR_1_NRST_HOST, AWR_2_NRST_HOST, AWR_3_NRST_HOST, AWR_4_NRST_HOST, SYSTEM_PGOOD

40MHz Generation/Distribution

40MHZ_CLOCK — PROC054E_40MHZ_Clock.SchDoc

AWR_1_OSC_CLKOUT, AWR_3_OSC_CLKOUT, AWR_1_MCU_CLKOUT, AWR_3_MCU_CLKOUT, EXT_40MHZ_BUFF_1V8_PRI, AWR_1_MCU_CLKOUT_CONN, AWR_1_XTALP/N, AWR_2_XTALP/N, AWR_3_XTALP/N, AWR_4_XTALP/N, AWR_1_XTAL_CLKP, AWR_1_XTAL_CLKM, AWR_2_XTAL_CLKP, AWR_2_XTAL_CLKM, AWR_3_XTAL_CLKP, AWR_3_XTAL_CLKM, AWR_4_XTAL_CLKP, AWR_4_XTAL_CLKM

EXT_40MHZ_CLK_1V8

Digital Sync and 20GHZ LO

DIG_SYNC_LO_20GHZ — PROC054E_FMCW_Sync.SchDoc

EXT_DIG_SYNC, AWR_1_DIG_SYNCOUT, AWR_1_FMCW_SYNCOUT, AWR_1_FMCW_CLKOUT, AWR_1_DIG_SYNCIN, AWR_2_DIG_SYNCIN, AWR_3_DIG_SYNCIN, AWR_4_DIG_SYNCIN

AWR_2 (Slave)

AWR_2 — PROC054E_AWR_Interfaces.SchDoc

AWR_2_NRST, AWR_2_WARM_RST, AWR_2_XTAL_CLKP, AWR_2_XTAL_CLKM, AWR_2_OSC_CLKOUT, AWR_2_MCU_CLKOUT, AWR_2_PMIC_CLKOUT, AWR_2_UART_RX, AWR_2_UART_TX, AWR_2_SPI_CS1, AWR_2_SPI_CLK1, AWR_2_SPI_MISO1, AWR_2_SPI_MOSI1, AWR_2_SPI_HOST_INTR1, AWR_2_FMCW_CLKOUT, AWR_2_FMCW_SYNCOUT, AWR_1_FMCW_CLKOUT, AWR_2_SCL, AWR_2_SDA, AWR_2_BSS_LOGGER, AWR_2_MSS_LOGGER, AWR_2_1V0_RF2_FILT

AWR_2 — PROC054E_AWR_Pull_Resistors.SchDoc

AWR_2_WARM_RST, AWR_2_DIG_SYNCIN, AWR_2_UART_TX, AWR_2_UART_RX, AWR_2_SCL, AWR_2_SDA, AWR_2_SPI_CS1, AWR_2_SPI_CLK1, AWR_2_SPI_MISO1, AWR_2_SPI_MOSI1, AWR_2_SPI_HOST_INTR1, AWR_2_NERROR_IN

AWR_2 — PROC054E_AWR_Power_Decoupling.SchDoc

AWR_2_1V2_FILT, AWR_2_1V8_FILT, AWR_2_1V0_RF1_FILT, AWR_2_1V0_RF2_FILT

AWR_4 (Slave)

AWR_4 — PROC054E_AWR_Interfaces.SchDoc

AWR_4_NRST, AWR_4_WARM_RST, AWR_4_XTAL_CLKP, AWR_4_XTAL_CLKM, AWR_4_OSC_CLKOUT, AWR_4_MCU_CLKOUT, AWR_4_PMIC_CLKOUT, AWR_4_UART_RX, AWR_4_UART_TX, AWR_4_SPI_CS1, AWR_4_SPI_CLK1, AWR_4_SPI_MISO1, AWR_4_SPI_MOSI1, AWR_4_SPI_HOST_INTR1, AWR_4_FMCW_CLKOUT, AWR_4_FMCW_SYNCOUT, AWR_1_FMCW_SYNCOUT, AWR_4_SCL, AWR_4_SDA, AWR_4_BSS_LOGGER, AWR_4_MSS_LOGGER, AWR_4_1V0_RF2_FILT

AWR_4 — PROC054E_AWR_Power_Decoupling.SchDoc

AWR_4_1V2_FILT, AWR_4_1V8_FILT, AWR_4_1V0_RF1_FILT, AWR_4_1V0_RF2_FILT

AWR_4 — PROC054E_AWR_Pull_Resistors.SchDoc

AWR_4_WARM_RST, AWR_4_DIG_SYNCIN, AWR_4_UART_TX, AWR_4_UART_RX, AWR_4_SCL, AWR_4_SDA, AWR_4_SPI_CS1, AWR_4_SPI_CLK1, AWR_4_SPI_MISO1, AWR_4_SPI_MOSI1, AWR_4_SPI_HOST_INTR1, AWR_4_NERROR_IN

System LED Indicators

SYSTEM_LED_INDICATORS — PROC054E_System_LED.SchDoc

AWR_1_NRST, AWR_2_NRST, AWR_3_NRST, AWR_4_NRST, NERROR_OUT

System Temperature Sensors

SYSTEM_TEMP_SENSORS — PROC054E_Temp_Sensor.SchDoc

PMIC2_TMPSNS_SCL, PMIC2_TMPSNS_SDA, TMPSNS_ALERT

System Test Connectors And Termination

SYSTEM_TEST_CONN_TERMINATION — PROC054E_SMA_SMP_Connectors.SchDoc

AWR_1_OSC_CLKOUT, AWR_2_OSC_CLKOUT, AWR_3_OSC_CLKOUT, AWR_4_OSC_CLKOUT, AWR_2_FMCW_CLKOUT, AWR_2_FMCW_SYNCOUT, AWR_3_FMCW_CLKOUT, AWR_3_FMCW_SYNCOUT, AWR_4_FMCW_CLKOUT, AWR_4_FMCW_SYNCOUT

Orderable: MMW_CAS_RF_EVM		Designed for: Public Release	Mod. Date: 8/14/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: System Top	
Sys Rev: Not in version control		Assembly Variant: 001	Sheet: 2 of 19
Drawn By: a0271760		File: PROC054E_System_Top.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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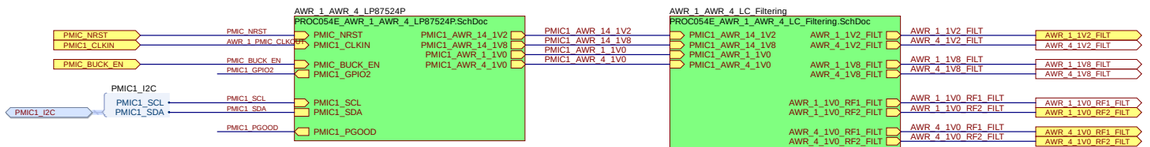
Cascade RF System Power

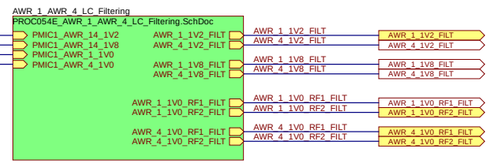
References

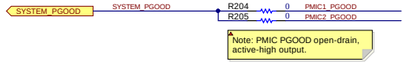
4-A + 2.5-A + Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

PMIC #1 - Master AWR_1 and Slave AWR_4

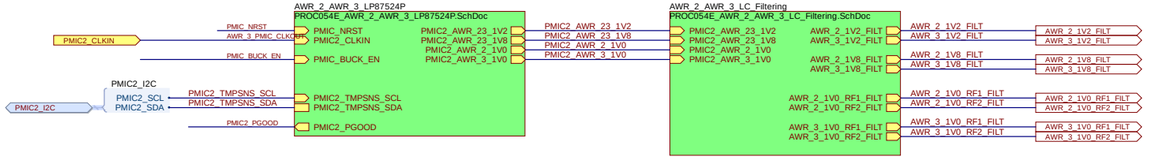


LC Filtering, Ferrite Filtering AWR_1 and AWR_4



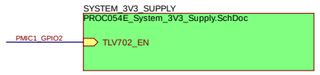


PMIC #2 - Master AWR_2 and Slave AWR_3

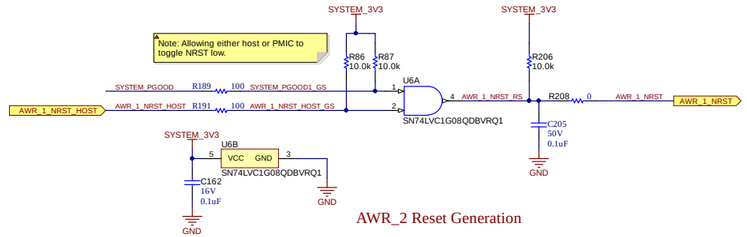


LC Filtering, Ferrite Filtering AWR_2 and AWR_3

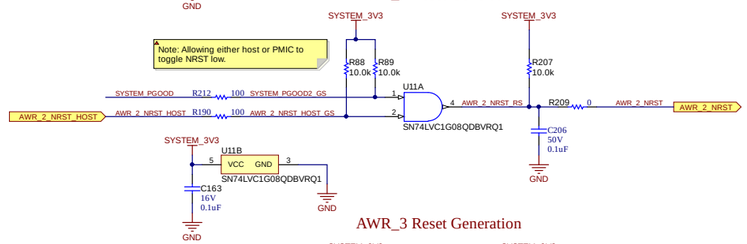
3.3V System LDO



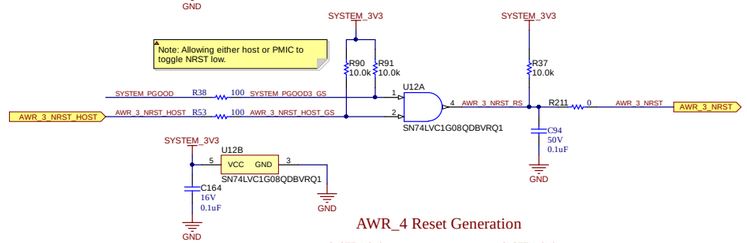
AWR_1 Reset Generation



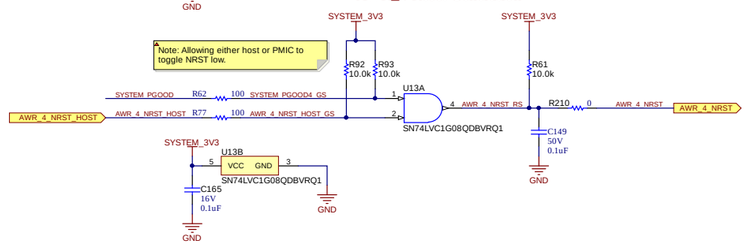
AWR_2 Reset Generation



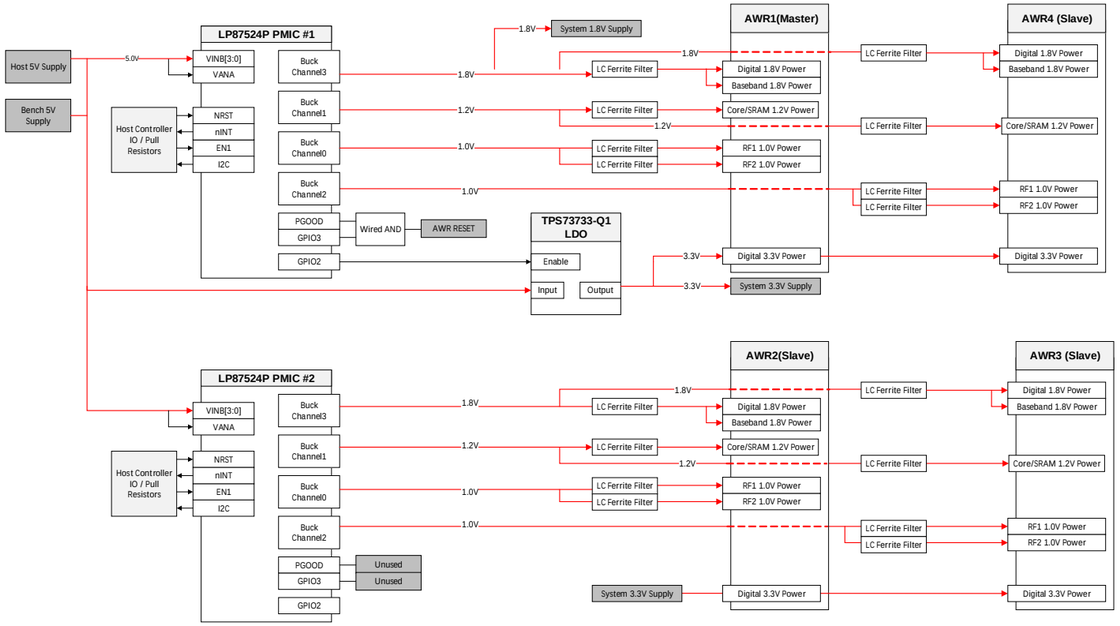
AWR_3 Reset Generation

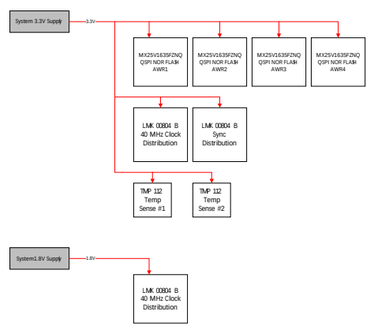


AWR_4 Reset Generation

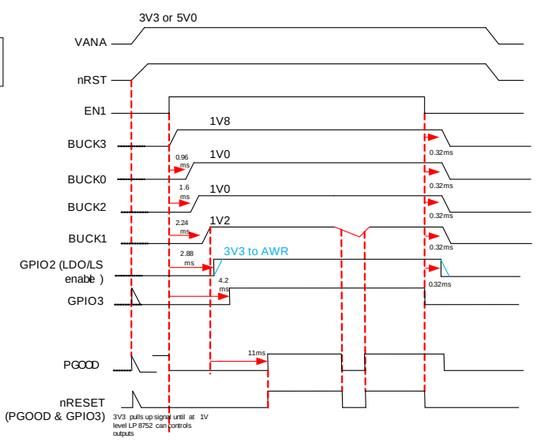


System Power Diagram





System Power Sequence Diagram



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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 8/14/2020
TID #: N/A		Project Title:MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: System Power	
Board Rev: Not in version control		Assembly VAWRiant:	Sheet:3 of 19
Drawn By:a0271760		File: PROC054E_System_Power.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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LP87524P Quad-Channel Synchronous Buck PMIC - Master AWR_1 and Slave AWR_4

References

4-A + 2.5-A + Two 1.5-A BLP875241-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

LP8752x input filtering, bulk and decoupling capacitance

SYSTEM_5V0 — L9 BLM21PG300SH1D — PMIC1_VIN_B0
C39 6.8nF 100V; DNP C40 6.3V; DNP C41 6.3V 100uF; C42 16V 0.1µF; C43 10V 10µF; GND

SYSTEM_5V0 — L10 BLM21PG300SH1D — PMIC1_VIN_B1
C44 6.8nF 100V; DNP C45 6.3V 100uF; DNP C46 6.3V 100uF; C47 16V 0.1µF; C48 10V 10µF; GND

SYSTEM_5V0 — L11 BLM21PG300SH1D — PMIC1_VIN_B2
C51 6.8nF 100V; DNP C52 6.3V; DNP C53 6.3V 100uF; C54 16V 0.1µF; C55 10V 10µF; GND

SYSTEM_5V0 — L12 BLM21PG300SH1D — PMIC1_VIN_B3
C56 6.8nF 100V; DNP C57 6.3V 100uF; DNP C58 6.3V 100uF; C59 16V 0.1µF; C60 10V 10µF; GND

LP8752x Output snubber RC filter

PMIC1_SW_B0 — C37 50V 390pF — R39 3.9 — GND
PMIC1_SW_B1 — C38 50V 390pF — R40 3.9 — GND
PMIC1_SW_B2 — C49 50V 390pF — R41 3.9 — GND
PMIC1_SW_B3 — C50 50V 390pF — R42 3.9 — GND

PMIC_NRST / PMIC1_CLKIN — PMIC_NRST / AWR_1_PMIC_CLKOUT — TP4 TP5
PMIC_BUCK_EN / PMIC1_GPIO2 — PMIC_BUCK_EN / PMIC1_GPIO2 — TP6 TP7
PMIC1_SCL / PMIC1_SDA — PMIC1_SCL / PMIC1_SDA — TP9 TP10
PMIC1_PGOOD — PMIC1_PGOOD — R96 0 PMIC1_PGOOD_RS — TP11
R73 0 PMIC1_GPIO3
PMIC1_AWR_1_1V0 — PMIC1_AWR_1_1V0
PMIC1_AWR_14_1V2 — PMIC1_AWR_14_1V2
PMIC1_AWR_4_1V0 — PMIC1_AWR_4_1V0
PMIC1_AWR_14_1V8 — PMIC1_AWR_14_1V8

SYSTEM_5V0 — R44 0 — PMIC1_VANA
LP87524 VANA input capacitance
C63 16V 0.1µF — GND

ClassName: SYSTEM_5V_INPUT
U3
PMIC1_VIN_B0 → 9 VIN_B0; PMIC1_VIN_B1 → 13 VIN_B1; PMIC1_VIN_B2 → 26 VIN_B2; PMIC1_VIN_B3 → 22 VIN_B3
TP14 — PMIC1_VANA → 18 VANA
20 RST ← PMC_NRST
3 CLKIN ← AWR_1_PMIC_CLKOUT
19 INT → PMIC1_INTN
16 PGOOD → PMIC1_PGOOD_RS
7 EN1 ← PMC_BUCK_EN
15 EN2 ← PMIC1_GPIO2
2 EN3 ← PMIC1_GPIO3
5 SCL ← PMIC1_SCL
6 SDA ↔ PMIC1_SDA
SW_B0 10 → PMIC1_SW_B0; FB_B0 8 ← PMIC1_FB_B0
SW_B1 12 → PMIC1_SW_B1; FB_B1 14 ← PMIC1_FB_B1
SW_B2 25 → PMIC1_SW_B2; FB_B2 1 ← PMIC1_FB_B2
SW_B3 23 → PMIC1_SW_B3; FB_B3 21 ← PMIC1_FB_B3
PGND_B01 11; PGND_B23 24
AGND 17; AGND 4; AGND 27
LP87524PRNFTQ1

ClassName: PMIC_CONTROL
PMC_NRST, AWR_1_PMIC_CLKOUT, PMIC1_INTN, PMIC1_PGOOD_RS, PMC_BUCK_EN, PMIC1_GPIO2, PMIC1_GPIO3, PMIC1_SCL, PMIC1_SDA

SYSTEM_3V3
LP87524 I2C Open-drain only 3.6V max compatible
R46 4.7k; R47 4.7k

LP87524 Buck-Converter Channels
SW0 - AWRx 1.0V RF
SW1 - AWRx/y 1.2V Core Digital
SW2 - AWRy 1.0V RF
SW3 - AWRx/y 1.8V Analog/Digital

ClassName: AWR1_POWER_RF
L13 470nH — PMIC1_SW_B0 — PMIC1_AWR_1_1V0 — R43 0 — PMIC1_FB_B0
AWR1 1.0V RF1/RF2 - 3A Max
C61 10V 22uF; C62 10V 22uF; GND

ClassName: AWR14_POWER_1V2
L14 470nH — PMIC1_SW_B1 — PMIC1_AWR_14_1V2 — R45 0 — PMIC1_FB_B1
AWR1/4 1.2V Core/SRAM - 1.5A Max
C64 10V 22uF; C65 10V 22uF; GND

ClassName: AWR4_POWER_RF
L15 470nH — PMIC1_SW_B2 — PMIC1_AWR_4_1V0 — R48 0 — PMIC1_FB_B2
AWR4 1.0V RF1/RF2 - 3A Max
C66 10V 22uF; C67 10V 22uF; GND

ClassName: AWR14_POWER_1V8
L16 470nH — PMIC1_SW_B3 — PMIC1_AWR_14_1V8 — R52 0 — PMIC1_FB_B3
AWR1/4 1.8V Baseband and Digital I/O - 2.5A Max
C68 10V 22uF; C69 10V 22uF; GND

LP87524 default pull resistors

RSTN - Pulled to 3.3V after SYSTEM_5V power on. Can be driven low by host.

CLKIN - Digital input, default pull-down. Can be driven by AWR

INTN - Open-drain, active-low interrupt output for host. De-asserted by pull-up to 3.3V after SYSTEM_3V3 power on.

PGOOD/GPIO3 - Open-drain, active-high output. Shorted together in wired AND. Pulled to PMIC_3V3 after all LP87524 rails active and additional delay.

BUCK_EN1 - Digital input, pull-ed up to 5.0V after power on to stAWRt LP87524 stAWRtup sequence. Can be driven low by host to stAWRt shutdown sequence.

GPIO2 - Digital ouput, default pull-down. Used by LP87524 to driv SYSTEM_3V3 LDO enable.

PMIC1_3V3
R94 10.0k; R54 10.0k; R49 10.0k; R56 10.0k; R50 10.0k; R51 10.0k
PMC_NRST; AWR_1_PMIC_CLKOUT; PMIC1_INTN; PMIC1_PGOOD_RS; PMC_BUCK_EN; PMIC1_GPIO2; PMIC1_GPIO3
R55 10.0k; R57 10.0k; R58 10.0k — GND

SYSTEM_5V0
R34 1.02k
PMIC1_3V3
R36 1.96k — GND

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Orderable: MMW_CAS_RF_EVM		Designed for: Public Release	Mod. Date: 8/14/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: AWR_1_AWR_4_LP87524P	
Scope: Not in version control		Assembly VAWRiant	Sheet: 4 of 19
Drawn By: a0271760		File: PROC054E_AWR_1_AWR_4_LP87524P.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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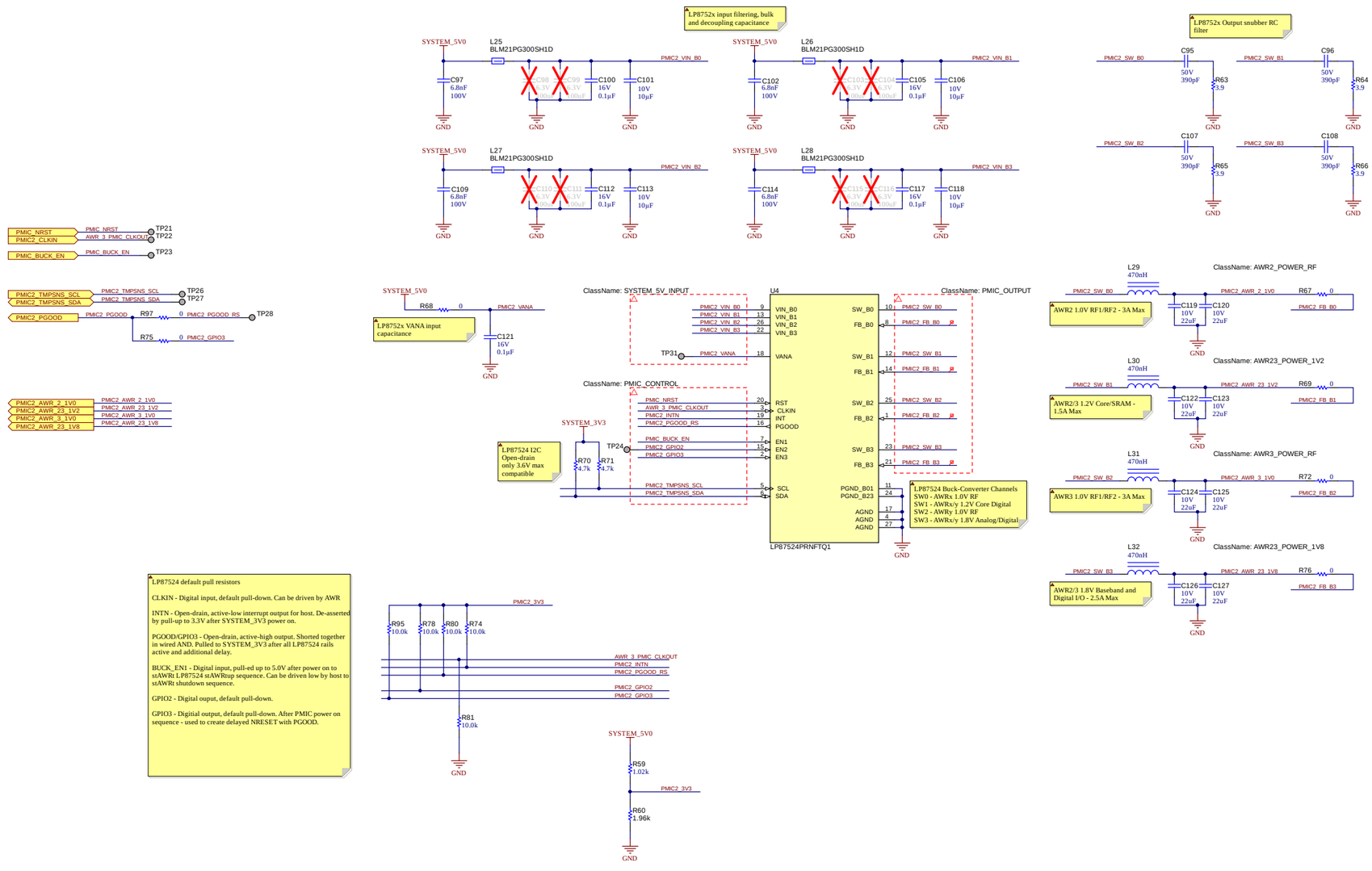
References

4-A + 2.5-A + Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

LP87524P Quad-Channel Synchronous Buck PMIC - Slave AWR_2 and Slave AWR_3



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TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: AWR_2_AWR_3_LP87524P	
Variant: Not in version control		Assembly VAWRiant:	Sheet: 5 of 19
Drawn By: a0271760		File: PROC054E_AWR_2_AWR_3_LP87524P.SchDoc	Size: C
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AWR Power Filtering and Decoupling - Master AWR_1 and Slave AWR_4

References

4-A + 2.5-A + Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

PMIC1_AWR_14_1V2 → PMIC1_AWR_14_1V2
PMIC1_AWR_14_1V8 → PMIC1_AWR_14_1V8
PMIC1_AWR_1_1V0 → PMIC1_AWR_1_1V0
PMIC1_AWR_4_1V0 → PMIC1_AWR_4_1V0

AWR_1_1V2_FILT → AWR_1_1V2_FILT
AWR_4_1V2_FILT → AWR_4_1V2_FILT
AWR_1_1V8_FILT → AWR_1_1V8_FILT
AWR_4_1V8_FILT → AWR_4_1V8_FILT
AWR_1_1V0_RF1_FILT → AWR_1_1V0_RF1_FILT
AWR_1_1V0_RF2_FILT → AWR_1_1V0_RF2_FILT
AWR_4_1V0_RF1_FILT → AWR_4_1V0_RF1_FILT
AWR_4_1V0_RF2_FILT → AWR_4_1V0_RF2_FILT

LP87524P PMIC switcher LC ripple filtering and decoupling for AWR1 and AWR4

PMIC1_AWR_14_1V2 — L1 NLCV32T-R10M-EFRD 100nH — AWR_1_1V2_FILT — ClassName: AWR_1_POWER_1V2
1.2V Digital Core/SRAM AWR1/AWR4
C10 10V 10uF; C11 10V 22uF; C12 10V 10uF; C13 16V 1µF
GND

PMIC1_AWR_14_1V2 — L3 NLCV32T-R10M-EFRD 100nH — AWR_4_1V2_FILT — ClassName: AWR_4_POWER_1V2
1.2V Digital Core/SRAM AWR1/AWR4
C161 10V 10uF; C21 10V 22uF; C29 10V 10uF; C78 16V 1µF
GND

PMIC1_AWR_14_1V8 — L2 NLCV32T-R10M-EFRD 100nH — AWR_1_1V8_FILT — ClassName: AWR_1_POWER_1V8
1.8V Digitial I/O and Analog Baseband AWR1/AWR4
C14 10V 10uF; C15 10V 22uF; C16 10V 10uF; C17 16V 1µF
GND

PMIC1_AWR_14_1V8 — L6 NLCV32T-R10M-EFRD 100nH — AWR_4_1V8_FILT — ClassName: AWR_4_POWER_1V8
1.8V Digitial I/O and Analog Baseband AWR1/AWR4
C86 10V 10uF; C150 10V 22uF; C151 10V 10uF; C152 16V 1µF
GND

PMIC1_AWR_1_1V0 — L4 NLCV32T-R10M-EFRD 100nH — AWR_1_1V0_RF1_FILT — ClassName: AWR_1_POWER_1V0_RF
1.0V Analog RF AWR1
C25 10V 10uF; C22 10V 22uF; C23 10V 10uF; C26 16V 1µF
GND

L5 NLCV32T-R10M-EFRD 100nH — AWR_1_1V0_RF2_FILT — ClassName: AWR_1_POWER_1V0_RF
C27 10V 10uF; C24 10V 22uF; C32 10V 10uF; C28 16V 1µF
GND

PMIC1_AWR_4_1V0 — L7 NLCV32T-R10M-EFRD 100nH — AWR_4_1V0_RF1_FILT — ClassName: AWR_4_POWER_RF
1.0V Analog RF AWR4
C33 10V 10uF; C30 10V 22uF; C31 10V 10uF; C34 16V 1µF
GND

L8 NLCV32T-R10M-EFRD 100nH — AWR_4_1V0_RF2_FILT — ClassName: AWR_4_POWER_RF
C35 10V 10uF; C81 10V 22uF; C89 10V 10uF; C36 16V 1µF
GND

ClassName: SYSTEM_1V8
PMIC1_AWR_14_1V8 — R35 0 — SYSTEM_1V8
C18 10V 22uF; C19 10V 10uF; C20 16V 1µF
GND

AWR_1 1.8V supply also generates SYSTEM_1V8
- LMK00804B clock distribution
- LMK00804B sync distribution

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TID #: N/A	Project Title: MMWCAS-RF-EVM	
Number: PROC054 Rev: E	Sheet Title: AWR_1_AWR_4_LC_Filtering	
Sys Rev: Not in version control	Assembly VAWRiant:	Sheet:6 of 19
Drawn By:a0271760	File: PROC054E_AWR_1_AWR_4_LC_Filtering.SchDoc	Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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AWR1243 Power Filtering and Decoupling - Master AWR_2 and Slave AWR_3

References

4-A + 2.5-A + Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

PMIC2_AWR_23_1V2 → PMIC2_AWR_23_1V2
PMIC2_AWR_23_1V8 → PMIC2_AWR_23_1V8
PMIC2_AWR_2_1V0 → PMIC2_AWR_2_1V0
PMIC2_AWR_3_1V0 → PMIC2_AWR_3_1V0

AWR_2_1V2_FILT → AWR_2_1V2_FILT
AWR_3_1V2_FILT → AWR_3_1V2_FILT
AWR_2_1V8_FILT → AWR_2_1V8_FILT
AWR_3_1V8_FILT → AWR_3_1V8_FILT
AWR_2_1V0_RF1_FILT → AWR_2_1V0_RF1_FILT
AWR_2_1V0_RF2_FILT → AWR_2_1V0_RF2_FILT
AWR_3_1V0_RF1_FILT → AWR_3_1V0_RF1_FILT
AWR_3_1V0_RF2_FILT → AWR_3_1V0_RF2_FILT

LP87524P PMIC switcher LC ripple filtering and decoupling for AWR2

PMIC2_AWR_23_1V2 → L17 NLCV32T-R10M-EFRD 100nH → AWR_2_1V2_FILT
ClassName: AWR_2_POWER_1V2
1.2V Digital Core/SRAM AWR2
C70 10V 10uF
C71 10V 22uF
C72 10V 10uF
C73 16V 1µF
GND

LP87524P PMIC switcher LC ripple filtering and decoupling for AWR3

PMIC2_AWR_23_1V2 → L19 NLCV32T-R10M-EFRD 100nH → AWR_3_1V2_FILT
ClassName: AWR_3_POWER_1V2
1.2V Digital Core/SRAM AWR3
C153 10V 10uF
C154 10V 22uF
C155 10V 10uF
C156 16V 1µF
GND

PMIC2_AWR_23_1V8 → L18 NLCV32T-R10M-EFRD 100nH → AWR_2_1V8_FILT
ClassName: AWR_3_POWER_1V8
1.8V Digitial I/O and Analog Baseband AWR2
C74 10V 10uF
C75 10V 22uF
C76 10V 10uF
C77 16V 1µF
GND

PMIC2_AWR_23_1V8 → L22 NLCV32T-R10M-EFRD 100nH → AWR_3_1V8_FILT
ClassName: AWR_3_POWER_1V8
1.8V Digitial I/O and Analog Baseband AWR3
C157 10V 10uF
C158 10V 22uF
C159 10V 10uF
C160 16V 1µF
GND

PMIC2_AWR_2_1V0 → L20 NLCV32T-R10M-EFRD 100nH → AWR_2_1V0_RF1_FILT
ClassName: AWR_2_POWER_1V0_RF
1.0V Analog RF AWR2
C82 10V 10uF
C79 10V 22uF
C80 10V 10uF
C83 16V 1µF
GND

L21 NLCV32T-R10M-EFRD 100nH → AWR_2_1V0_RF2_FILT
ClassName: AWR_2_POWER_1V0_RF
C84 10V 10uF
C166 10V 22uF
C201 10V 10uF
C85 16V 1µF
GND

PMIC2_AWR_3_1V0 → L23 NLCV32T-R10M-EFRD 100nH → AWR_3_1V0_RF1_FILT
ClassName: AWR_3_POWER_RF
1.0V Analog RF AWR3
C90 10V 10uF
C87 10V 22uF
C88 10V 10uF
C91 16V 1µF
GND

L24 NLCV32T-R10M-EFRD 100nH → AWR_3_1V0_RF2_FILT
ClassName: AWR_3_POWER_RF
C92 10V 10uF
C204 10V 22uF
C207 10V 10uF
C93 16V 1µF
GND

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TID #: N/A	Project Title: MMWCAS-RF-EVM
Number: PROC054 Rev: E	Sheet Title: AWR_2_AWR_3_LC_Filtering
Cust Rev: Not in version control	Assembly VAWRiant: Sheet: 7 of 19
Drawn By: a0271760	File: PROC054E_AWR_2_AWR_3_LC_Filtering.SchDoc Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave

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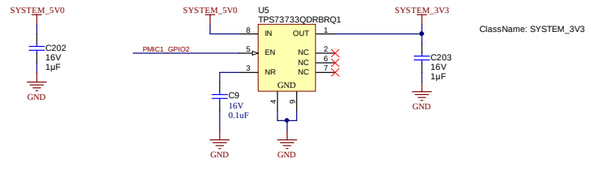
System 3.3V Supply

References

TLV70028EVM-463 Evaluation Module
TPS22965 Evaluation Module

TPS73733-Q1 5.0V to 3.3V LDO - System 3.3V Power



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TID #: N/A	Project Title: MMWCAS-RF-EVM	
Number: PROC054 Rev: E	Sheet Title: System_3V3_Supply	
Variant: Rev: Not in version control	Assembly VAWRiant:	Sheet:8 of 19
Drawn By:a0271760	File: PROC054E_System_3V3_Supply.SchDoc	Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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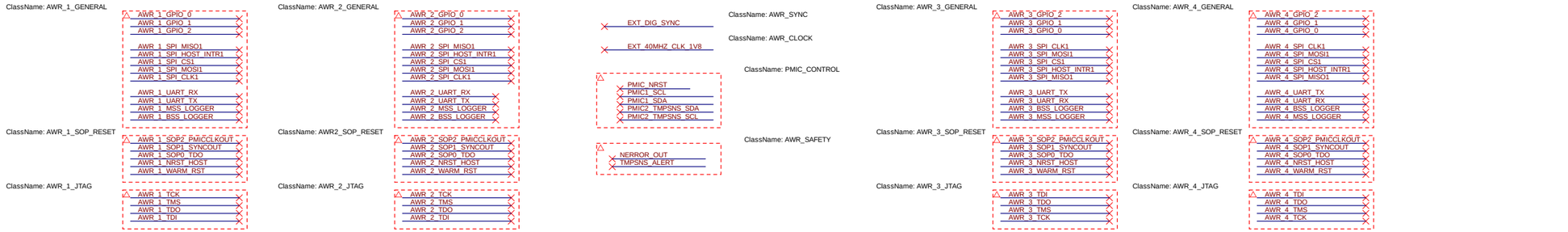
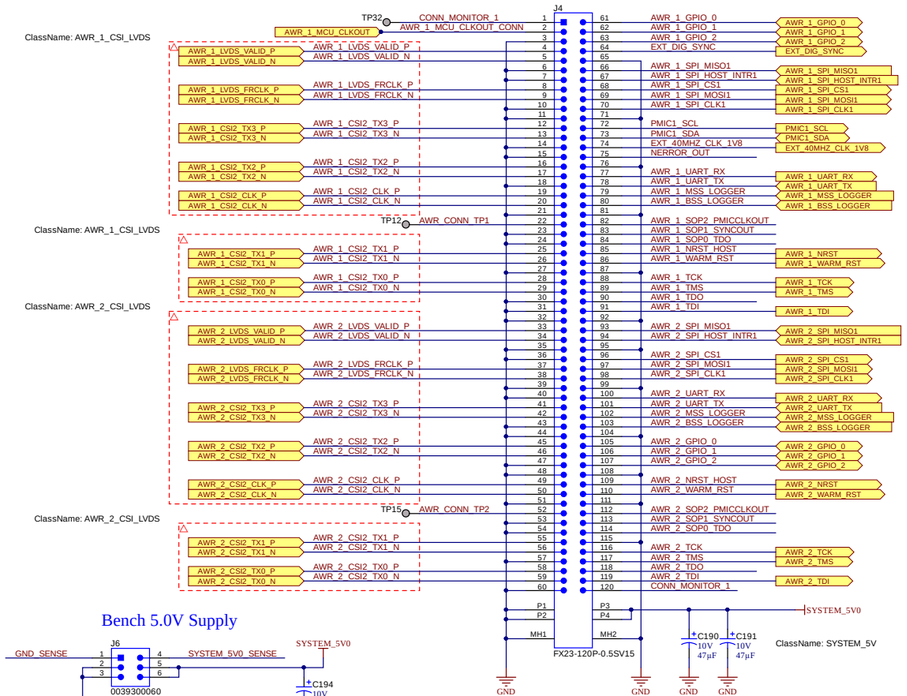
Host to RF Board Connectors



Host Board Connector 1



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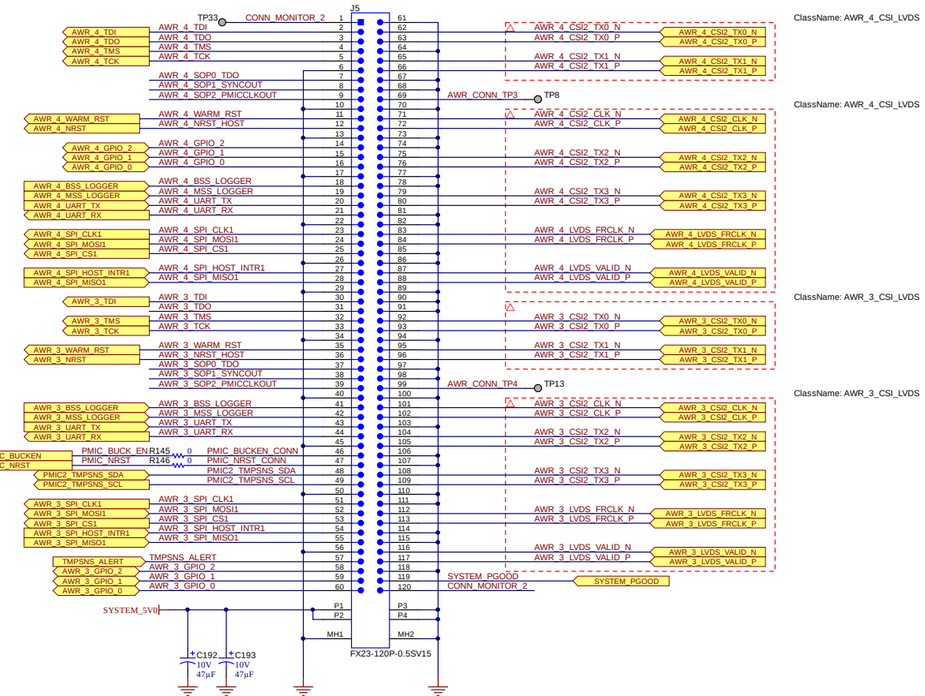
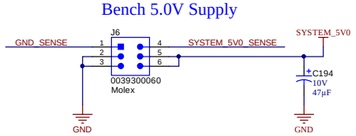
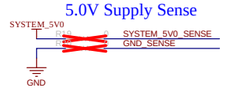


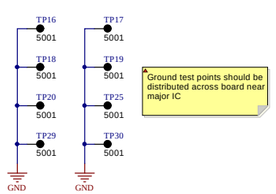
Bench 5.0V Supply



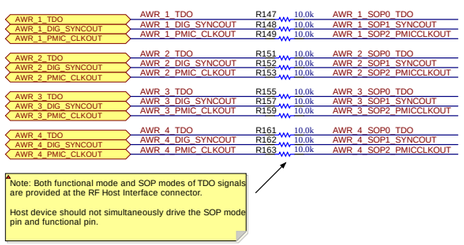
5.0V Supply Sense



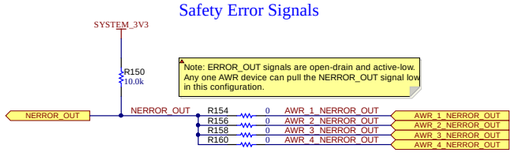
GROUND TEST POINTS



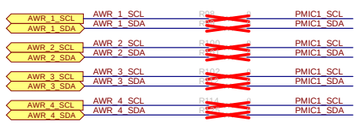
SOP Mode / Functional Mode Signals



Safety Error Signals



AWR and PMIC I2C Signals



Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 8/14/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: HOST_CONNECTOR	
Cust Rev: Not in version control		Assembly VAWRiant:	Sheet:9 of 19
Drawn By:a0271760		File: PROC054E_Host_Connector.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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AWR Radar SoC - Interfaces

References

http://www.ti.com/product/AWR2243

AWR LDO and Bandgap Output Capacitors

Place output capacitors as close to power pins as possible - minimum mounting inductance.

AWR_1V4_SYNTH_1 — C1_1 16V 1uF — GND
AWR_VBGAP_1 — C2_1 25V 0.047uF — GND
AWR_1V4_APLL_1 — C3_1 16V 1uF — GND
AWR_VOUT_PA_1 — C4_1 16V 0.22uF — C5_1 10V 10uF — GND

AWR Interfaces

U1_1A — AWR2243APBGABLQ1

G13	RESERVED	
M2	RX1	AWR_RX1_1
K2	RX2	AWR_RX2_1
H2	RX3	AWR_RX3_1
F2	RX4	AWR_RX4_1
B4	TX1	AWR_TX1_1
B6	TX2	AWR_TX2_1
B8	TX3	AWR_TX3_1
B1	FM_CW_SYNCIN1	AWR_1_FMCW_CLKOUT
D15	FM_CW_SYNCIN2	
B15	FM_CW_CLKOUT	AWR_1_FMCW_CLKOUT
D1	FM_CW_SYNCOUT	AWR_1_FMCW_SYNCOUT
N10	SYNC_IN	AWR_1_DIG_SYNCIN
P11	SYNC_OUT	AWR_1_DIG_SYNCOUT
A14	OSC_CLKOUT	AWR_1_OSC_CLKOUT
E14	CLKP	AWR_1_XTAL_CLKP
F14	CLKM	AWR_1_XTAL_CLKM
P13	PMIC_CLK_OUT	AWR_1_PMIC_CLKOUT
N9	MCU_CLK_OUT	AWR_1_MCU_CLKOUT
C14	VSENSE	GPADC8_1
C13	ANAMUX	GPADC5_1
P1	ANALOGTEST1	GPADC1_1
P2	ANALOGTEST2	GPADC2_1
P3	ANALOGTEST3	GPADC3_1
R2	ANALOGTEST4	GPADC4_1
P12	RESET	AWR_1_NRST
N12	WARM_RESET	AWR_1_WARM_RST
P7	NERROR_IN	AWR_1_NERROR_IN
N8	NERROR_OUT	AWR_1_NERROR_OUT
N5	RS232_RX	AWR_1_UART_RX
N6	RS232_TX	AWR_1_UART_TX
P4	RESERVED	AWR_1_SCL
R3	RESERVED	AWR_1_SDA
R4	RESERVED	AWR_1_BSS_LOGGER
R5	RESERVED	AWR_1_MSS_LOGGER

A13	VOUT_14SYNTH	AWR_1V4_SYNTH_1
A10	VOUT_14APLL1	AWR_1V4_APLL_1
B10	VBGAP	AWR_VBGAP_1
A2	VOUT_PA	AWR_VOUT_PA_1
B2	VOUT_PA	
G15	CSI2_TXP[0]	AWR_1_CSI2_TX0_P
G14	CSI2_TXM[0]	AWR_1_CSI2_TX0_N
H15	CSI2_TXP[1]	AWR_1_CSI2_TX1_P
H14	CSI2_TXM[1]	AWR_1_CSI2_TX1_N
J15	CSI2_CLKP	AWR_1_CSI2_CLK_P
J14	CSI2_CLKM	AWR_1_CSI2_CLK_N
K15	CSI2_TXP[2]	AWR_1_CSI2_TX2_P
K14	CSI2_TXM[2]	AWR_1_CSI2_TX2_N
L15	CSI2_TXP[3]	AWR_1_CSI2_TX3_P
L14	CSI2_TXM[3]	AWR_1_CSI2_TX3_N
M15	HS_DEBUG1_P	AWR_1_LVDS_FRCLK_P
M14	HS_DEBUG1_M	AWR_1_LVDS_FRCLK_N
N15	HS_DEBUG2_P	AWR_1_LVDS_VALID_P
N14	HS_DEBUG2_M	AWR_1_LVDS_VALID_N
P8	QSPI_CS	QSPI_CS_RS_1
R10	QSPI_CLK	QSPI_CLK_RS_1
R11	QSPI[0]	QSPI_D0_1
P9	QSPI[1]	QSPI_D1_1
R12	QSPI[2]	QSPI_D2_1
R10	QSPI[3]	QSPI_D3_1
M13	TCK	AWR_1_TCK
L13	TMS	AWR_1_TMS
J13	TDO	TDO_RS_1
H13	TDI	AWR_1_TDI
P6	SPI_HOST_INTR_1	SPI_HOST_INTR1_RS_1
R9	SPI_CLK_1	AWR_1_SPI_CLK1
R7	SPI_CS_1	AWR_1_SPI_CS1
P5	MISO_1	SPI_MISO1_RS_1
R8	MOSI_1	AWR_1_SPI_MOSI1
N4	GPIO[0]	AWR_1_GPIO_0
N7	GPIO[1]	AWR_1_GPIO_1
N13	GPIO[2]	AWR_1_GPIO_2

ClassName: AWR_20GHZ_LO

FMCW_SYNCIN1_1 — AWR_1_FMCW_CLKOUT
FMCW_CLKOUT_1 — AWR_1_FMCW_CLKOUT
FMCW_SYNCOUT_1 — AWR_1_FMCW_SYNCOUT

ClassName: AWR_ANTENNA

NOTE: AWR antenna routed as GCPW transmission lines to etched antenna.

NOTE: AWR FMCW_SYNCIN2 unused. Shorted to GND per datasheet requirements.

NOTE: AWR FMCW_CLKOUT/SYNCOUT unused terminated to 50-ohms per datasheet requirements.

GND

ClassName: AWR_POWER_ANA

Place R188 as close as possible to VOUT_PA/RF2 pins

Note: AWR_1V0_RF2 optionally shorted to AWR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.

R188 installed - shorts AWR_VOUT_PA to AWR_1V0_RF2 (default)
R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

R188_1 0 AWR_1_1V0_RF2_FILT

DIG_SYNCIN_1 — AWR_1_DIG_SYNCIN
DIG_SYNCOUT_1 — AWR_1_DIG_SYNCOUT — TP1_1

OSC_CLKOUT_1 — AWR_1_OSC_CLKOUT
XTAL_CLKP_1 — AWR_1_XTAL_CLKP
XTAL_CLKM_1 — AWR_1_XTAL_CLKM

PMIC_CLKOUT_1 — AWR_1_PMIC_CLKOUT
MCU_CLKOUT_1 — AWR_1_MCU_CLKOUT — TP2_1

NRST_1 — AWR_1_NRST
WARM_RST_1 — AWR_1_WARM_RST
NERROR_IN_1 — AWR_1_NERROR_IN
NERROR_OUT_1 — AWR_1_NERROR_OUT

ClassName: AWR_SYNC

UART_RX_1 — AWR_1_UART_RX
UART_TX_1 — AWR_1_UART_TX

ClassName: AWR_CLOCK

TCK_1 — AWR_1_TCK
TMS_1 — AWR_1_TMS
TDO_1 — AWR_1_TDO
TDI_1 — AWR_1_TDI — TP3_1

SPI_HOST_INTR1_1 — AWR_1_SPI_HOST_INTR1
SPI_CLK1_1 — AWR_1_SPI_CLK1
SPI_CS1_1 — AWR_1_SPI_CS1
SPI_MISO1_1 — AWR_1_SPI_MISO1
SPI_MOSI1_1 — AWR_1_SPI_MOSI1

GPIO_0_1 — AWR_1_GPIO_0
GPIO_1_1 — AWR_1_GPIO_1
GPIO_2_1 — AWR_1_GPIO_2

ClassName: AWR_GENERAL

SCL_1 — AWR_1_SCL
SDA_1 — AWR_1_SDA
BSS_LOGGER_1 — AWR_1_BSS_LOGGER
MSS_LOGGER_1 — AWR_1_MSS_LOGGER

NOTE: UART_RX and UART_TX directions AWRe with respect to AWR

ClassName: AWR_GENERAL

AWR_1_NERROR_OUT — R9_1 0 — NERROR_OUT_RS_1
AWR_1_UART_RX — AWR_1_UART_TX — R11_1 33.2 — UART_TX_RS_1
AWR_1_SCL
AWR_1_SDA — R13_1 33.2 — SDA_RS_1
AWR_1_BSS_LOGGER — R14_1 33.2 — BSS_LOGGER_RS_1
AWR_1_MSS_LOGGER — R15_1 33.2 — MSS_LOGGER_RS_1

ClassName: AWR_GENERAL

CSI2_CLK_1_P — AWR_1_CSI2_CLK_P
CSI2_CLK_1_N — AWR_1_CSI2_CLK_N
CSI2_TX0_1_P — AWR_1_CSI2_TX0_P
CSI2_TX0_1_N — AWR_1_CSI2_TX0_N
CSI2_TX1_1_P — AWR_1_CSI2_TX1_P
CSI2_TX1_1_N — AWR_1_CSI2_TX1_N
CSI2_TX2_1_P — AWR_1_CSI2_TX2_P
CSI2_TX2_1_N — AWR_1_CSI2_TX2_N
CSI2_TX3_1_P — AWR_1_CSI2_TX3_P
CSI2_TX3_1_N — AWR_1_CSI2_TX3_N
LVDS_FRCLK_1_P — AWR_1_LVDS_FRCLK_P
LVDS_FRCLK_1_N — AWR_1_LVDS_FRCLK_N
LVDS_VALID_1_P — AWR_1_LVDS_VALID_P
LVDS_VALID_1_N — AWR_1_LVDS_VALID_N

AWR_1V0_RF2_1 — AWR_1_1V0_RF2_FILT

QSPI_FLASH_3V3_1 — R3_1 47.5k

Place termination and pull-up resistors close to QSPI controller - minimize stubs.

ClassName: AWR_QSPI

QSPI_CS_RS_1 — R6_1 0 — QSPI_CS_1
QSPI_CLK_RS_1 — R7_1 0 — QSPI_CLK_1
QSPI[0] — QSPI_D0_1
QSPI[1] — QSPI_D1_1
QSPI[2] — QSPI_D2_1
QSPI[3] — QSPI_D3_1

ClassName: AWR_JTAG

TDO_RS_1 — R8_1 33.2 — AWR_1_TDO
AWR_1_TDI

ClassName: AWR_GENERAL

SPI_HOST_INTR1_RS_1 — R10_1 33.2 — AWR_1_SPI_HOST_INTR1
AWR_1_SPI_CLK1
AWR_1_SPI_CS1
SPI_MISO1_RS_1 — R12_1 33.2 — AWR_1_SPI_MISO1
AWR_1_SPI_MOSI1

ClassName: AWR_GENERAL

AWR_1_GPIO_0
AWR_1_GPIO_1
AWR_1_GPIO_2

R16_1 10.0k — R17_1 10.0k — R18_1 10.0k — GND

SOP[2:0] Pins

NOTE: SOP (start on power) Pins
SOP[2]/PMIC_CLK_OUT
SOP[1]/SYNC_OUT
SOP[0]TDO

SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
SOP[2:0] = 0b001 -> SOP_MODE4 "Functional"
SOP[2:0] = 0b101 -> SOP_MODE5 "QSPI Flashing"

NOR QSPI FLASH (For Development Purposes)

Pull-ups disable write-protect and hold functions by default.

QSPI_FLASH_3V3_1 — R27_1 10.0k — R28_1 10.0k

U2_1 — MX25V1635FZNQ

8	VCC	QSPI_FLASH_3V3_1
1	CS	QSPI_CS_1
6	SCLK	QSPI_CLK_1
5	SI/SIO0	QSPI_D0_RS_1 — R30_1 0 — QSPI_D0_1
2	SO/SIO1	QSPI_D1_RS_1 — R31_1 0 — QSPI_D1_1
3	WP/SIO2	QSPI_D2_RS_1 — R32_1 0 — QSPI_D2_1
7	HOLD/SIO3	QSPI_D3_RS_1 — R33_1 0 — QSPI_D3_1
9	EP	GND
4	GND	GND

NOR Flash 16Mb (2M x 8) 80MHz CLK

Place termination and pull-up resistors close to QSPI flash - minimize stubs.

ClassName: SYSTEM_3V3

SYSTEM_3V3 — R29_1 0 — QSPI_FLASH_3V3_1

Flash 3.3V Power Disconnect - Use to disconnect power to flash.

C6_1 10V 10uF — C7_1 16V 1uF — C8_1 50V 0.1uF — GND

Debug Test Header (For Development Purposes)

GPADC1_1	R21_1 0	GPADC1_CONN_1
GPADC2_1	R22_1 0	GPADC2_CONN_1
GPADC3_1	R23_1 0	GPADC3_CONN_1
GPADC4_1	R24_1 0	GPADC4_CONN_1
GPADC5_1	R25_1 0	GPADC5_CONN_1
GPADC6_1	R26_1 0	GPADC6_CONN_1

J1_1 — TSM-106-01-L-DV — GND

ClassName: AWR_DEBUG

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TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: AWR_1	
Cust Rev: Not in version contrl		Assembly VAWRiant:	Sheet:10of 19
Drawn By:a0271760		File: PROC054E_AWR_Interfaces.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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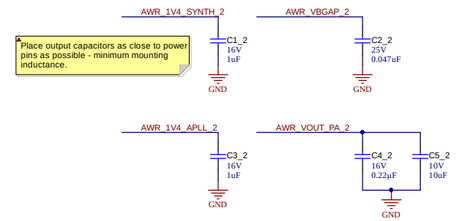
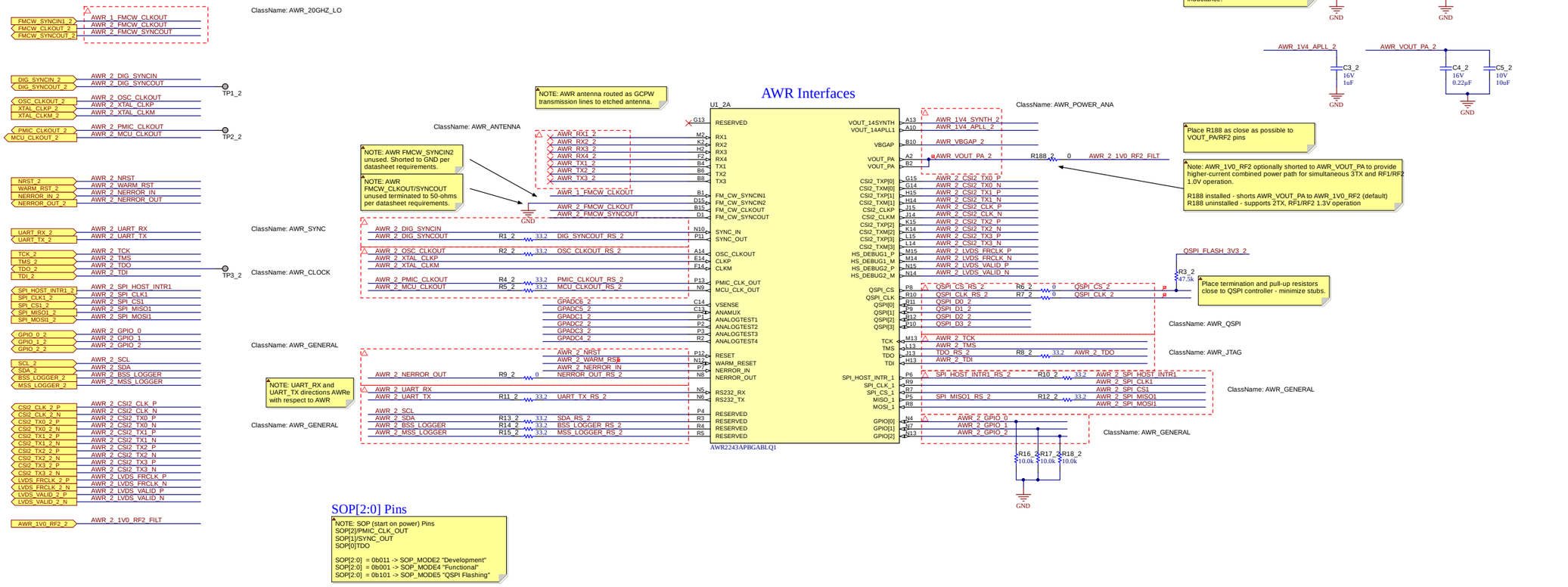
References

http://www.ti.com/product/AWR2243

AWR LDO and Bandgap Output Capacitors



AWR Interfaces



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NOTE: SOP (start on power) Pins
SOP[2]/PMIC_CLK_OUT
SOP[1]/SYNC_OUT
SOP[0]TDO

SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
SOP[2:0] = 0b001 -> SOP_MODE4 "Functional"
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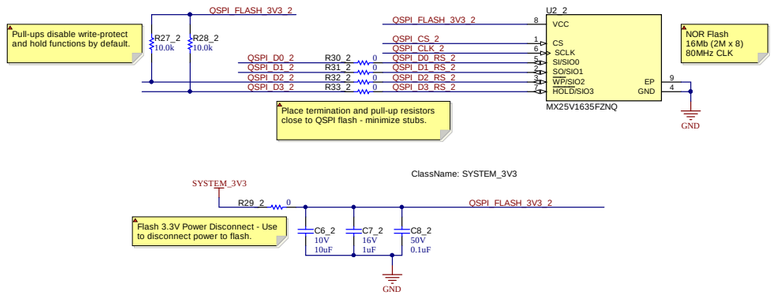
NOR QSPI FLASH (For Development Purposes)



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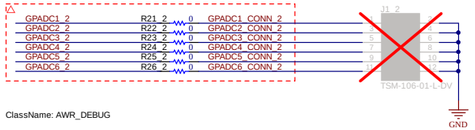

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TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: AWR_1	
Variant:	Rev: Not in version control	Assembly VAWRiant:	Sheet: 10 of 19
Drawn By: a0271760		File: PROC054E_AWR_Interfaces.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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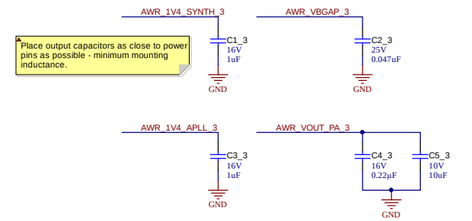
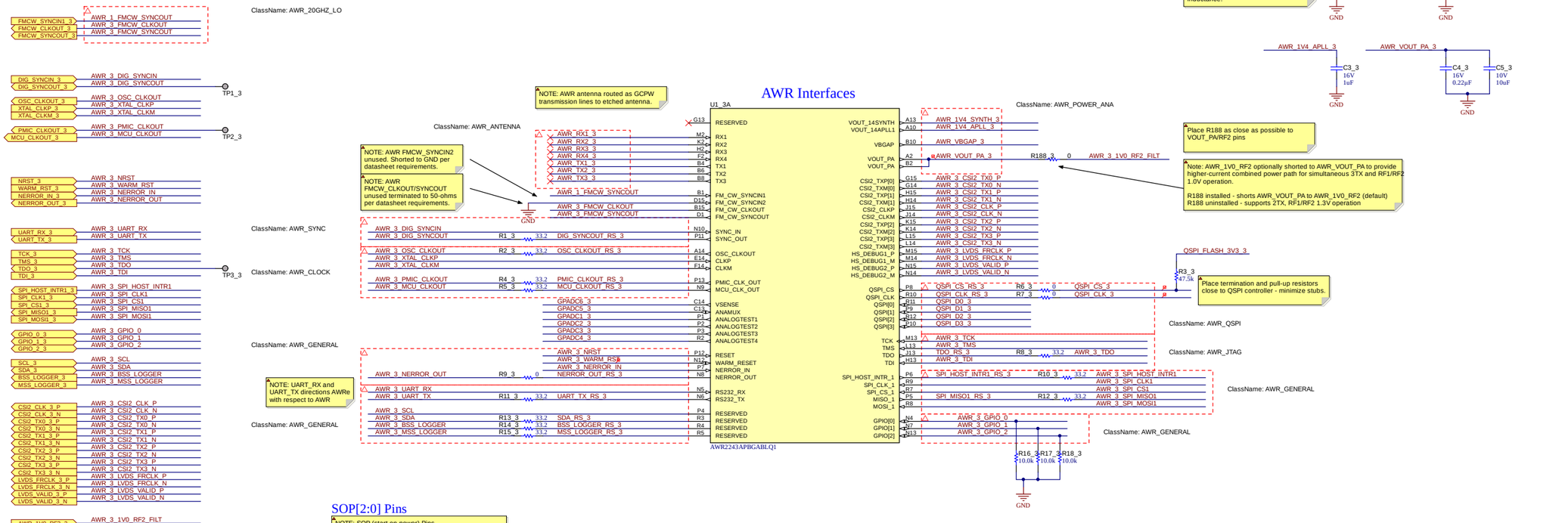
AWR LDO and Bandgap Output Capacitors



AWR Interfaces

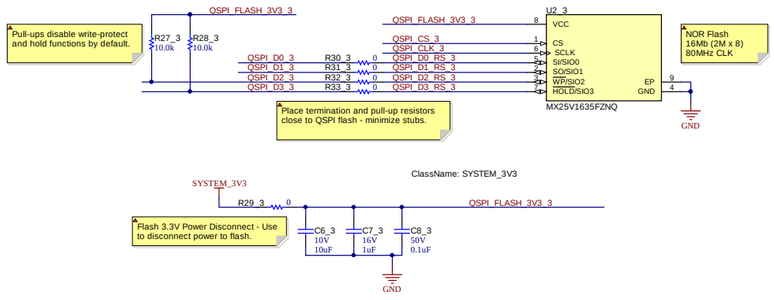


SOP[2:0] Pins

NOTE: SOP (start on power) Pins
SOP[2]/PMIC_CLK_OUT
SOP[1]/SYNC_OUT
SOP[0]TDO

SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
SOP[2:0] = 0b001 -> SOP_MODE4 "Functional"
SOP[2:0] = 0b101 -> SOP_MODE5 "QSPI Flashing"

NOR QSPI FLASH (For Development Purposes)



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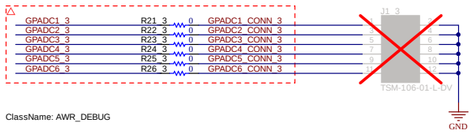

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Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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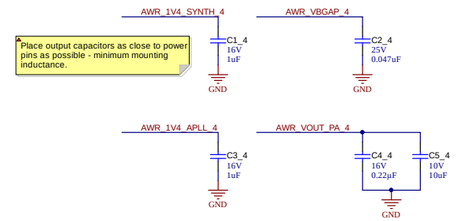
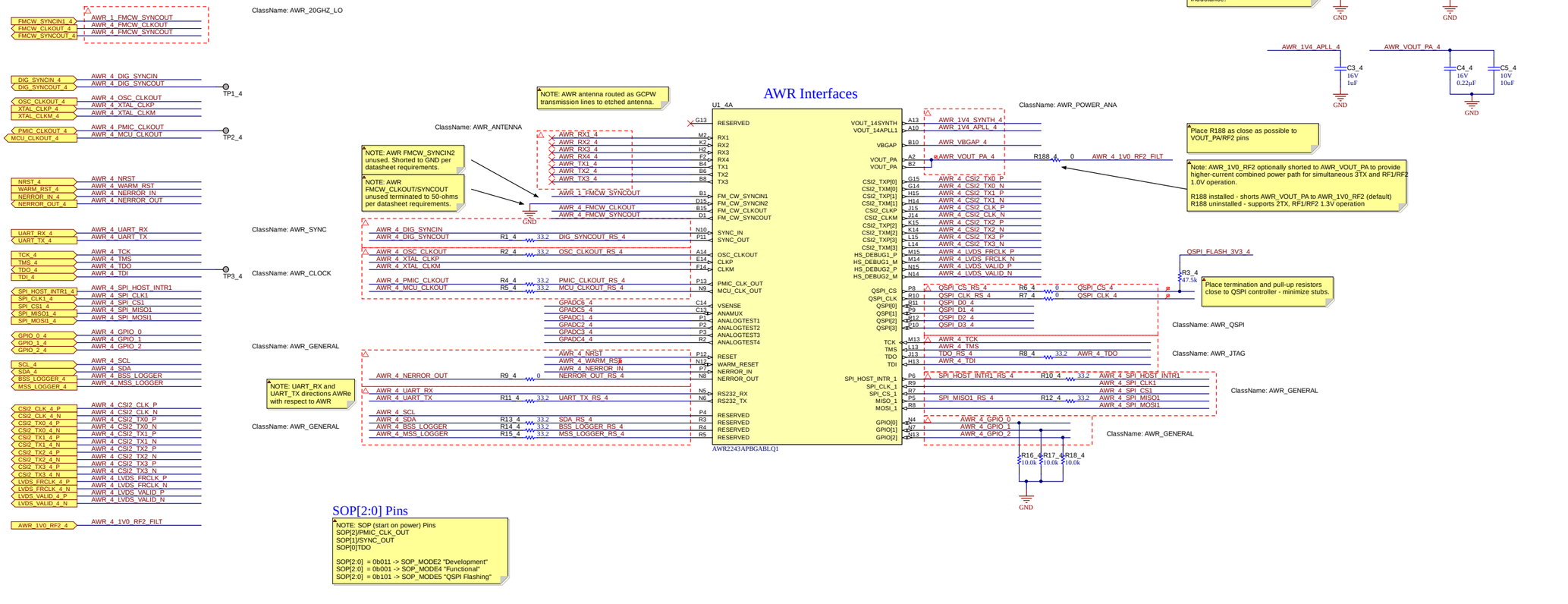
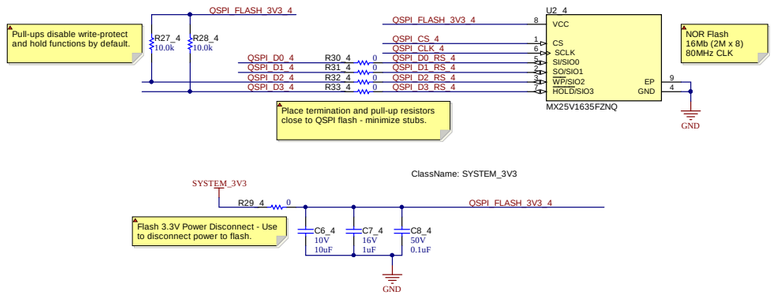


AWR Interfaces



SOP[2:0] Pins

NOR QSPI FLASH (For Development Purposes)



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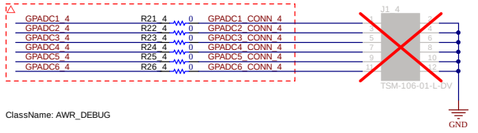

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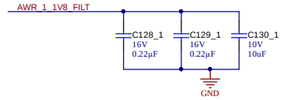
References
http://www.ti.com/product/AWR2243

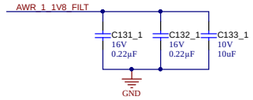
AWR Radar SoC - Power and Decoupling

AWR Power - BGA Decoupling

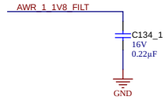
VIN_18BB SUPPLY



VIN_18VCO, VIN_18CLK SUPPLY



VIOIN_18DIFF SUPPLY



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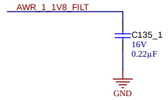

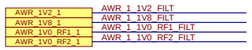

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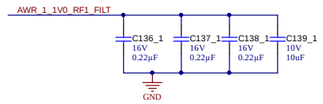

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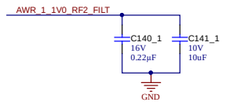
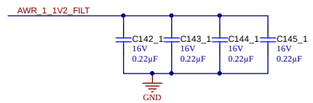


VDDIN SUPPLY



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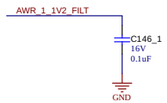

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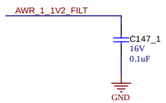

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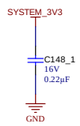

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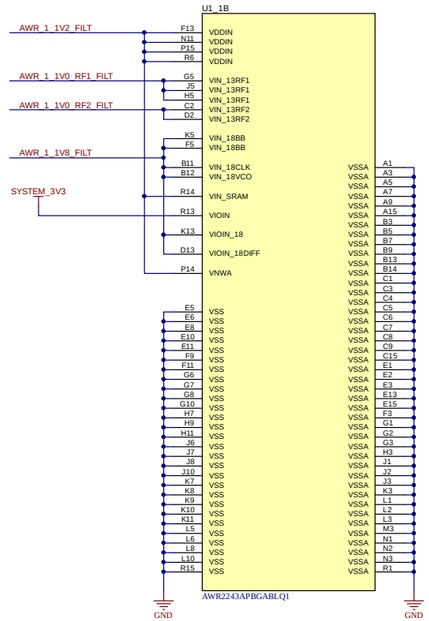

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Number: PROC054	Rev: E	Sheet Title: DECOUPLING_CAPS_1	
Variant:	Rev: Not in version control	Assembly VAWRiant:	Sheet: 11 of 19
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Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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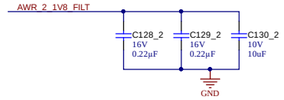

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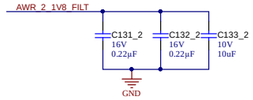

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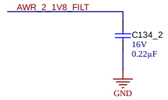

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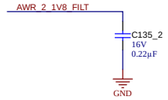

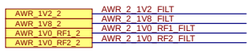

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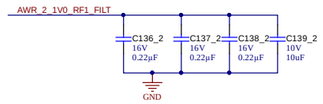

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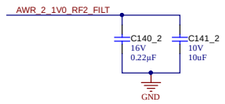

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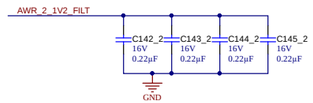

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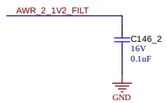

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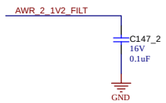

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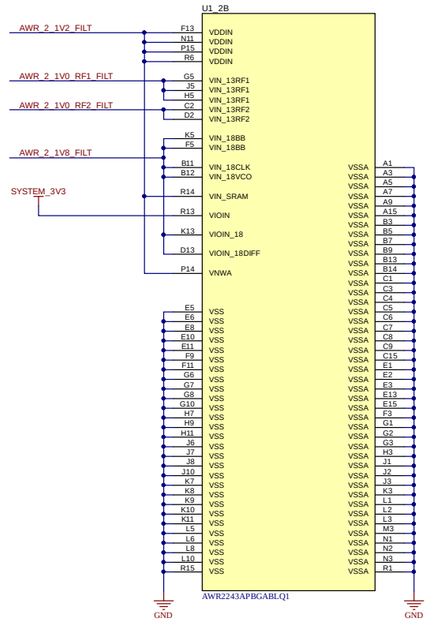

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Number: PROC054	Rev: E	Sheet Title: DECOUPLING_CAPS_1	
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Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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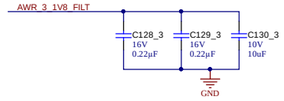
VIN_18BB SUPPLY



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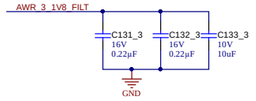

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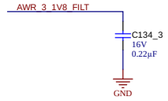

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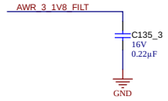

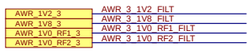

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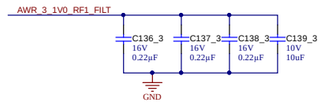

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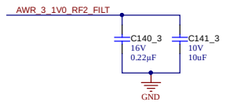

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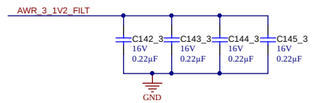

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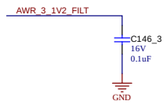

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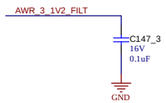

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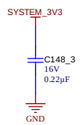

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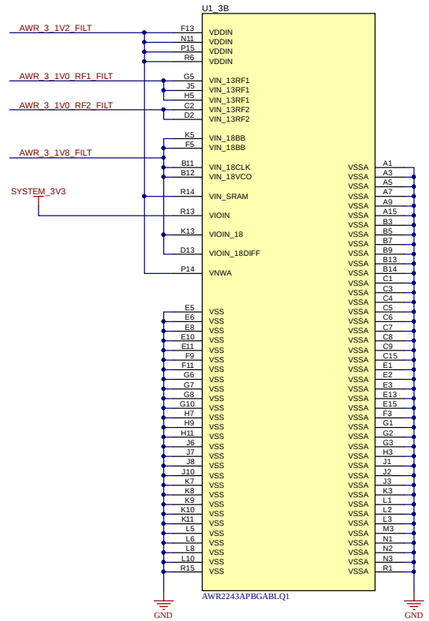

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Number: PROC054	Rev: E	Sheet Title: DECOUPLING_CAPS_1	
VAWRiant:	Rev: Not in version control	Assembly VAWRiant:	Sheet: 11 of 19
Drawn By:a0271760		File: PROC054E_AWR_Power_Decoupling.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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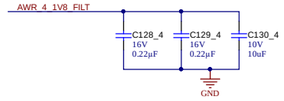

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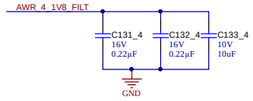

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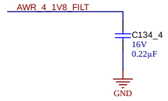

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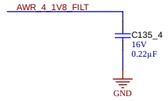

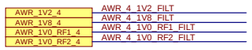

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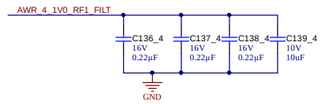

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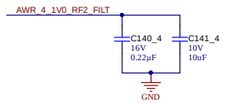

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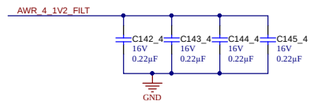

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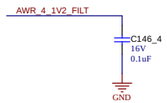

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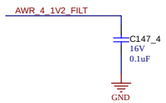

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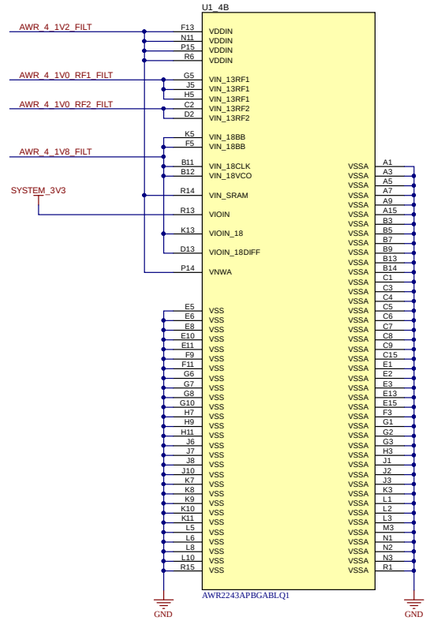

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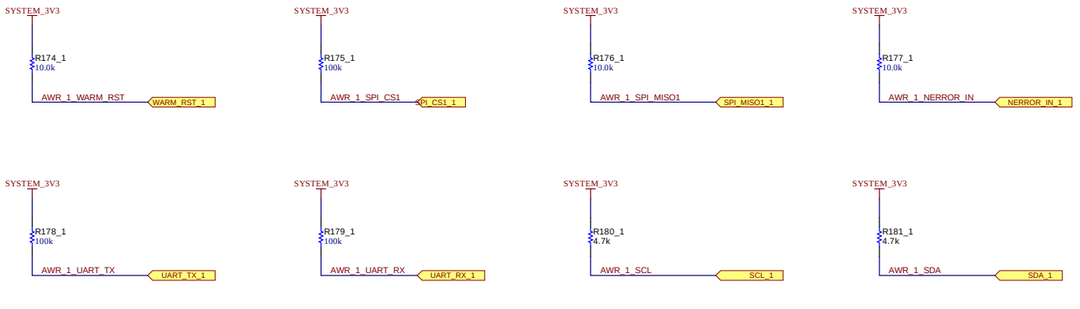
AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



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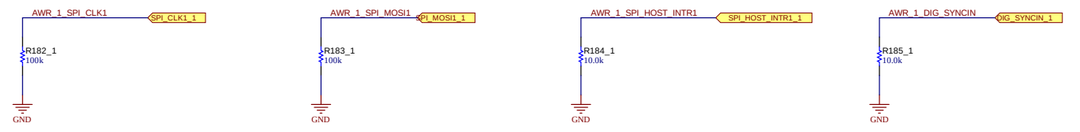

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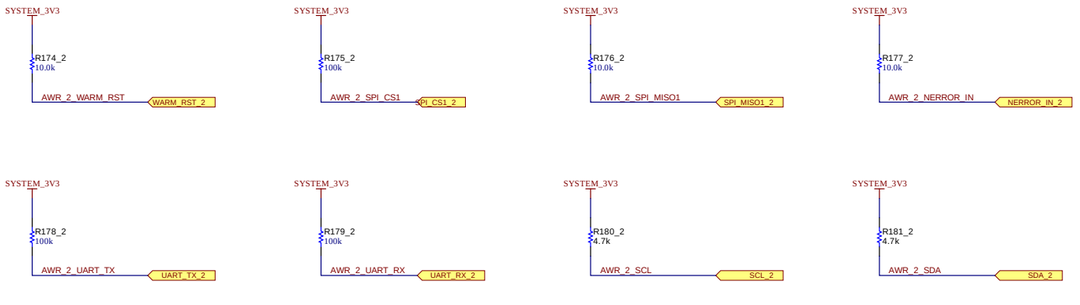
PULL-UP OPTIONS



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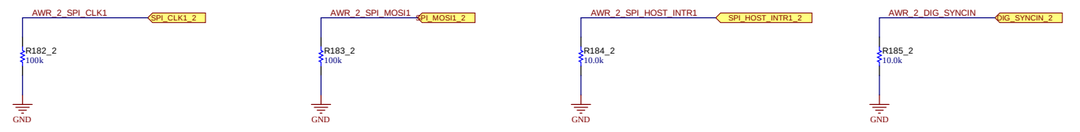

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 8/14/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: PULL_UP_DOWN_1	
Cust Rev: Not in version control		Assembly VAWRiant:	Sheet:12 of 19
Drawn By:a0271760		File: PROC054E_AWR_Pull_Resistors.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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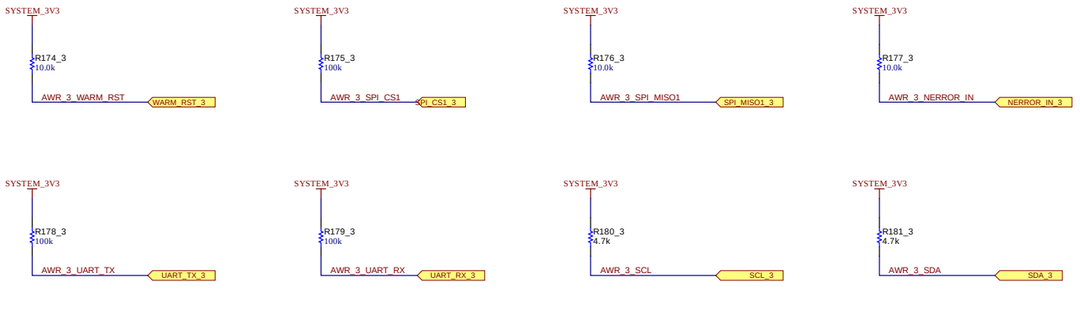
References
http://www.ti.com/product/AWR2243

AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



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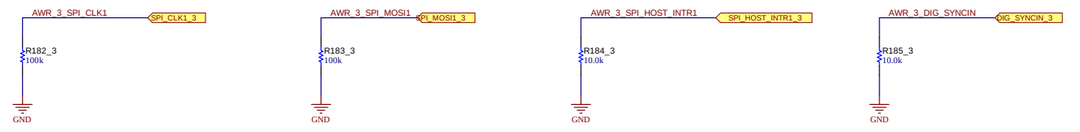

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Number: PROC054	Rev: E	Sheet Title: PULL_UP_DOWN_1	
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Drawn By:a0271760		File: PROC054E_AWR_Pull_Resistors.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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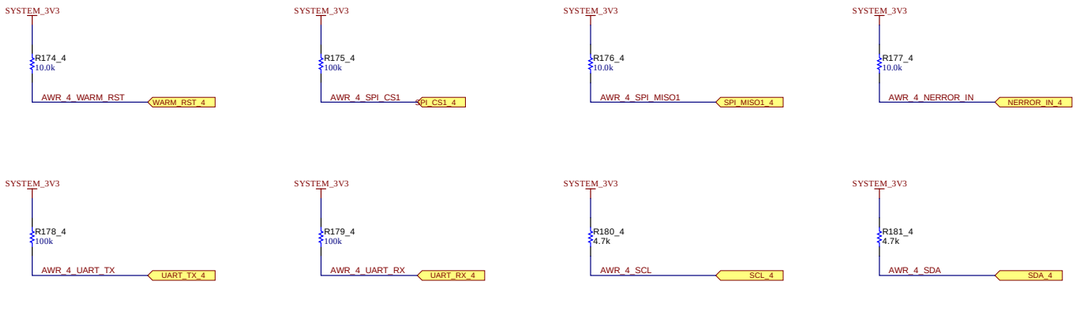
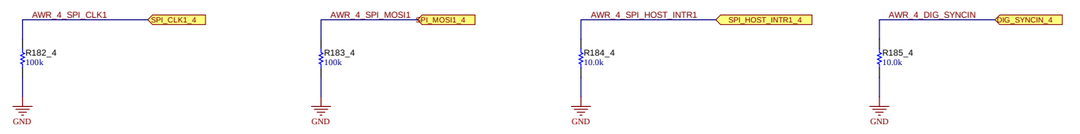
References
http://www.ti.com/product/AWR2243

AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



PULL DOWN OPTIONS



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Orderable: MMW_CAS_RF_EVM	Designed for:Public Release	Mod. Date: 8/14/2020
TID #: N/A	Project Title: MMWCAS-RF-EVM	
Number: PROC054 Rev: E	Sheet Title: PULL_UP_DOWN_1	
Custom Rev: Not in version control	Assembly VAWRiant:	Sheet: 12 of 19
Drawn By: a0271760	File: PROC054E_AWR_Pull_Resistors.SchDoc	Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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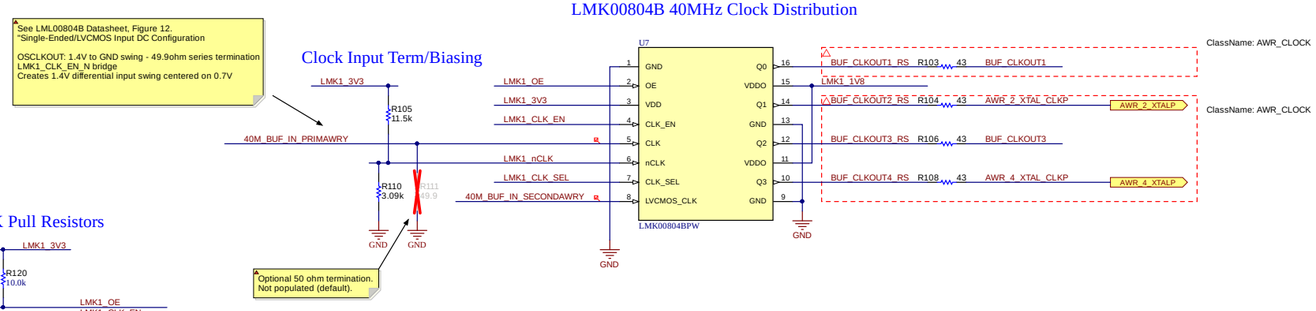
40 MHz Clock Generation and Distribution

References

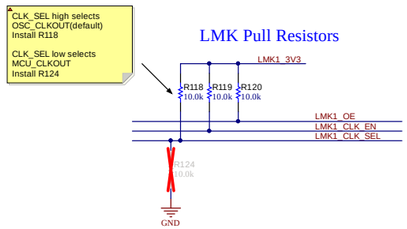
LMK00804BEVM User's Guide

LMK00804B 40MHz Clock Distribution

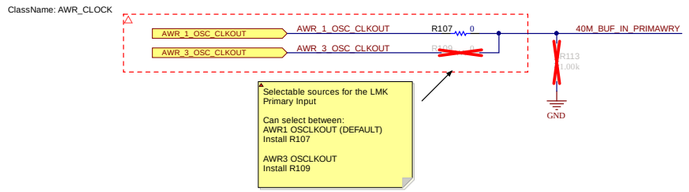
Clock Input Term/Biasing



LMK Pull Resistors



LMK Buffer - PrimAWRy Input Select



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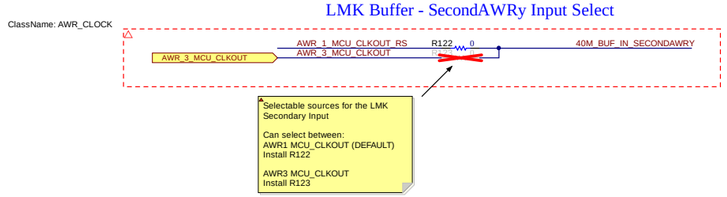
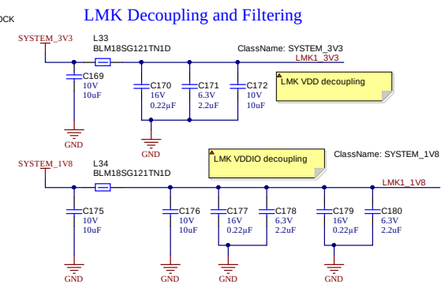


LMK Decoupling and Filtering



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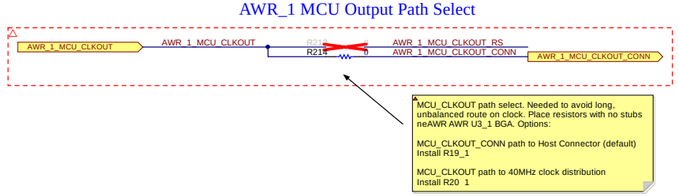

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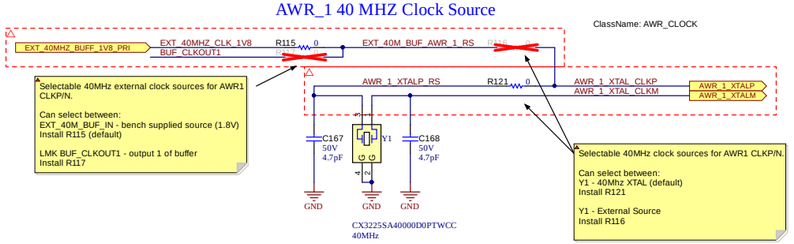
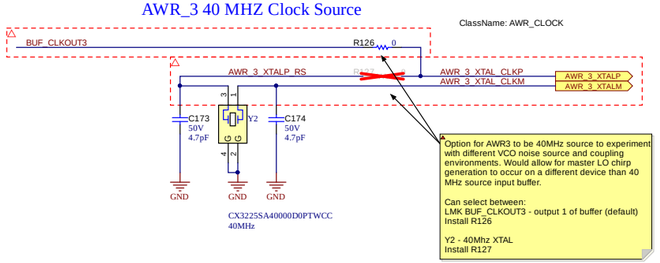
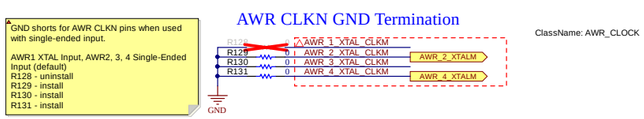


AWR_3 40 MHZ Clock Source



AWR CLKN GND Termination



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Orderable: MMW_CAS_RF_EVM		Designed for: Public Release	Mod. Date: 8/14/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: 40MHZ_CLOCK_1	
Scope:	Rev: Not in version control	Assembly VAWRant:	Sheet: 13 of 19
Drawn By: a0271760		File: PROC054E_40MHZ_Clock.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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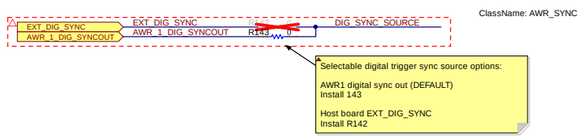
Digital Sync Trigger and 20GHz LO Distribution

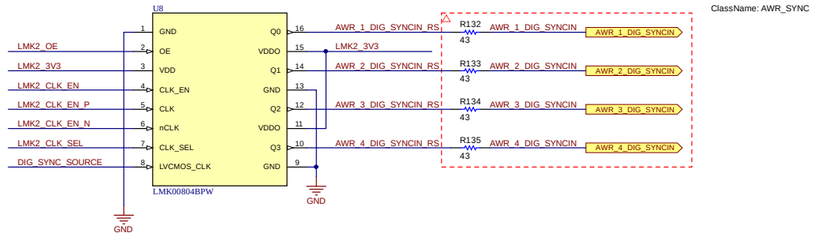
References

LMK00804BEVM User's Guide

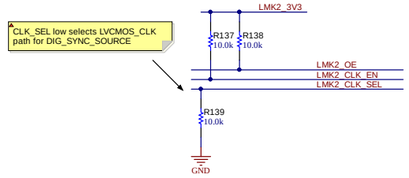
Digital Sync Source Select



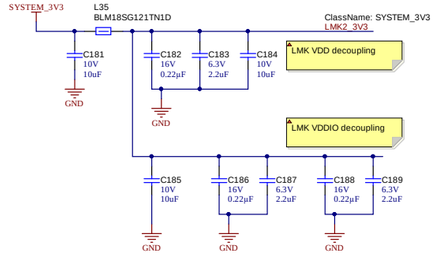
LMK00804B Digital Sync Distribution



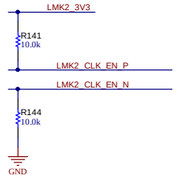
LMK Pull Resistors



LMK Decoupling and Filtering

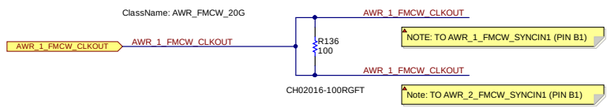


LMK Unused Input

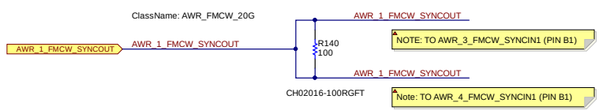


FMCW 20GHz LO SYNC

Wilkenson Power Divider #1



Wilkenson Power Divider #2



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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 8/14/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: FMCW_SYNC	
Sch Rev: Not in version control		Assembly VAWRiant:	Sheet:14of 19
Drawn By:a0271760		File: PROC054E_FMCW_Sync.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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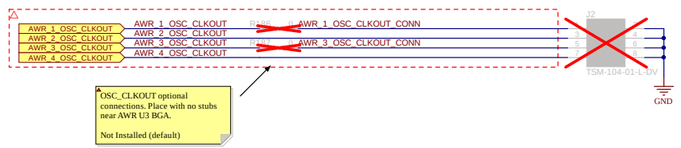
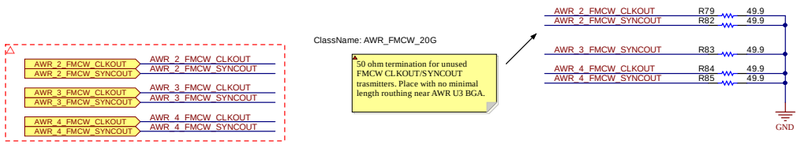
Test Headers, Connectors and Terminations

Oscillator Clock Output Header

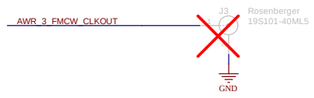
ClassName: AWR_CLOCK



Unused 20GHz LO Output Termination



20GHz LO Test Output



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Orderable: MMW_CAS_RF_EVM	Designed for:Public Release Mod. Date: 8/14/2020
TID #: N/A	Project Title: MMWCAS-RF-EVM
Number: PROC054 Rev: E	Sheet Title: SMA_SMP_CONNECTORS
Variant: Not in version control	Assembly VAWRiant: Sheet 15of 19
Drawn By:a0271760	File: PROC054E_SMA_SMP_Connectors.SchDoc Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave

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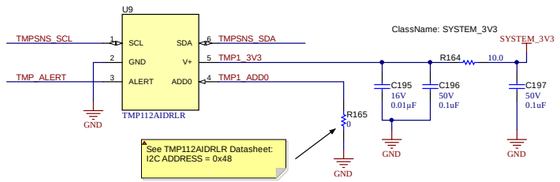
System Temperature Sensors

TMP112 #1



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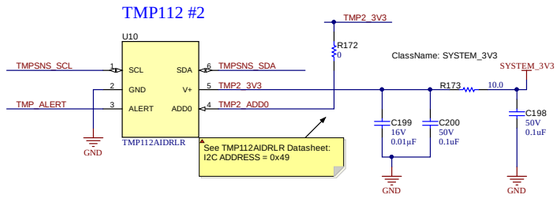

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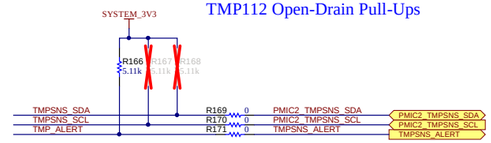

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TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: ON_BRD_TEMP_SENSOR	
Custom Rev: Not in version control		Assembly VAWRiant:	Sheet: 16 of 19
Drawn By: a0271760		File: PROC054E_Temp_Sensor.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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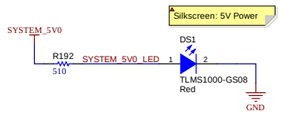
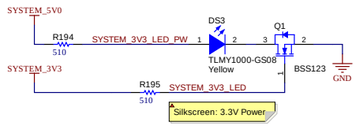
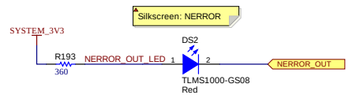
System Indicator LED

POWER LEDS





ERROR LEDS



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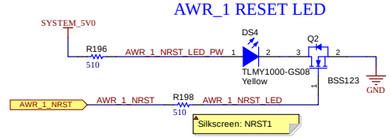
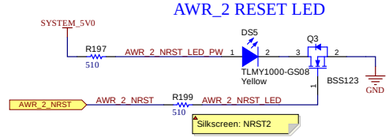
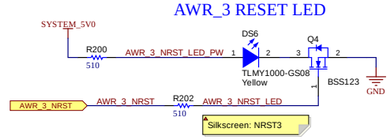


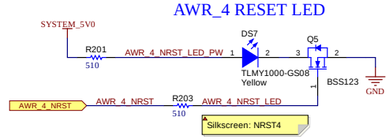
AWR_2 RESET LED



AWR_3 RESET LED



AWR_4 RESET LED



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Orderable: MMW_CAS_RF_EVM	Designed for: Public Release	Mod. Date: 8/14/2020
TID #: N/A	Project Title: MMWCAS-RF-EVM	
Number: PROC054 Rev: E	Sheet Title: SYSTEM_LED	
Variant: Not in version control	Assembly VAWRiant:	Sheet: 17 of 19
Drawn By: a0271760	File: PROC054E_System_LED.SchDoc	Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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Hardware, Mounting Holes and Logos

FID1 FID2 FID3 FID4 FID5 FID6

PCB Number: PROC054
PCB Rev: E

PCB LOGO
Texas Instruments

CE MAWRk

PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

PCB LOGO
ESD Susceptible

CAUTION HOT SURFACE

ZZ1
Assembly Note
These assemblies AWRe ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standAWRds IPC-A-610 Class 2, unless otherwise specified.

ZZ4
Assembly Note
R136/R140 require special attention due to no solder-mask RF construction. For any questions, please contact TI design team.

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Number: PROC054	Rev: E	Sheet Title: HAWRdwAWRe	
Cust Rev: Not in version control		Assembly VAWRiant:	Sheet: 18 of 19
Drawn By: a0271760		File: PROC054E_EVM_Hardware.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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Cascade Radar RF Board - Revision History

Revision History

Rev	Date	Released By	Notes
1	2018/07/09	Randy Rosales <rosales.r@ti.com>	Initial release for layout cleanup and internal review.
2	2018/07/17	Randy Rosales <rosales.r@ti.com>	Updating based on 2018/07/09 comments. Combined PMIC_BUCK_EN and PMIC_NRST Combined PMIC1_PGOOD and PMIC2_PGOOD into single SYSTEM_PGOOD Updating NRST generation scheme from LP87524P PMIC Created sepAWRate AWR_X reset generation paths Combined GPIO2 and PGOOD into PGOOD net Removing leftover resistor selection options from the previous LDO and PMIC power paths. Removing first level LC filtering options from the previous LDO and PMIC power paths. Removed: L3, L6, L19, L22 Removed: C21, C29, C78, C86 Removed: C21, C29, C78, C86 This also removed a few power net segments which will now be fed directly from PMIC output Combined AWR_1_1V8_FILT and AWR_4_1V8_FILT into AWR_14_1V8_FILT Combined AWR_2_1V8_FILT and AWR_3_1V8_FILT into AWR_23_1V8_FILT Changing XWR LC filter to use TDK NLCV32T-R10M-EFRD identified by power team analysis PMIC1_AWR_14_1V8 now directly feeds into SYSTEM_1V8 supply - there was no reason to run this through XWR 1.8V LC filter. Added SYSTEM_5V0 to 3.3V resistor divider for LP87524 PMIC pull-up resistors Updated U2 to the Macronix MX25V1635FZNQ - aligning with other XWR EVM kits Removed R125 - Optional resistor remaining from previously removed option for alternative XTAL input Changed NERROR_OUT LED bias to SYSTEM_3V3 Updated coversheet block diagram Updated power distribution block diagram
2	2018/07/17	Randy Rosales <rosales.r@ti.com>	Added variant information for do not populate stuffing options.
3	2018/07/18	Randy Rosales <rosales.r@ti.com>	Removed 50 ohm terminations to ground at the J2 OSCCLK_OUT test header Removed test headers on PMIC output rails Added zero-ohm resistor between PMIC GPIO3 and PGOOD Replaced all note, class and netname instances of AWR with XWR for industrial/automotive alignment of schematics Replaced all series termination on LMK00804B output with 43 ohm resistors per LMK00804B datasheet Replaced XWR reset generation circuit with discrete AND gate Required for achieving clean reset of XWR devices across all device mAWRgins Netname error on XWR SPI interface - MISO netname change R112 and EXT_40MHZ_CLK_1V8 removed - this was an alternative clock path that is no longer supported Eliminated RF1/2 channel naming error in PROC054_System_Power.SchDoc and PROC054_System_Top.SchDoc
4	2018/07/21	Randy Rosales <rosales.r@ti.com>	Changed R54 to pull-up resistor. LP87524P GPIO2 and GPIO3 both configured as open-drain output.
5	2018/07/21	Randy Rosales <rosales.r@ti.com>	Added 10kohm pull-up to LP87524P GPIO3 - required after change separating out GPIO3 and PGOOD nets Aligned PMIC1 and PMIC2 RF1 and RF2 LC filter components with 1.2V and 1.8V filter Previous RF1 and RF2 LC values were still not merged from removal of LDO option separation of RF1 and RF2 supplies
6	2018/07/28	Randy Rosales <rosales.r@ti.com>	Changing all layout critical resistors and capacitors to small-outline version in Altium Vault library Required to allow Tessolve to implement original decoupling and series resistor layout near the AWR BGA Will allow for more compact routing throughout the design as well Changed R136, R140 FMCW LO power divider resistor to RF resistor CH02016-100RJFT Changed U3 and U4 PMIC to reference proper P-version in Altium vault. Adding zero-ohm resistors to AWR_1/2/3/4 I2C interfaces, optionally shorting those interfaces to the PMIC1_2C Changed NERROR_OUT LED to sourced from shorted NERROR_OUT Originally being fed AWR_1_ERROR_OUT
7	2018/08/08	Randy Rosales <rosales.r@ti.com>	Added R188 which shorts AWR_VOUT_PA to AWR_1V0_RF2 supply nets. Recommended for supporting increased current into the RF2 supplies in 1.0V mode supporting simultaneous 3 TX operation
8	2018/08/09	Randy Rosales <rosales.r@ti.com>	Added burn danger logo Added ESD danger logo Consolidated FMCW 20G LO, digital sync and clock net classes. Created the following net classes: AWR_FMCW_20G AWR_CLOCK AWR_SYNC Removed extraneous MCU_CLKOUT_CONN path from XWR2, XWR3 and XWR4 Consolidated XWR1 MCU_CLKOUT path output options on PROC054_40MHZ_CLK1 schematic sheet Renamed schematic PROC054_40MHZ_FMCW_SYNC to PROC054_FMCW_SYNC Aligned antennas with AWR prefix naming convention Added all nets on 40MHZ_CLOCK_1 schematic sheet to netclass XWR_CLOCK
9	2018/08/10	Randy Rosales <rosales.r@ti.com>	Added additional nets to the AWR_SYNC net class Added additional nets to the AWR_FMCW_20G net class Replaced J3 with correct Rosenberger 19S101 part from TI Altium Vault.
10	2018/08/16	Randy Rosales <rosales.r@ti.com>	Added additional R19 and R20 0-ohm resistors to create optional feedback path for bench supply connector P3
11	2020/01/16	Randy Rosales <rosales.r@ti.com>	Revision D updates Changing primary IC (U1_1, U1_2, U1_3 and U1_4) to AWR2243P Cleaning up net names, ports, net classes, and notes to reference AWR vs. AWR12 specificially
12	2020/08/13	Randy Rosales <rosales.r@ti.com>	Revision E updates Changing primary IC (U1_1, U1_2, U1_3 and U1_4) to AWR2243P ES1.1, AWR2243APBGABLQ1 Changing AWR VBGAP capacitor (C1_1, C1_2, C1_3 and C1_4) to 47nF capacitor GRM155R71E473KA88D Changing PMIC digital input voltage divider resistors (R34, R59) to from 1.0ohhm to 1.0kohm resistors This matches initial design intent Simplified BOM by removing duplicate 0402 0-ohm resistors models on optional signal paths Cleaned up top layer soldermask near edges of RF regions Cleaning up various note spelling errors

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 8/14/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: E	Sheet Title: Revision History	
Variant:	Rev: Not in version control	Assembly VAWRiant:	Sheet:19 of 19
Drawn By:a0271760		File: PROC054E_Revision_History.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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