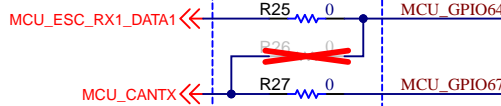


### EtherCAT / MCAN-A Boot Selection

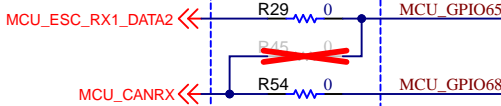
Mode	Resistor Configuration
EtherCAT support*	Populate R25/R27 and R29/R54 with 0-ohm resistor, remove R26/R45.
MCAN-A boot support	Populate R26/R45 with 0-ohm resistor, remove R25/R27 and R29/R54.

\*Default

Place near U1, use Z pattern to eliminate trace stubs



Place near U1, use Z pattern to eliminate trace stubs

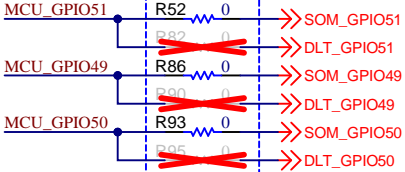


### FSI Baseboard / DLT Selection

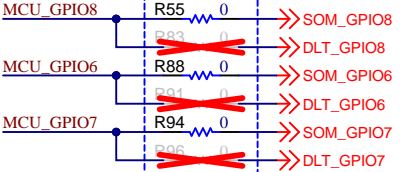
Mode	Resistor Configuration
Baseboard support*	Populate all 0-ohm resistors on SOM_GPIO nets. Remove all resistors on DLT_GPIO nets.
DLT support	Populate all 0-ohm resistors on DLT_GPIO nets. Remove all resistors on SOM_GPIO nets.

\*Default

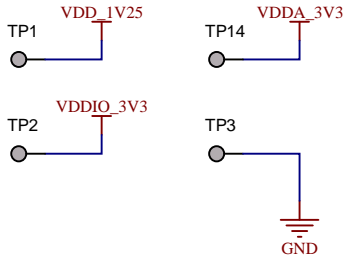
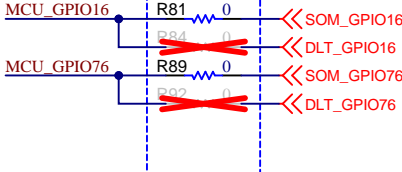
Place near U1

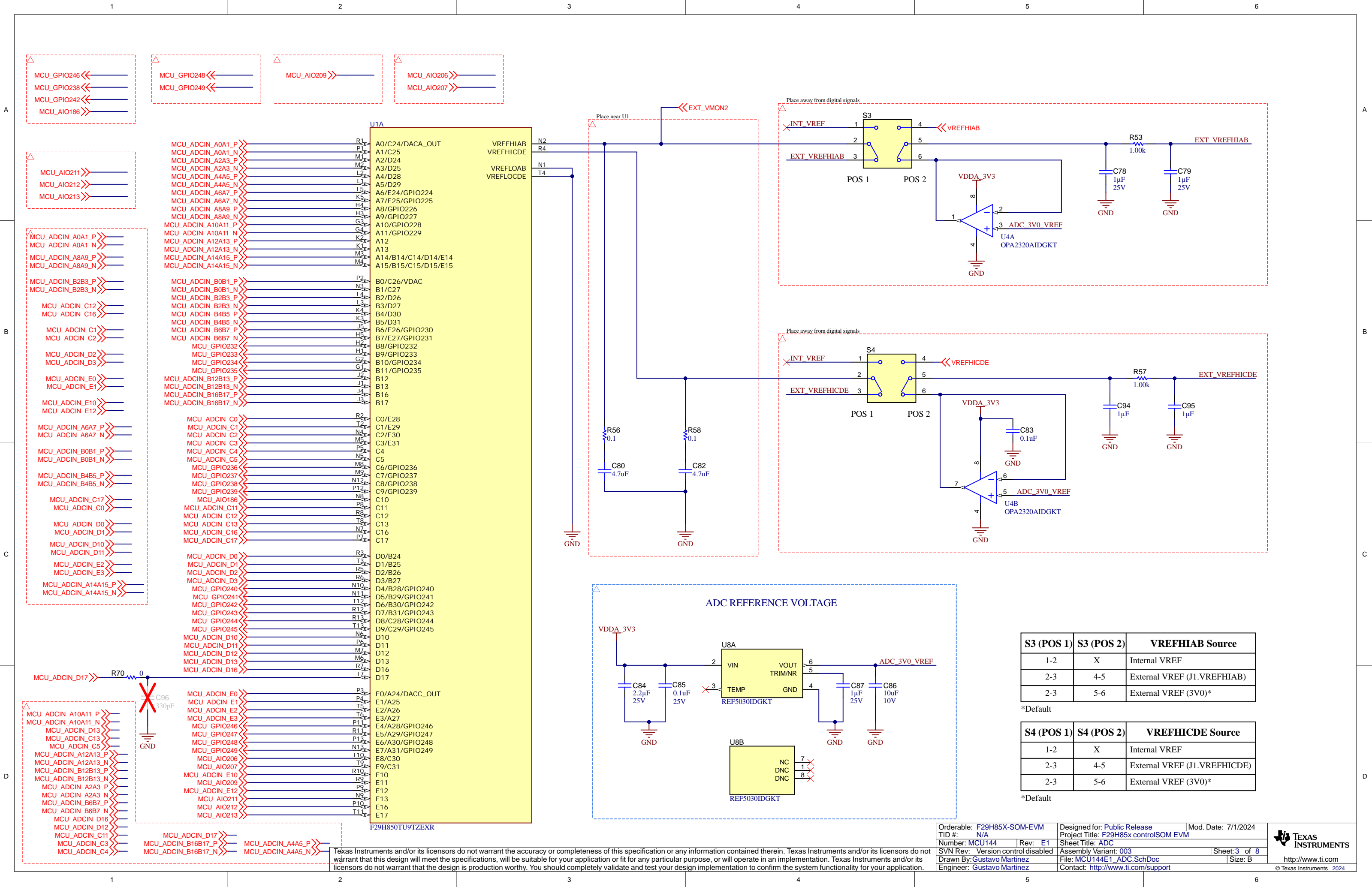


Place near U1



Place near U1





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Orderable:	F29H85X-SOM-EVM	Designed for:	Public Release	Mod. Date:	7/1/2024
TID #:	N/A	Project Title:	F29H85x controlSOM EVM		
Number:	MCU144	Rev:	E1	Sheet Title:	ADC
SVN Rev:	Version control disabled	Assembly Variant:	003		Sheet: 3 of 8
Drawn By:	Gustavo Martinez	File:	MCU144E1_ADC.SchDoc		Size: B
Engineer:	Gustavo Martinez	Contact:	http://www.ti.com/support		

### Clock

The schematic shows the clock circuit for the F29H85x device. It includes two clock generators, Y1 (LMK6CE02500CDLFT) and U5 (LMK1C1103PWR), and their connections to the F29H85x device.

**Y1 (LMK6CE02500CDLFT) Connections:**

- VDD (Pin 4) is connected to 3V3\_OUT through capacitor C75 (0.1uF, 25V).
- OE (Pin 1) is connected to GND through a red 'X' (R37, 0).
- OUT (Pin 3) is connected to GND through a red 'X' (R30, 10.0k).
- GND (Pin 2) is connected to GND.

**U5 (LMK1C1103PWR) Connections:**

- VDD (Pin 6) is connected to 3V3\_OUT through capacitor C74 (0.1uF, 25V).
- 1G (Pin 2) is connected to GND through a red 'X' (R33, 10.0k).
- CLKIN (Pin 1) is connected to GND through resistor R36 (0).
- GND (Pin 4) is connected to GND.

**F29H85x Device Connections:**

- YO (Pin 3) is connected to PHY0\_25MHZ\_CLK through resistor R34 (75.0).
- Y1 (Pin 8) is connected to PHY1\_25MHZ\_CLK through resistor R38 (75.0).
- Y2 (Pin 5) is connected to PHY1\_25MHZ\_CLK through resistor R80 (75.0).
- NC (Pin 7) is connected to GND through a red 'X'.

**Notes:**

- Place near U5: A red dashed box indicates the location for components near U5.
- Red dashed boxes highlight the connections to the F29H85x device.

# Clock Source Selection

The image displays two circuit diagrams for clock source selection. Both diagrams feature a multiplexer (indicated by a circle with two input lines) that selects between two clock sources: `MCU_GPIO54` and `PHY0_25MHZ_CLK` (for the top diagram) or `PHY1_25MHZ_CLK` (for the bottom diagram). The selected output is labeled `ECAT_PHY0_CLK` and `ECAT_PHY1_CLK` respectively. In both cases, the `PHY` clock path is highlighted in red, indicating it is the selected source. The multiplexers are labeled `R31` and `R35` with a value of `0`, and the `PHY` clock paths are labeled `R32` and `R97` with a value of `0`.

## Reset and JTAG

**Reset and JTAG**

NOTE: PMIC (U2) adds internal pull-up resistor on MCU\_XRSn. Hence R46 is not populated by default.

## Boot Mode Selection Switch

The diagram illustrates a circuit for selecting boot modes using a switch S1. The switch has six pins. Pins 1 and 4 are connected to 3V3\_OUT. Pins 2 and 5 are connected to MCU\_GPIO72 and MCU\_GPIO84 respectively, each through a 2.49k resistor (R42 and R43). Pins 3 and 6 are connected to GND.

Modes	GPIO72	GPIO84	Boot Modes
00	0	0	Boot from Parallel GPIO*
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN
03	1	1	Boot from Flash

\*Default


## Board ID EEPROM

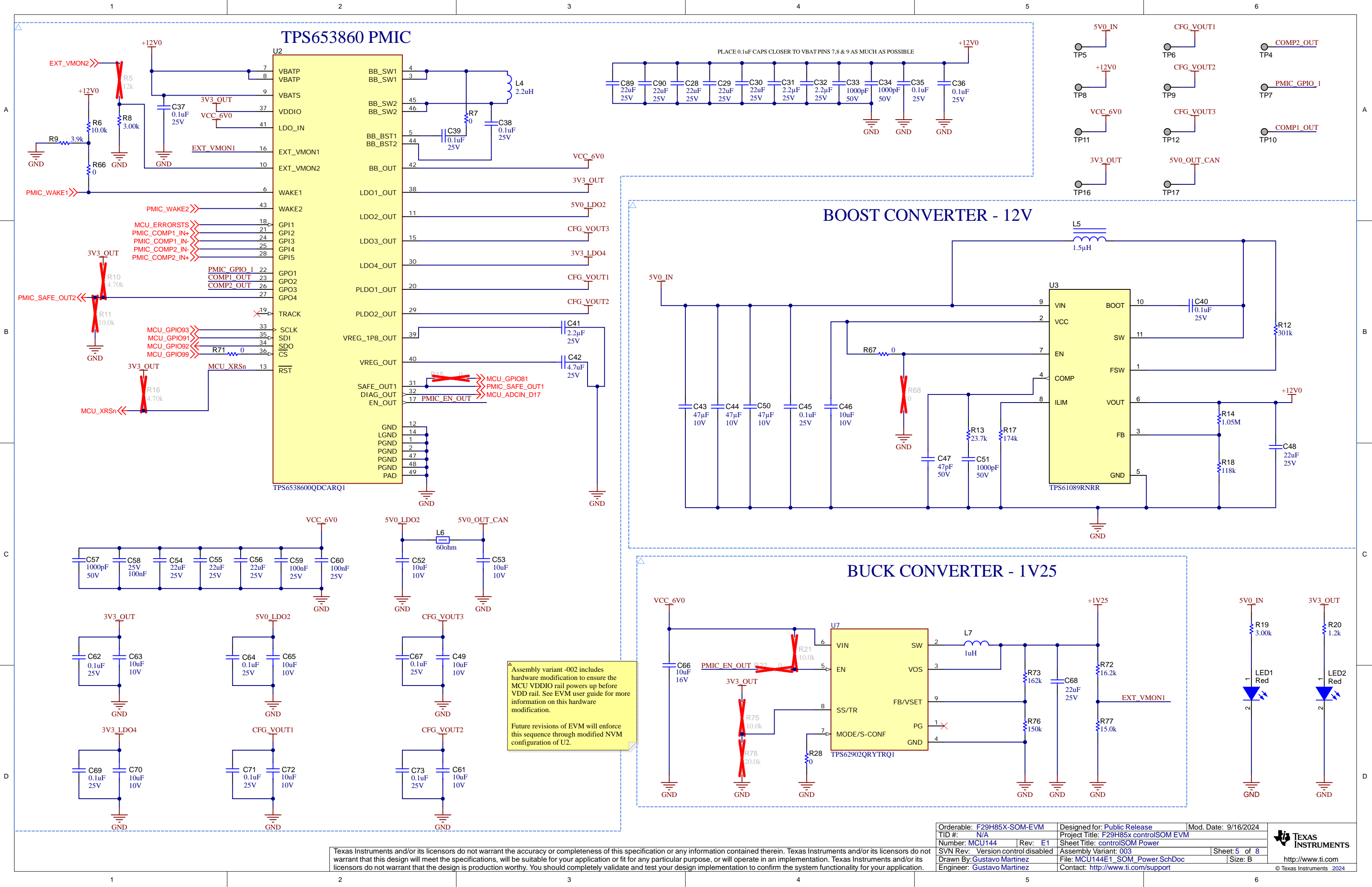
The diagram illustrates the Board ID EEPROM circuit. The EEPROM chip (U6) is connected to the 3V3\_OUT supply. The VCC (pin 8) is connected to 3V3\_OUT through a 4.70k resistor (R49). The WP (pin 7) is connected to 3V3\_OUT through a 4.70k resistor (R50). The SCL (pin 6) is connected to the EEPROM\_I2CSCL signal. The SDA (pin 5) is connected to the EEPROM\_I2CSDA signal. The chip's NC (pins 1, 2, 3) and VSS (pin 4) are connected to GND. A 0.1uF 25V capacitor (C77) is connected between 3V3\_OUT and GND. A 0 ohm resistor (R69) is connected between the SDA line and GND.

# User LEDs

The diagram shows two identical LED circuits. Each circuit consists of a 3V3\_OUT supply connected to a 1.2k resistor (R47 for LED3, R48 for LED4). The other end of the resistor is connected to the anode (pin 1) of the LED. The cathode (pin 2) of each LED is connected to a microcontroller pin: MCU\_GPIO23 for LED3 and MCU\_GPIO9 for LED4. Both LEDs are labeled 'LED3 Green' and 'LED4 Green'.

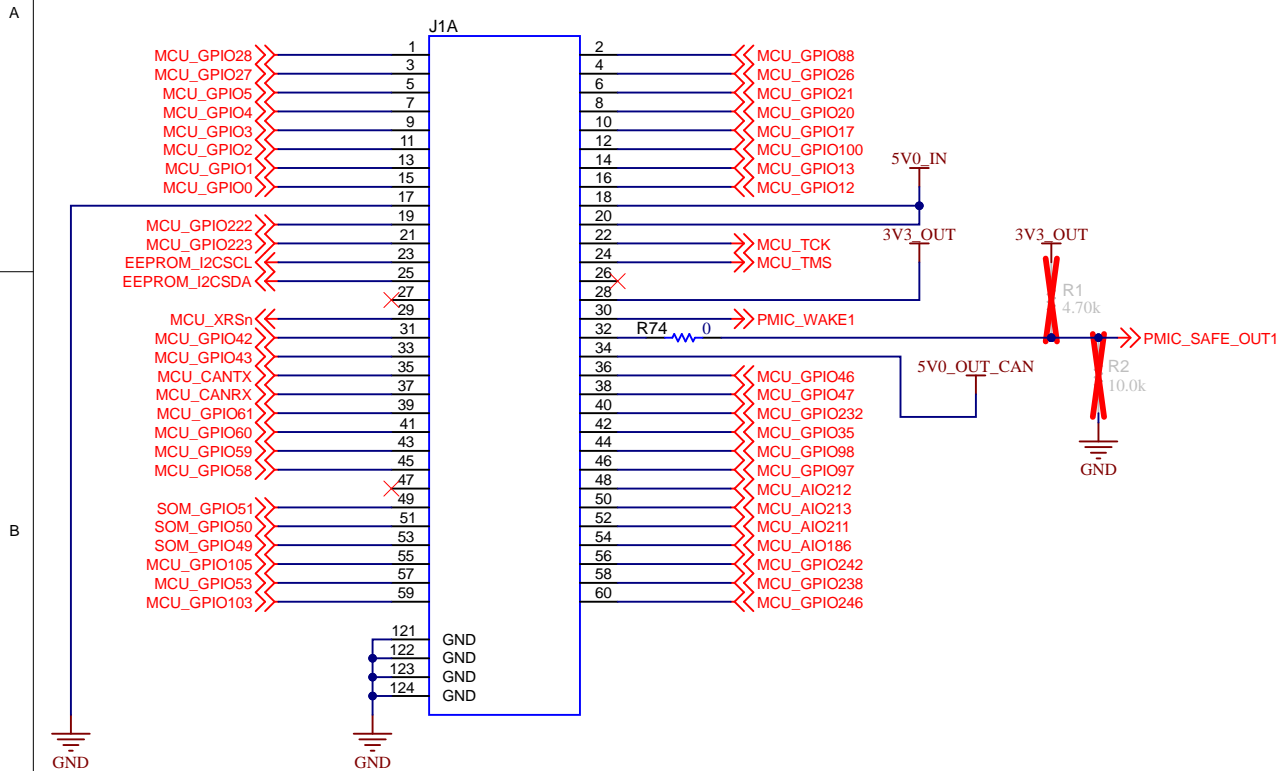
\*Default

Orderable: <a href="#">F29H85X-SOM-EVM</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 12/9/2024	 <b>TEXAS INSTRUMENTS</b>  <a href="http://www.ti.com">http://www.ti.com</a> © Texas Instruments 2024
TID #: <a href="#">N/A</a>	Project Title: <a href="#">F29H85x controlSOM EVM</a>		
Number: <a href="#">MCU144</a>	Rev: <a href="#">E1</a>	Sheet Title: <a href="#">Clock, Reset, and Boot</a>	
SVN Rev: Version control disabled	Assembly Variant: <a href="#">003</a>	Sheet: <a href="#">4</a> of <a href="#">8</a>	
Drawn By: <a href="#">Gustavo Martinez</a>	File: <a href="#">MCU144E1_Clock_Reset_Boot_SchDoc</a>	Size: B	
Engineer: <a href="#">Gustavo Martinez</a>	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>		

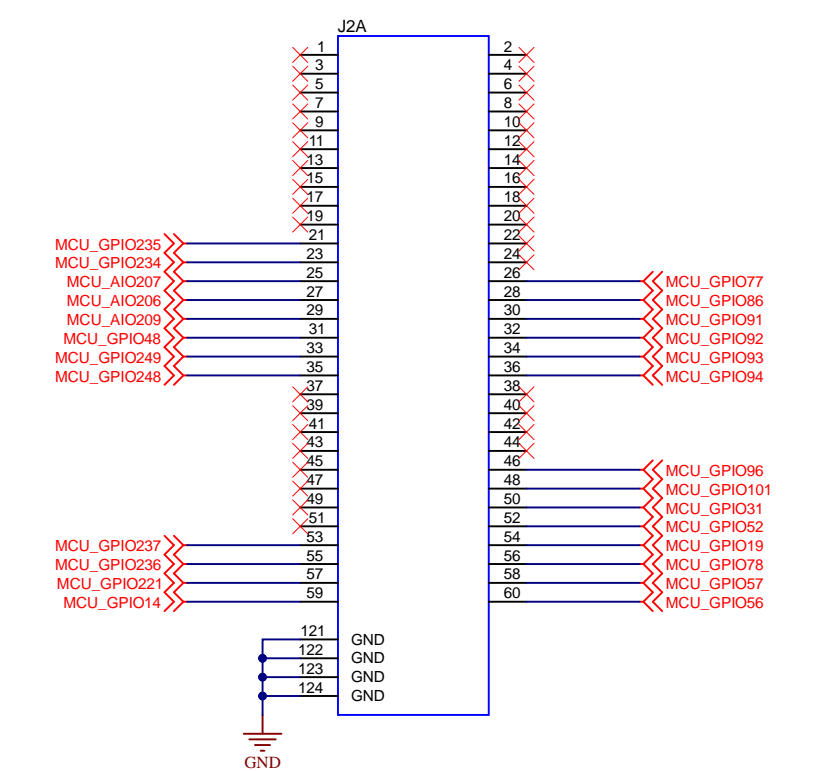




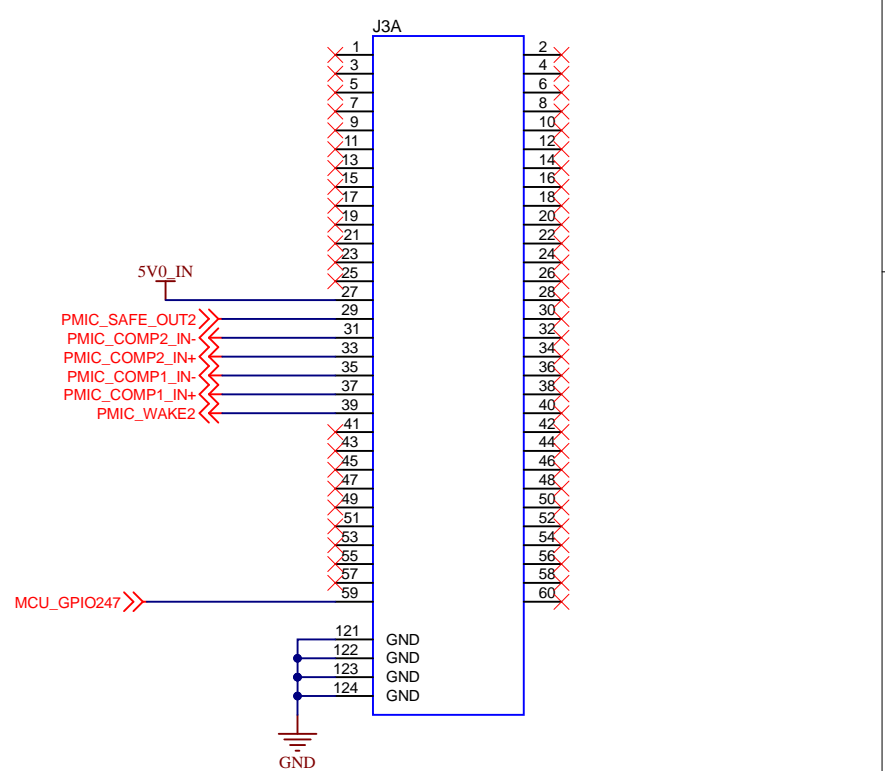
## High Density Connector J1



## High Density Connector J2



## High Density Connector J3



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Orderable: F29H85X-SOM-EVM	Designed for: Public Release	Mod. Date: 7/1/2024
TID #: N/A	Project Title: F29H85x controlSOM EVM	
Number: MCU144	Rev: E1	Sheet Title: Baseboard Connectors
SVN Rev: Version control disabled	Assembly Variant: 003	Sheet: 6 of 8
Drawn By: Gustavo Martinez	File: MCU144E1_Baseboard_Connectors.SchDoc	Size: B
Engineer: Gustavo Martinez	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

A

A

B

B

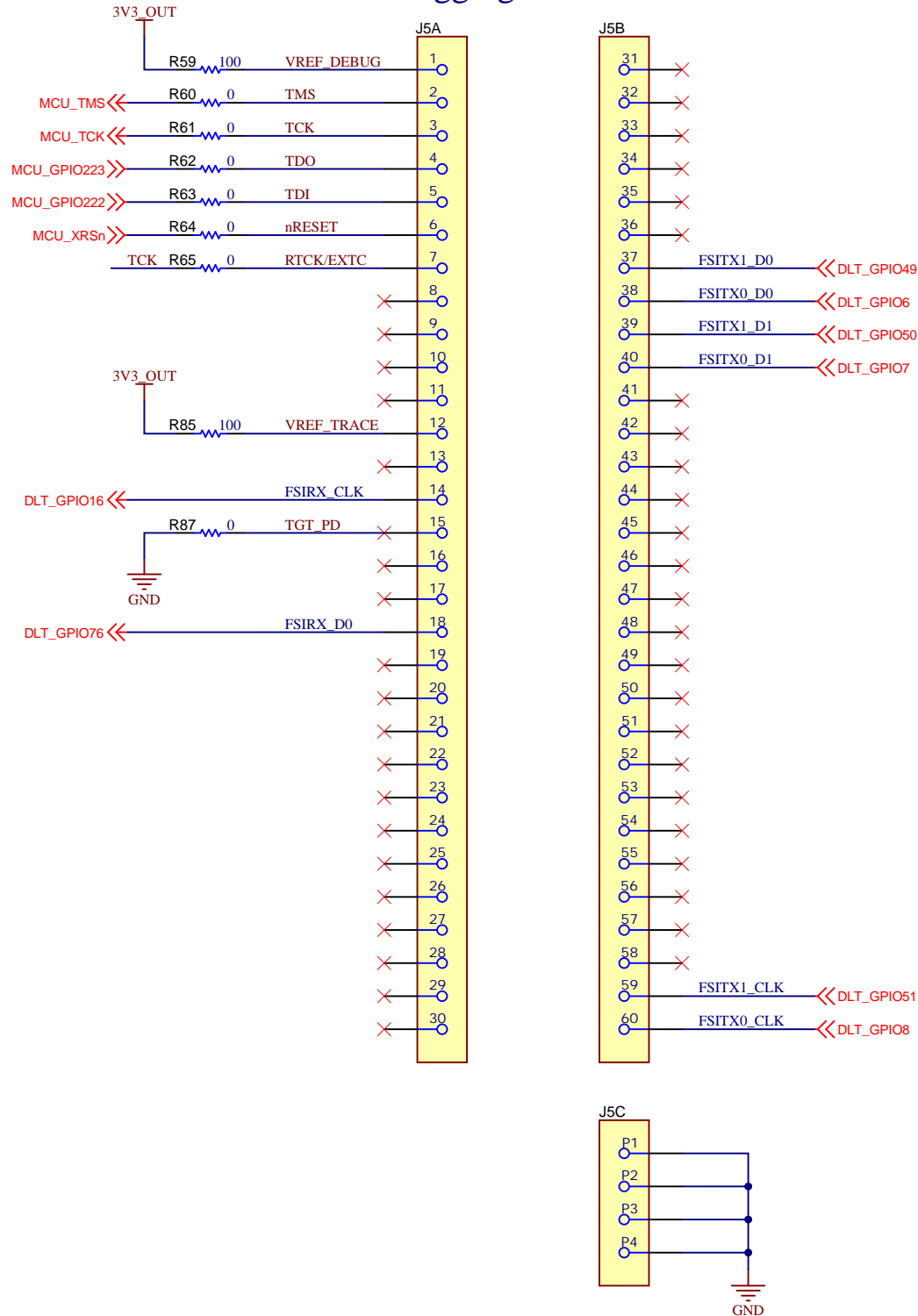
C

C

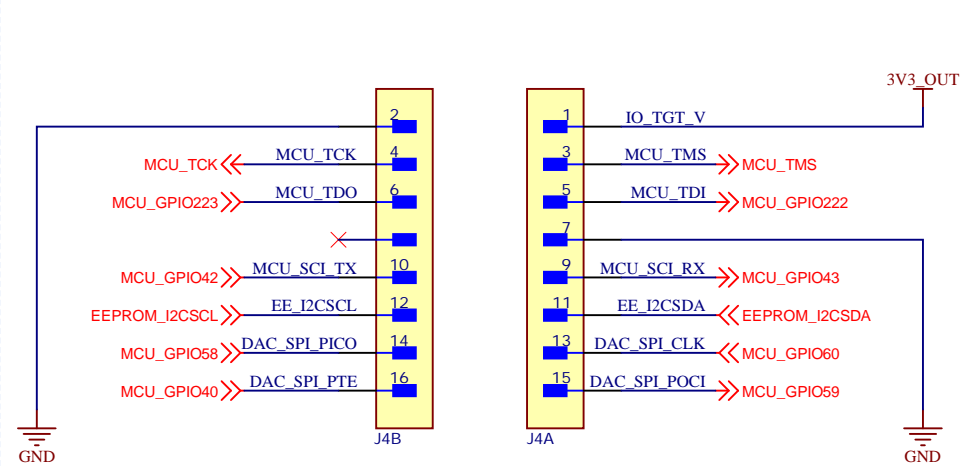
D

D

### Data Logging and Trace Connector



### Emulator Connector



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Orderable: F29H85X-SOM-EVM		Designed for: Public Release	Mod. Date: 7/1/2024
TID #: N/A		Project Title: F29H85x controlSOM EVM	
Number: MCU144	Rev: E1	Sheet Title: Emulation Connectors	
SVN Rev: Version control disabled		Assembly Variant: 003	Sheet: 7 of 8
Drawn By: Gustavo Martinez		File: MCU144E1_Emulation_Connectors.SchDoc	Size: B
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