NOTE:

1. 5 MIL DIFFERENTIAL PAIRS ON L1 AND L3 LAYERS ARE 100 OHMS +/- 10%
2. ALL VIA HOLES NEED TO BE TENTED ON TOP AND BOTTOM SIDE.
3. VIA HOLES UNDER IC U2 NEED TO BE FILLED WITH SOLDER MASK TO PREVENT SOLDER PASTE FLOW INTO VIAS.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.50mil	3.5	
3	L1_Top Layer	Copper	0.70mil		
4	Dielectric 1		8.50mil	4.7	
5	L2_GND1	Copper	0.70mil		
6	Dielectric 2		14.00mil	4.7	
7	L3_Signal	Copper	0.70mil		
8	Dielectric 3		8.50mil	4.7	
9	L4_Plane	Copper	0.70mil		
10	Dielectric 4		14.00mil	4.7	
11	L5_GND2	Copper	0.70mil		
12	Dielectric 5		8.50mil	4.7	
13	L6_Bottom Layer	Copper	0.70mil		
14	Bottom Solder	Solder Resist	0.50mil	3.5	
15	Bottom Overlay				

DESIGN INFORMATION

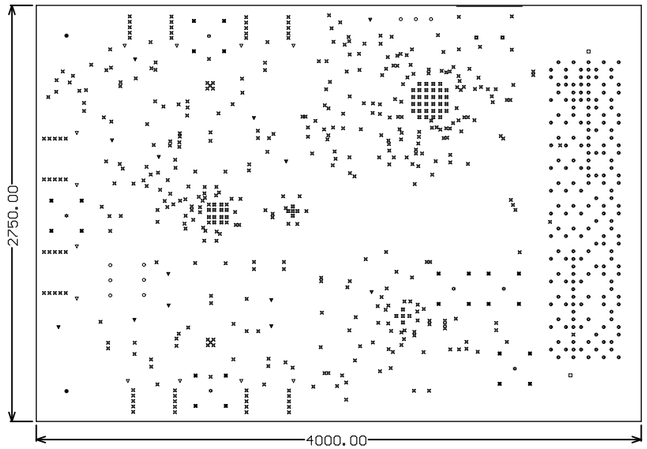
MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 5 mil
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING IPC Class 2 specifications PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER 370HR
THICKNESS: [X] 62 MIL +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER RED
[ ] MATTE [X] SEMI-GLOSS
SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [X] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Routed Path Length	Hole Length	Drill Layer Pair	Tolerance
	2	35.43mil (0.900mm)	NPTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	2	50.00mil (1.270mm)	NPTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	54	7.87mil (0.200mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	+/- 3 mil
	434	8.00mil (0.203mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	183	10.00mil (0.254mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	+/- 3 mil
	12	18.00mil (0.457mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	9	35.00mil (0.889mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	6	59.06mil (1.500mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	13	63.00mil (1.600mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	+/- 3 mil
	24	66.93mil (1.700mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	2	125.98mil (3.200mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	741 Total							

1000.00mil

TEXAS INSTRUMENTS

PROJECT TITLE: ADC3683EVM
DESIGNED FOR: Public Release
FILE NAME: DC134_PCB.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: DC134	REV: E	SUN REV: Not In VersionControl
LAYER NAME = [illegible]ions	TID #: N/A		
PLOT NAME = DC134	GENERATED : 10/6/2020 3:20:31 PM		TEXAS INSTRUMENTS

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ENGINEER:	LAYOUT BY:
Daniel Brock	Daniel Brock
SCALE: 1.00	ALTIUM DESIGNER VERSION: 18.1.9.240