Design Guide: TIDA-010076

Daisy-Chained Power and Data Over Single Pair Ethernet (T1) Reference Design

Description

Communication systems in a daisy-chain topology can significantly benefit from savings on hardware and wiring. A local power supply is no longer needed with power on the data line, and Single Pair Ethernet reduces the cabling to only two wires. The biggest design challenge of such systems is power stability. This reference design shows a stable, 220-W power delivery and a 100-Mbit/s data transmission over Single Pair Ethernet (SPE, 100BASE-T1).

Resources

TIDA-010076	Design Folder
DP83TC811R-Q1, TPS2663	Product Folder
TPD2E2U06-Q1, LMZM33603	Product Folder
MSP430G2332-EP, LM76003	Product Folder
INA180, TLC6C598-Q1	Product Folder
LM74700-Q1, LP2951, LMZ10500	Product Folder

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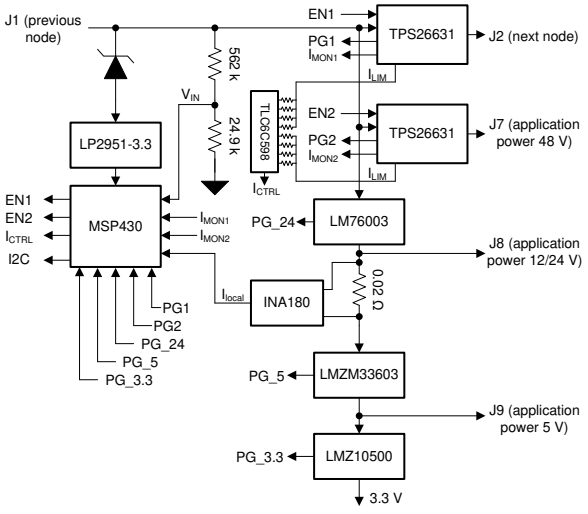
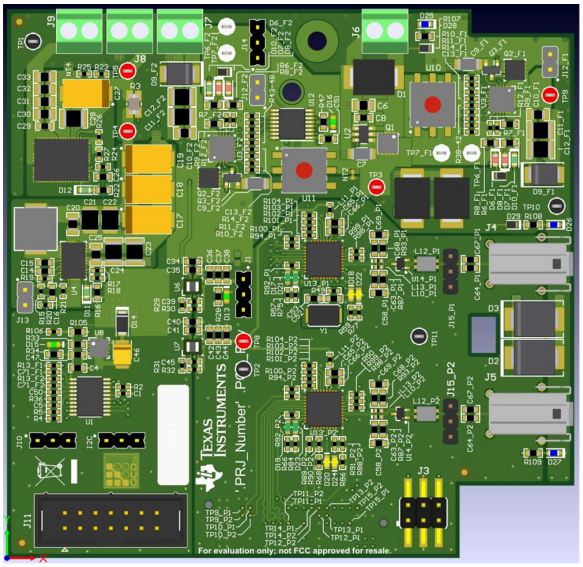
Features

- Single Pair Ethernet (SPE) with 100 Mbit/s
- One twisted pair for power and communication
- 48-V/4.5-A (220-W) system power supply
- Daisy chaining of nodes
- Protection against mis-wiring and surge
- Power budgeting at commissioning and power-up
- Dynamic power assignment during operation

Applications

- Power and communication in robot manipulators
- Daisy-chained field bus systems with power
- Distributed operator panels (HMI, Elevator)
- Sensor systems for drones
- Sensor chains in motor drive





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1 System Description

Many applications in industrial systems require power and communication, including:

- Sensor systems in robots
- Field bus systems with multiple sensors and actuators
- User panel for Programmable Logic Controllers (PLC) (Human Machine Interface = HMI)
- Distributed speaker systems
- Operator panels in air conditioners or elevators

This reference design enables the easiest form of interconnect, a switchless, two-wire Ethernet daisy chain including power. It complements a K2G Sitara™ reference board with T1 Ethernet communication and power over T1 Ethernet. This configuration (node) can provide power up to 180 W to a local consumer through its 5-V, 12-V/24-V, and application power connections. Multiple identical nodes can be connected in a daisy-chain topology to build a system. The daisy-chained nodes communicate with a host controller such as a PLC, a robotics controller, or a drive controller. The design is protocol agnostic and supports any industrial Ethernet protocol as well as proprietary solutions. The nodes can talk to each other like in any other Ethernet system. The host delivers the power through the T1 Ethernet connection to the first node. The first node then powers the next node, and this method continues from node to node. The total system power can be as much as 220 W. This total power level is available for all nodes together. The design ensures that each node receives only as much power as an operator has configured during the set-up process. The power can be split between the nodes as needed. Each node has a configurable current limit for the power to the next node and for the locally used power. This configuration ensures that the system stays operational in the presence of a local overload situation from an application fail or from a short circuit. The design has also the technical provisions for dynamic load sharing. With an enhanced software, the nodes can communicate their power requirements, and the current limits can adjust accordingly.

1.1 Key System Specifications

Table 1 shows the key parameters of the design.

Table 1. Key System Specifications

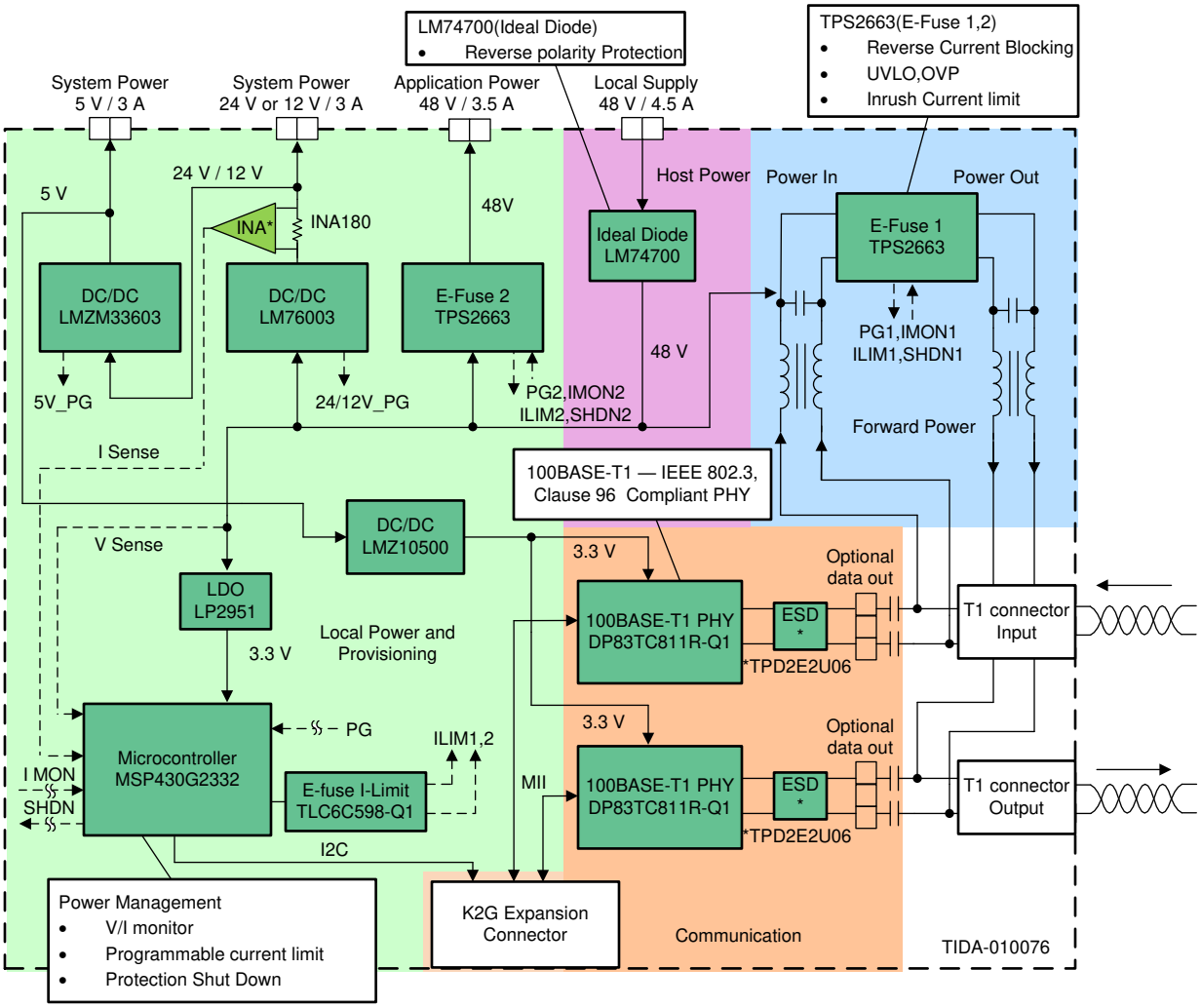
PARAMETER	SPECIFICATIONS	DETAILS
V_{IN} (J6)	Main power supply	35 V - 48 V
I_{IN} (J6)	Main power supply	4.5 A
P_{OUT} (J7)	Application power (J7) at 35 V	>100 W
V_{OUT} (J7)	Application voltage (J7)	Equals V_{IN}
I_{OUT} (J7)	Application current	3 A
V_{OUT} (J8)	Output voltage 12-V / 24-V output, setting 12 V, jumper J13 shorted	11.76 V - 12.24 V
V_{OUT} (J8)	Output voltage 12-V / 24-V output, setting 24 V, jumper J13 open	23.52 V - 24.48 V
I_{OUT} (J8)	Output current 12-V / 24-V output	1 A (3-A peak)
V_{OUT} (J9)	Output voltage 5-V output	4.9 V - 5.1 V
I_{OUT} (J9)	Output current 5-V output	1 A (3-A peak)
Bit rate	Communication speed over T1 interfaces (J4, J5)	100 Mbit/s
BER	Bit error rate including 5 m of cable	$<10^{-9}$
L_1	Maximum cable length, all power at the end, using AWG 22 (1)	20 m
L_2	Maximum cable length, equal power between all nodes, with AWG 20 wire	70 m
T	Ambient temperature	-40°C - 105°C (85°C) (2)

(1) Full amperage of 4.5 A drawn at the end of AWG 22 wire
(2) Maximum cable and T1 connector temperature in parentheses

2 System Overview

2.1 Block Diagram

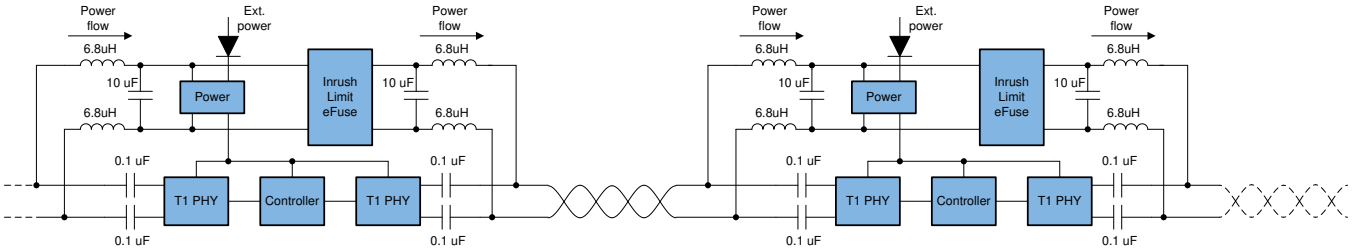
Figure 1. TIDA-010076 Block Diagram



2.2 Design Considerations

Power distribution in Ethernet communication systems is well established in the industry as Power over Ethernet (PoE). These systems feature point-to-point connections between a PoE capable Ethernet switch and corresponding endpoints. There are also IEEE standards for powering systems through Single Pair Ethernet introduced as Power over Data Lines (PoDL). Companies are developing switches with PoDL capabilities. This reference design looks into a different power and data distribution scheme for which there is not yet a full coverage by standards. In this scheme, power and data are daisy chained through a series of communication nodes. In standard implementations, whether PoE or PoDL, power negotiation is only done once at power up. This doesn't fit daisy chaining because the power of the daisy chain is only known after the whole system is powered up. At that time, the power is no longer negotiable with the host. Therefore, each node must negotiate maximum power of itself and all following nodes with the previous node. This leads to a principle stability issue that is covered in Section 2.4.2. In this design, the problem is solved by implementing a dynamic power assignment per node which enables continuous adjustments during start-up and operation. This is a better fit for an industrial environment. Once the system has completely powered up, it is also possible to disable the dynamic adjustment and freeze the power settings. Figure 2 shows the node-to-node connection in more detail.

Figure 2. Daisy-Chain Topology



2.3 Highlighted Products

2.3.1 DP83TC811 Family

The communication function in the design is done by the DP83TC811R-Q1. This is an IEEE 802.3bw-compliant Ethernet physical layer transceiver. It provides all physical layer functions needed to transmit and receive data over twisted-pair cables. The device provides xMII flexibility with support for standard MII, RMII, and RGMII MAC interfaces. It includes the Diagnostic Tool Kit, providing an extensive list of real-time monitoring tools, debug tools, and test modes. Within the tool kit is the first integrated electrostatic discharge (ESD) monitoring tool. It is capable of counting ESD events on both the xMII and MDI as well as providing real-time monitoring through the use of a programmable interrupt. Additionally, the DP83TC811R-Q1 includes a pseudo random binary sequence (PRBS) frame generation tool, which is fully compatible with internal loopbacks to transmit and receive data without the use of a MAC. The full device description is available in the *DP83TC811R-Q1 Low Power Automotive PHY 100BASE-T1 Automotive Ethernet Physical Layer Transceiver Data Sheet*.

2.3.2 TPS2663 Family

The integrated electronic fuse TPS2663 is used on two places in the design. The first fuse separates the application power from the system power. When there is a too-high current draw from the application, the application power is disconnected before it can affect the system power. The second fuse limits the current into the next node. When the next node draws too much power or when the cable is damaged, the power is disconnected before it can affect the operation of the local node. For system stability, the current levels must be set so that only the eFuse breaks that has the faulty load connected. The current limit (I_{LIM}) of the eFuse is therefore made programmable in this design. It can be set through a resistor value which is switchable using four pins of an LED driver TLC6C598 or manual through a rotary switch. For more details about the device family, see the *TPS2663x 60-V, 6-A Power Limiting, Surge Protection Industrial eFuse Data Sheet*.

2.3.3 LM74700

The input power to the design can have miswiring. To protect the circuit from incorrect mounting, a diode function is necessary at the power input. Normal Schottky diodes with their drop voltage of approximately 0.5 V produce significant heat at higher currents. The LM74700 is an ideal diode controller which operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low loss reverse polarity protection with a 20-mV forward voltage drop. This low drop voltage reduces the power loss by a factor of 20 - 30 compared to a Schottky diode. Details about the device features and functions are available in the *LM74700-Q1 Low I_Q Reverse Battery Protection Ideal Diode Controller Data Sheet*.

2.3.4 LM76003

The design supports a selectable 12-V or 24-V supply rail for powering the K2G or any other MII socket compatible board. The selection is done through a switchable feedback resistor network. The LM76003, with its internal compensation, keeps the design simple. The LM76003 regulator is an easy-to-use synchronous step-down DC-DC converter capable of driving up to 3.5 A of load current from an input up to 60 V. For details about the device, see the *LM76002/LM76003 3.5-V to 60-V, 2.5-A/3.5-A Synchronous Step-Down Voltage Regulator Data Sheet*.

2.3.5 LMZM33603

A 5-V rail is powered through the LMZM33603 fully integrated power module. This allows a very dense design and keeps the form factor small. The module is powered from the 12-V or 24-V rail. The overall efficiency is still better than when using a buck regulator with higher input voltage capability. The LMZM33603 power module is an easy-to-use integrated power solution that combines a 3-A, step-down, DC/DC converter with power MOSFETs, a shielded inductor, and passives into a low-profile package. This power solution requires as few as four external components and eliminates the loop compensation and magnetics part selection from the design process. The 9 mm × 7 mm × 4 mm 18-pin, QFN package is

easy to solder onto a printed circuit board and allows a compact, low-profile, point-of-load design. The full feature set, including power good, programmable UVLO, prebias start-up, and overcurrent and overtemperature protection, make the LMZM33603 an excellent device for powering a wide range of applications. Details about the device are shown in the *LMZM33603 4-V to 36-V Input, 3-A Step-Down DC/DC Power Module in QFN Package Data Sheet*.

2.3.6 LMZ10500

The PHYs require 3.3 V and, in the Gbit version, 1 V. These voltages are generated in the design from the 5-V rail through two LMZ10500 modules. These modules enable a high-power density for a compact design. The LMZ10500 nano module is an easy-to-use step-down DC/DC solution capable of driving up to 650 mA load in space-constrained applications. Only an input capacitor, an output capacitor, a small VCON filter capacitor, and two resistors are required for basic operation. Information about applications and the device functionality can be found in the *LMZ10500 650-mA Nano Module With 5.5-V Maximum Input Voltage Data Sheet*.

2.3.7 MSP430G2332-EP

The power management in the design is controlled by an MSP430 family member, the MSP430G2332-EP. In the design, this device performs the following tasks:

- Monitors application current and next-node current using its internal A/D converters connected to the eFuse's ISENSE outputs
- Measures supply voltages and currents
- Sets eFuse current limits
- Communicates with the host controller through I2C

The MSP430G2332-EP is the ideal candidate for this design because it combines multiple ADC channels, digital I/O, an I2C controller, and a high operating temperature of 125°C with extreme low power consumption. For more details about this device, see the *MSP430G2332-EP Mixed Signal Microcontroller Data Sheet*.

2.3.8 INA180

In this design, the input current needed for generating the 24-V/12-V and 5-V rails is calculated based on the output current and input voltage of the 24-V/12-V converter. Because of this, the cost efficient INA180 can be used. The INA180 has a voltage limit of 26 V. The calculation is done by the MSP430 and doesn't add to the cost. The INA180 current sense amplifier is designed for cost-optimized applications. These devices are part of a family of current-sense amplifiers (also called current-shunt monitors) that sense voltage drops across current-sense resistors at common-mode voltages from –0.2 V to 26 V, independent of the supply voltage. The INAx180 devices integrate a matched resistor gain network in four, fixed-gain device options: 20 V/V, 50 V/V, 100 V/V, or 200 V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift. All of these devices operate from a single 2.7-V to 5.5-V power supply. All device options are specified over the extended operating temperature range of –40°C to 125°C. See the device details in the *INAx180 Low- and High-Side Voltage Output, Current-Sense Amplifiers Data Sheet*.

2.3.9 TLC6C598

The setting of I_{LIM} in both of the eFuses requires resistors which are driven low by low-leakage, open-drain outputs. The TLC6C598, with its open-drain outputs, provides a low pin-count solution to this challenge. Each four of the 8 outputs are connected to a binary resistor array for each of the eFuses. With its serial communication, the TLC6C598 occupies only two MCU outputs for one data and one clock signal. The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. Full details are available in the *TLC6C598 8-Bit Shift-Register LED Driver Data Sheet*.

2.3.10 LP2951

In this design, a 3-pin LP2951 with a fixed, 3.3-V setting powers the MSP430. The MSP430 in the design must have power independently from the eFuses and the other voltage rails because it does control and diagnostic. For example, the MSP430 sets the I_{LIM} of the eFuses and enables them. It has a very low power consumption and can therefore be powered through an LDO which significantly simplifies the design. The LP2951 is a bipolar, low-dropout voltage regulator that can accommodate a wide input supply-voltage range of up to 30 V. To enable higher input voltage and to split the power losses across multiple devices, a Zener diode is placed in series with the input. A 27-V Zener diode increases the voltage tolerance to 57 V and still supports a minimum input voltage of 32 V for a 3.3-V output. The LP2950 is also available with other fixed-output voltages like 5 V and 3 V, as well as in a variable voltage version. More details are available in the *LP295x Adjustable Micropower Voltage Regulators with Shutdown Data Sheet*.

2.3.11 TPD2E2U06

The design is intended for use in an industrial environment and therefore requires protection from ESD, EFT, and surge events. The protection of the T1 PHY consists of multiple stages. A common-mode filter together with a network from resistors and capacitors removes the large transients. The reminder of overvoltage is blocked using the TPD2E2U06. This device is a dual-channel, low-capacitance TVS diode ESD protector. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The low 1.5-pF line capacitance of the TPD2E2U06 ensures that the T1 communication is not affected from the protection. Other supported application interfaces are USB 2.0, LVDS, and I2C. Applications and technical details are available in the *TPD2E2U06 Dual-Channel High-Speed ESD Protection Device Data Sheet*.

2.4 System Design Theory

This design splits into a power part and a communication part. The following sections describe the individual design challenges for daisy chaining communication and power.

2.4.1 Daisy Chaining Communication

The straight-forward structure of the daisy chain makes it attractive for a communication structure. Independent of the number of nodes, the communication is always injected at only one port. This property makes the system scalable. If more nodes are needed, then they can be added at any place in the chain. A classical, switched-Ethernet system needs a communication port per node at a central location. Every port connects then with a point-to-point cable to its corresponding node. If all ports of the switch are used, then another switch is needed for more nodes.

Figure 3 shows the daisy-chain topology compared to the switched-Ethernet topology in Figure 4.

Figure 3. Daisy-Chained Ethernet

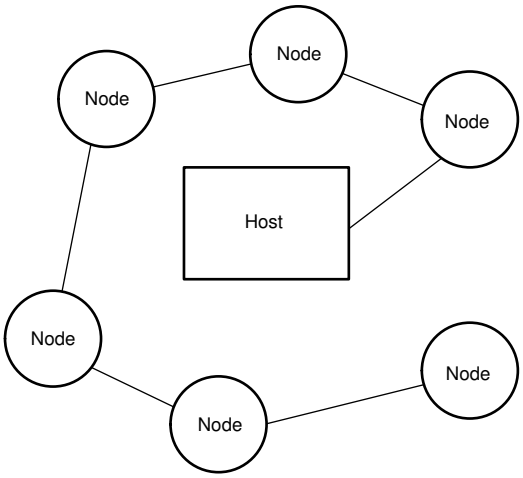
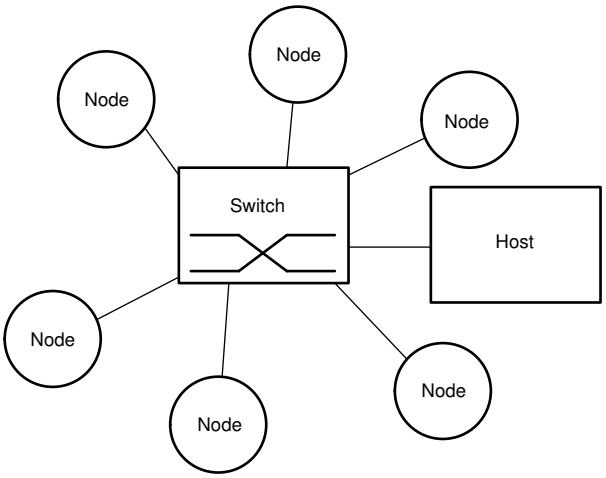


Figure 4. Switched Ethernet

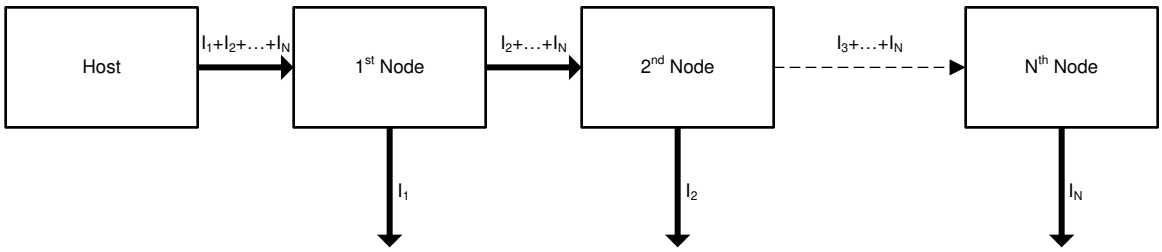


In a switched Ethernet, each node has the same latency between node and host. This makes the latency calculation easy. In a real-time implementation of such a system, the host only must ensure that all of the nodes receive their packets within the cycle time. In the daisy-chain topology, each node adds latency. Therefore, the last node in the chain has the longest latency between node and host. In a real-time Ethernet, the protocol must take care of this extra latency. The protocol can, for example, send the packet for the last node as the first packet within the cycle. The system design then only needs to ensure that the longest latency fits into the cycle time. A short latency adder per node is key for such a system to support many nodes. When the MAC is implemented with a device member of the Texas Instruments Sitara™ MPU family, the adder is only 320 ns. This is a 5% adder per node to the minimum time of 6.7 us for a 64-byte packet including a 12-byte, inter-packet gap and 8-byte synchronisation.

2.4.2 Daisy Chaining Power

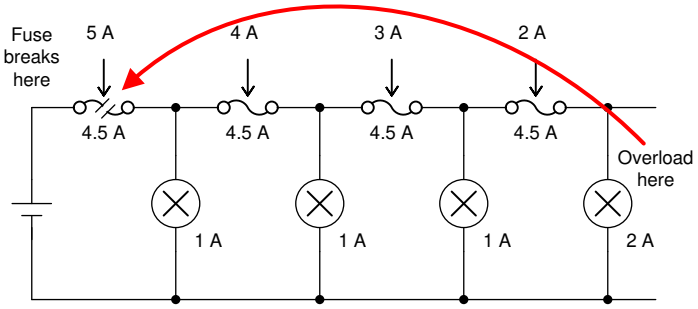
Stability in a daisy-chain power system comes from precise current limiting in the individual nodes of the system. Each node's input current is the sum of its own current and all following nodes. The first node has therefore the highest current throughput.

Figure 5. Power Daisy Chain



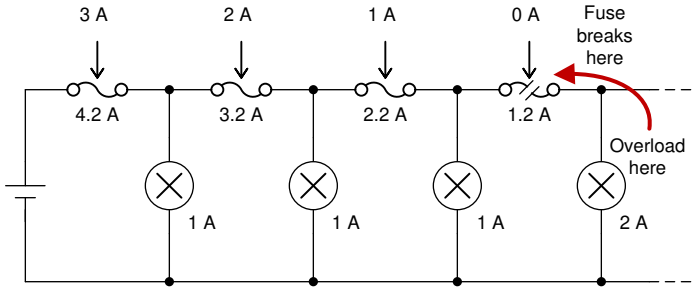
Any of the nodes can have an overcurrent situation if the connected load has an error. In case of an error, and independent of the current distribution, the expectation is that only the fuse breaks, protecting the overloaded power port. However, if every node has the same fuse rating, the fuse with the highest current tends to break first. In a daisy-chain power system, this is the main fuse in the first node. As a consequence, the whole system shuts down at any place, and failure isolation is impossible. Figure 6 shows the problem in a simplified way using fuses and lamps as loads.

Figure 6. Incorrect Current Limiting



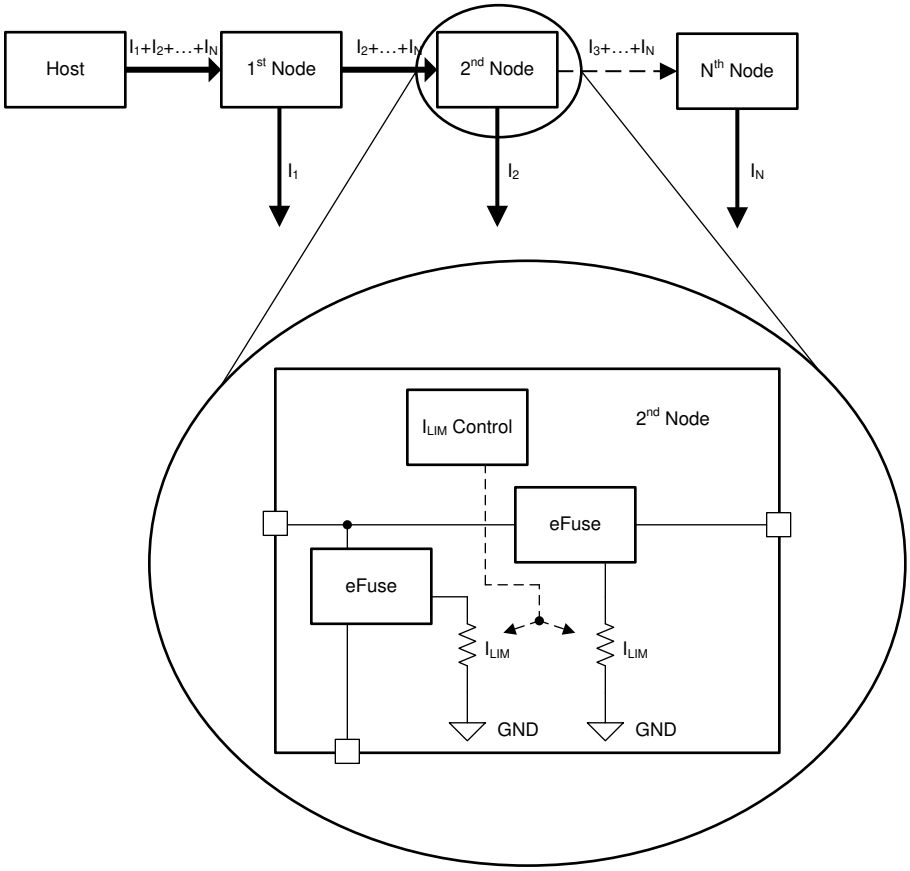
In a stable system, unaffected nodes maintain their function without interruption. Therefore, it is necessary to adjust the current limit of the fuses according to the load distribution. Figure 7 shows in the same example how the correct current limit setting would look.

Figure 7. Correct Current Limiting



Electronic fuses (eFuses) are the ideal devices to fulfill this requirement so that all nodes can be built identical and configured ad hoc. Figure 8 shows such a configuration as it is implemented in this design. Each node can then be protected with a current level according to the sum of its own maximum current and all currents of the next nodes.

Figure 8. Current Limit Setting



By adding an additional programmable eFuse for each node's power extraction port, it is possible to isolate a fault to a single location. This keeps the system up and running also in case of an overload condition at any place.

All eFuses are implemented using the TPS2663 family of devices. They allow connection of an ILIM resistor to set the current level at which the fuse trips. The programmability is implemented by replacing this ILIM resistor with a set of switchable resistors as shown in Figure 9 for the 3.2-A application eFuse and in Figure 10 for the 4.8-A next node eFuse.

Figure 9. Resistor Setting for 3.2 A (Maximum)

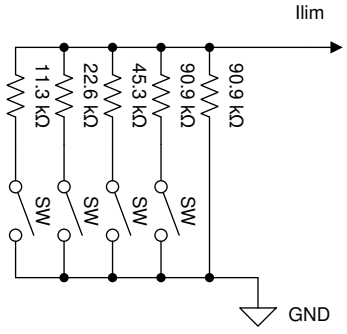
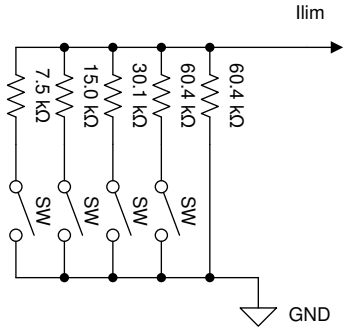


Figure 10. Resistor Setting for 4.8 A (Maximum)



With this methodology, four switches can select 16 current levels. Both eFuses support different levels. The eFuse for the next node has steps of 300 mA and a maximum current of 4.8 A. The eFuse for the load connected to the node has steps of 200 mA and a maximum current of 3.2 A. Table 2 shows the relationship between the current levels and the switch settings for the application power eFuse. Table 3 shows the same information for the next node eFuse.

Table 2. Current Settings for the Application eFuse

SWITCH CODE	RESISTOR VALUE (kΩ)	CURRENT (A)	SWITCH CODE	RESISTOR VALUE (kΩ)	CURRENT (A)
0	90.90	0.2	8	10.05	1.8
1	45.45	0.4	9	9.05	2.0
2	30.23	0.6	10	8.23	2.2
3	22.69	0.8	11	7.54	2.4
4	18.10	1.0	12	6.96	2.6
5	15.01	1.2	13	6.46	2.8
6	12.93	1.4	14	6.03	3.0
7	11.32	1.6	15	5.66	3.2

Table 3. Current Setting for the Next Node eFuse

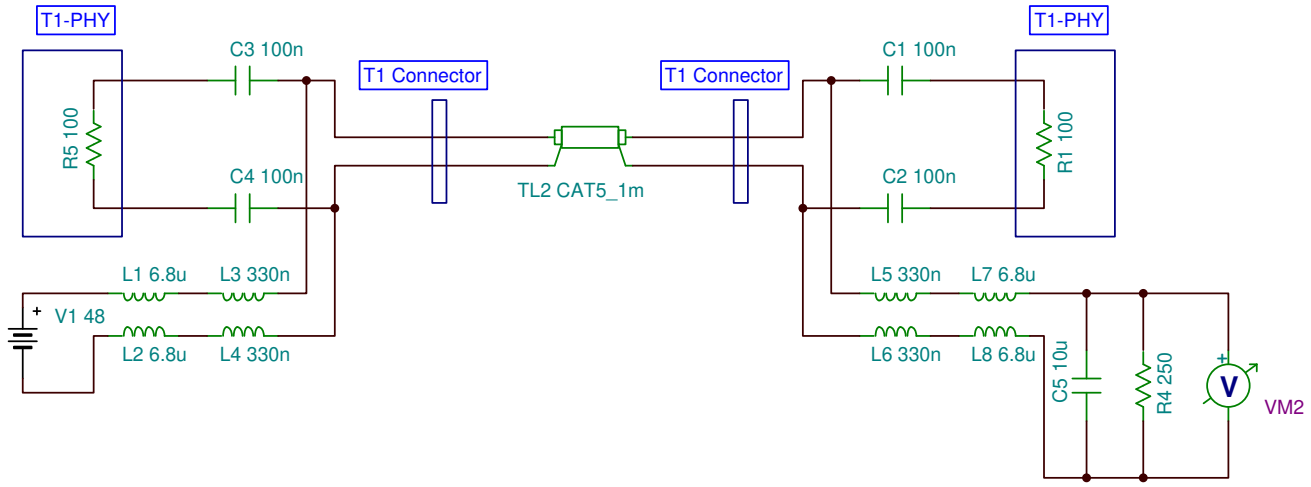
SWITCH CODE	RESISTOR VALUE (kΩ)	CURRENT (A)	SWITCH CODE	RESISTOR VALUE (kΩ)	CURRENT (A)
0	60.5	0.3	8	6.67	2.7
1	30.23	0.6	9	6.01	3.0
2	20.10	0.9	10	5.46	3.3
3	15.08	1.2	11	5.01	3.6
4	12.02	1.5	12	4.62	3.9
5	10.02	1.8	13	4.29	4.2
6	8.59	2.1	14	4.00	4.5
7	7.52	2.4	15	3.76	4.8

In this design, mechanical switches are used for manual setting of the current limits during testing. Electronic switches are connected in parallel to the mechanical switches for the automatic power setting in the final application. The mechanical switches must be set to zero (0) if automatic power setting is used.

2.4.3 Merging Power and Data

Power and data can travel over the same twisted pair because they reside in different frequency domains. Power is a DC signal and can be separated from data through a low-pass filter. Data is an AC signal and can be separated from the power through DC blocking capacitors. The value of such DC blocking capacitor for 100BASE-T1 and 1000BASE-T1 is not specified in the IEEE 802.3 Ethernet specification. A value of 0.1 uF is mandated in the *IEEE 100BASE-T1 System Implementation Specification V1.0* issued by the OPEN Alliance (One-Pair Ether-Net) Special Interest Group (SIG) consortium. Together with the input termination of 100 Ohm, these capacitors form a high-pass filter with a -3-dB point at 32 kHz. The 6.8-uH inductor for the DC path forms a high-pass filter with the termination resistor as well. It's -3-dB point is at 1.2 MHz, so it is the limiting component for the lower part of the operating frequency band of the PHY. The DP83TC811 prioritizes frequencies in the range of 3 MHz up to 40 MHz, so a cut-off frequency of 1.2 MHz is far enough off to not distort the operating frequency band. Figure 11 shows the principle of how data and power are merged.

Figure 11. Principle of Merging Power and Data



In this design, the 6.8-uH inductors are implemented as a single-coupled inductor to save board space and improve routing. In series with the 6.8-uH inductor is a second inductor of 330 nH to cancel capacitive coupling effects of the 6.8-uH inductors. They are also needed to isolate the effects of long and wide high-current traces close to the T1 connector. With their small size, they can connect with short stubs to the T1 traces. This reduces the effects of the high-current traces on the trace impedance of the T1 traces.

All power inductors in the DC path must have a saturation current greater than the maximum expected DC current. Otherwise, the communication gets distorted when there is a high loading condition because the inductance is reduced in saturation. The core saturation of the coupled inductor must be twice the DC current because it sees the forward and the backward current in the same magnetic core. The 330-nH inductor has a saturation current of 8.3 A and the 6.8-uH coupled inductor has a saturation current of 12 A.

2.4.4 T1 Physical Interface

The 100-Mbit/s T1 interface is implemented using the DP83TC811. It is qualified by OPEN Alliance and therefore meets the automotive requirements. These requirements specify a minimum reach of 40 m. This minimum distance is already sufficient for the scope of this design. For applications with a longer reach requirement, the DP83TC811 has been tested up to 100 m. All necessary functions are integrated into the PHY and only decoupling capacitors are required. Additional passive components are mainly dictated by the previously mentioned implementation specification. The selection of these passive components is elaborated in more detail in the *DP83TC811R-Q1 Low Power Automotive PHY 100BASE-T1 Automotive Ethernet Physical Layer Transceiver Data Sheet* and the corresponding application notes available on the DP83TC811R-Q1 product folder.

In this reference design, the PHY is connected to the host CPU through a 4-bit wide MII interface at a clock rate of 25 MHz. For the daisy-chaining, two MII channels are needed — one for each PHY, the downstream PHY, and the upstream PHY. The Texas Instruments K2G evaluation module has all of these signals within one connector and is therefore suited as a host for this design. With respect to its communication functions, the K2G MPU is compatible with the Sitara™ family of MPU devices. Any Sitara MPU device with two MII interfaces and a PRU inside can use this design for T1 Ethernet real-time communication.

The MII interface signals are length matched between the PHY and connector. This ensures that the MII timing margins are maximized.

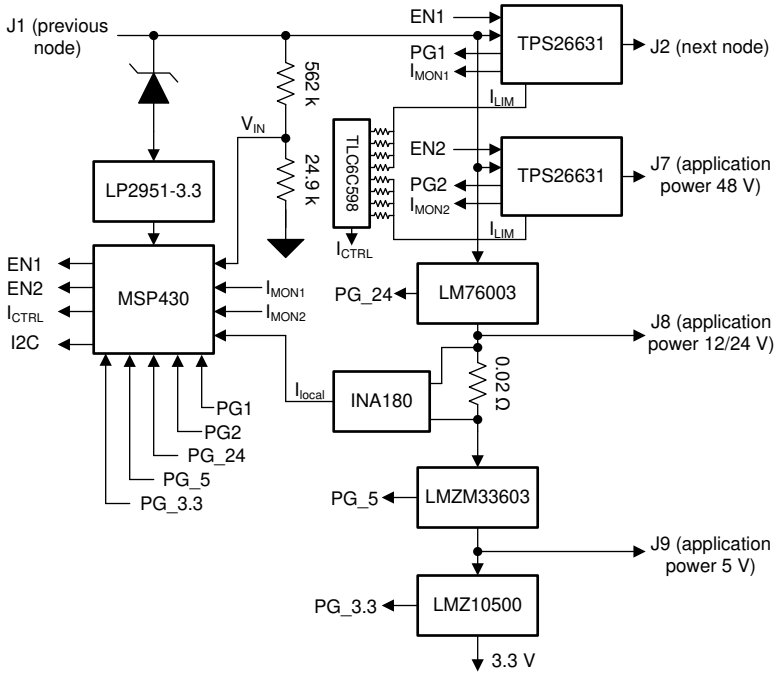
2.4.5 Power Supply

The power supply produces all supply rails and voltages for internal and external use. The highest power level for a local consumer is available on the 48-V local port. This port is connected to the Ethernet line voltage through an eFuse only. No further voltage conversion is included. Therefore, this voltage can vary from 35 V up to 48 V depending on the load of the daisy chain and the location of this node in the chain. The first stage of regulated voltage provides selectable regulated 12 V or 24 V, 1 A continuous with 3-A peak. This voltage is available on external connector J8 and also used internally. The LM76003 is an ideal buck regulator for this conversion because it does not need loop compensation and can handle up to 60 V at the input. The switching between 12 V and 24 V therefore needs only the change of one single resistor value. A low external part count helps with a compact design.

The second stage converts the regulated 12 V or 24 V to 5 V. The LMZM33603 converter module with a Vin maximum of 36 V can be used for this task because the input voltage is already limited to a maximum of 24 V by the first stage. With its internal inductor, only two external capacitors and two resistors are needed for a complete design. This sequential topology has a higher efficiency than connecting suitable 24-V and 5-V converters both directly to the 48-V rail. It also simplifies the power measurement because the high-side shunt current sensor can now be positioned at the output of the first stage. This way, the INA180 can be used as it has a common-mode voltage limit of 26 V. The 5 V is brought out on connector J9 and also used internally by the 3.3-V converter for the two DP83TC811 devices. This 5-V to 3.3-V conversion is performed by the LMZ10500 point-of-load MicroSiP module. It can deliver up to 650 mA. The two PHYs require a maximum of 300 mA together, and the LMZ10500 has a conversion efficiency of 95% in this range compared to an LDO which would be only at 66% efficiency.

The complete power tree block diagram is shown in Figure 12.

Figure 12. Power Tree for Internal and External Supply



2.4.6 Power Distribution Control

Control over the power distribution is mandatory for stable operation. The control function consist of following elements:

- Voltage and current measurement
- Power calculation
- Current limiting
- Communication

The communication is implemented in two stages. The first stage is an I2C link between the T1 card and the K2G board, and the second stage is the communication through the Ethernet connection. On the T1 board, I2C is terminated in an MSP430G2332 which also performs the sensing and settings on the T1 card. The MSP is responsible for measuring all relevant current and voltages and for setting the eFuses to the required limits. It can also shut down both of the eFuses individually. It also consolidates all power-good signals from the eFuses, the 12-V/24-V supply, the 5-V supply, and the 3.3-V supply of the PHYs. To bootstrap the board, the MSP430 has its own power supply made from a high-voltage LDO LP2951 with a Zener diode on its VIN side. Therefore, the MSP430 always has power when the board input power is present. Key for this operation is the ultra low power consumption of the MSP430. It enables the use of a simple LDO for creating the MSP430's supply power. The Zener limts the voltage to the LP2951 and splits the heat generation from the drop voltage into two halves. The MSP430 can measure the 48-V input voltage level, the imon signals from the eFuses, and the sensed current from the INA180. Based on this information, it can calculate the actual power levels of the local power and the next node power. Through I2C, this data is available to the MPU on the K2G board which can then further communicate it to the host of the system. There it can be used for visualization purposes and to calculate the optimum settings for all of the eFuses of the whole daisy-chain. These settings can then be communicated back to the individual nodes where the MSP430 receives them again through I2C. It uses these settings for the eFuses. The actual setting of the eFuses is done by a TLC6C598 high-power, serial-to-parallel shift register. Its low-leakage, high-voltage, open-drain outputs serve as switches to the resistor networks on the ILIM eFuse inputs.

As a side task, the MSP430 flash can be used to keep usage parameters and settings.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

For full operation, the design can be plugged into a K2G ICE board. It is then possible to re-route the traffic from the K2G Ethernet ports to this design.

For testing power only, the board can also operate as a stand-alone system. For programming the onboard MSP430, connection, except to an MSP-FET, is unnecessary.

3.1.1 Hardware

The following equipment is needed for testing:

- One board of this design
- One K2G ICE board
- 5m, shielded SPE cable from HARTING® with T1 connectors as per IEC 63171-6
- Power supply with 48 V and 5 A
- Voltmeter
- Amperemeter
- Electronic load

Testing consists of two parts: power test and bit error rate test. The power test is performed in a stand-alone configuration. For the communication test, the board is connected to the K2G ICE board.

3.1.2 Software

Software is not required for the power test.

For testing the bit error rate, a special software has been designed that transmits pseudo-random, bit-pattern packets with one 32-bit word of CRC appended (68 byte in total). The software executes on the two PRUs of one ICE channel. It is manually loaded into the PRUs from Code Composer Studio™. The design board is used in a loopback configuration so that all software modules can execute on one ICE board. Both software modules of the test, the Tx and the Rx module, start with the same pseudo-random seed value. The Rx software module must start first. It then waits for packets to arrive. Next, the Tx module starts. It will send packets with pseudo-random data based on a known seed value. The Rx module receives this packet and compares it bitwise with locally generated, pseudo-random data based on the same seed value. If one or more bits deviate from the expected values, this condition is flagged as an error and recorded in the PRU register set. As part of the recording, the number of error-free packets before that error can be found in a PRU register. An error counter register is incremented. The packet with the error and the corresponding expected packet are available for inspection. They are overwritten by the software when the next packet arrives. For error root cause analysis, a break point must be set in the error handler. Block diagrams of the BER test modules are shown in Figure 13 and Figure 14.

Figure 13. Rx Flowchart

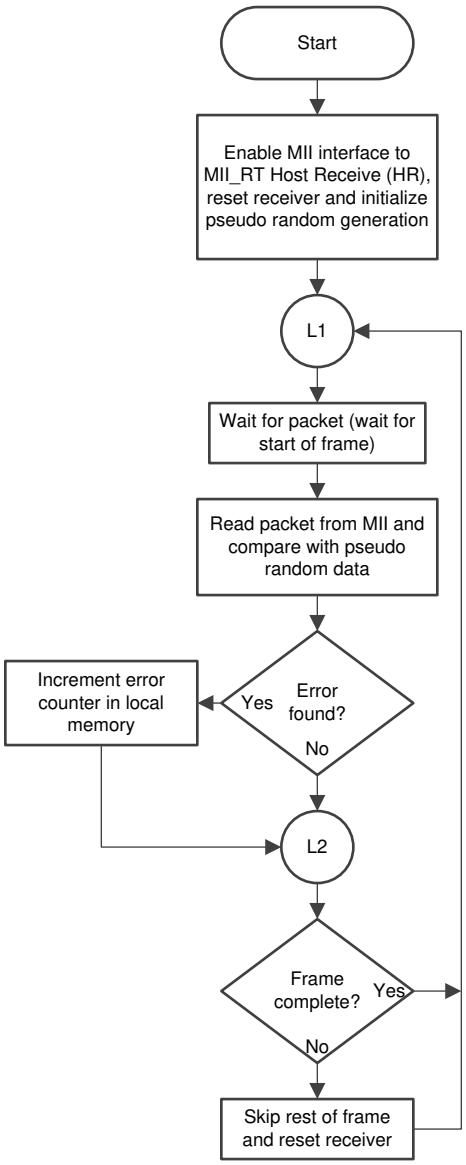
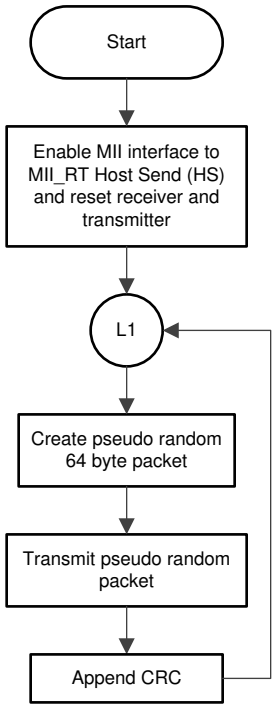


Figure 14. Tx Flowchart



The random packet transmits in a frame consisting of an 8-byte header, 64-byte random data, and 4-byte CRC checksum. The CRC is ignored on the receiver side because the more stringent test form of comparing data bit-by-bit with a reference data set is used.

3.2 Testing and Results

Before testing can start, all jumper positions on the board must be checked for correctness. Figure 15 shows the position of these jumpers.

Figure 15. Jumpers, Connectors, and Test Points

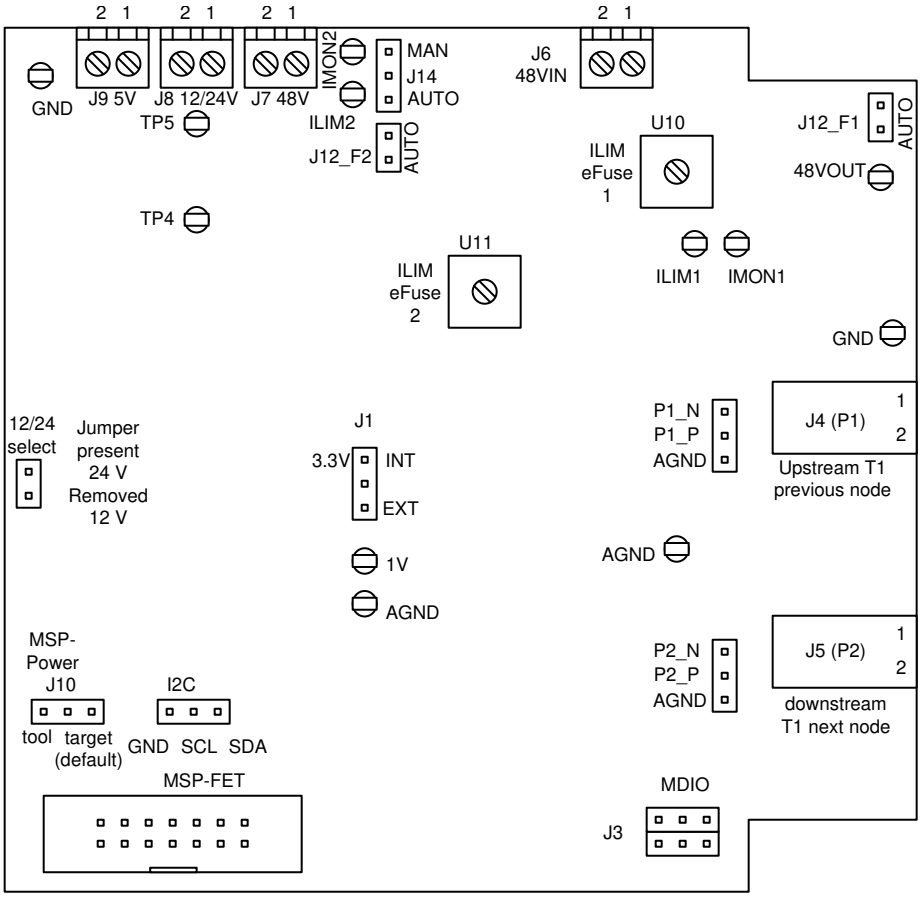


Table 4 shows the correct jumper position to begin the testing.

Table 4. Jumper Positioning

JUMPER/SWITCH	POSITION
J1	INT
J10	target
J12_F1 and J12_F2	AUTO
J14	AUTO
12/24 select	present
U10	0
U11	0

3.2.1 Test Setup for Power Test

The first test checks the host function where the input power is delivered into connector J6:

- Overvoltage and undervoltage lockout
- Reverse polarity protection
- Application power accuracy
- Current limit

The second test checks the node function where the input power is delivered into port P1:

- Voltage drop
- Mis-wiring (power delivered into wrong T1 connector port P2)

3.2.2 Test Results for Power Test

Functional testing shows that once power is applied to connector J6, the board powers up as soon as the voltage is in the range of 35 V to 48 V. Figure 16 shows the LEDs lighting on a board that is working correctly. Figure 17 shows the overvoltage and undervoltage lockout condition. Figure 18 shows the board with wrong input voltage polarity. In all cases, the board shows the correct function.

Figure 16. Normal Operation

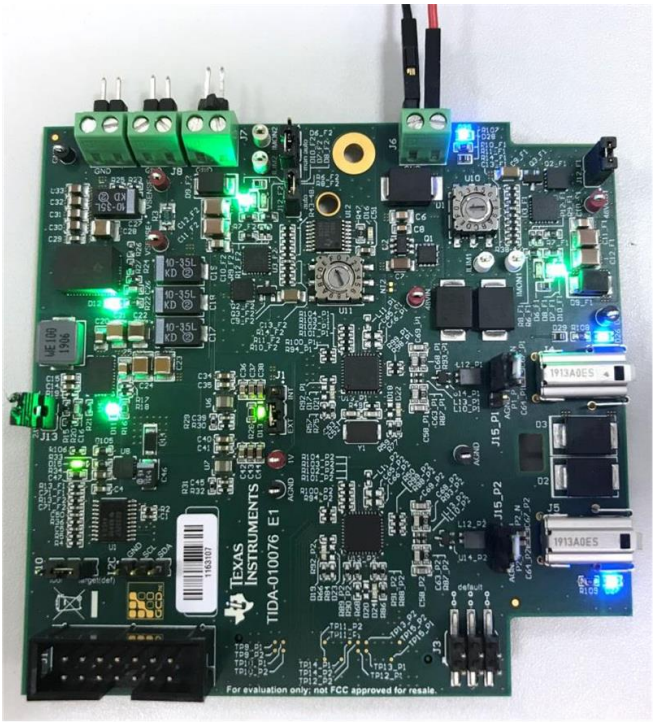


Figure 17. Overvoltage or Undervoltage

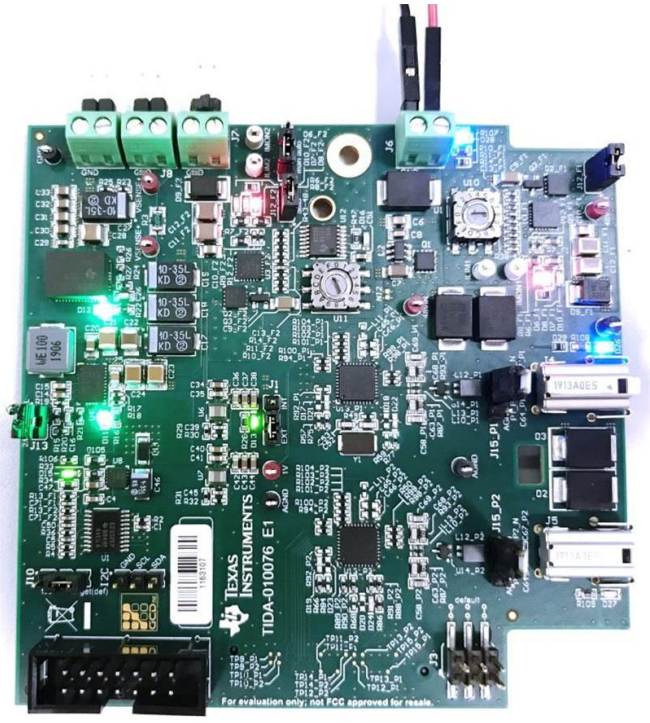


Figure 18. Wrong Input Polarity

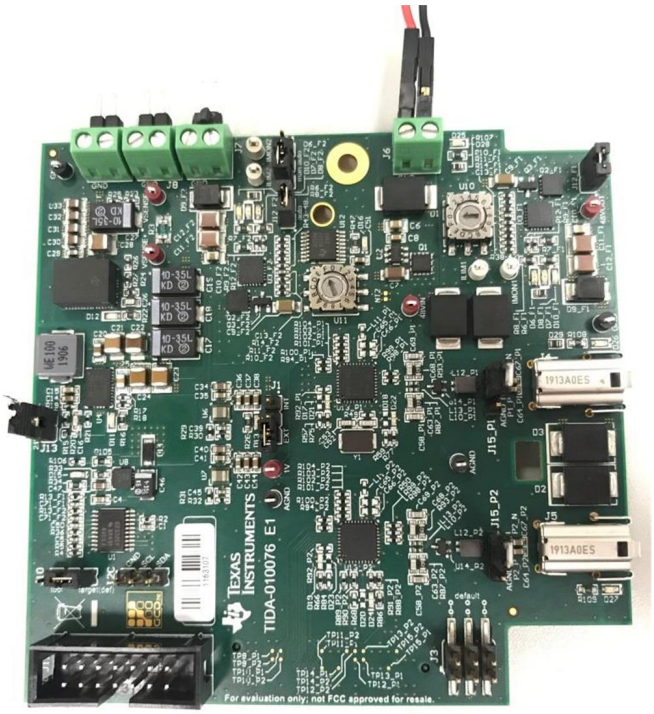


Figure 19. Jumpers, Connectors, and Test Points

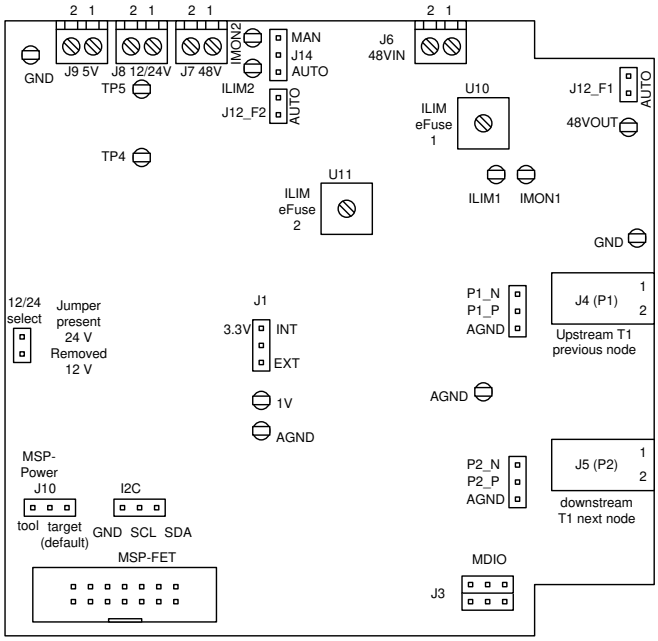


Figure 20 and Figure 21 show the board powered through the T1 connections. Figure 20 shows the board with power on the correct T1 port, P1. The blue port power LEDs and all green LEDs indicate correct function light up. Figure 21 shows the board powered through the wrong port, P2. Both the blue port power LEDs and the red port power LEDs light up, indicating powering from the wrong port.

Figure 20. Power Through Correct Port

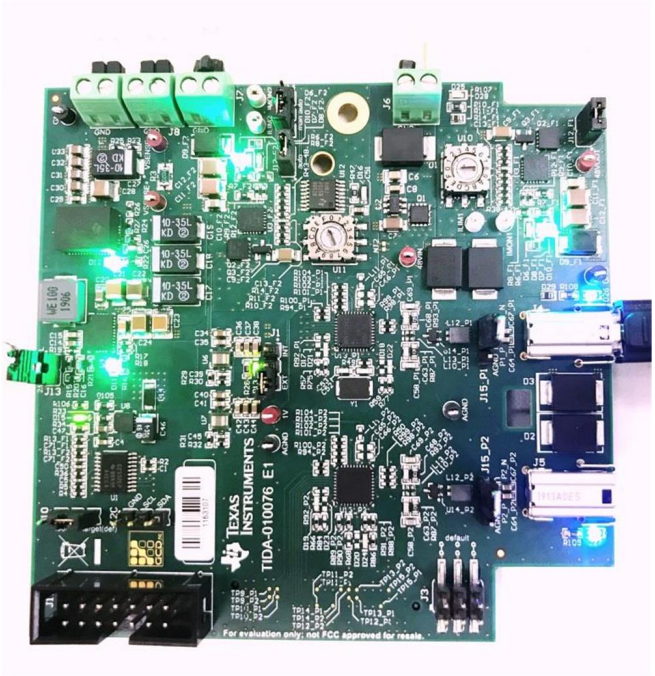


Figure 21. Power Through Wrong Port

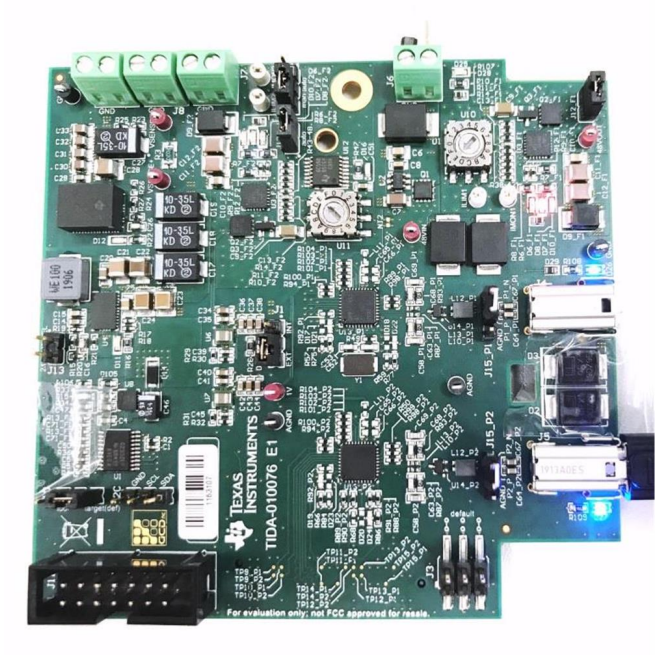


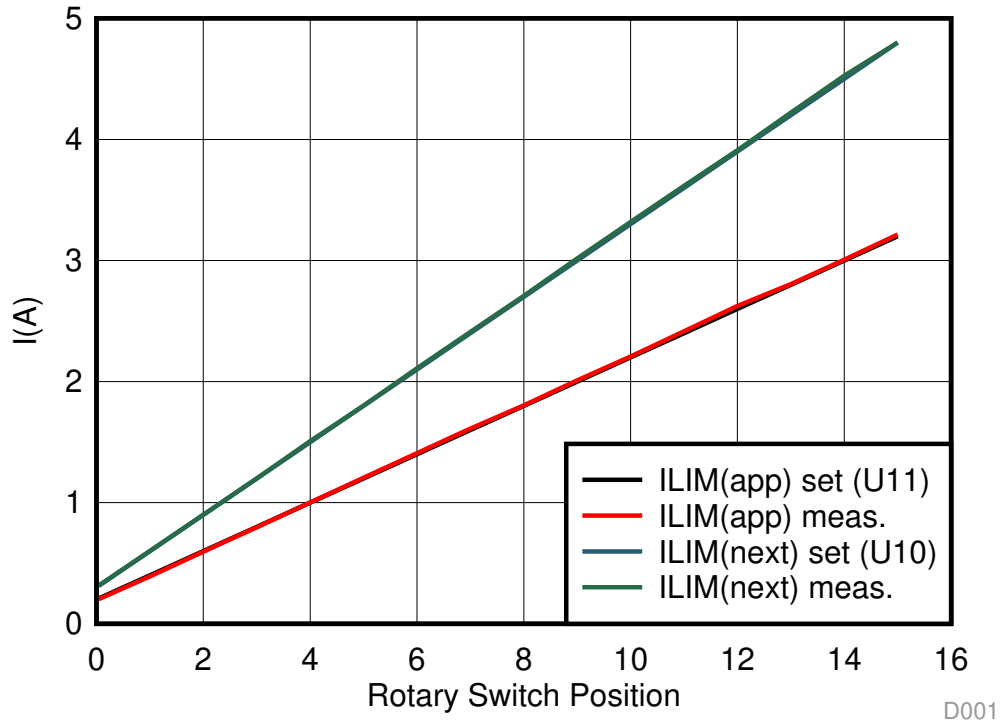
Table 5 shows the relationship between switch setting and calculated ILIM for both of the eFuses. Figure 22 compares the calculated values with the actual measurement data in a graphical form. The graph shows that the measured data follows closely the theoretical values.

Table 5. Relationship of Rotary Switch Position to eFuse Trigger Current

SWITCH POSITION	ILIM (APP) (A)	ILIM (NEXT) (A)	SWITCH POSITION	ILIM (APP) (A)	ILIM (NEXT) (A)
0	0.2	0.3	8	1.8	2.7
1	0.4	0.6	9	2.0	3.0
2	0.6	0.9	A	2.2	3.3
3	0.8	1.2	B	2.4	3.6
4	1.0	1.5	C	2.6	3.9
5	1.2	1.8	D	2.8	4.2
6	1.4	2.1	E	3.0	4.5
7	1.6	2.4	F	3.2	4.8

Figure 22 shows the accuracy of the measured current versus the set current.

Figure 22. Relationship Between Rotary Switch Setting and Measured Current



The results of the EXCEL functions for slope, intercept, and correlation on the previous data set are listed in Table 6.

Table 6. Results of the EXCEL Functions

SLOPE ILIM (APP)	INTERCEPT ILIM (APP)	CORRELATION ILIM (APP)	SLOPE ILIM (APP)	INTERCEPT ILIM (APP)	CORRELATION ILIM (APP)
0.201	0.195	99.998%	0.301	0.301	99.999%

These results can be interpreted such that there is a gain error of 0.5% for the application current limit and a gain error of 0.3% for the next node current limit. The correlation of 99.998% and 99.999% means that the deviation from linearity is less than the resolution of the measurement equipment.

3.2.3 Test Setup for Bit Error Rate Test

For the bit error rate test, the board is connected to a K2G ICE board. Power is injected through connector J6. The data transmission is done in a loopback configuration with 5 m of T1 SPE cable between both ports. The test limits are such that a single error causes a stop of the measurement to read out the PRU register values. These show the number of good packets before the single bit error occurs. Because of the high transmission speed and the limited register size, the amount of data is limited to 2^{41} Bits respective 2 Tbit. This amount of data is sent within 6 hours and 6 minutes.

3.2.4 Test Results for Bit Error Rate Test (BER)

Within five of these six-hour runs, an error occurred twice. Of these two errors, the first one occurred after three hours, corresponding with 2×10^9 packets or 2^{40} Bits. The second one came after five hours, corresponding with 3.6×10^9 packets or 1.8 Tbit. The test finished without errors three times. This indicates with a very high probability that the error rate is better than the IEEE802.3 postulated BER of 10^{-9}. With a probability of 95%, it is better than 10^{-11}.

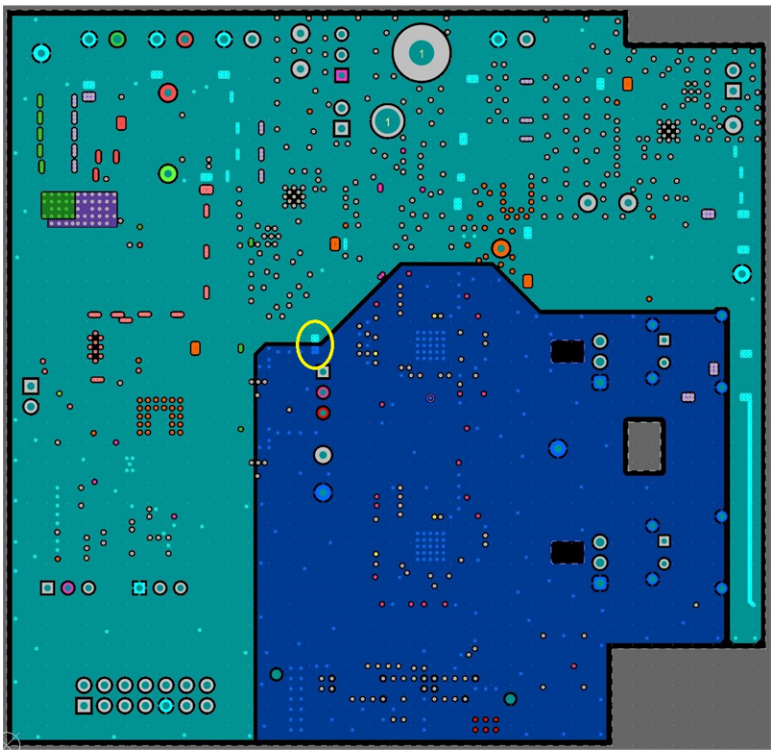
4 Design Files

Design files consist of schematics, bill of materials, Gerber files, and the complete Altium project as a basis for all reference designs. Layout prints and assembly drawings are also available as PDF documents. All related files can be found on the TIDA-010076 product folder.

4.1 PCB Layout Recommendations

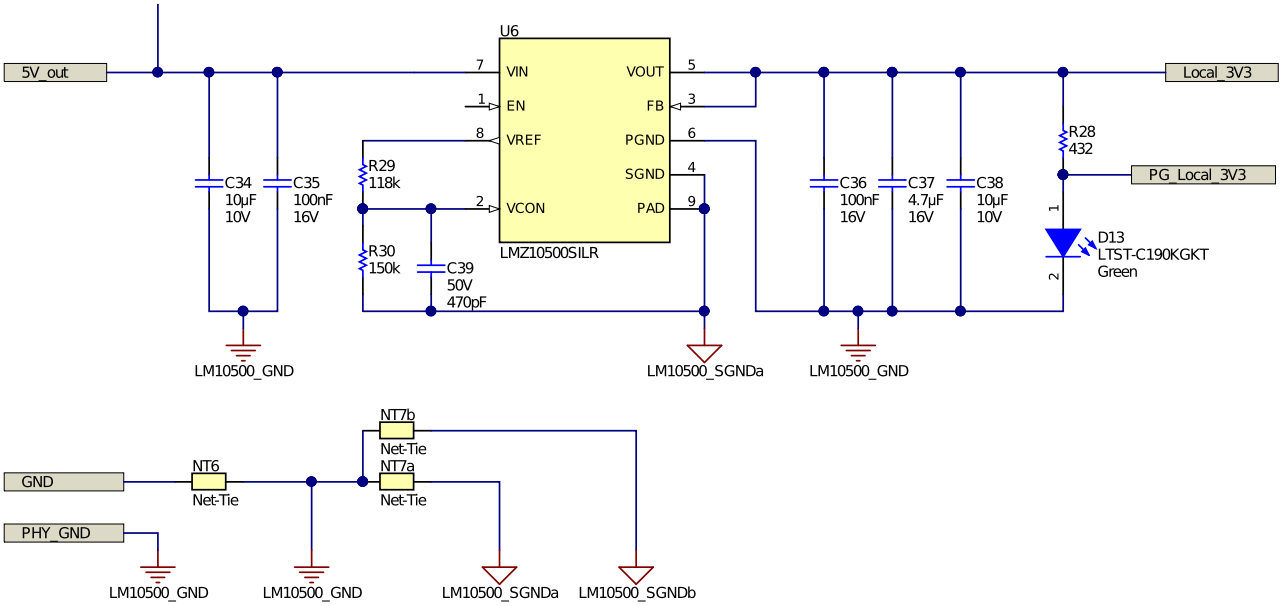
The design has multiple DC/DC switch mode power supplies which could act as noise sources. Another potential source of error are the high currents that the design is supporting because they may lead to significant drop voltages across the traces. To eliminate adverse influence on the accuracy of the design, all ground connections are separated from each other using net-ties. This enables the design of a controlled ground path with no current loops. Large heat sink areas are also possible with a controlled current flow, as well as wide traces for the high currents. Figure 23 shows the yellow oval as the place where a net-tie connects analog and digital ground. This connection is necessary for the power supply of the PHYs if their power jumper J1 is set to internal supply.

Figure 23. Ground Plane on Layer 5



These ties are used on every building block so that the local components have their own ground which is then connected to the global ground where applicable. Noise from current loops in the switch mode power supplies is then kept local and doesn't travel across the board. Figure 24 shows how this is handled in the schematics.

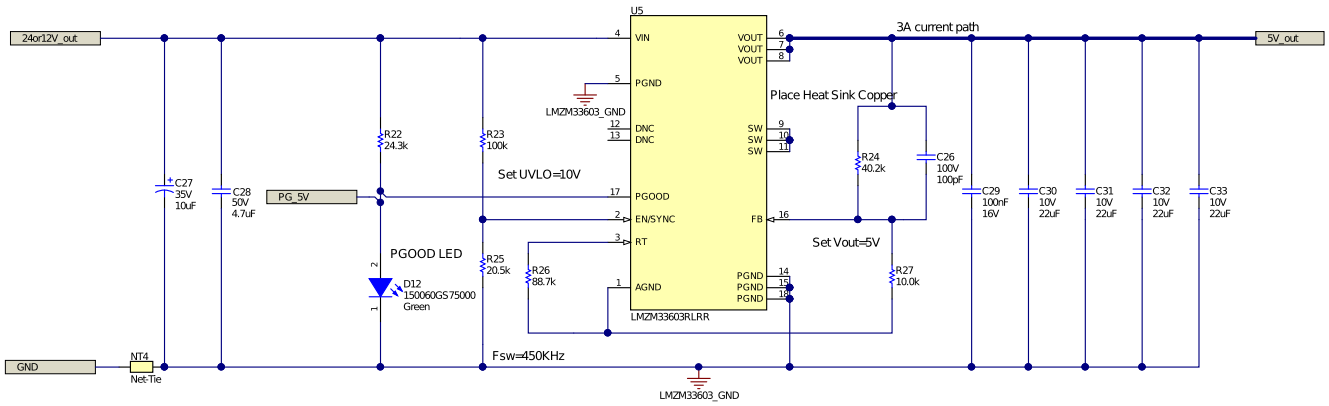
Figure 24. PHY Power Supply



Net-tie NT6 connects the PHY analog ground AGND with the digital ground GND and the local LMZ10500 PHY power supply ground. This eases layout design because the position of the net-tie, and therefore the connection between AGND and GND, can be determined exactly. There is no need to cut the ground polygon to create the analog ground island.

Figure 25 shows the same method for the 5-V power supply.

Figure 25. 5-V Power Supply



Net-tie NT4 separates the local ground of the buck converter from the system. This keeps all of the ground connections of this building block together and the current loops small. At the net-tie is a noise-free place so it can connect to the rest of the system without noise transfer.

4.2 Altium Project

The Altium files are part of the design files and give an instant start. Details of the design could be imported into own designs in a cut-and-paste form. The Altium project is hierarchically organized and includes the block diagram, schematics, and the final layout in an editable format.

5 Related Documentation

1. Texas Instruments, *DP83TC811 Systems and Reference Schematics User's Guide*
2. Texas Instruments, *DP83TC811EVM User's Guide*
3. Texas Instruments, *DP83TC811 Diagnostic Toolkit Application Report*
4. OPEN Alliance SIG, *OPEN ALLIANCE IEEE 100BASE-T1 System Implementation Specification*
5. Texas Instruments, *100BASE-T1 Ethernet: the evolution of automotive networking white paper*

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6 About the Authors

INGOLF FRANK is a systems engineer in the Texas Instruments System Engineering and Marketing team for Factory Automation and Control, focusing on motor control and encoder technology. Ingolf works across multiple product families and technologies to leverage the best solutions possible for system level application design. Ingolf earned his electrical engineering degree (Dipl. Ing. (FH)) in the field of information technology at the University of Applied Sciences Bielefeld, Germany in 1991.

ANDY LIN is a Field Application Engineer for Texas Instruments in Taiwan, where he is responsible for the technical support of a major communication company. Andy created this reference design during his rotation period in the System Engineering and Marketing team for Factory Automation and Control. He earned his electrical engineering MS degree at the National Taiwan University of Science and Technology in Taipei, Taiwan in 2018.

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