PMP20807 Rev A

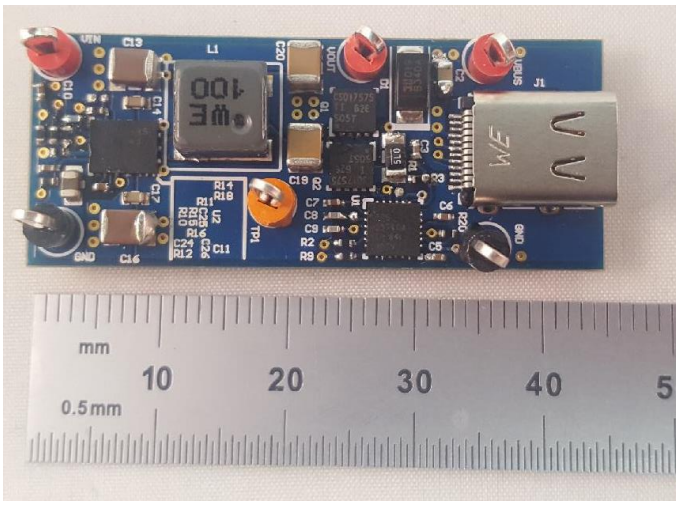
5V/3A, 9V/3A USB Type C PD with Port Power Management

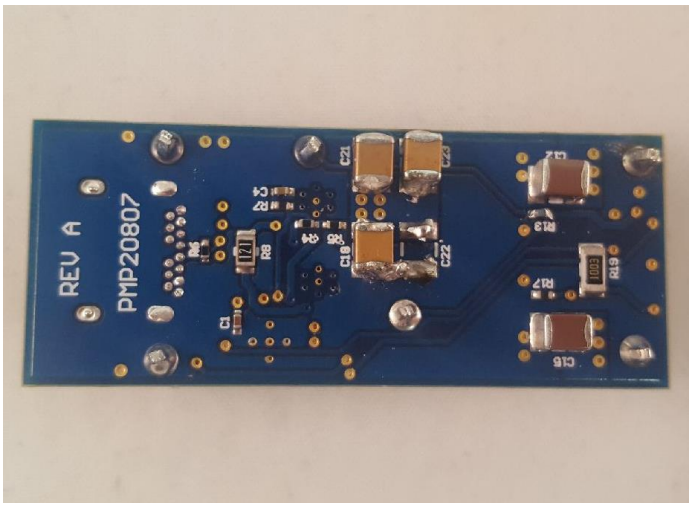
Test Results

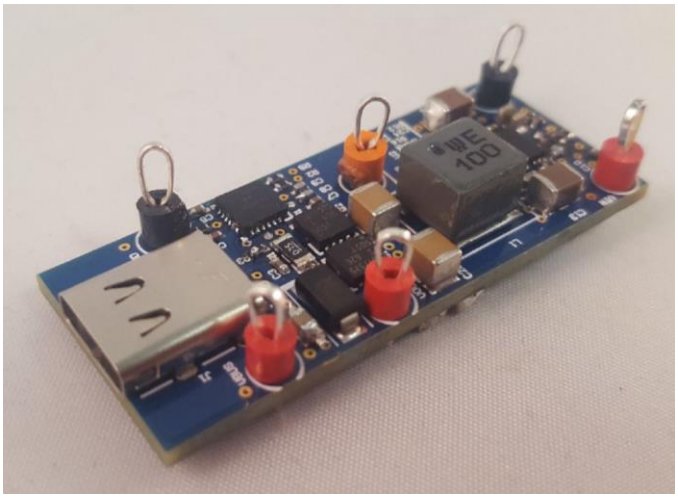
Contents

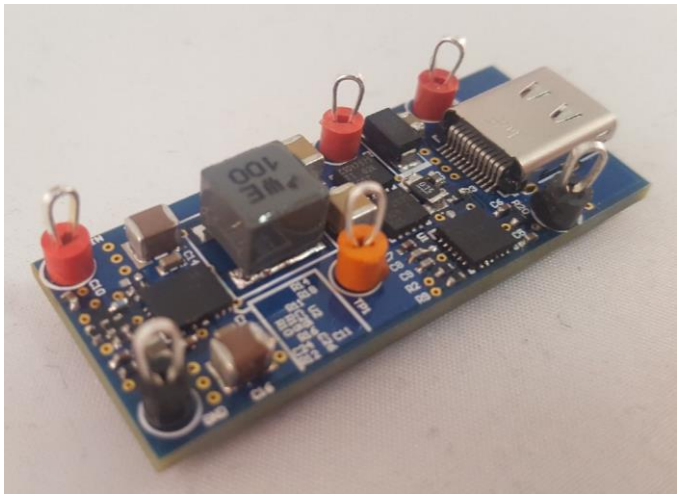
1 Photos

The photographs below show the PMP20807 Rev A prototype assembly.







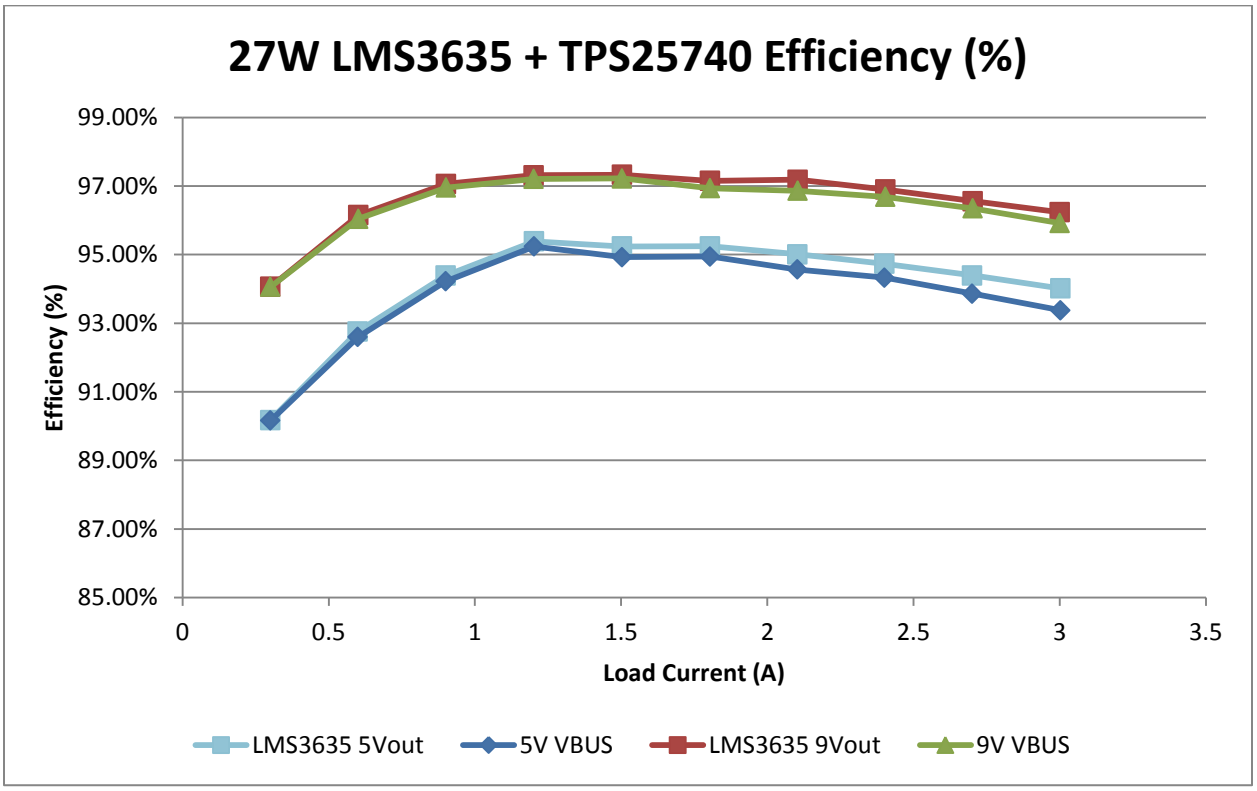


2 Standby Power (Cable Unplugged)

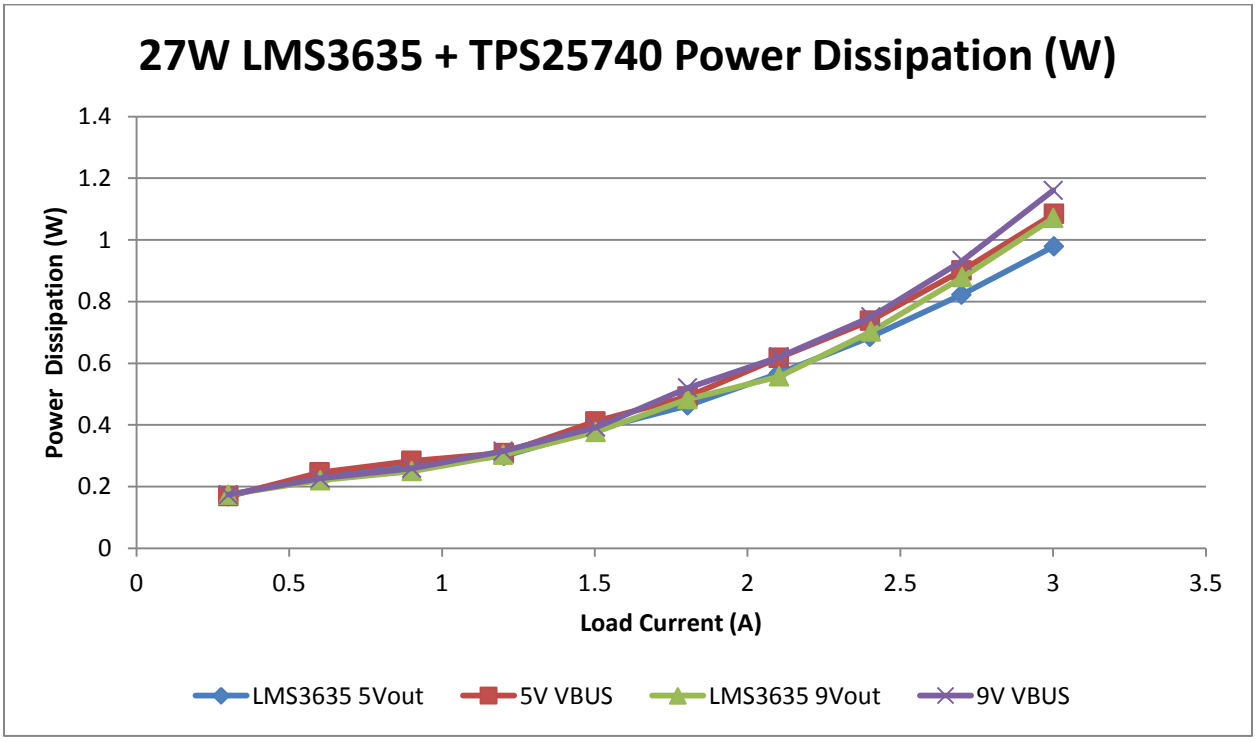
Input Voltage	Input Power
12 V	0.908 mW

3 Efficiency

3.1 Efficiency Chart



3.2 Power Loss Chart



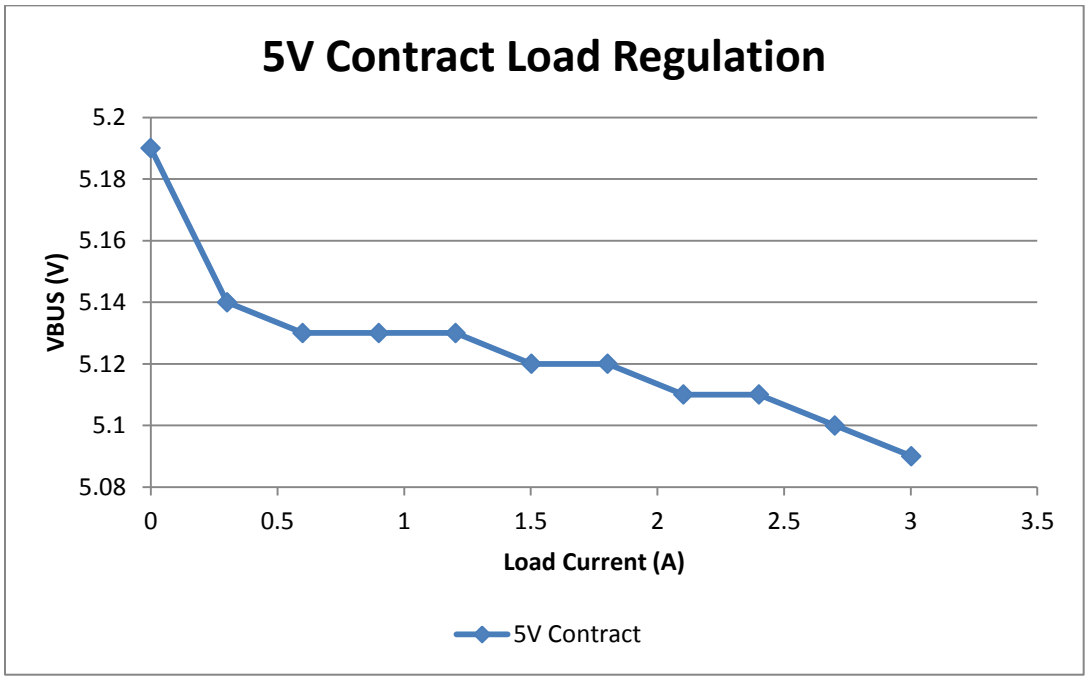
3.3 Raw Data

Vin	Iin	Vout (Converter)	Vout (VBUS)	Iout	Pin	Pout (Converter)	Pout (VBUS)	Efficiency (Converter)	Efficiency (VBUS)	Power Dissipation (Converter)	Power Dissipation (VBUS)
12	0.007	5.19	5.19	0	0.084	0	0	0	0	0.084	0.084
12	0.143	5.141	5.14	0.301	1.716	1.547441	1.54714	90.18%	90.16%	0.168559	0.16886
12	0.277	5.139	5.13	0.6	3.324	3.0834	3.078	92.76%	92.60%	0.2406	0.246
12.01	0.408	5.139	5.13	0.9	4.90008	4.6251	4.617	94.39%	94.22%	0.27498	0.28308
12	0.54	5.138	5.13	1.203	6.48	6.181014	6.17139	95.39%	95.24%	0.298986	0.30861
12.01	0.675	5.137	5.12	1.503	8.10675	7.720911	7.69536	95.24%	94.93%	0.385839	0.41139
12.01	0.81	5.136	5.12	1.804	9.7281	9.265344	9.23648	95.24%	94.95%	0.462756	0.49162
12	0.947	5.134	5.11	2.103	11.364	10.796802	10.74633	95.01%	94.56%	0.567198	0.61767
12.01	1.083	5.132	5.11	2.401	13.00683	12.321932	12.26911	94.73%	94.33%	0.684898	0.73772
12	1.223	5.129	5.1	2.701	14.676	13.853429	13.7751	94.40%	93.86%	0.822571	0.9009
12.01	1.363	5.125	5.09	3.003	16.36963	15.390375	15.28527	94.02%	93.38%	0.979255	1.08436

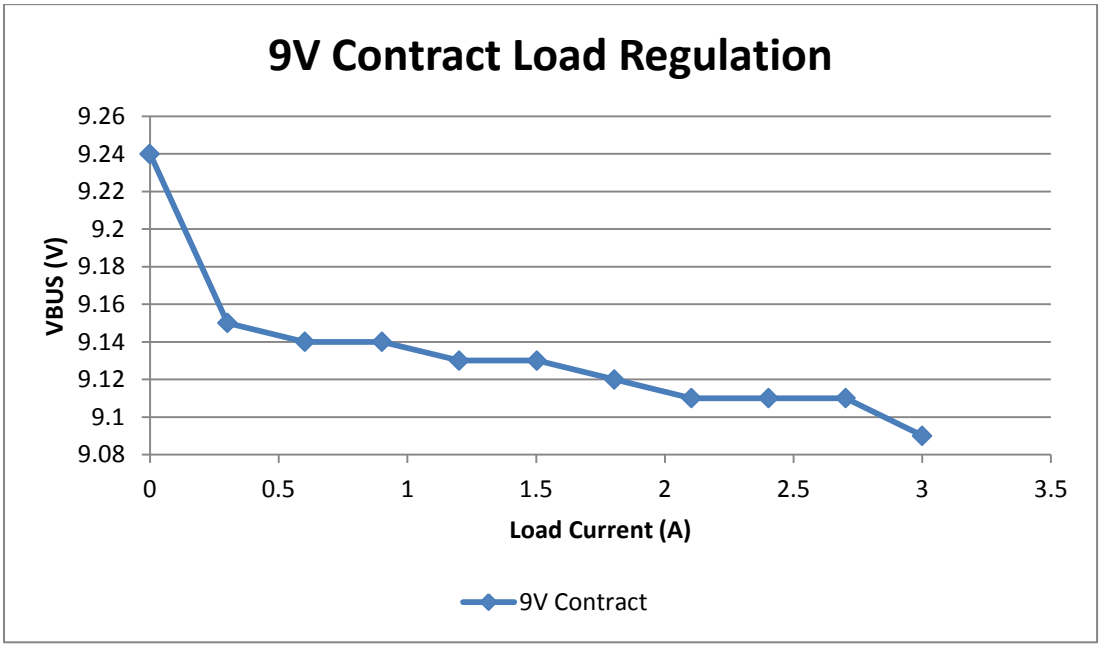
Vin	Iin	Vout (Converter)	Vout (VBUS)	Iout	Pin	Pout (Converter)	Pout (VBUS)	Efficiency (Converter)	Efficiency (VBUS)	Power Dissipation (Converter)	Power Dissipation (VBUS)
12.01	0.011	9.24	9.24	0	0.13211	0	0	0	0	0.13211	0.13211
12	0.244	9.15	9.15	0.301	2.928	2.75415	2.75415	94.06%	94.06%	0.17385	0.17385
12.01	0.477	9.15	9.14	0.602	5.72877	5.5083	5.50228	96.15%	96.05%	0.22047	0.22649
12.01	0.708	9.15	9.14	0.902	8.50308	8.2533	8.24428	97.06%	96.96%	0.24978	0.2588
12	0.94	9.14	9.13	1.201	11.28	10.97714	10.96513	97.32%	97.21%	0.30286	0.31487
12.01	1.176	9.14	9.13	1.504	14.12376	13.74656	13.73152	97.33%	97.22%	0.3772	0.39224
12.02	1.412	9.14	9.12	1.804	16.97224	16.48856	16.45248	97.15%	96.94%	0.48368	0.51976
12	1.649	9.14	9.11	2.104	19.788	19.23056	19.16744	97.18%	96.86%	0.55744	0.62056
12.01	1.886	9.13	9.11	2.404	22.65086	21.94852	21.90044	96.90%	96.69%	0.70234	0.75042
12.01	2.128	9.13	9.11	2.703	25.55728	24.67839	24.62433	96.56%	96.35%	0.87889	0.93295
12	2.37	9.12	9.09	3.001	28.44	27.36912	27.27909	96.23%	95.92%	1.07088	1.16091

4 Regulation

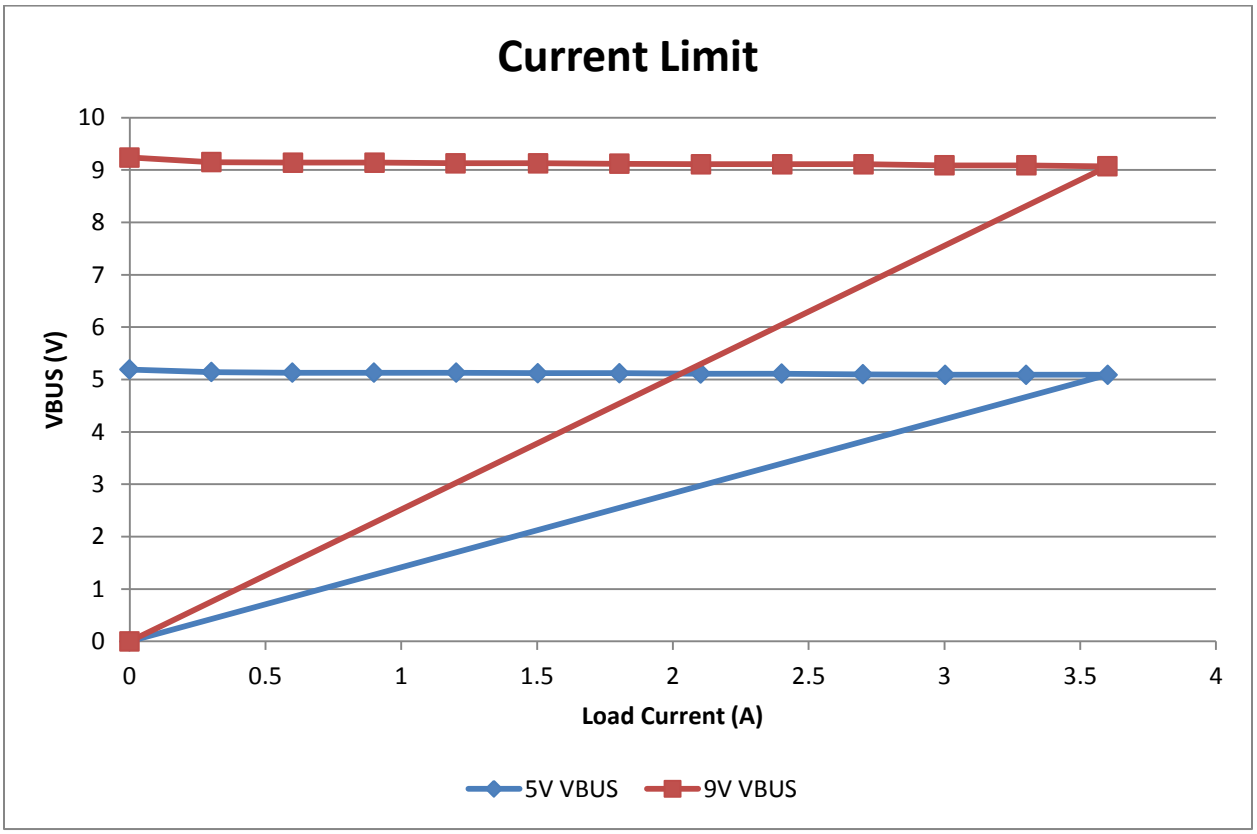
4.1 5V Output



4.2 9V Output

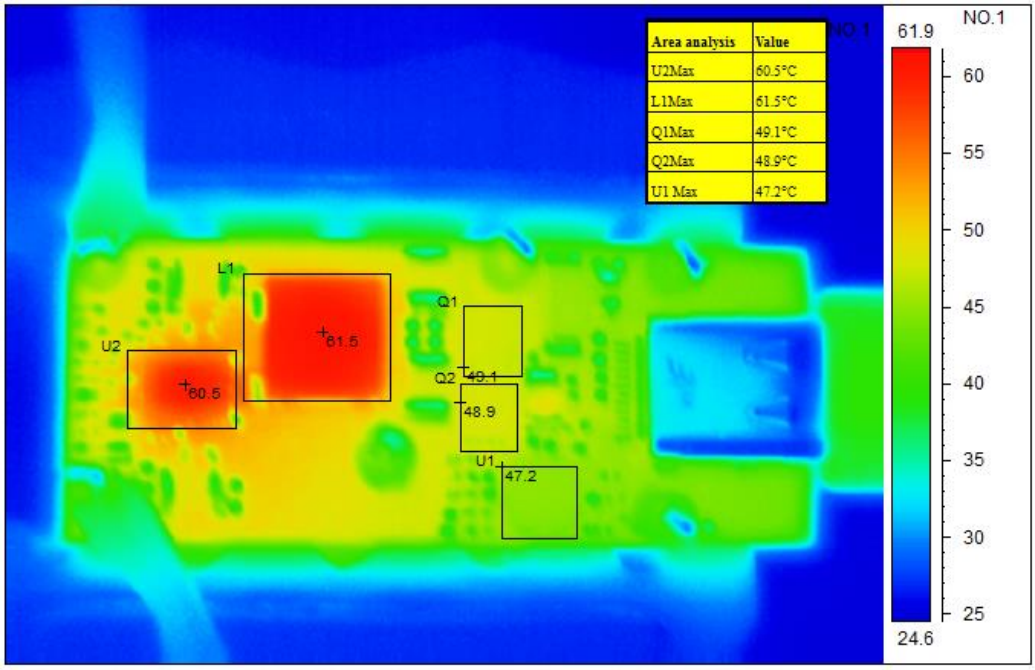


5 Current Limit

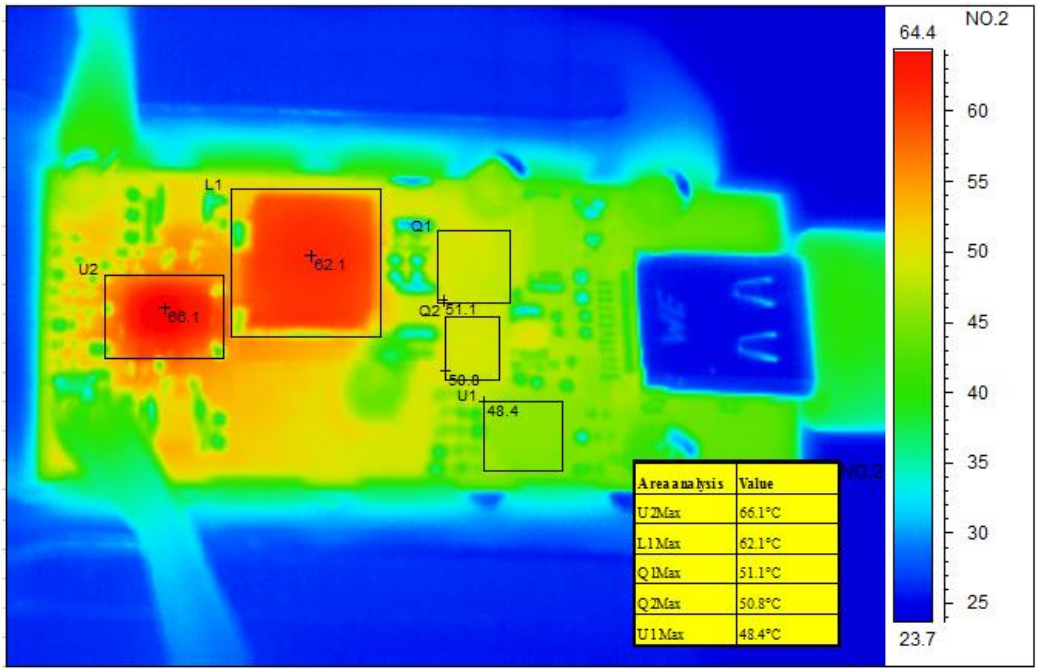


6 Thermal Images

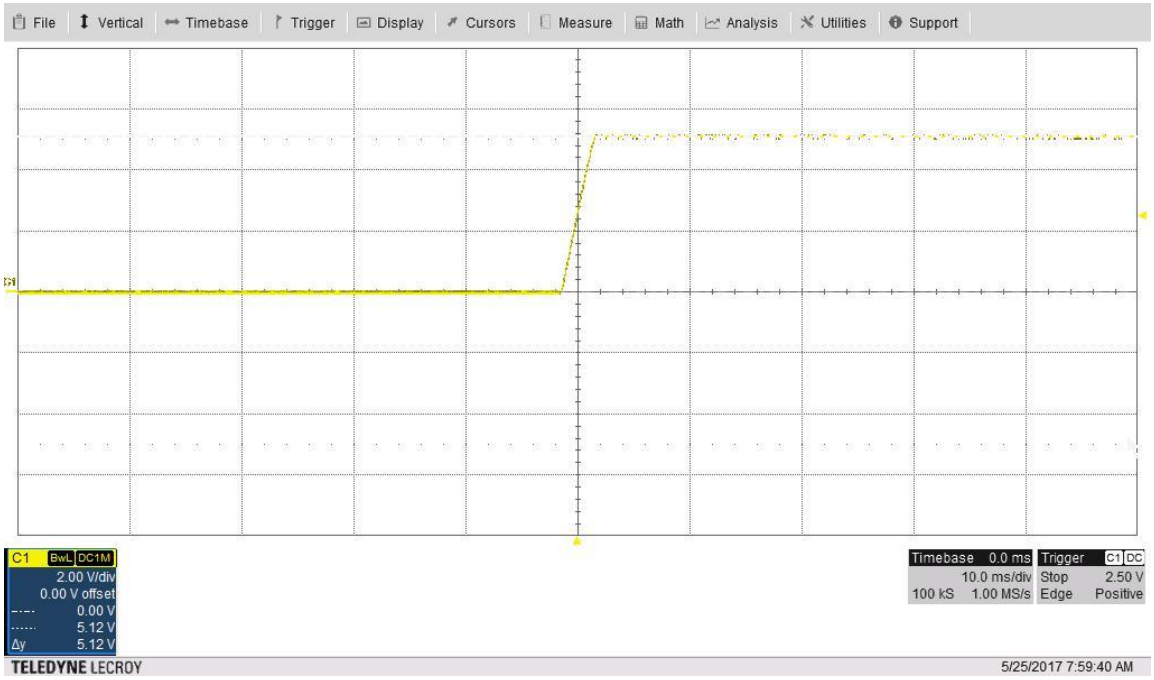
6.1 12V Input, 5V Output at 3A



6.2 12V Input, 9V Output at 3A



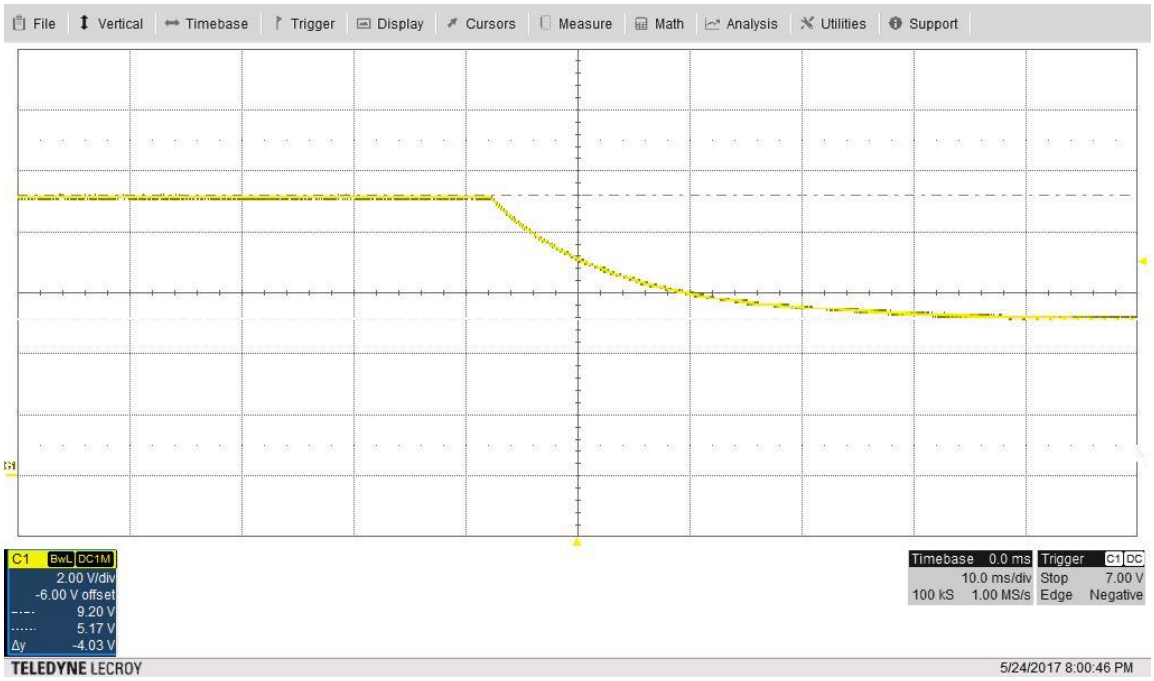
7 Startup



8 Output Voltage Transitions

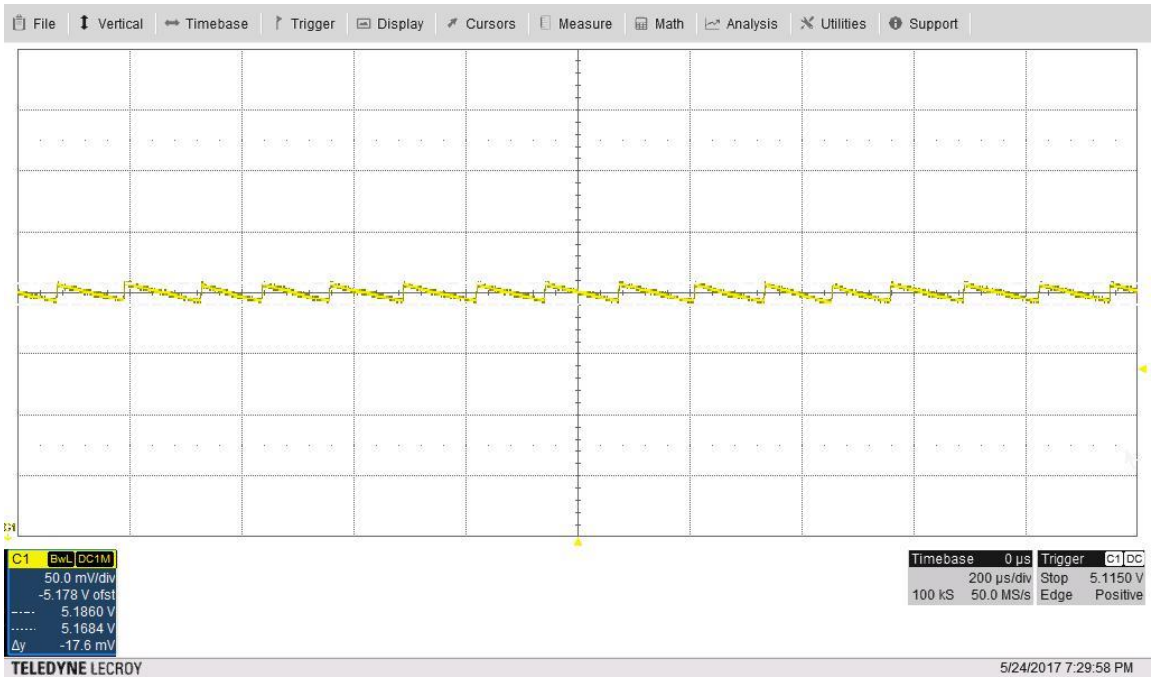
8.1 5V to 9V

8.2 9V to 5V

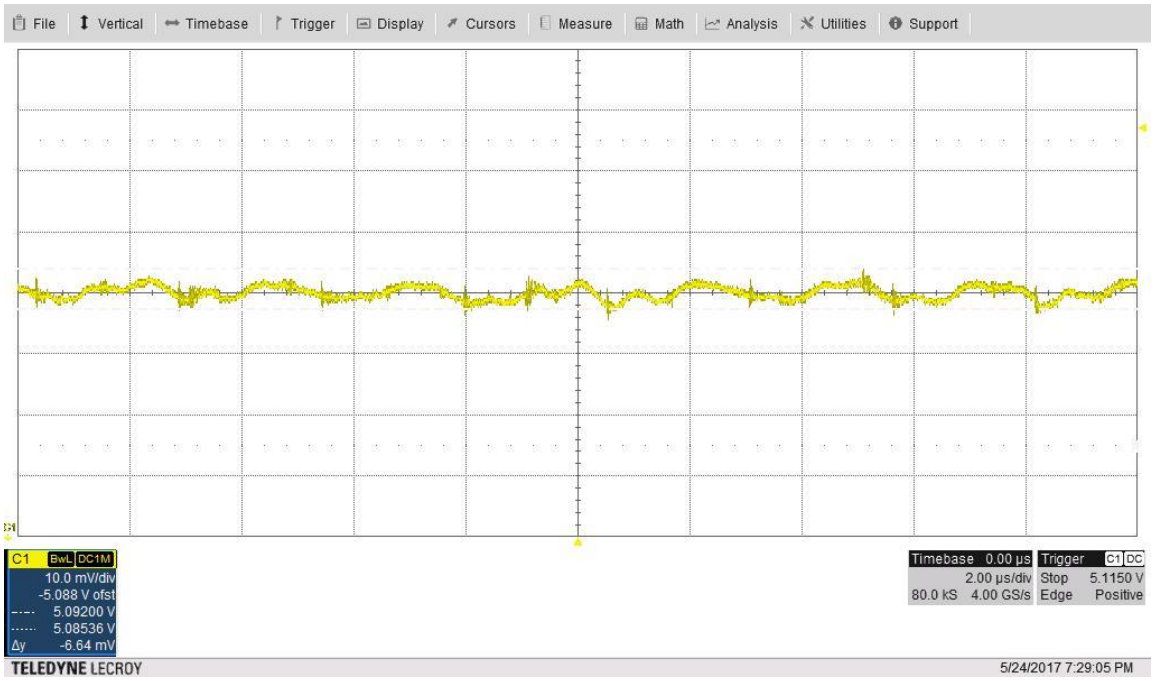


9 Output Voltage Ripple

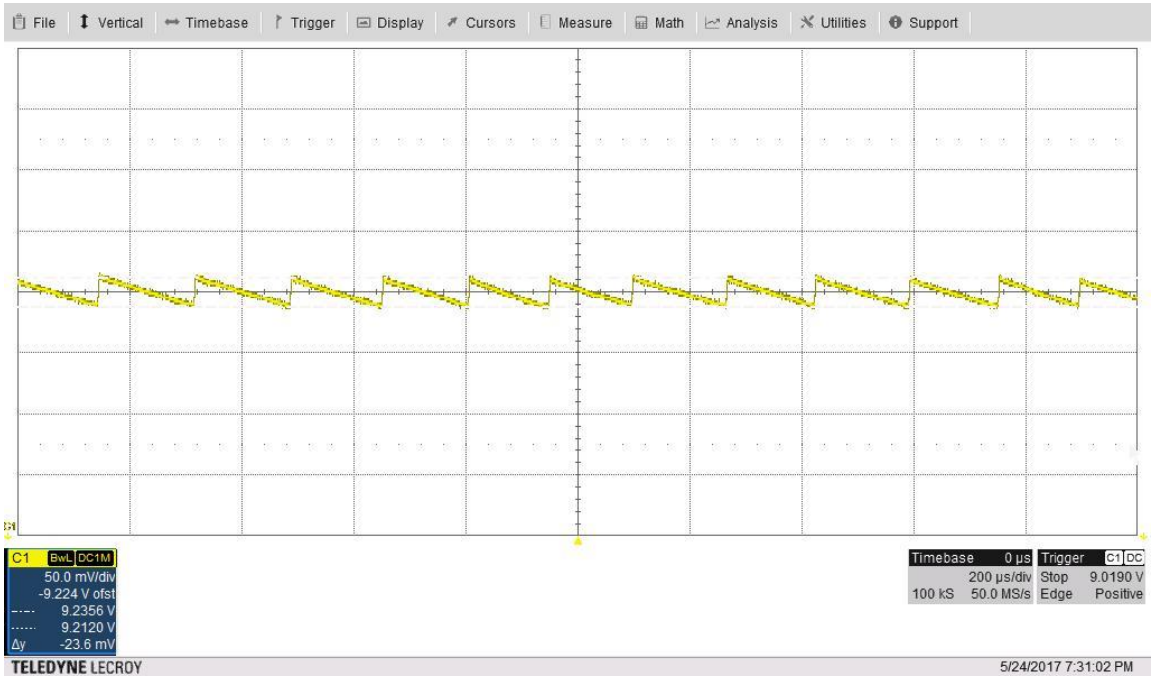
9.1 12V Input, 5V Output at No Load – Measured at C2



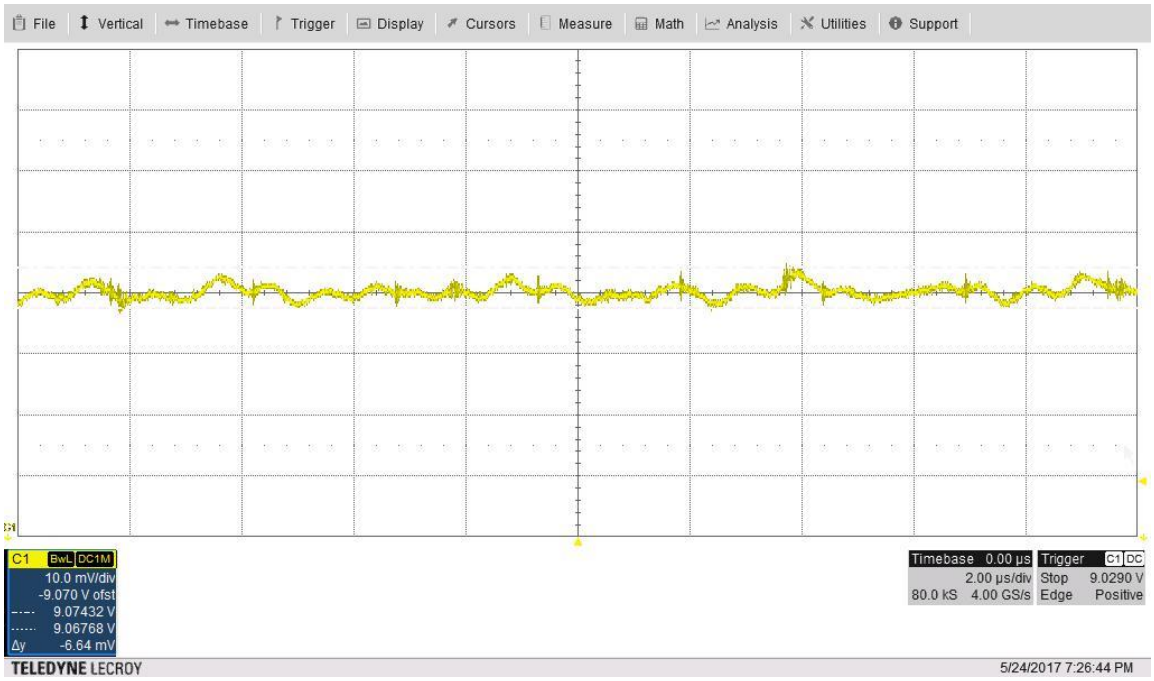
9.2 12V input, 5V Output at 3A – Measured at C2



9.3 12V Input 9V Output at No Load – Measured at C2

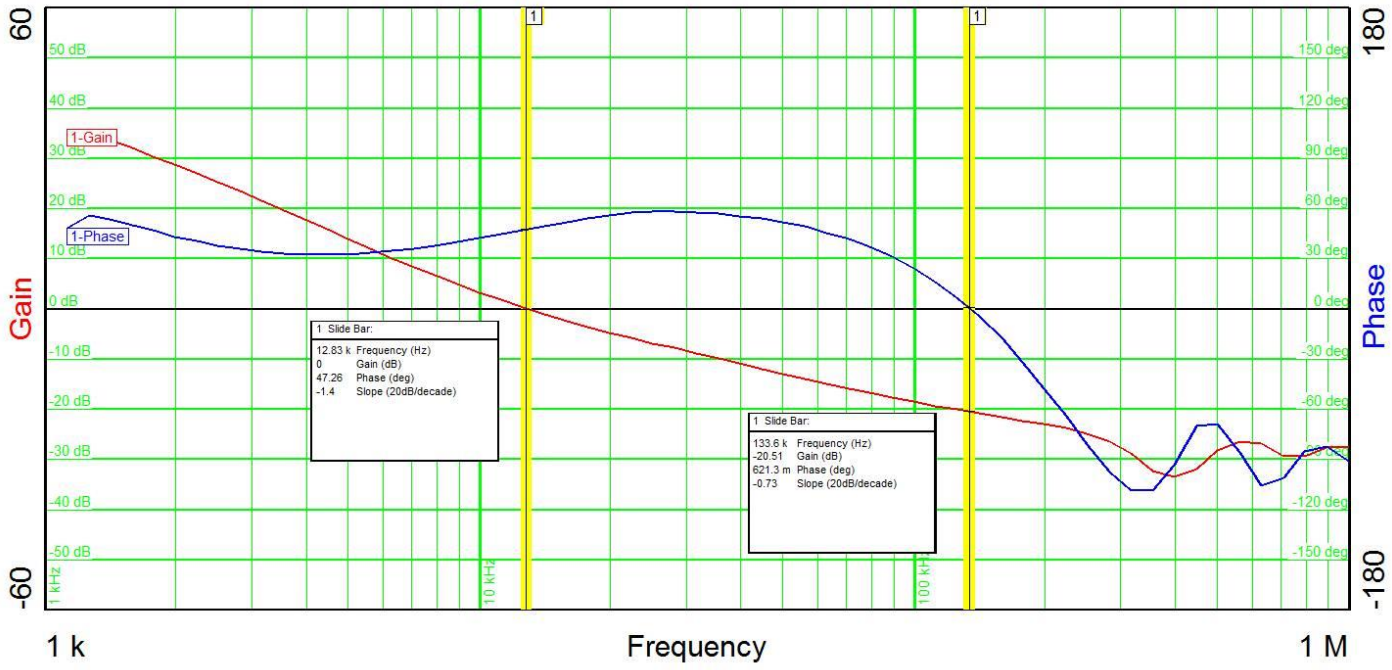


9.4 12V input, 9V Output at 3A – Measured at C2

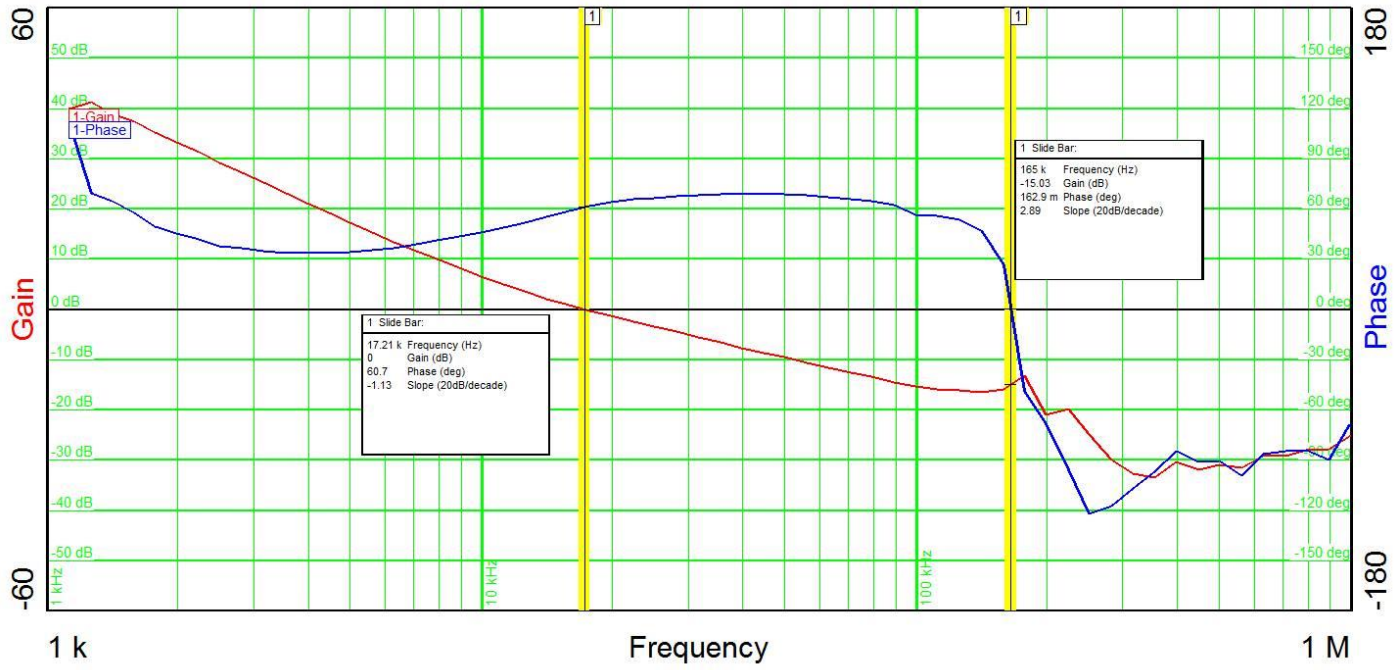


10 Loop Response

10.1 12V Input, 5V Output at 3A



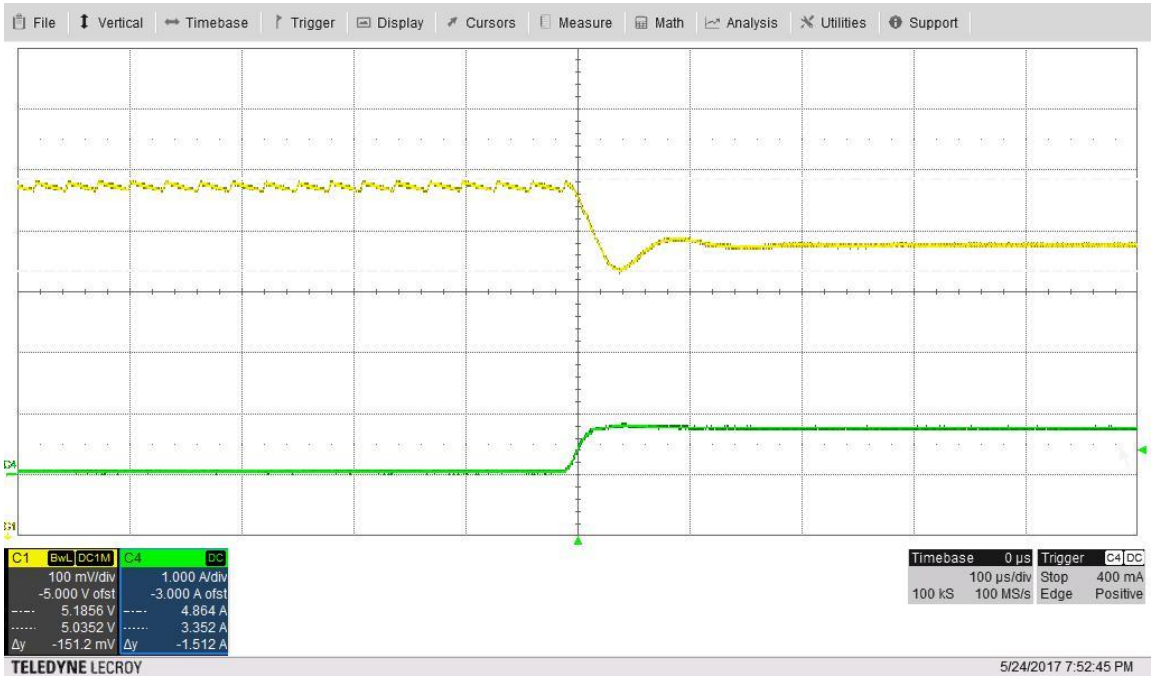
10.2 12V Input, 9V Output at 3A

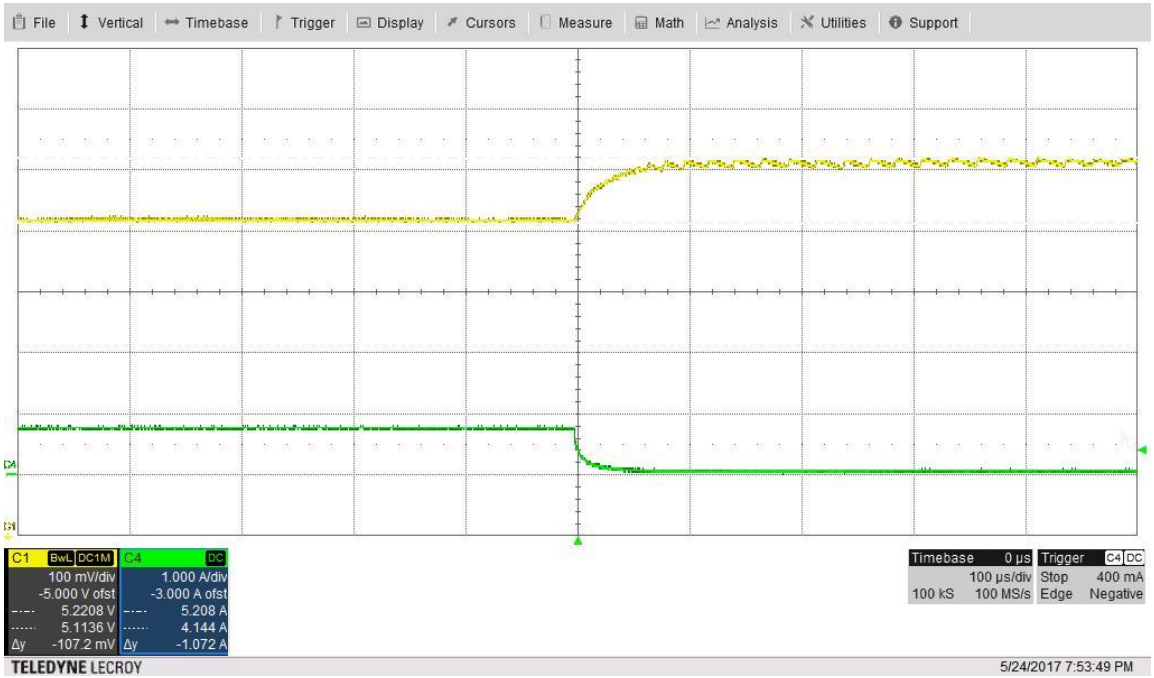


11 Load Transients

11.1 5Vout, 0A to 750mA (0% - 25%), 12Vin

CH1: VBUS CH2: Iout




File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Support
C1 BwL DC1M
100 mV/div
-5.000 V ofst
5.2208 V
5.1136 V
Δy -107.2 mV
C4 DC
1.000 A/div
-3.000 A ofst
5.208 A
4.144 A
Δy -1.072 A
Timebase 0 µs
100 µs/div
100 kS 100 MS/s
Trigger C4 DC
Stop 400 mA
Edge Negative
TELEDYNE LECROY
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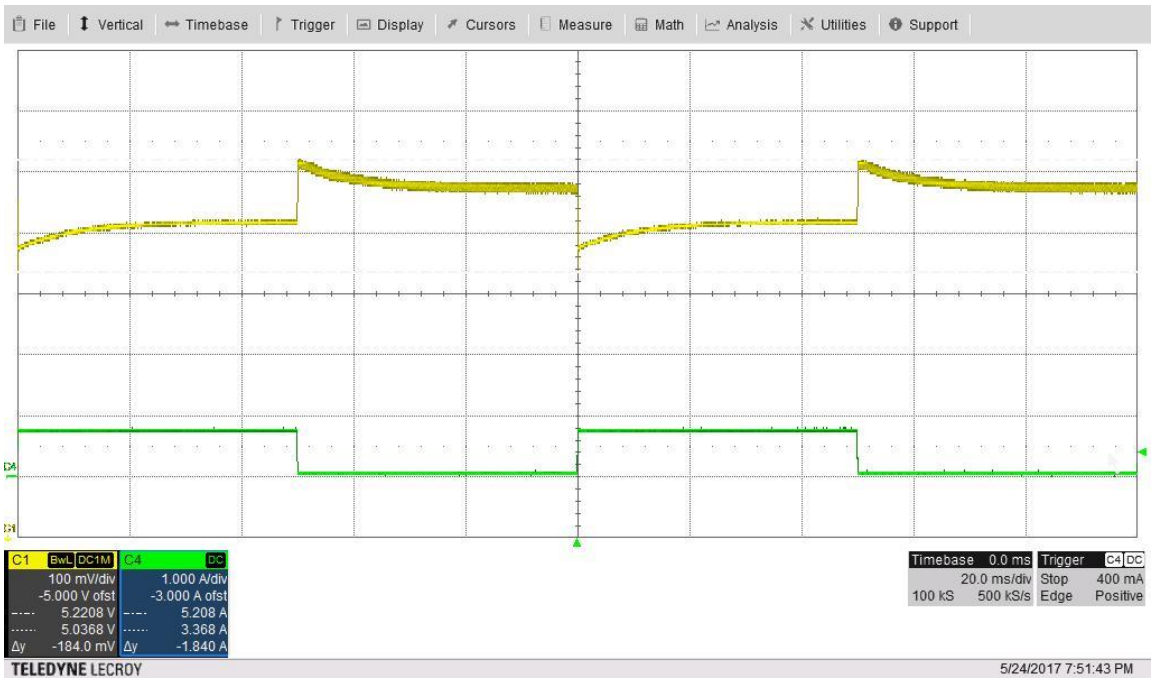
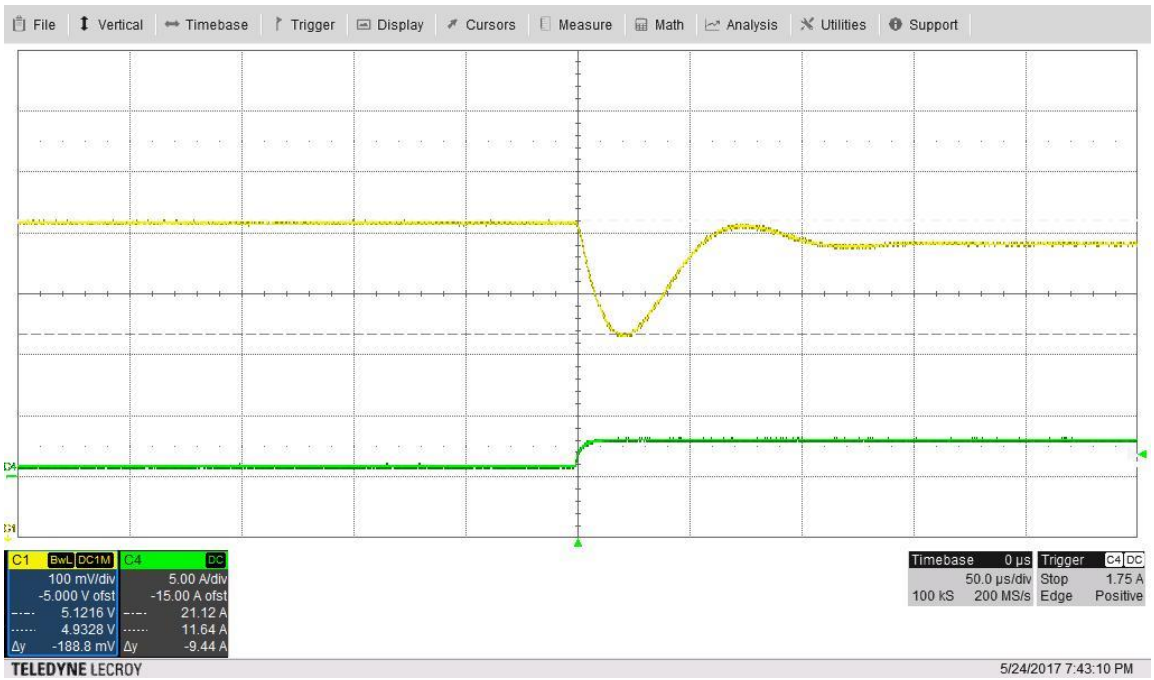
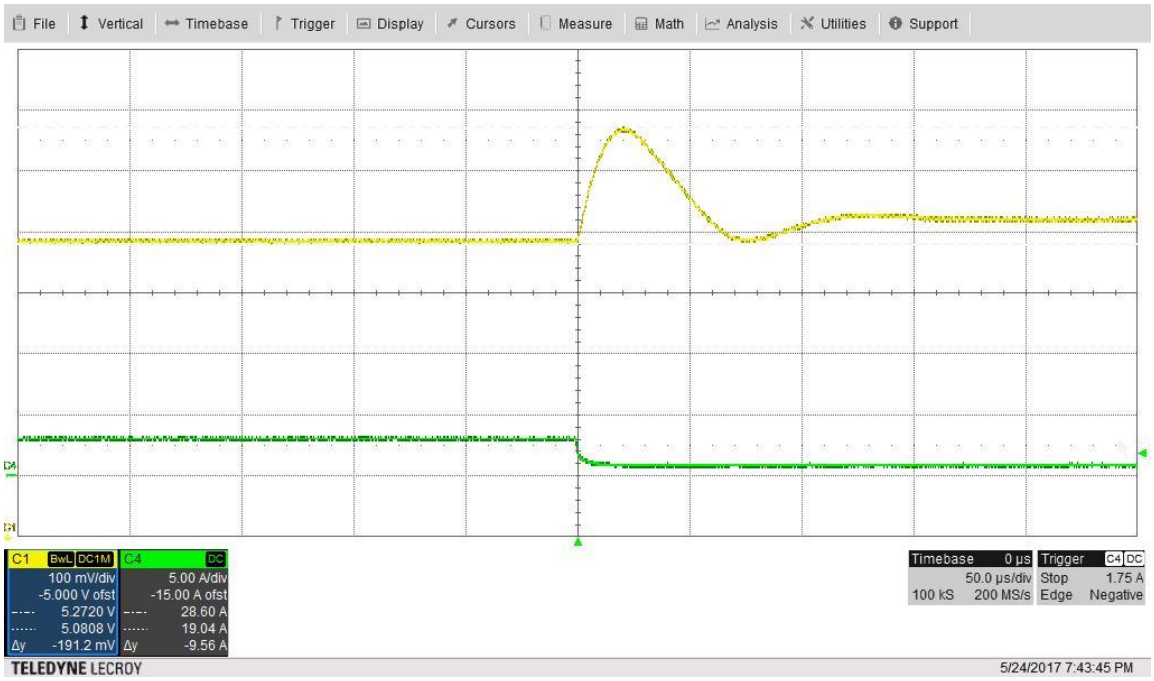
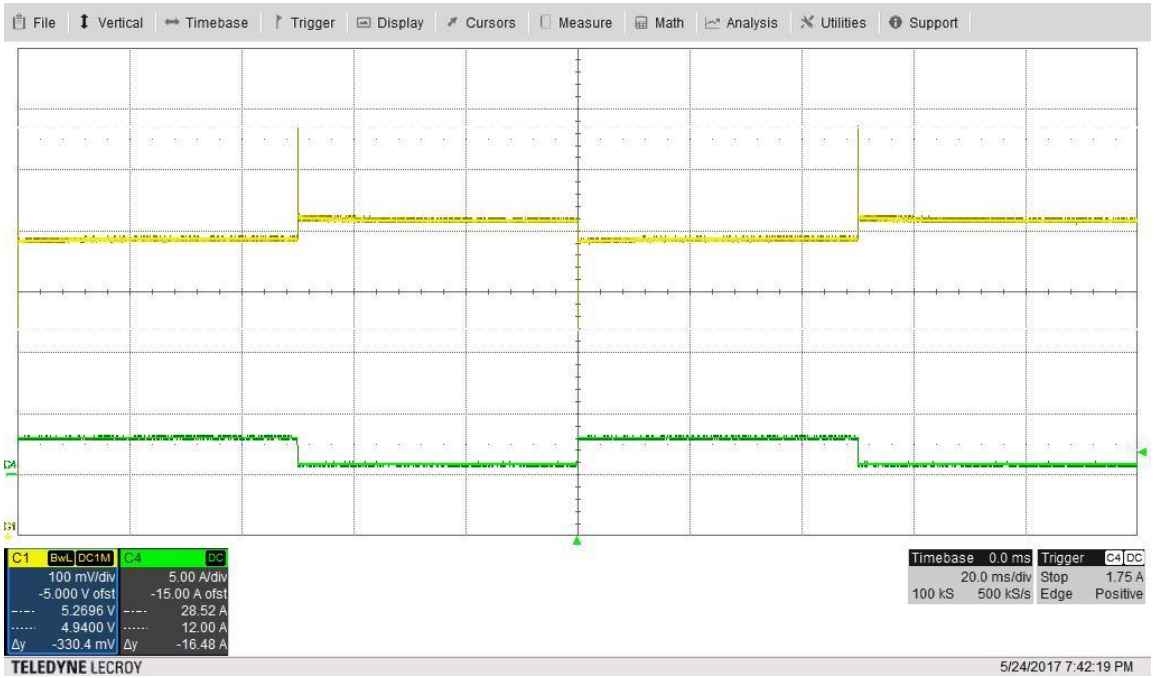

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Support
C1 BwL DC1M
100 mV/div
-5.000 V ofst
5.2208 V
5.0368 V
Δy -184.0 mV
C4 DC
1.000 A/div
-3.000 A ofst
5.208 A
3.368 A
Δy -1.840 A
Timebase 0.0 ms
20.0 ms/div
100 kS 500 kS/s
Trigger C4 DC
Stop 400 mA
Edge Positive
TELEDYNE LECROY
5/24/2017 7:51:43 PM

11.2 5Vout, 750mA to 3A (25% - 100%), 12Vin

CH1: VBUS CH2: Iout

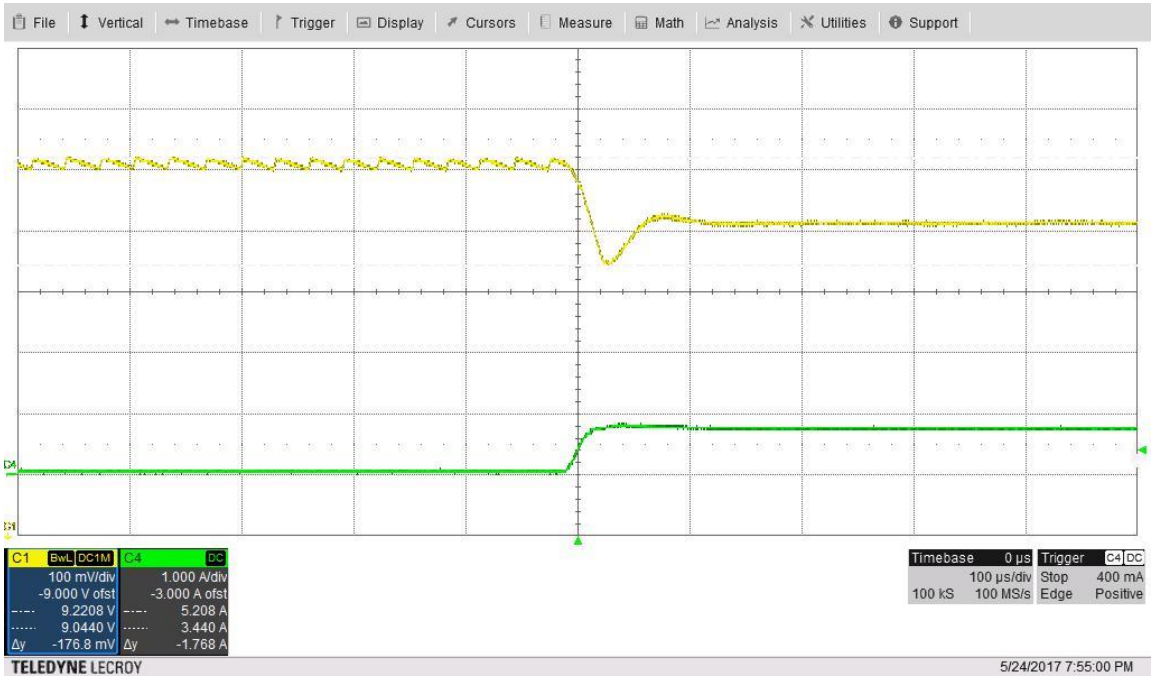


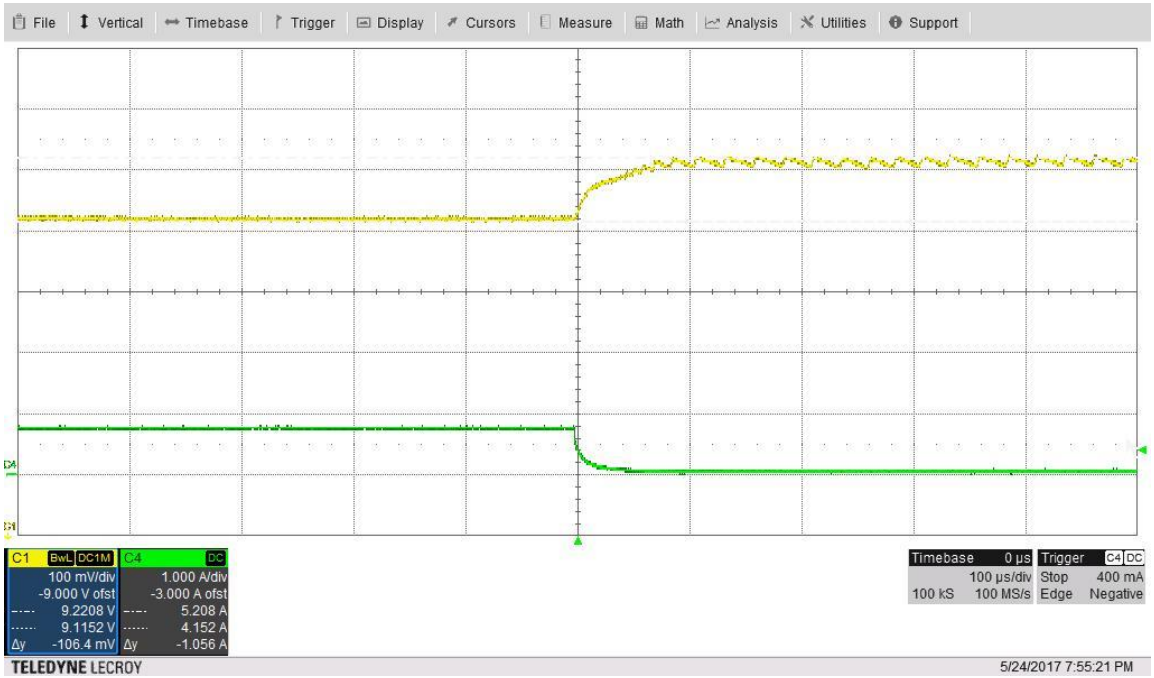


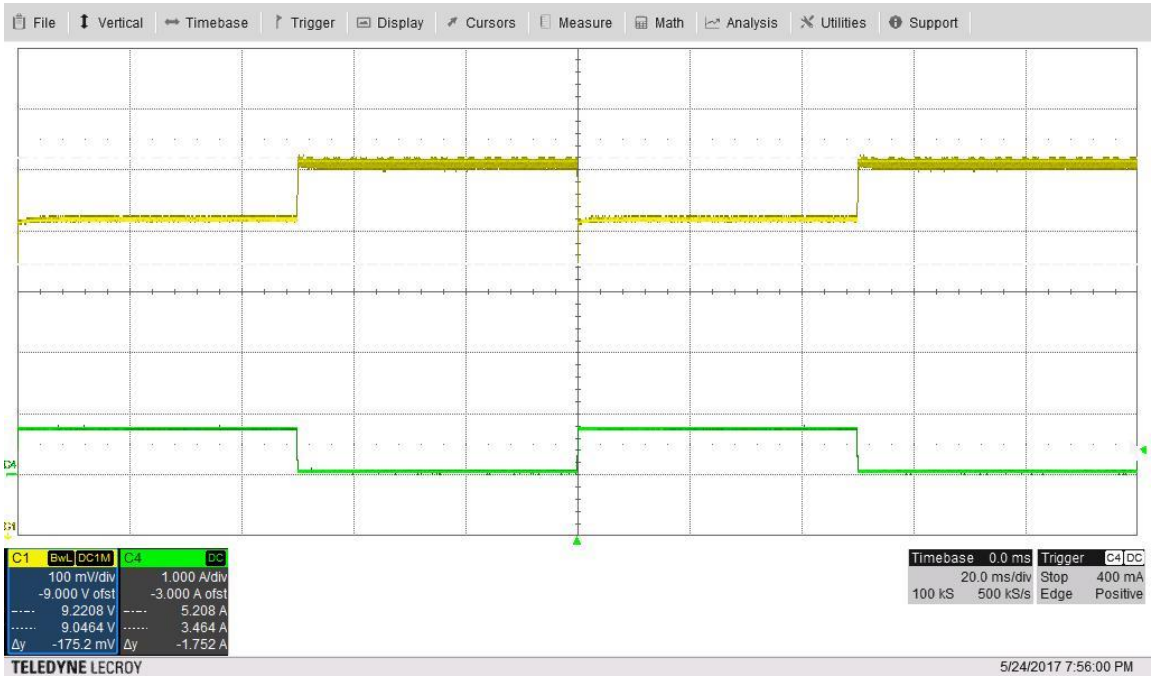


11.3 9Vout, 0A to 750mA (0% - 25%), 12Vin

CH1: VBUS CH2: Iout

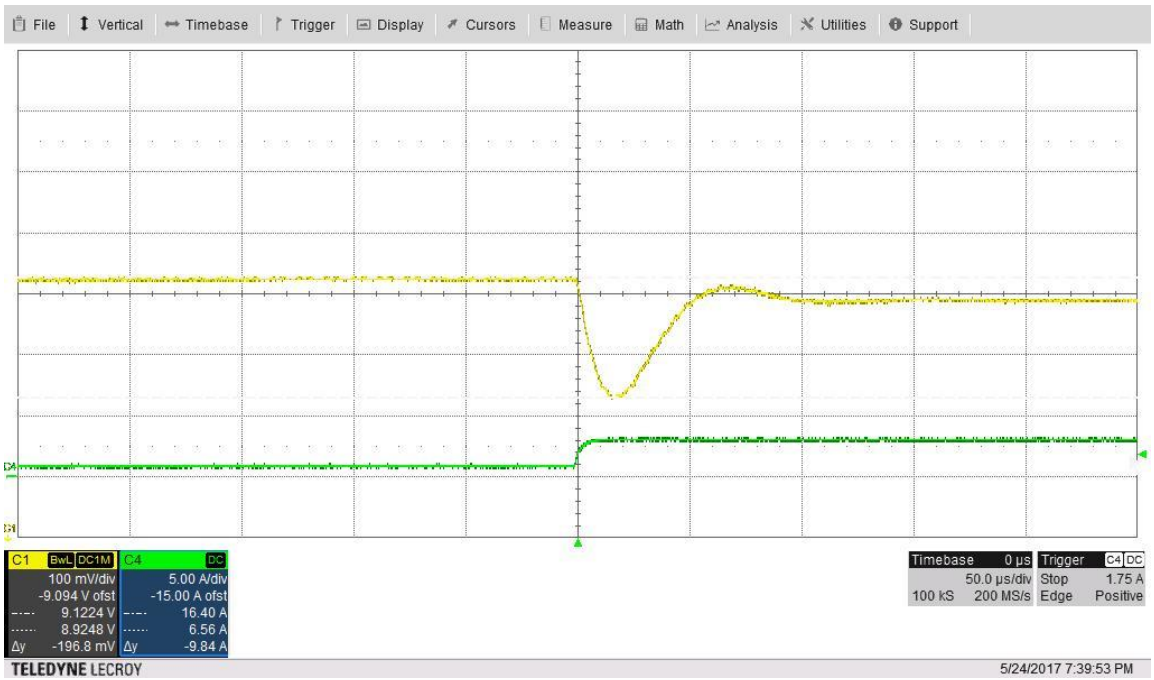


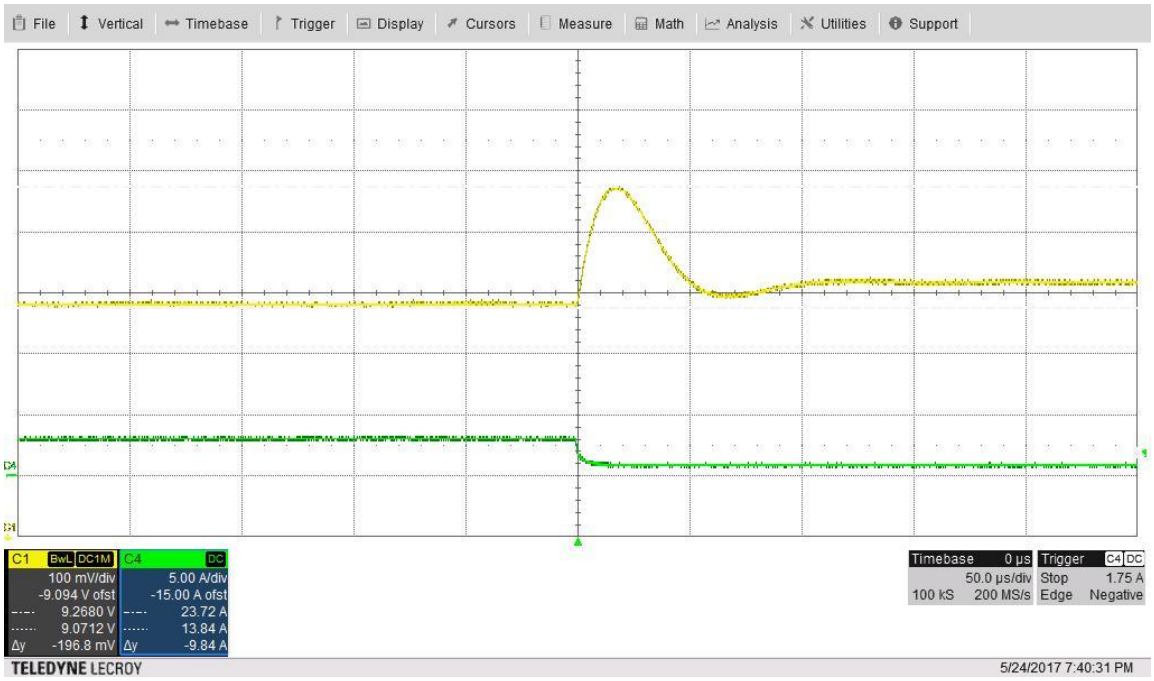

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Support
C1 BwL DC1M
100 mV/div
-9.000 V ofst
9.2208 V
9.1152 V
Δy -106.4 mV
C4 DC
1.000 A/div
-3.000 A ofst
5.208 A
4.152 A
Δy -1.056 A
Timebase 0 µs
100 µs/div
100 kS 100 MS/s
Trigger C4 DC
Stop 400 mA
Edge Negative
TELEDYNE LECROY
5/24/2017 7:55:21 PM

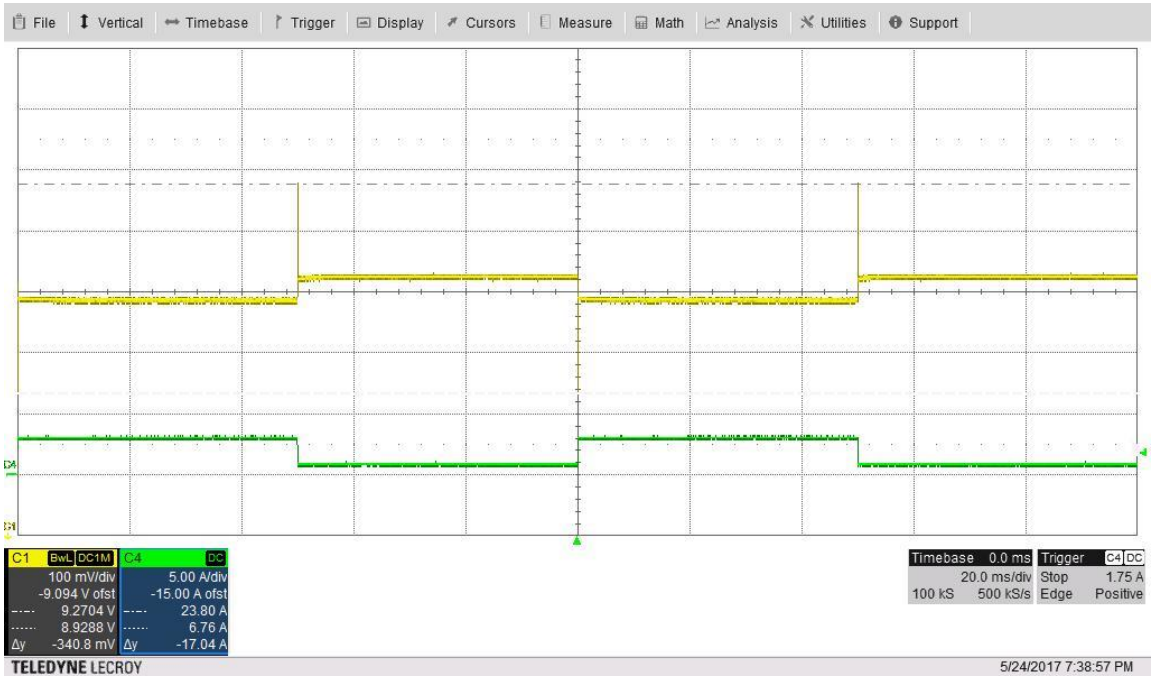

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Support
C1 BwL DC1M
100 mV/div
-9.000 V ofst
9.2208 V
9.0464 V
Δy -175.2 mV
C4 DC
1.000 A/div
-3.000 A ofst
5.208 A
3.464 A
Δy -1.752 A
Timebase 0.0 ms
20.0 ms/div
100 kS 500 kS/s
Trigger C4 DC
Stop 400 mA
Edge Positive
TELEDYNE LECROY
5/24/2017 7:56:00 PM

11.4 9Vout, 750mA to 3A (25% - 100%), 12Vin

CH1: VBUS CH2: Iout

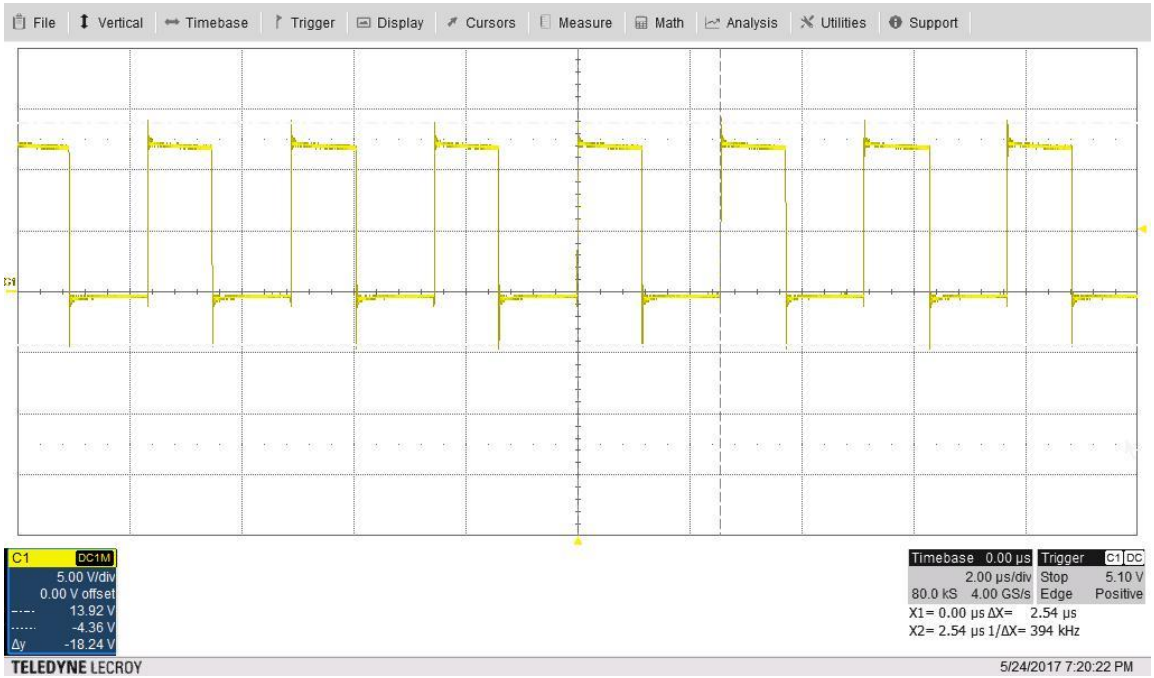




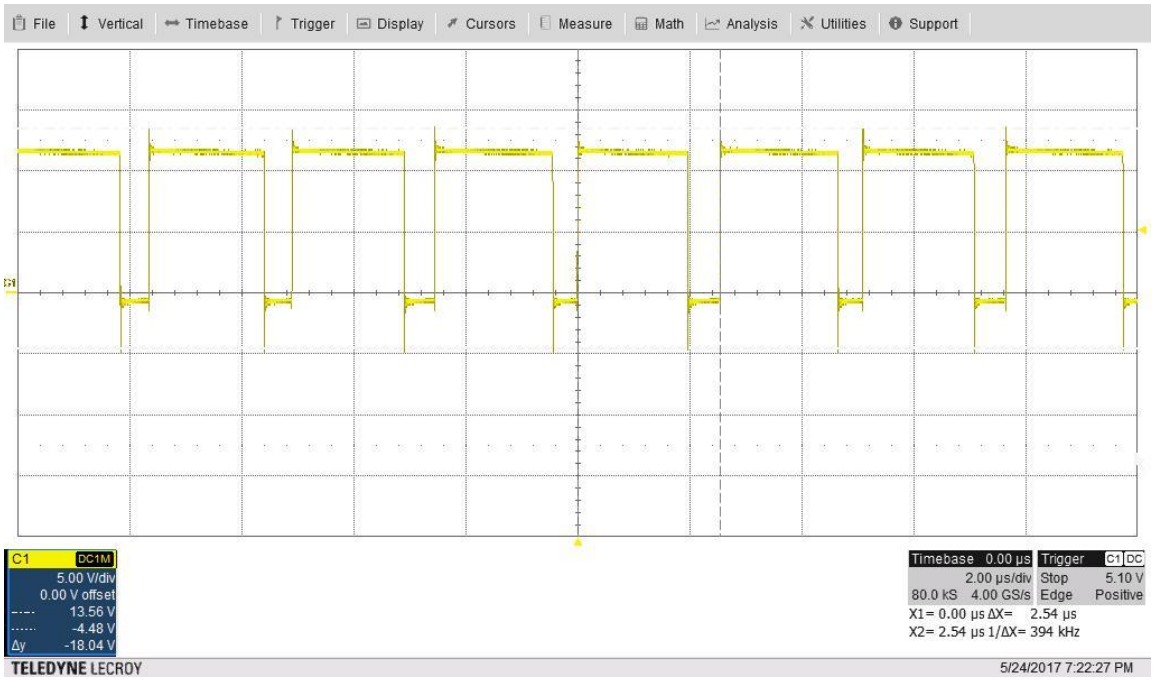


12 Switching Waveforms

12.1 Switch Node – 12V Input, 5V Output at 3A



12.2 Switch Node – 12V Input, 9V Output at 3A



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