

TI Designs

Wideband Receiver Reference Design for Upstream DOCSIS 3.1 Applications



Description

This reference design consists of an analog front-end (AFE) signal chain for wideband receiver applications using the LMH2832 digitally-controlled variable gain amplifier and ADS54J40 analog-to-digital converter. The design is primarily targeted for upstream DOCSIS 3.1 receiver applications specified for cable modem termination systems (CMTS) and supports up to 196 MHz of upstream signal bandwidth. The circuit solves the filtering and analog signal processing requirements for the DOCSIS 3.1 standard, which makes it easier for system designers to readily incorporate the design on the CMTS-side of the upstream signal path.

Resources

TIDA-01378	Design Folder
LMH2832	Product Folder
ADS54J40	Product Folder
LMK04828	Product Folder

Features

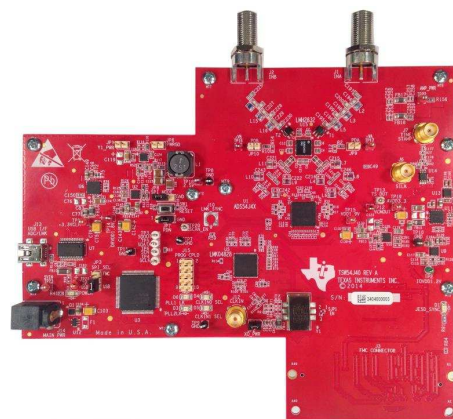
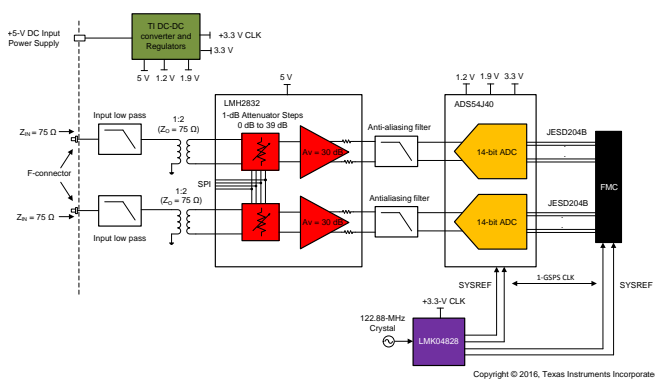
- AC-Coupled Signal Path From 100 kHz to 204 MHz With 196 MHz of Upstream-Signal Bandwidth Support for DOCSIS 3.1 Applications
- 75-Ω F-Connector Input Interface
- Single-Ended-to-Differential Conversion Achievable Using 1:2 ($Z_o = 75 \Omega$) Transformer
- High-Performance, Digitally-Controlled Variable Gain Amplifier (LMH2832) Programmable From 30-dB to -9-dB Gain in 1-dB Steps to Maintain Full-Scale Input at ADC
- 14-Bit ADC (ADS54J40) Operating at 983.04 MSPS for Sampling Input Signals
- Design Supports 5-V Supply Using Wall-Mount Power Adapter

Applications

- Cable Infrastructure
- High-Speed Video Analyzer
- High-Speed Data Acquisition



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1 System Overview

1.1 System Description

The TIDA-01378 reference design mainly consists of an analog front-end (AFE) signal chain using a digitally-controlled variable gain amplifier (LMH2832) and an analog-to-digital converter (ADS54J40) for upstream DOCSIS 3.1 CMTS receiver applications. This guide addresses important parameters such as the system signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) performance to aid in the system design.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input power source	5.0-V nominal voltage from wall-mount power adapter
Input connector type	75-Ω F-connector input
Maximum input frequency	210 MHz
Minimum system SNR (200 MHz BW) for -1-dBFs input at the ADC	58 dBFs
Minimum system SFDR for -1-dBFs input at the ADC	70 dBFs
ADC bit resolution	14-bit
ADC clock frequency sample rate	500 MHz to 1 GHz
Output data rate	Four lanes per ADC at 5.0 Gbps with JESD204B interface subclass-1 support
Average active-state current consumption	1.71 A
Operating temperature	-40°C to 85°C (estimated based on individual device datasheets)

1.3 Block Diagram

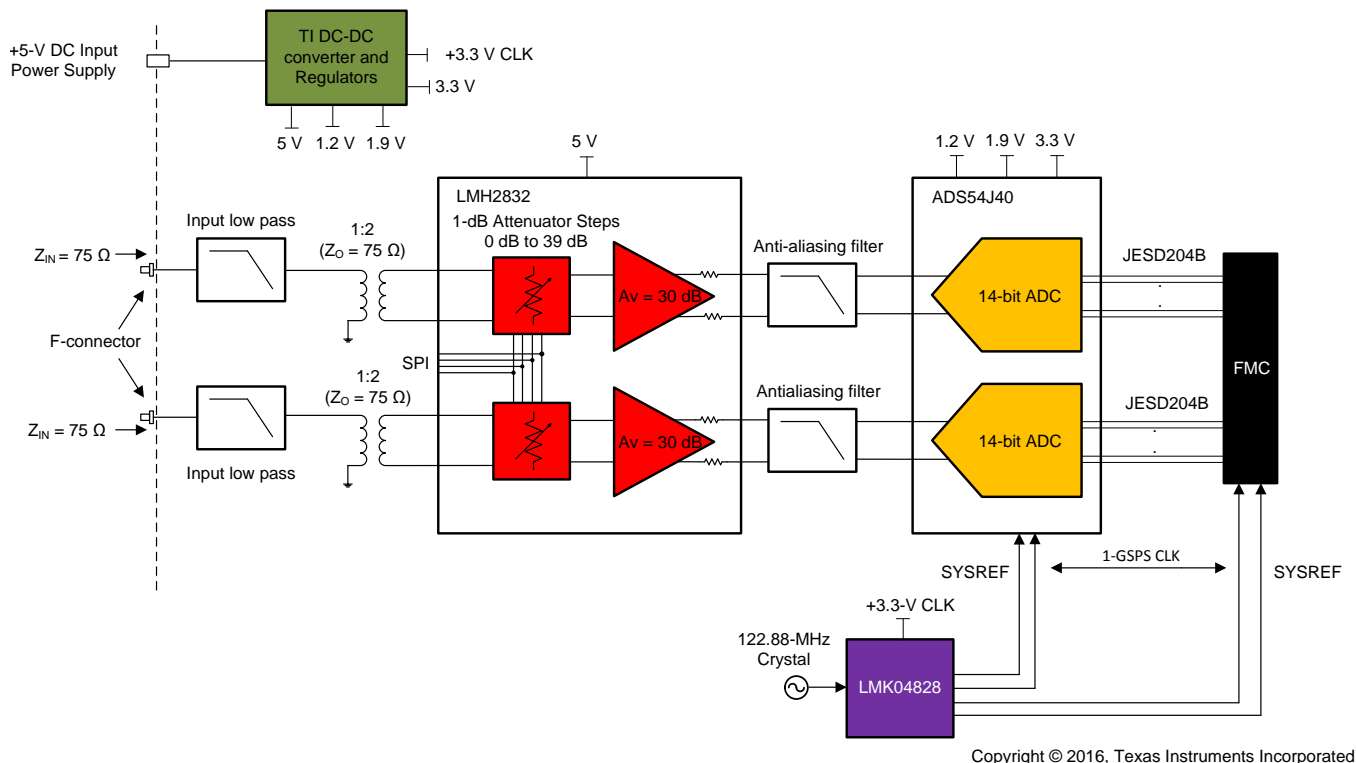


Figure 1. System-Level Block Diagram

1.4 Highlighted Products

1.4.1 LMH2832

The LMH2832 is a high-linearity, dual-channel, digital variable-gain amplifier (DVGA) for high-speed signal chain and data-acquisition systems. The LMH2832 is optimized to provide high bandwidth, low distortion, and low noise, thus making the device ideally suited as a dual, 14-bit, analog-to-digital converter (ADC) driver.

Key features of the device include:

- –3-dB bandwidth of 1.1 GHz at maximum gain
- Individual channel, serial peripheral interface (SPI)-controlled gain programmable from 30 dB to –9 dB in 1-dB attenuator steps
- Output third-order intercept point (OIP3) of 51 dBm at 200 MHz
- Noise figure of 6.5 dB (maximum gain) at 300 MHz for $Z_{IN} = 150 \Omega$
- Input return loss of 17 dB at 300 MHz ($Z_{IN} = 150 \Omega$)
- Single 5-V supply operation with adjustable power consumption of 90 mA to 108 mA per channel

1.4.2 ADS54J40

The ADS54J40 is a low-power, wide-bandwidth, 14-bit, 1.0-GSPS, dual-channel, analog-to-digital converter (ADC). Key features of the device include:

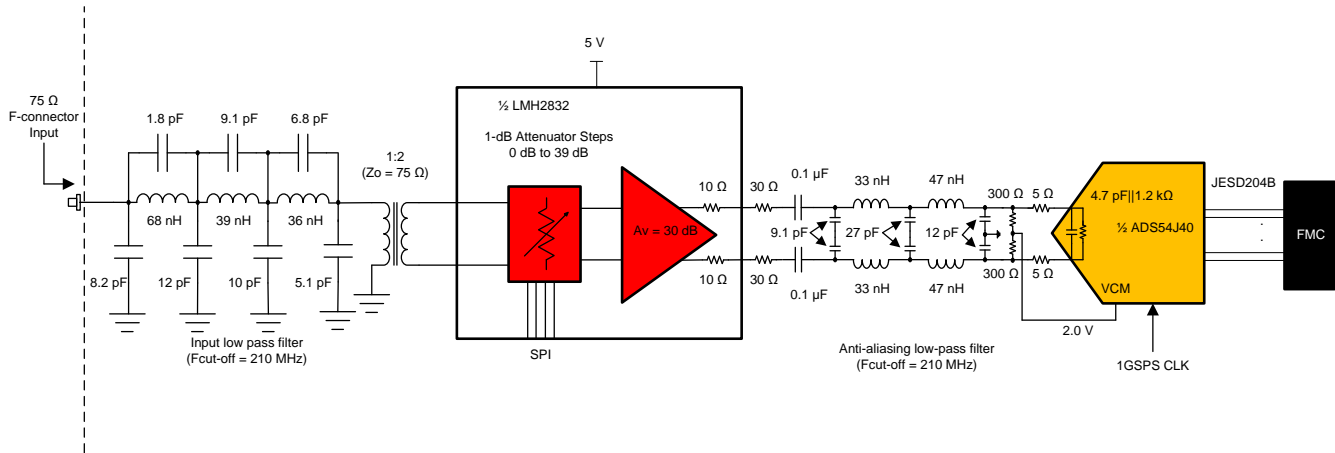
- 14-bit resolution, dual-channel, 1-GSPS ADC
- Noise floor: –158 dBFS/Hz
- spectral performance ($f_{IN} = 170$ MHz at –1 dBFS):
 - SNR: 69.0 dBFS
 - NSD: –155.9 dBFS/Hz
 - SFDR: 86 dBc
 - SFDR: 89 dBc (except HD2, HD3, and interleaving tones)
- Input 3-dB bandwidth of 1.2GHz
- JESD204B interface with subclass-1 support for two or four lanes per ADC at 10.0 Gbps or 5.0 Gbps, respectively
- Power dissipation: 1.35 W per channel at 1 GSPS

1.4.3 LMK04828

The LMK04828 is an ultra-low-noise JESD204B-compliant clock-jitter cleaner with dual-loop phase-locked loops (PLLs) that generates the 1-GHz input clock signal to the ADC using a 122.88-MHz crystal oscillator. This device also generates the SYSREF signal, which along with the clock signal, is used to properly synchronize the JESD204B digital outputs coming from the ADC to the Virtex field-programmable gate array (FPGA).

2 System Design Theory

The critical signal path of this reference design involves an input 75-Ω low-pass filter followed by a 1:2 ($Z_0 = 75 \Omega$) transformer, a digitally-controlled variable gain amplifier (DVGA), an antialiasing filter, and then the ADC (see [Figure 2](#)).



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Figure 2. Diagram of Complete Front-End Signal Chain

[Figure 3](#) shows the upstream- and downstream-channel frequency profile for the new DOCSIS 3.1 standard. Reducing out-of-band spurious emissions in an upstream-receiver signal path requires limiting the bandwidth of the upstream signals by suppressing the out-of-band, spurious, downstream-channel frequencies. As a result, the input consists of a 75-Ω single-ended, seventh-order, Caueer-Chebyshev low-pass filter. [Figure 3](#) shows the characteristics of this filter. Using the Caueer-Chebyshev architecture, the input filter provides greater than 40 dB of stop-band attenuation at 258 MHz with a corner frequency (F_0) of 210 MHz.

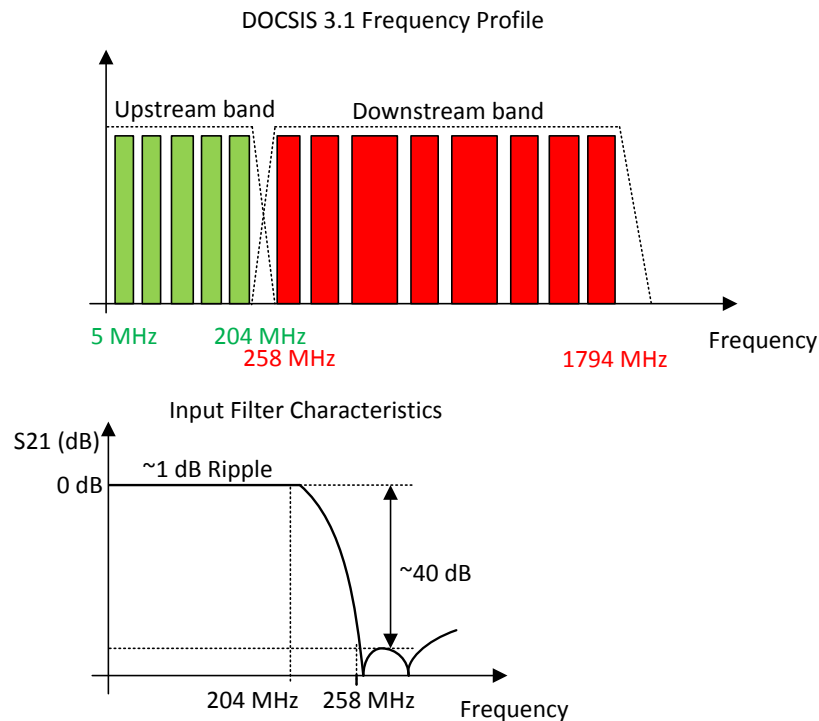


Figure 3. DOCSIS 3.1 Frequency Profile and Upstream-Input Filter Requirements

The input filter is followed by a 1:2 ($Z_o = 75 \Omega$) impedance transformer that matches the single-ended 75- Ω input with the 150- Ω differential input impedance of the DVGA (LMH2832). This application uses a transformer with a minimum flat-band response of up to 270 MHz and also provides DC isolation between the RF coaxial input and the DVGA common-mode input voltages. The 1:2 impedance ratio of the transformer creates a voltage gain of approximately 3 dB.

The DVGA (LMH2832) functions in an automatic gain control (AGC) loop so as to maintain constant signal power going into the ADC. The DVGA architecture consists of 39 steps of a 1-dB ladder attenuator followed by a 30-dB voltage-gain fixed-gain amplifier. The device exhibits a relatively-constant noise figure (NF) for the first 4-dB attenuator steps with the NF degrading proportional to the fifth attenuator step, thereby providing a dynamic range improvements. Low distortion and noise with greater than 300 MHz of operating frequency make the LMH2832 an ideal candidate for DOCSIS 3.1 signal-conditioning applications.

Following the DVGA, an antialiasing filter suppresses the out-of-band noise and harmonics generated by the signal amplification of the DVGA. The antialiasing filter has a fifth-order low-pass characteristic with a cutoff frequency of 210 MHz.

An ADC (ADS54J40) samples the input signal at 983.04 MSPS with 14-bit resolution and outputs the data in four lanes of JESD204B format. The interface between the DVGA and the ADC is AC-coupled, which isolates the DVGA output common-mode (CM) voltage and the ADC input CM voltage. Operating the ADC inputs near their full scale of $1.9 V_{PP_DIFF}$ is important to effectively maximize the dynamic range of the ADC. The clock to the ADC is provided by a low-noise clock-jitter cleaner (LMK04828) which is derived from a 122.88-MHz onboard crystal oscillator. Operating the ADC at a slower sample rate of 600 MSPS is possible given that the requirement for upstream channel bandwidth is only up to 204 MHz, which can reduce the overall system power consumption.

2.1 Input Filter Characteristics

The narrow separation (of ~54 MHz) between the upstream band and the downstream band requires the stop-band attenuation to be sharp following the upstream band cutoff frequency ($f_o = 204$ MHz). This narrow separation also requires achieving greater than 40 dB of stop-band attenuation to avoid any downstream spurs from interacting with the upstream bands. For this reason, the input filter selected is a 75- Ω , single-ended, seventh-order, Cauer-Chebyshev low-pass filter. Also, to avoid any signal reflections due to long coaxial cables, the return loss requirement for a 75- Ω input must be greater than 12 dB. Figure 4 shows the simulated return loss (S11) and forward-transfer function (S21) of the input filter.

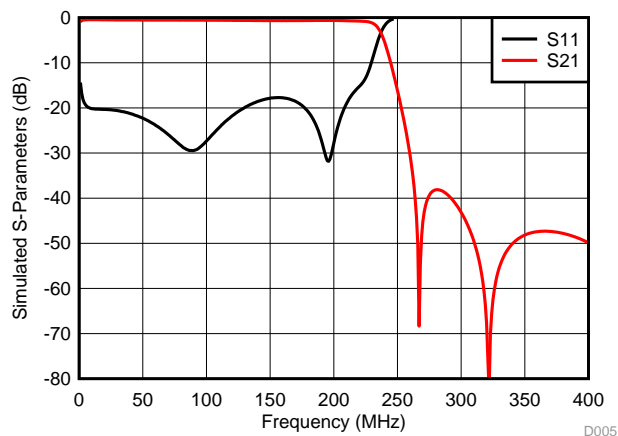


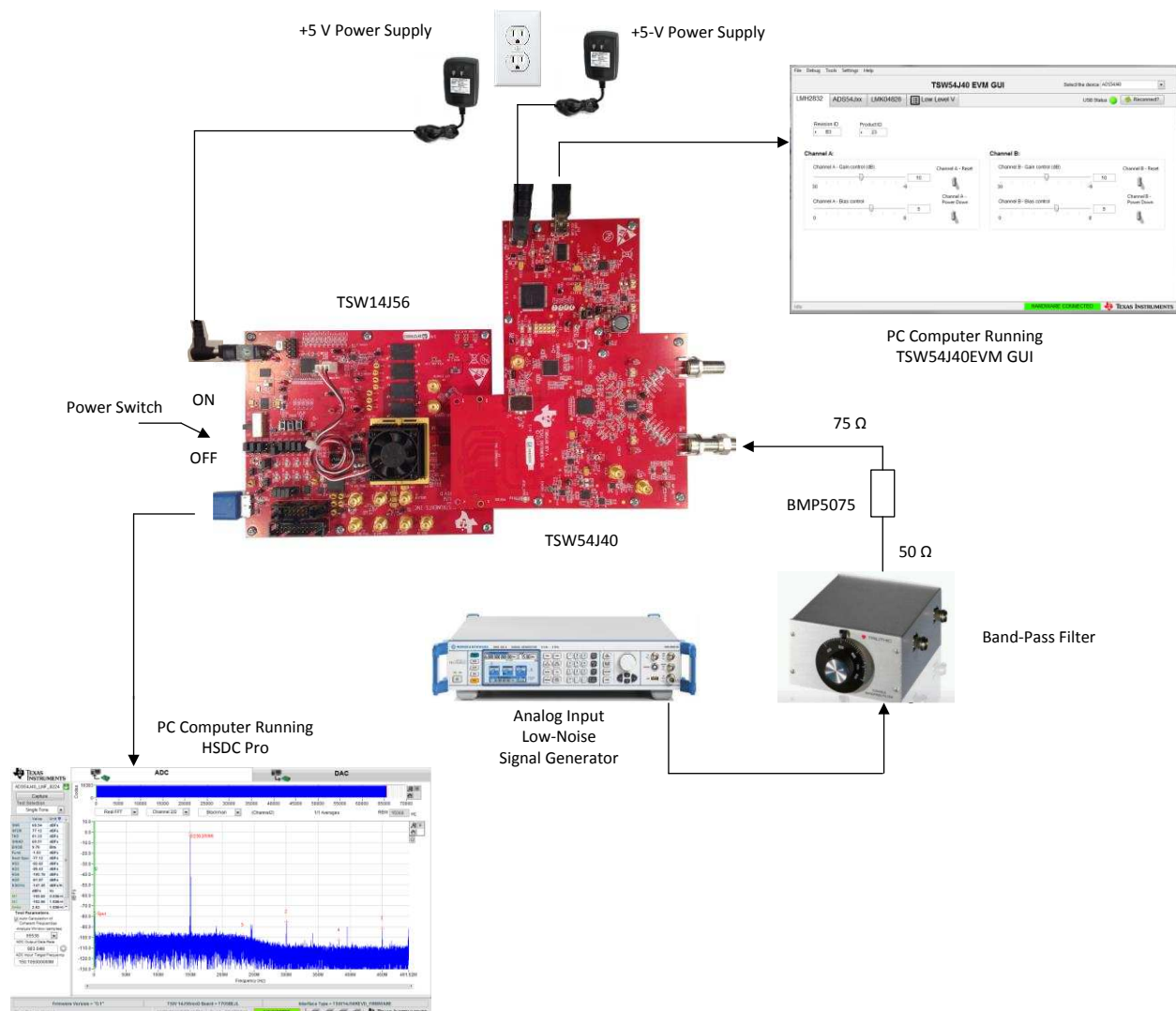
Figure 4. Simulated Input Filter Transfer Function

3 Getting Started Hardware and Software

3.1 Hardware

Figure 5 shows the default bench setup for evaluating the reference design. A low-noise signal generator is used to generate the required single-tone signal. A band-pass filter is used to suppress the signal-generator harmonics from the input signal and drives the BMP5075 device, which is a 50-Ω to 75-Ω impedance-conversion pad. The 75-Ω side of the BMP5075 device is connected to the F-connector input of the TSW54J40 evaluation module (EVM).

The TSW54J40 EVM connects to the TSW14J56 EVM data-capture platform through an FPGA Mezzanine card (FMC) connector and uploads data to a computer that is running the High-Speed Data Converter Pro (HSDCPro) software, which analyzes the data.



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Figure 5. Hardware Setup Diagram

Figure 6 shows a screenshot of the board image.

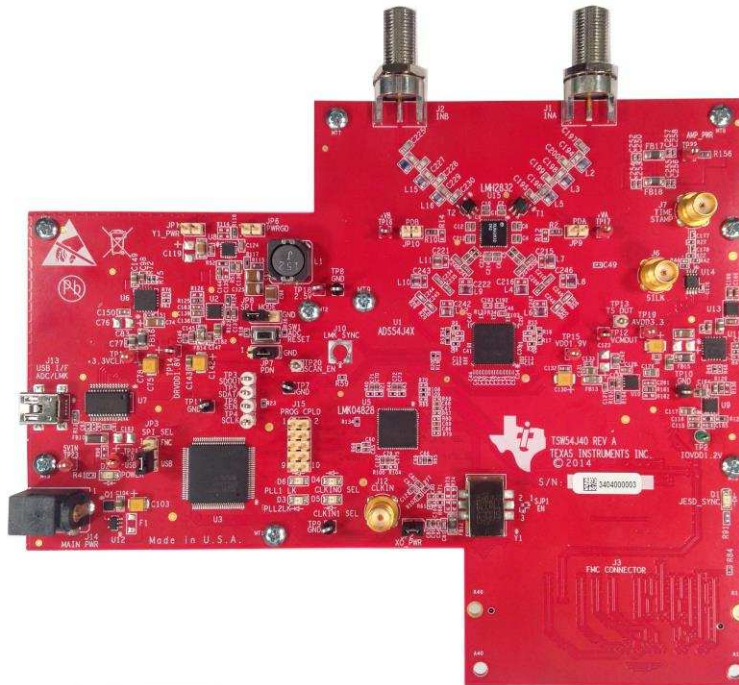


Figure 6. TIDA-01378 Board Image

3.2 Software

The TSW54Jxx graphical user interface (GUI) is used to configure the onboard DVGA (LMH2832) and the ADC (ADS54J40). The TSW54Jxx GUI software is similar to the ADS54J40 EVM GUI software except for an added tab to program the LMH2832 device gain. Follow the steps for programming the ADC and clock in the [ADS54J40EVM](#) user's guide [1].

The HSDCPro software is used to analyze the digital data captured by the TSW14J56 EVM. Refer to the [High Speed Data Converter Pro Software](#) tool folder for a detailed description on how to use the GUI.

4 Testing and Results

The following graphs and HSDCPro screenshots show the measured results using the TSW54J40 EVM. The hardware test setup for these results is shown in the preceding Figure 5. The typical conditions for the test are: a 5-V nominal wall-mount power supply, input clock sampling rate of 983.04 MSPS, nominal room temperature (25°C), and -1-dB full-scale input-signal level at the ADC. The two-tone tests are at -7-dB full-scale for each tone at the ADC centered at ± 1 MHz from the fundamental tone (f_0). The LMH2832 gain has been set to 27 dB for the test plots in Figure 9 through Figure 13.

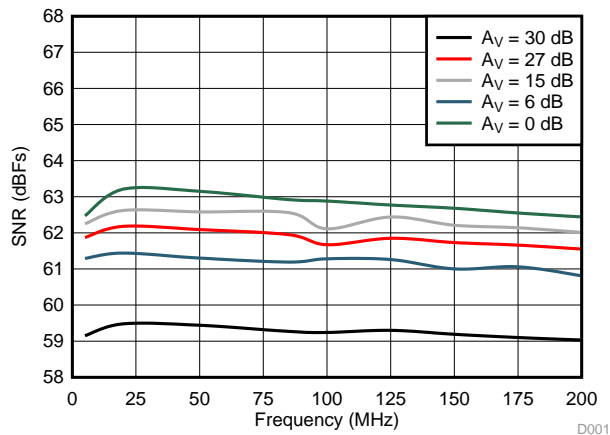


Figure 7. SNR versus Frequency

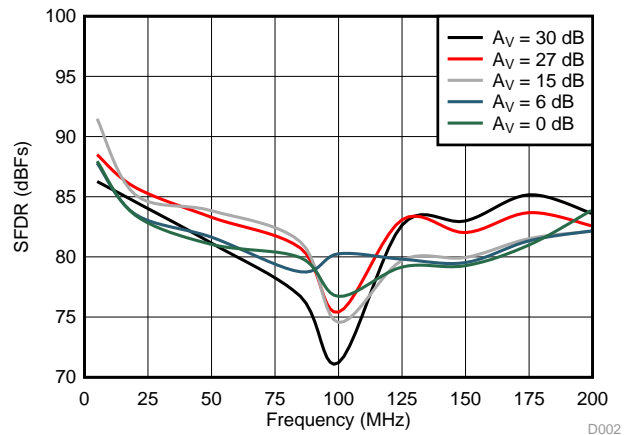


Figure 8. SFDR versus Frequency

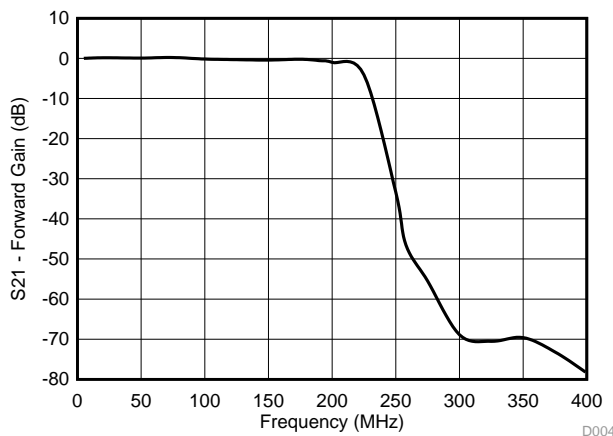


Figure 9. Typical Measured Complete Signal Frequency Response

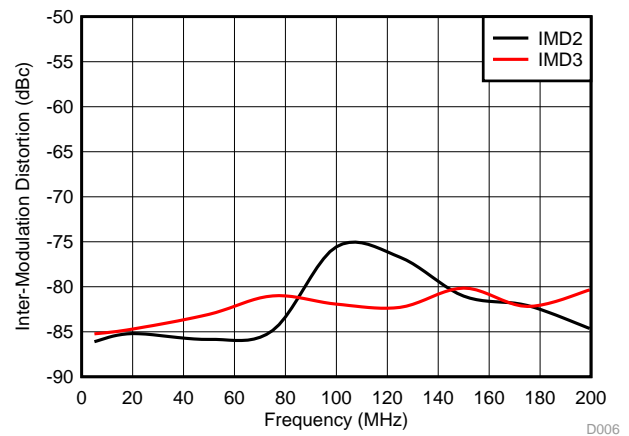


Figure 10. Two-Tone Intermodulation Distortion Products versus Frequency

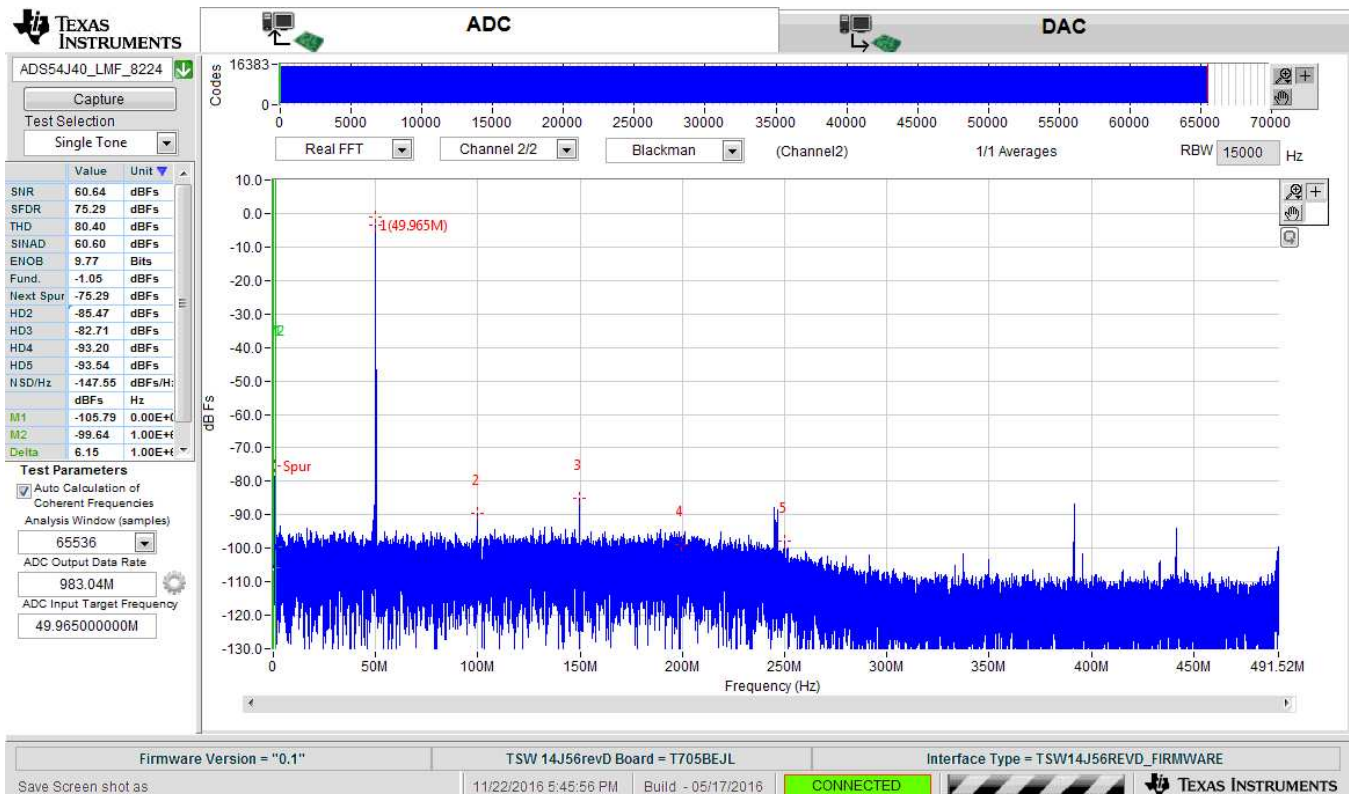


Figure 11. 50-MHz Input Frequency HSDCPro Capture

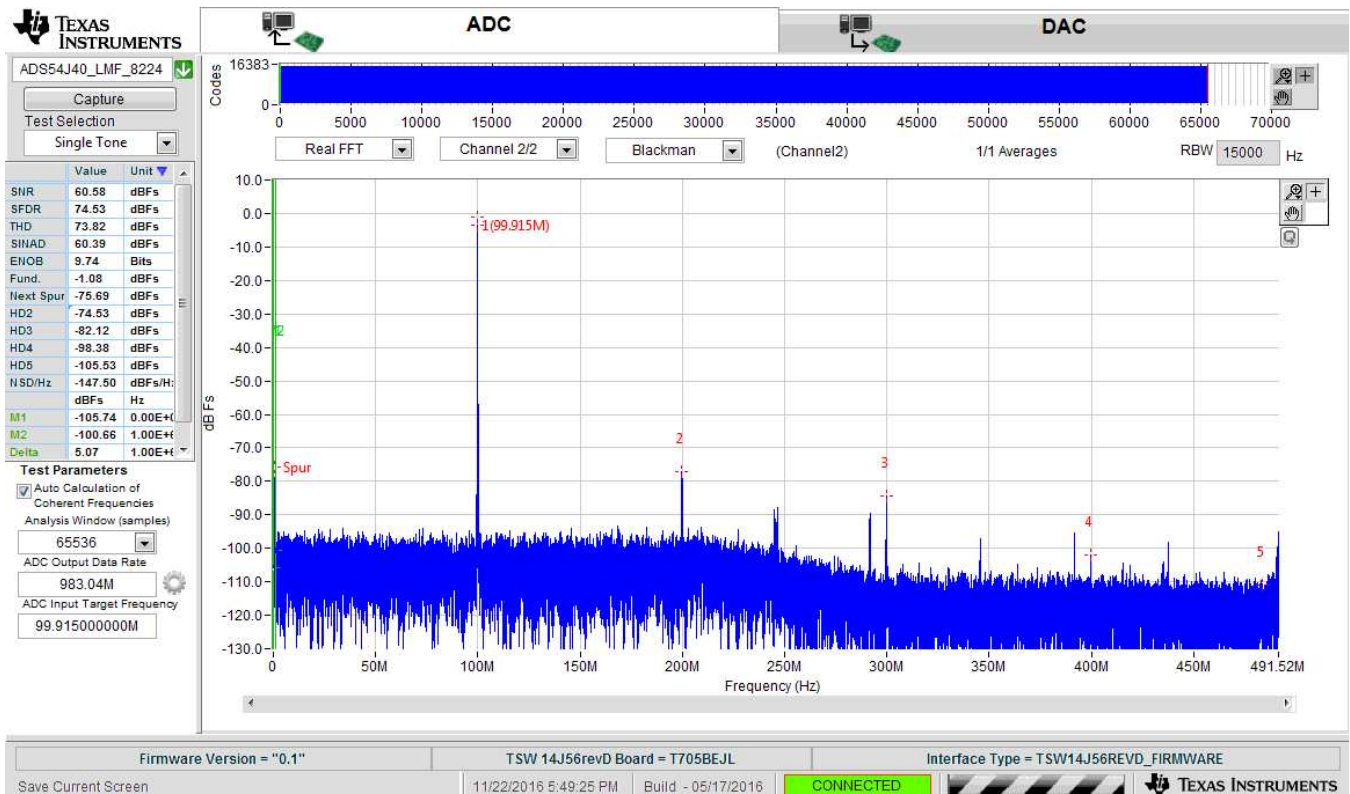


Figure 12. 100-MHz Input Frequency HSDCPro Capture

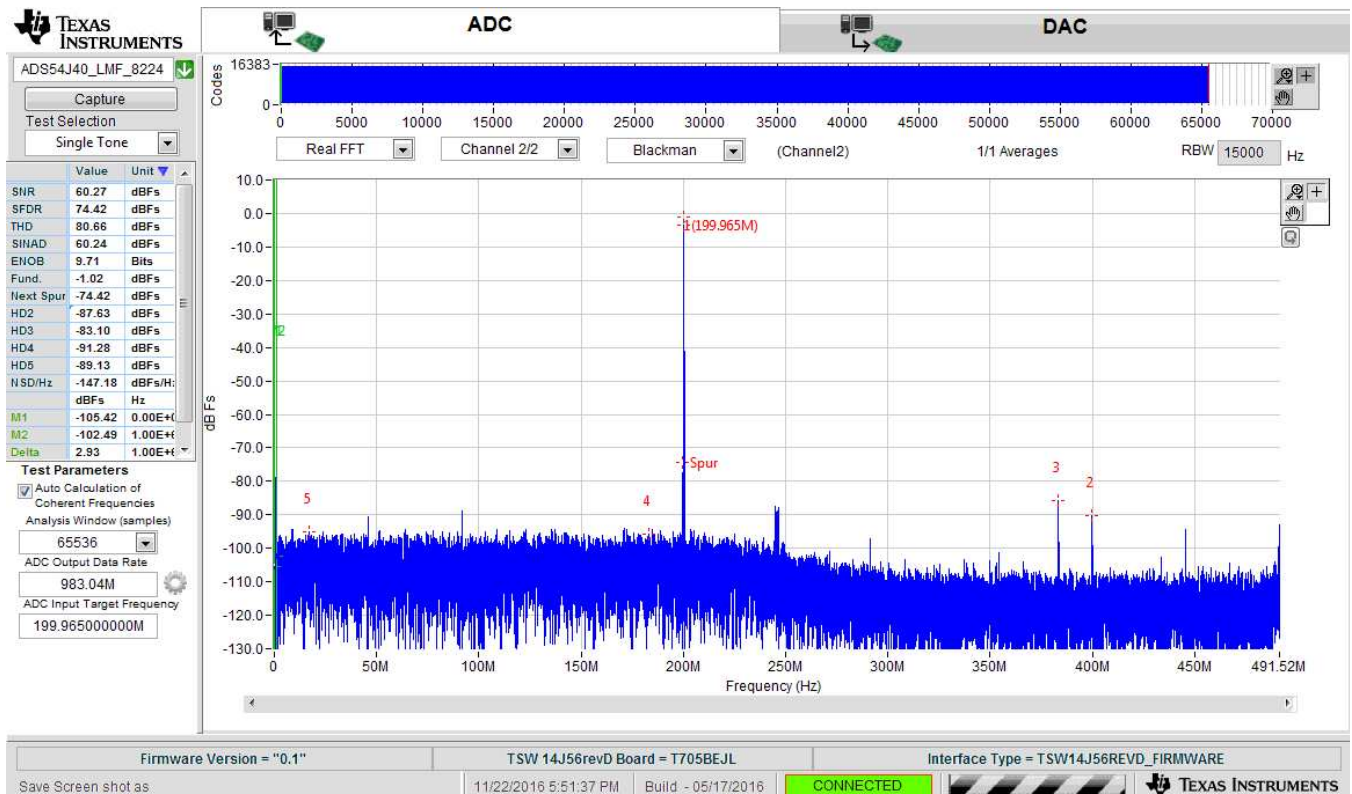


Figure 13. 200-MHz Input Frequency HSDCPro Capture

5 Design Files

5.1 Schematics

To download the schematics, see the design files at [TIDA-01378](#).

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01378](#).

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01378](#).

5.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01378](#).

5.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01378](#).

5.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01378](#).

6 Software Files

To download the software files, see the design files at [TIDA-01378](#).

7 Related Documentation

1. Texas Instruments, [ADS54J40EVM](#), ADS54J40EVM User's Guide (SLAU652)
2. Texas Instruments, [High-IF Receiver Reference Design Board](#), LMH6517 + ADC16DV160 + LMK04031B User's Guide (SNAU079)
3. CableLabs®, *DOCSIS 3.1 Physical Layer Specification*, Version I09 (June 02, 2016)
4. Zverev, Anatol I., *Handbook of Filter Synthesis*, Wiley-Interscience; Revised Edition (June 23, 2005)

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