TI Designs

75-V/10-A Protected Full-Bridge Power Stage Reference Design for Bipolar Stepper Drives

Design Overview

The TIDA-00210 uses two protected full-bridge power stages based on TIDA-00365 in parallel configuration. Each full-bridge operates nominal 75-V DC and 10-A_{RMS} phase current and features bipolar high-side current sensing leveraging a 100-V full-bridge gate driver SM72295 with integrated amplifiers and four 100-V NexFET power MOSFETs with ultra-low gate charge and small SON5x6 package with low thermal resistance. The power stage is fully protected against over-temperature, overcurrent, and short-circuit between the motor terminals and motor terminals to ground. Onboard power supplies provide 12-V and 3.3-V rails for the gate driver and signal chain. The host processor interface is a 3.3-V I/O to connect a host MCU like C2000™ Piccolo™ for stepper motor control.

Design Resources

TIDA-00210	Design Folder
SM72295	Product Folder
CSD19534Q5A	Product Folder
LM5018	Product Folder
LM317L	Product Folder
LM2901V	Product Folder
LMT89	Product Folder
ATL431	Product Folder
TIDA-00365	Design Folder
C2000 LaunchPad	Product Folder

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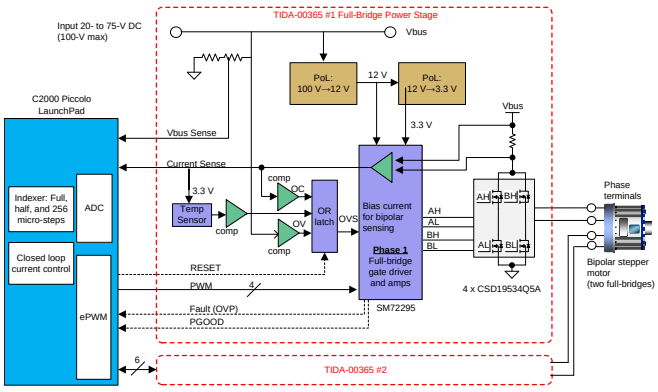
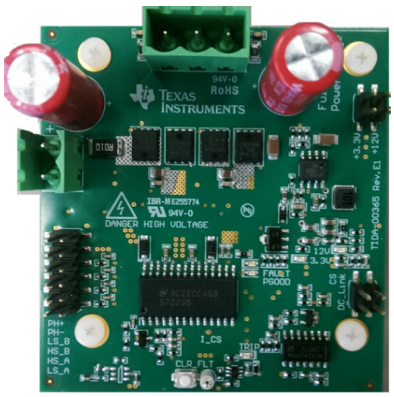
Design Features

- Protected Full-Bridge Power Stage With Input Voltage up to 100-V DC (75-V DC Nominal) and 10-A Phase Current
- BOM Reduction Using SM72295 100-V Full-Bridge Gate Driver With Integrated Amplifiers Used for High-Side Bipolar Phase Current Sensing, Supporting up to 256 Microsteps
- 95% Efficiency at 16-kHz PWM and Nominal Load With Very Low Switching Losses to Support Higher PWM Frequencies as Well. No Heatsink Required at 25°C Ambient and Nominal Load Due to TI NexFET Power MOSFET
- Full-Bridge Optimized for Low EMI Due to NexFET's Fast Turnon and Turnoff Switching Time, 25 ns With No Overshoot on Switch-Node Voltages
- Hardware Protected Against Over-Temperature, Overcurrent, and Short-Circuit Between Phase-to-Phase, Phase-to-GND, and UVLO
- Can Implement Custom Stepper Motor Control With 3.3-V Host Processor Interface

Featured Applications

- Bipolar Stepper Motors
- Brush DC Motors





1 System Description

Stepper motors are motion systems that allow very high precision in positioning. With their high power already at a low speed, their stall torque, and the possibility to divide the steps in microsteps, stepper motors can provide direct and precise motions in a small volume. The absence of mechanical commutation gives to these motors a long lifetime, which is usually given by the sleeves according to the load applied on the shaft.

The TIDA-00210 reference design is a cost effective protected power stage solution for bipolar stepper motors, allowing a high input voltage range up to 75-V nominal and a high output current with accurate high-side phase current sensing. A 3.3-V I/O interface is provided to connect to a host processor for closed-loop current and microstepping indexer.

This TI Design is based on two TIDA-00365 (Full-Bridge for DC Motor Driver) boards to drive a bipolar stepper motor.

With a full set of protections [undervoltage (UVP), overvoltage (OVP), overcurrent (OCP), short-circuit (SCP), and over-temperature (OTP)], the TIDA-00210 leverages the embedded high-side current sense amplifiers of the TI full-bridge gate driver SM72295 to achieve a robust and a cost effective full-bridge power stage to be used for stepper motor drives.

Figure 1 shows a simplified block diagram:

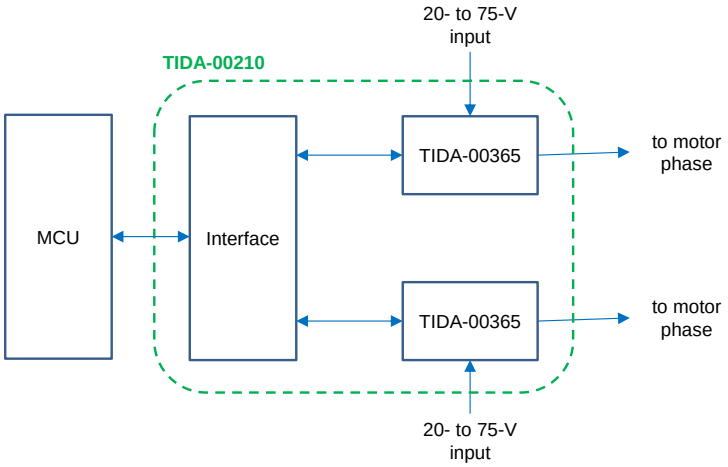


Figure 1. TIDA-00210 (Concept) Block Diagram

Figure 2 shows a more detailed block diagram of the TIDA-00365:

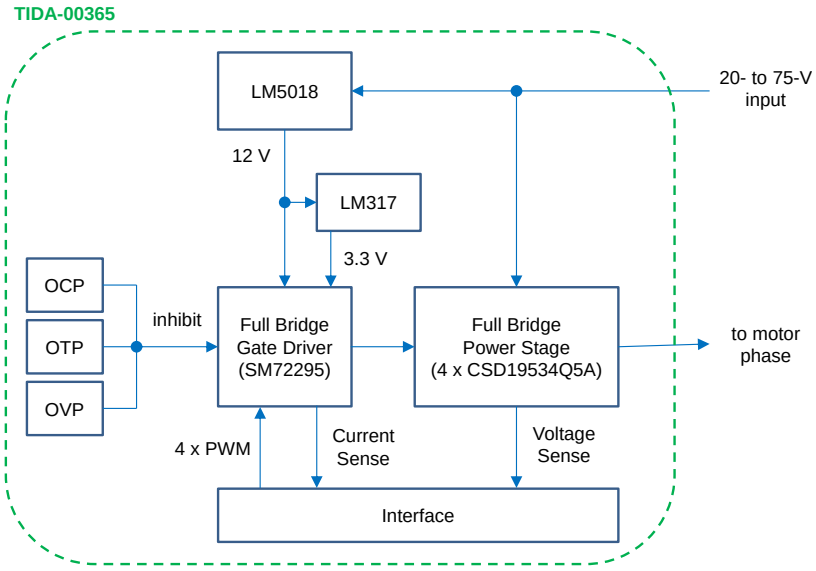


Figure 2. TIDA-00365 Block Diagram

The system consists of:

- A full-bridge power stage based on 4 × NexFet CSD19534Q5A
- A full-bridge gate driver (SM72295) with embedded current sense amplifier
- A DC/DC converter (LM5018) to provide the 12-V rail to supply the gate drive SM72295
- An LDO (LM317) to provide a 3.3-V rail to supply the logic of the gate drive SM72295
- Aa temperature sensor (LMT89)
- A barrier of comparators (LM2901) to detect a failure condition (OC, OT, or OV) and inhibit (disable) the gate drive in case of such an event
- A D-Latch FF (SN74LVC1G175) to keep the drive disabled when a fault is detected (a reset is required to clean the register and restore the normal working condition) to allow the host processor to take over control in such an event
- A connector with 3.3-V compatible interface to drive the hardware with a host processor like a C2000 or MSP430™ MCU

The signals on the interface are:

- Four digital inputs (dual complementary PWMs)
- Four analog outputs (phase current sense, DC-link voltage sense, two motor terminal voltage sense per Back Electro Motoric Force (BEMF) control)

  All these signals are 3.3-V rated and scaled.

  There are also other signals (not routed for simplicity) that can be provided to the MCU or from the MCU, such as:

  - PGOOD: a power good signal coming out from the gate drive SM72295 (open drain output)

    An LED is also present on the board to signal its status
  - FAULT: a fault indicator coming out from the gate drive SM72295 (open drain output), as consequence of any protection triggered. An LED is also present on the board to signal its status
  - RESET: a digital input from the MCU to the TIDA-00365 that clears the protection latch condition (the previous FAULT)

2 Key System Specifications

Table 1. TIDA-00210 System Specifications

PARAMETER	SPECIFICATIONS
Power stage	Dual TIDA-00365 full-bridge
DC input voltage range	20-V min, 75-V nom, 100-V max
Gate drive power supply rail	12 V ±5%, 50-mA max
Gate drive logic supply rail	3.3 V ±5%, 20-mA max
Output current per phase	10-A_{RMS} max
Current sense accuracy	Uncalibrated: < 5% Calibrated gain and offset error: < 1% (±10-A range), < 0.2% (within ±1-A range)
Protections	UVP, OCP, OTP, and OVI
OCP	15 A ±4%
OTP	120°C ±4%
Overvoltage indicator (OVI)	84 V ±3%
UVP	18-V raising UVLO, 16-V falling UVLO
Short-circuit protected against:	Phase to GND and phase to phase
PWM switching frequency	16-kHz nominal
Operating ambient temperature	–40°C to 85°C
Efficiency	95% (estimated)
Host processor interface signal level	3.3-V CMOS for digital input signals like PWM 0 to 3.3 V for analog output signals
TIDA-00365 PCB size	64 × 68.3 mm^2 / 4 layers / 2-oz copper

3 Block Diagram

A detailed block diagram of the TIDA-00210 block diagram is showed in Figure 3:

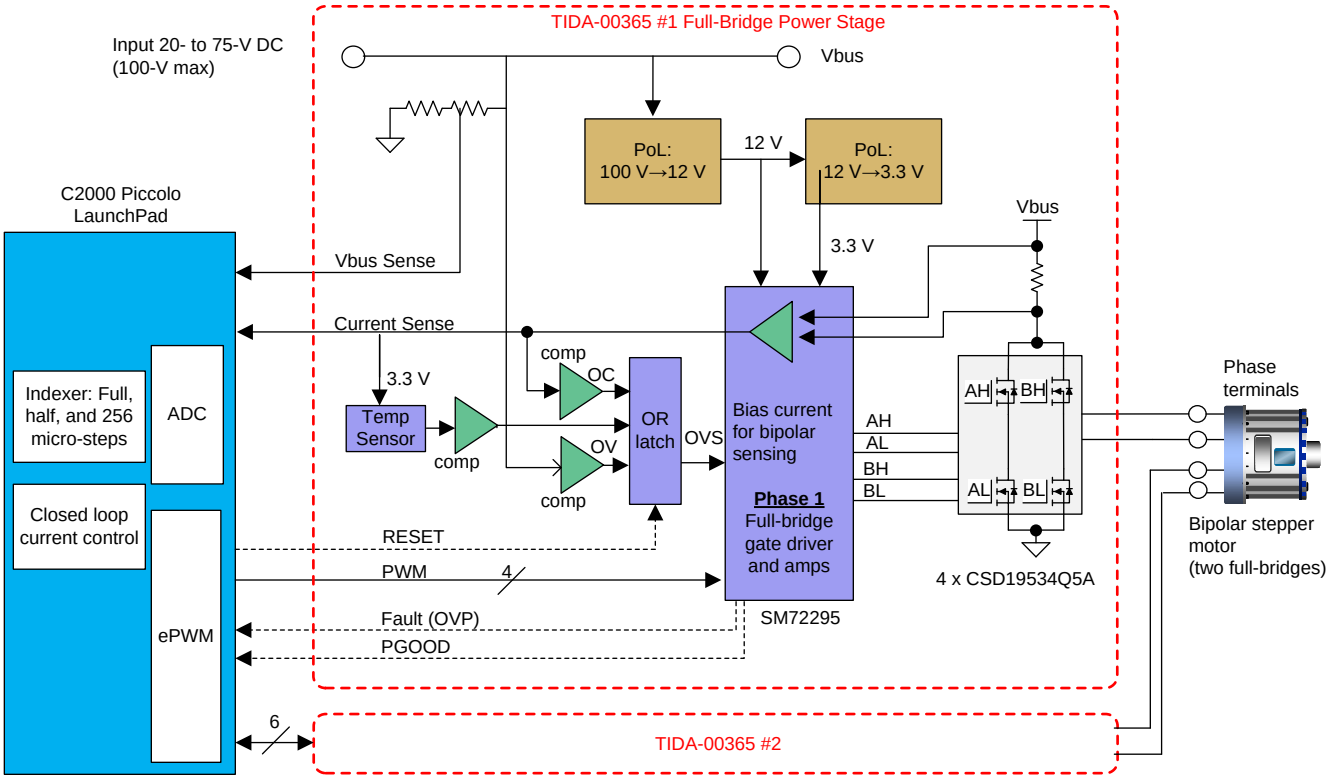


Figure 3. TIDA-00210 Block Diagram

3.1 Highlighted Products

3.1.1 SM72295

The SM72295 is designed to drive four discrete N type MOSFETs in a full-bridge configuration. The drivers provide 3 A of peak current for fast efficient switching and integrated high-speed bootstrap diodes. Current sensing is provided by two trans-conductance amplifiers with externally programmable gain and filtering to remove ripple current to provide average current information to the control circuit. The current sense amplifiers have buffered outputs available to provide a low impedance interface to an A/D converter if needed. An externally programmable input overvoltage comparator is also included to shut down all outputs. Undervoltage lockout (UVLO) with a PGOOD indicator prevents the drivers from operating if VCC is too low.

The main features of this device are:

- Integrated 100-V bootstrap diodes
- Bootstrap supply voltage range up to 115 V
- Independent high and low driver logic inputs
- Two current sense amplifiers with externally programmable gain and buffered outputs
- Programmable OVP

3.1.2 CSD19534Q5A

This 100-V, 12-mΩ, SON 5-mm×6-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

The main features of this device are:

- Ultra-low Q_g and Q_{gd}
- Very-low Q_{rr}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free

NOTE: Depending on the needs, a different FET could suit better for performance, like the CSD19532Q5A or CSD19533Q5A (pin-to-pin compatible). The CSD19534Q5A seems the best performing part for EMI (no voltage spikes, no ringing on the software nodes), offering the best balance between Q_{rr} of the body diode and R_{DSon}.

3.1.3 ATL431

The ATL431 is a three-terminal adjustable shunt regulator with specified thermal stability over applicable automotive, commercial, and industrial temperature ranges. The output voltage can be set to any value between the reference voltage (2.5 V or 1.25 V, depending on the version) and 36 V with two external resistors. Active output circuitry provides a very sharp turnon characteristic, making these devices excellent replacements for Zener diodes in many applications.

The ATL431 has a more than ×20 improvement cathode current range over its TL43x predecessor. It also is stable with a wider range of load capacitance types and values.

The ATL431 and ATL432 are the exact same parts but with different pinouts and order numbers. The ATL43x is offered in two grades, with initial tolerances (at 25°C) of 0.5% and 1% for the B and A grade, respectively. In addition, low output drifts versus temperature ensures good stability over the entire temperature range.

The ATL43xxI (industrial) devices are characterized for operation from –40°C to 85°C, and the ATL43xxQ (automotive) devices are characterized for operation from –40°C to 125°C.

The main features of this device are:

- Very-low operating current: $I_{KA(min)}$ = 35 μA (max)
- Internally compensated for stability: Stable with no capacitive load
- Very-low reference voltage tolerances at 25°C
- Typical temperature drift: 5 mV (I version) and 6 mV (Q version)
- Extended cathode current range: 35 μA to 100 mA

3.1.4 LM5018

The LM5018 is a 100-V, 300-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant-on-time (COT) control scheme employed in the LM5018 requires no loop compensation, provides excellent transient response, and enables very low step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high-voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers.

A peak current limit circuit protects against overload conditions. The UVLO circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply UVLO.

The main features of this device are:

- Wide 7.5-V to 100-V input range
- Integrated 300-mA high-side and low-side switches
- No bootstrap diode required
- COT control:
  - No loop compensation required
  - Ultra-fast transient response
- Nearly constant operating frequency
- Intelligent peak current limit
- Adjustable output voltage from 1.225 V with 2% accuracy
- Frequency adjustable to 1 MHz
- Adjustable UVLO

NOTE: Beside the LM5018, when higher or lower current is required, consider the pin-to-pin parts from the same family LM5017 (600 mA) or LM5019 (100 mA).

3.1.5 LM2901V

The LM2901V consists of four independent voltage comparators that are designed specifically to operate from a single supply or split supply over a wide range of voltages. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships; this is useful when using the comparators to implement the various protections.

The main features of this device are:

- Wide supply ranges
  - Single supply: 3 to 32 V
  - Dual supplies: ±1 to ±16 V
- Low supply-current drain independent of supply voltage: 0.8 mA typical
- Low input bias and offset parameters
  - Input offset voltage: 2 mV typical
  - Input offset current: 3 nA typical
  - Input bias current: 25 nA typical
- Internal frequency compensation
- Common-mode input voltage range includes ground
- Differential input voltage range equal to maximum-rated supply voltage
- Low output saturation voltage

3.1.6 LM317LIPK

The LM317LIPK fixed-output, low-dropout regulator offers exceptional, cost-effective performance for both portable and non-portable applications. Available in voltages of 1.8, 2.5, 2.8, 2.9, 3, 3.1, 3.3, 5, and 10 V, the device has an output tolerance of 1% for the A version (1.5% for the standard version) and is capable of delivering a 150-mA continuous load current. Standard regulator features such as OCP and OTP are included.

The main features of this device are:

- Tight output tolerance: 1% (A grade) or 1.5% (standard grade)
- Ultra-low dropout: 280 mV at full load of 150 mA, 7 mV at 1 mA
- Wide V_{IN} range: 16 V max
- Low I_Q: 850 μA at full load at 150 mA
- Shutdown current: 0.01 μA typ
- Low noise: 30 μV_{RMS} with 10-nF bypass capacitor
- Stable with low-ESR capacitors, including ceramic
- OCP and OTP
- High peak-current capability
- ESD protection exceeds JESD 22

The LM317L-N is available in a different package as well. The LM317L-N is available packaged in a standard, easy-to-use TO-92 transistor package.

NOTE: For a more cost effective solution, consider the LM317LIPK; however, the accuracy decreases from 1.5% to 5%. This could limit the applicability of the LM317LIPK versus the LP2985-33, when for example a 3.3 V ±5% is needed.

3.1.7 LMT89

The LMT89 is a precision analog output CMOS integrated-circuit temperature sensor that operates over a –55°C to 130°C temperature range. The power supply operating range is 2.4 to 5.5 V. The transfer function of the LMT89 is predominately linear, yet has a slight predictable parabolic curvature. When specified to a parabolic transfer function, the accuracy of the LMT89 is typically ±1.5°C at an ambient temperature of 30°C. The temperature error increases linearly and reaches a maximum of ±2.5°C at the temperature range extremes.

The quiescent current of the LMT89 is less than 10 μA. Therefore, self-heating is less than 0.02°C in still air. Shutdown capability for the LMT89 is intrinsic because its inherent low power consumption allows it to be powered directly from the output of many logic gates or does not necessitate shutdown at all.

The LMT89 is a cost-competitive alternative to thermistors.

The relationship between the output voltage and the sensed temperature (in Celsius) is:

$$V_{OUT} = 1.8639 - 1.15 \times 10^{-2} \times T - 3.88 \times 10^{-6} \times T^2 \approx 1.8639 - 1.15 \times 10^{-2} \times T \quad (1)$$

4 Hardware Design

The full system can be split into the following subsystems.

NOTE: Most of the dividers in the TIDA-00210 present two or more resistor in series because the 0402 package has a limited max voltage rating of 75 V.

4.1 Power Management

The specifications are 20- to 75-V DC input, V_{OUT1} = 12 V at 20 mA, and V_{OUT2} = 3.3 V at 15 mA, in which the 12 V is minded to supply the gate driver while the 3.3 V the signal conditioning and processor interface circuits.

A simplified block diagram of the power management solution is showed in Figure 4:

Figure 4. Power Management Solution Block Diagram

Because of the little current level, the 3.3 V could be simply achieved by using a common LDO like the LM317L (the most affordable option).

The supply for the driver (12 V at 20 mA) turns into the new spec 12 V at 35 mA because the load of the LDO directly applies to the input. Indeed, the driver switches at a nominal frequency of 16 kHz and having a peak current of 3 A the RMS value is very little.

Looking at the SM72295 datasheet (SNVS688), the consumption of the driver is around 3 mA (LS drivers) + 1 mA (HS drivers) = 4 mA; in addition, the gate charge has to be added, so assuming a rise/fall time of 50 ns and a 3-A peak current, the RMS value at a 16-kHz switching frequency is 50 ns × 3 A × 16 kHz × 4 FET drivers ≈ 4 mA, leading to a total current consumption of the SM72295 < 10 mA.

Because of the little current again a linear regulator could be used, in particular when the cost is key factor of the design: something like the TL783 is a valid choice. In this design anyway the efficiency is the key factor, so a SMPS is chosen instead: the LM5017/LM5018/LM5019 offer a valid selection pattern for wide V_{IN} and good price/performance ratio. The LM5018 is used to leave the flexibility to supply other 12-V rated devices, like a cooling fan.

In case of different needs, the LM5019 (100 mA) or the LM5017 (600 mA) could be replaced because all three parts are pin-to-pin compatible.

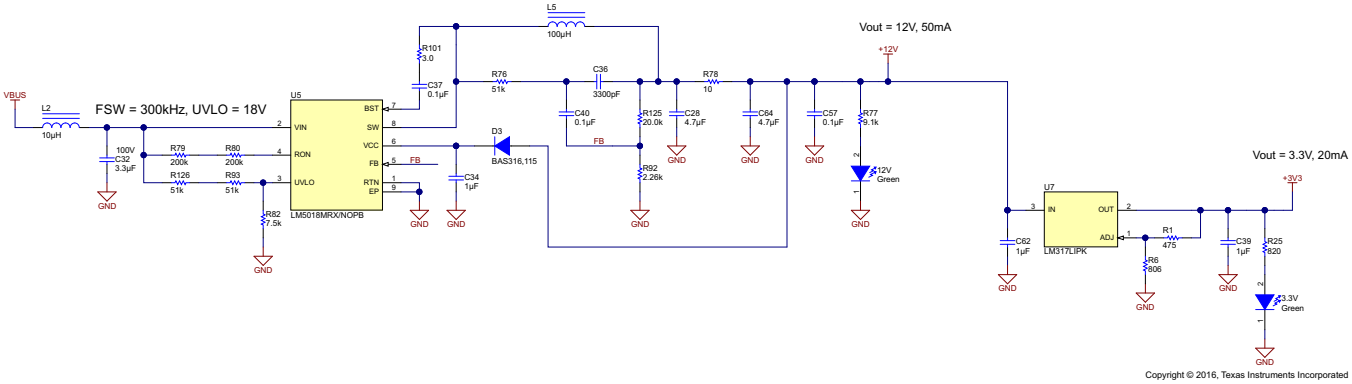


Figure 5. Schematic of Power Management Solution

To design the solution the spreadsheet associated to the part can be used. Also note that the output supplies and override the internal LDO for a better efficiency performance of the LM501x.

An input filter is also proved to reduce conducted EMI. Because of the big input cap needed for the motor driver power stage, the input inductor could be selected as small as possible.

The switching frequency could be also reduced down to 300-kHz maximum. UVLO is set at a 18-V input (rising) with a hysteresis of 2 V (meaning the turn off threshold is at a 16-V input). For more details, see the LM501x design guidelines (SNVS787).

4.2 Full Bridge

The full-bridge gate driver can be split into three main parts:

- The FET gate driver
- The FET bridges
- The current sense circuit

4.2.1 Full-Bridge Gate Drivers

The actual driver is implemented by using the SM72295, a general purpose four-switch (buck-boost) controller.

To supply these drivers, two rails are required: one for the actual power driver (12 V nominal) and one for the control logic (3.3 V or 5 V).

The expected current consumption on these rails is in the range of 10 mA for the 12 V (due to the fact that the typical switching frequency in motor drives application is 16 kHz, and the drivers embedded into the SM72295 can provide 3 A max, so the RMS current would be very low) and around 5 mA for the logic. This simply because the peak current of the driver is 3 A (in both direction) that, over a nominal switching frequency of 16 kHz, leads to an RMS gate drive current of a few milliamps.

Any SM72295 has two half-bridge drivers embedded: for the high-side driver section, two gate resistors are provided to provide flexibility to independently fine tune the switching time (on and off). A single gate resistor can be used to optimize BOM cost.

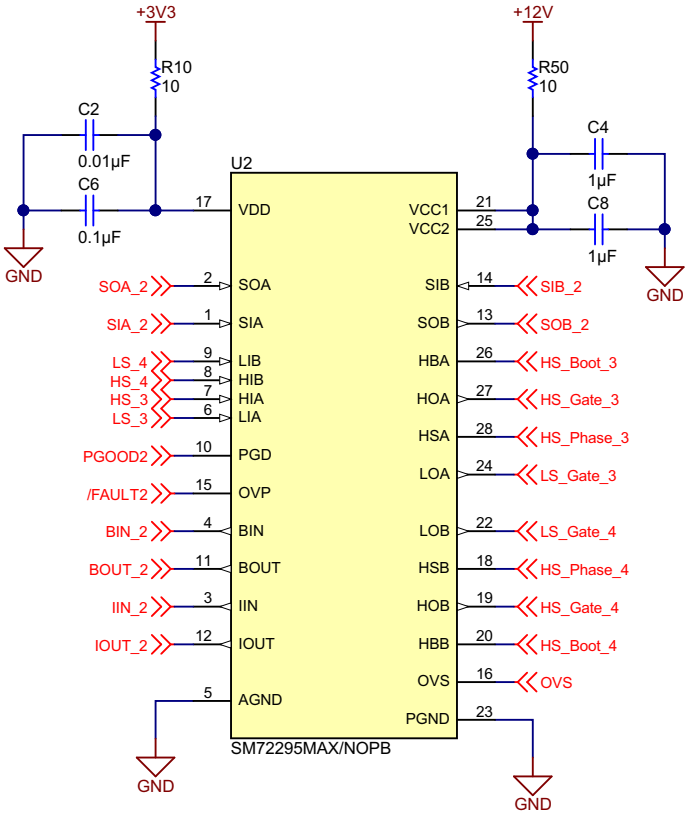


Figure 6. Schematic of Full-Bridge Gate Driver

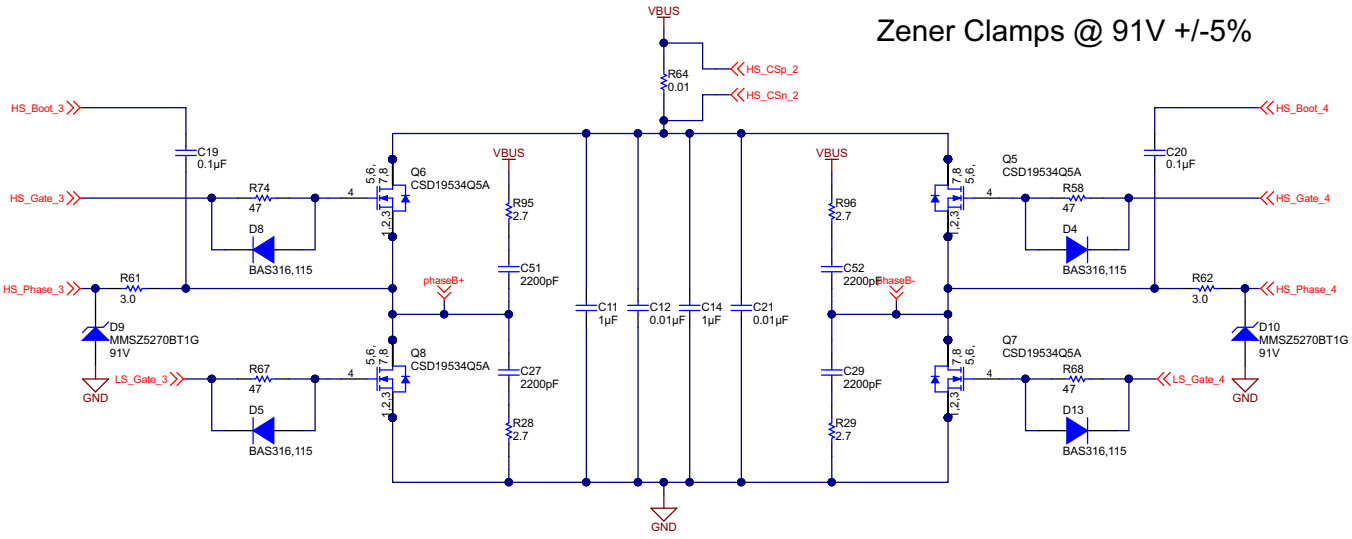


Figure 7. Schematic of Full-Bridge Power Stage

Because the TIDA-00365 on which the TIDA-00210 is based is 100 V rated, a Resistor-Zener network is provided on the switch nodes of the driver to protect it from overshoots and undershoots. Further, a 47R gate resistor is provided to reduce the EMI due to the too fast switching of the NexFET.

4.2.2 Full-Bridge (FET Selection Guide)

The biggest challenge of this design is selecting the best FET for the application, where "best" means the right one in terms of trade-off between price, size, and performance.

First of all, the total power losses for the FET have to be calculated; because of the symmetry of the system, losses in HS and LS MOSFETs can be considered identical in the first instance:

$$P_{LS} = P_{HS} = P_{Switching} + P_{Conduction} + P_{DeadTime} \quad (2)$$

$$P_{Switching} = V_{DS} \times I_{PHASE} \times F_{SW} \times \frac{\left(T_{Rise} + T_{Fail}\right)}{2} \quad (3)$$

$$P_{Conduction} = R_{DSon} \times I^2_{PHASE} \times D \quad (4)$$

$$P_{DeadTime} = V_F \times I_{PHASE} \times F_{SW} \times T_{DeadTime} \quad (5)$$

The two currents in the phases are 90° phase shifted. Depending on the motion control technique (if full-step or microstep driving), these currents are square or sine waves, respectively.

Regardless, for the thermal analysis purpose, consider the RMS values so that:

- Duty cycle = D = 50%
- I_{PHASE} = 10 A_{RMS}
- V_{DS} = 75 V (the maximum value is considered)
- f_{SW} = 16 kHz
- V_F = 1 V typ
- R_{DSon} = 23 mΩ at 125°C
- Dead time = 100 to 120 ns

And assuming a T_{RISE} = T_{FALL} = 30 ns (which is expected with a 47R gate resistor + CSD19534Q5A), then

$$P_{LS} = P_{HS} \approx 1.5 \text{ W} \quad (6)$$

NOTE: The device needs a proper heat sink or air cooling system to guarantee proper system functionality and to detect overcurrent (threshold at 15 A). Also, the SON5x6 package allows superior layout optimization versus other package options as well as spikes and ringing reduction on the switch nodes because of the smaller stray (parasitic) inductances.

See Section 7.3 for more details.

NOTE: Snubber networks are also provided with the design. To calculate the best value to achieve ringing reduction on the switch nodes, both high-side and low-side snubbers are provided. The best results are obtained with $C_{SNUBBER}$ = 2.2 nF and $R_{SNUBBER}$ = 2.7 Ω. See snubber design application notes for more details.

4.2.3 Current Sense Circuit

The SM72295 provides two embedded current sense amplifiers with a high common-mode voltage (100 V) to measure both input and output currents (because the driver itself is minded for a buck-boost converter).

These amplifiers are used to sense the HS current per phase; sensing the high-side current allows for a higher degree of protection since any potential short circuit could be detected by triggering the over-current protection.

Figure 8 shows the block diagram of the SM72295 integrated current sensing amplifiers:

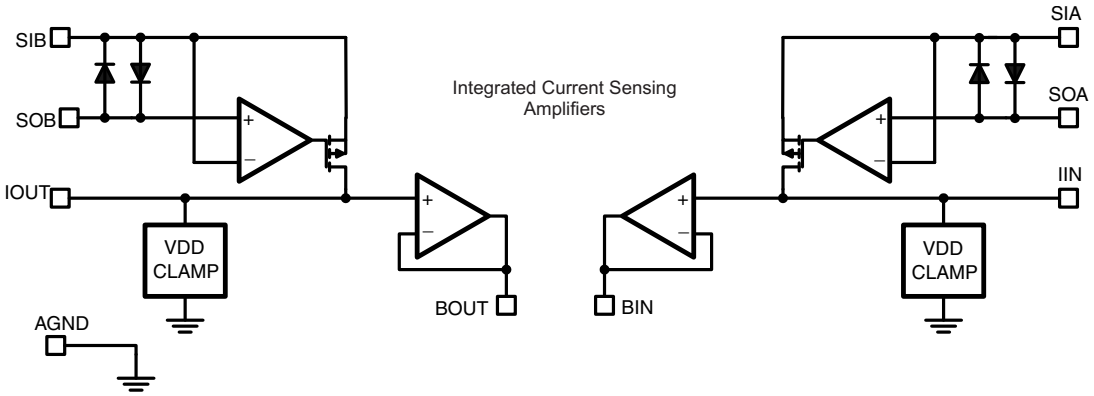


Figure 8. Block Diagram of SM72295 Integrated Current Sense Amplifiers

The pin descriptions for the integrated amplifiers and several guidelines are:

- SIA and SIB (inputs): Tie to the positive side of the sense resistor through an external gain programming resistor (RI). RI is in series with the SIA/SIB pin. Make sure the value of RI at the SIA/SIB pin is the same value at the SOA/SOB pin.
- SOA and SOB (inputs): Tie to the negative side of the sense resistor through an external gain programing resistor (RI). RI is in series with the SOA/SOB pin. Make sure the value of RI at the SOA/SOB pin is the same value at the SIA/SIB pin.
- IIN and IOUT: The output of the input current sense amplifier. Requires an external resistor to ground (RL). Do not connect this pin to anything else. The gain is RL/RI, where RI is the external resistor in series with both the SIA and SOA pin, and the SIB and SOB.
- BIN and BOUT (outputs): Buffered output of the IIN and IOUT, respectively. The voltage at BIN/BOUT is linear with the current through the sense resistor.
- The recommended differential voltage between current sense amplifier inputs (SIA to SOA, SIB to SOB) must be less ±0.5 V, with an absolute max differential voltage of ±0.8 V.
- The gain can be programmed to any value with the max output of the amplifier limited to VDD (3.3 V or 5 V). There is a VDD clamp at the current sense amplifier output BIN and BOUT.

Figure 9 shows the resistor connections of these pins and their implementation, according to Equation 7:

$$\left(R_{SENSE}\right) \times \left(I_{SENSE}\right) \times \left(\frac{R_L}{R_I}\right) = \text{Voltage at } B_{IN} \text{ and } B_{OUT} \text{ pins} \quad (7)$$

where the maximum voltage us clamped at VDD.

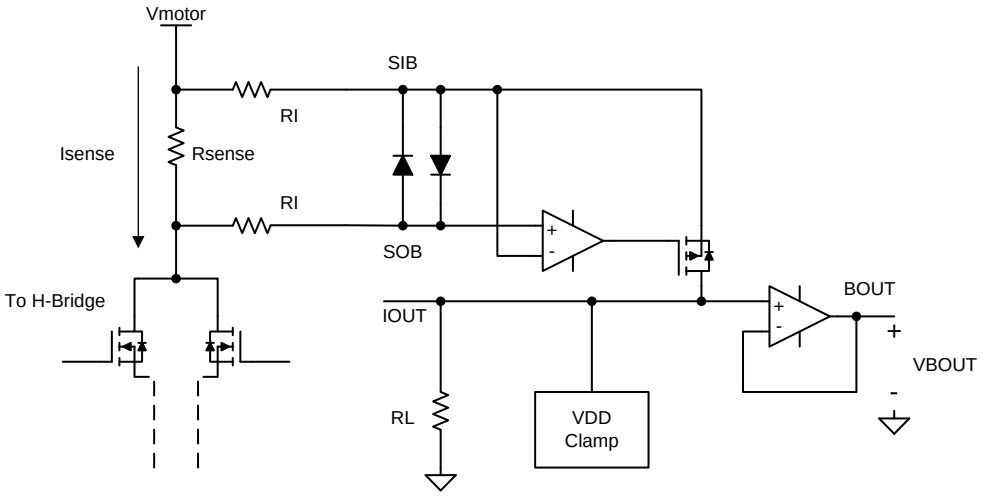


Figure 9. Current Sense Amplifier Connections

Now, these amplifiers are natively unipolar, meaning no bipolar current could be detected. In order to turn the unipolar current sense amplifiers into a powerful bipolar one, the two amplifiers are combined. To do this, a positive offset to the sensed current is applied.

Because this current offset has to be precise and stable over temperature, time, input voltage, and so on, a current mirror is recommended (preferably with a matched pair of transistors).

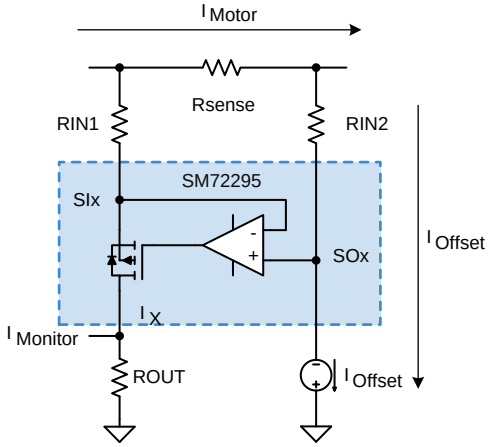


Figure 10. Current Offset to Turn an Unipolar Current Sense Amplifier Into a Bipolar One

4.2.3.1 Basic Solution

A basic solution consists in using a high-voltage rated matched pair of transistors (like the DMMT5551) to implement the current offset. However, this solution is quite expensive:

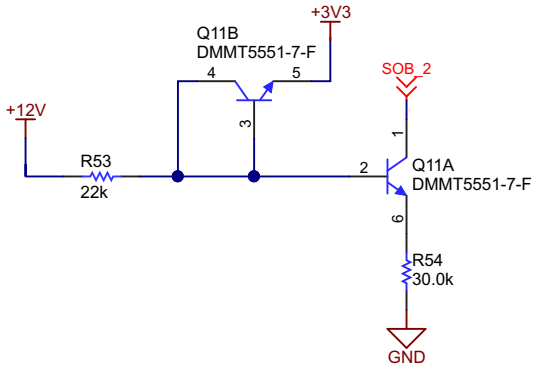


Figure 11. Current Offset Performed by a Matched Pair of Transistors

The matched pair of transistors, connected in an emitter follower configuration, work in a way that the 3.3 V is replicated on top of R54; in this way the

I_{OFFSET} = 3.3 V / R54

is applied to the current sense amplifier (SOBx pin). The precision and stability of this current depends mainly on the quality of the 3.3-V rail.

For more details about how this solution works, see the TIDA-00558 reference design (http://www.ti.com/tool/TIDA-00558).

4.2.3.2 Implement (Advanced) Solution

Another way to provide the current offset is to use the second (embedded) amplifier without extra external components (except for a voltage reference to guarantee the current offset is stable over temperature, and so on).

This solution has been implanted in the TIDA-00365 (and then in the TIDA-00210):

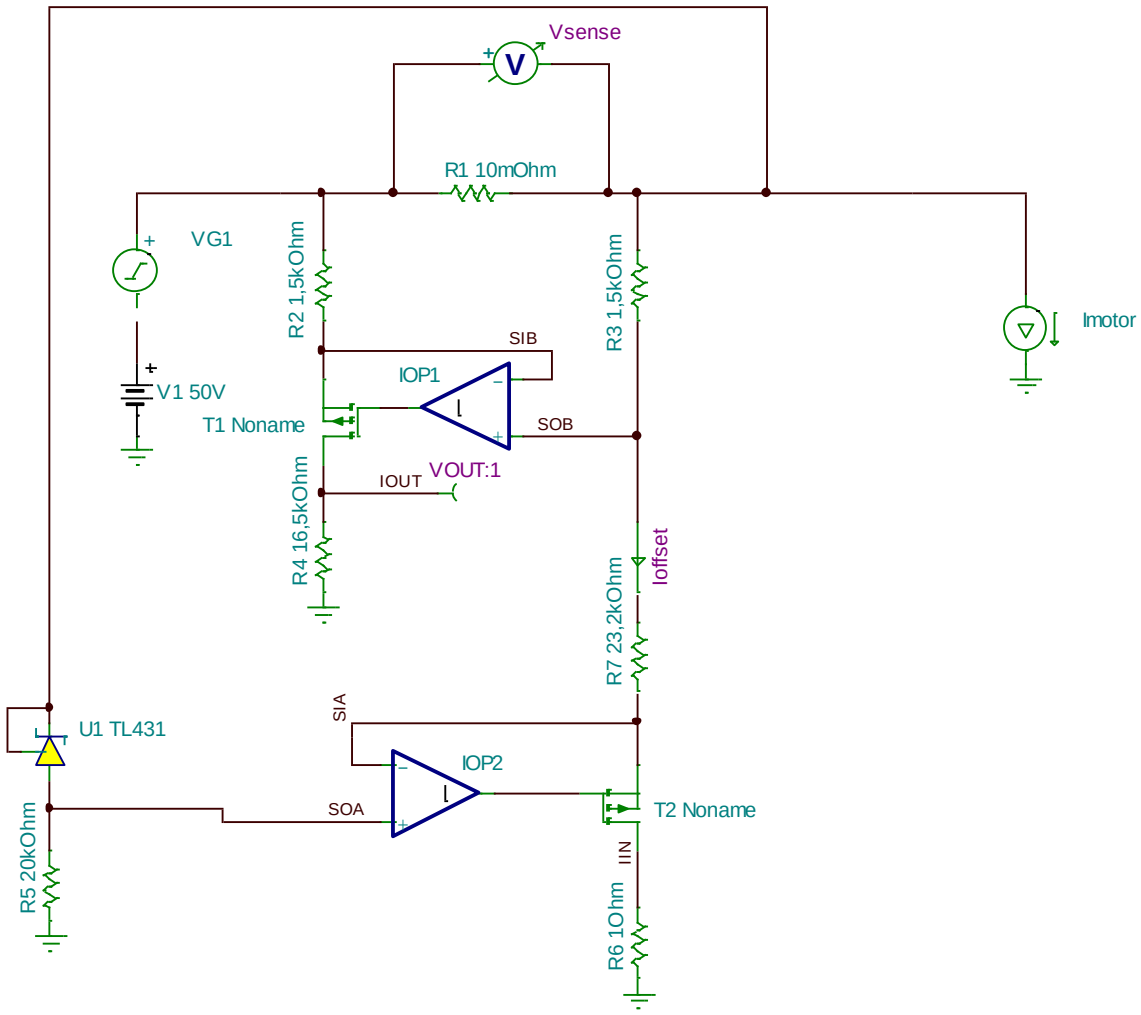


Figure 12. TI-TINA Simulation Circuit of Implement Current Sense Solution

In which:

- R1 is the sense resistor
- I_{MOTOR} is a generator that emulates the motor load
- IOP1 + T1 is one of the two unidirectional embedded current sense circuit of the SM72295
- R2, R3, and R4 are the external components to achieve the current sense, according to equation in Figure 10 (see RIN1, RIN2, and ROUT)
- IOP2 + T2 is the second embedded current sense configured as current sink to perform the I_{OFFSET}

  The loop of the IOP2 works in the way that the voltage of the reference TL431 is the same on the series R3+R7 while R5 is placed to guarantee the U1 is in regulation at any possible VIN. R6 has no actual purpose, except to have a signal referred to GND proportional to I_{OFFSET} (debug). The advantages of this solution (and also the one implemented in the TIDA-00210) versus the "state of the art" are:
  - No extra components are necessary (higher integration level)
  - Lower cost compared to a typical current sense solution
  - Higher protection level because the current sensing is performed on the high side of the bridge
  - Accuracy is guaranteed by the TL431, which offers the best performance in voltage reference at the lowest possible cost

Both the simulation model and the TIDA-00210 reference design have been set to have a 0- to 3.3-V voltage scale signal for a –15- to 15-A phase current, or:

$$V_{CURRENT\_SENSE} = V_{OFFSET} + Gain \times I_{MOTOR} = 1.65\ V + I_{MOTOR} \times \frac{1.65\ V}{15\ A} = 1.65\ V + 110\ m\Omega \times I_{MOTOR} \quad (8)$$

The following equations achieve the optimized current sense circuit:

- $V_{OUT} = (I_{MOTOR} \times R_{SENSE} + I_{OFFSET} \times R3) \times R4 / R2$
- $I_{OFFSET} = V_{REF} / (R3 + R8)$
- V_{REF} = 2.5 V (TL431)
- I_{OFFSET} and R3 are chosen in order to have
- $I_{OFFSET} \times R3 = I_{MOTOR\_MAX} \times R_{SENSE}$

while R4 and R2 defines the scale range of the output (0 to 3.3 V in this example is used for the simulation).

4.2.3.3 Step-by-Step Design of the Current Sensing Network

First of all, the current per phase is 10 A_{RMS} (by spec) at a 15-A peak (overcurrent). In order to guarantee a good signal-to-noise ratio over the sense resistor, a minimum value of 10 mΩ is recommended. In this design, the 10 mΩ, 3 W from BOURNS has been selected as the current sense resistor.

The output of the current sense circuit feeds the A/D converter, whose scale is 0 to 3.3 V, meaning that at 15 A the maximum output has to be 3.3 V. Indeed 10 A RMS means that $I_{MAX} = I_{RMS} \times \sqrt{2}$ when a microstepping mode with sinusoidal current is implemented.

With this information, decide where to set the positive offset; this depends on how big the negative current could be (generating mode) and directly affect the ENOB of the converter.

The simplest way is to set the offset at exact middle of the full-scale of the A/D, meaning that at a 0-A phase current the output of the current sense circuit has to be 1.65 V; under these conditions, the actual resolution is the A/D one minus 1 bit (half scale is actually used to sense the real current; that is, the positive one going to the mot Figure 10 or).

Now that R_{SENSE} and I_{PEAK} (overcurrent) are known, the rest of the network can be designed. Referring to Figure 10, the following equations are applied:

- $V_{OUT} = (I_{MOTOR} \times R_{SENSE} + I_{OFFSET} \times R3) \times R4 / R2$
- $I_{OFFSET} = V_{REF} / (R3 + R8)$
- V_{REF} = 2.5 V (TL431)
- I_{OFFSET} and R3 are chosen in order to have
- $I_{OFFSET} \times R3 = I_{MOTOR\_MAX} \times R_{SENSE}$

while R4 and R2 defines the scale range of the output (0 to 3.3 V in this example used for the simulation).

So,

- R_{SENSE} = 10 mΩ
- I_{MOTOR_MAX} = 15 A
- V_{REF} = 2.5 V
- I_{OFFSET} is set equal to 100 µA

$$100\,\mu \times R3 = 10\ m \times 15 \Rightarrow R3 = 1.5\ k\Omega \qquad 100\,\mu = \frac{2.5\ V}{(R3 + R8)} \Rightarrow R3 + R8 = 25\ L\Omega = 23.5\ k\Omega$$

(the closest commercial value 23.2K has been chosen)

R5 is chosen to guarantee the TL431 is in regulation all the time, that is the minimum cathode current equal to 1 mA. Having V_{IN} = 18 V, the maximum R5 value has to be (20 V – 2.5 V) / 1 mA = 17.5 kΩ. 16.4 kΩ has been selected for R5 while at max V_{IN} (OVP is triggered at a 84-V input), the current into R5 is around 5 mA.

The power rating of this resistor has to be then 16.4 kΩ × 5 mA × 5 mA = 410 mW, which cannot be achieved with a single resistor. For this purpose, two resistors at 8.2 kΩ 1206 5% 0.25-W rated connected in series have been selected.

And then the last one sets the gain to match the FSR of the A/D converter (0 to 3.3 V):

$$V_{OUT} = \left(I_{MOTOR} \times R_{SENSE} + I_{OFFSET} \times R3\right) \times \frac{R4}{R2} \tag{9}$$

And since the offset is placed in the middle $3.3\ V = 15\ A \times 10\ m\Omega \times 2 \times \frac{R4}{R2} \Rightarrow \frac{R4}{R2} = 11$

Selecting R2 = R3 = 1.5 kΩ → R4 = 16.5 kΩ

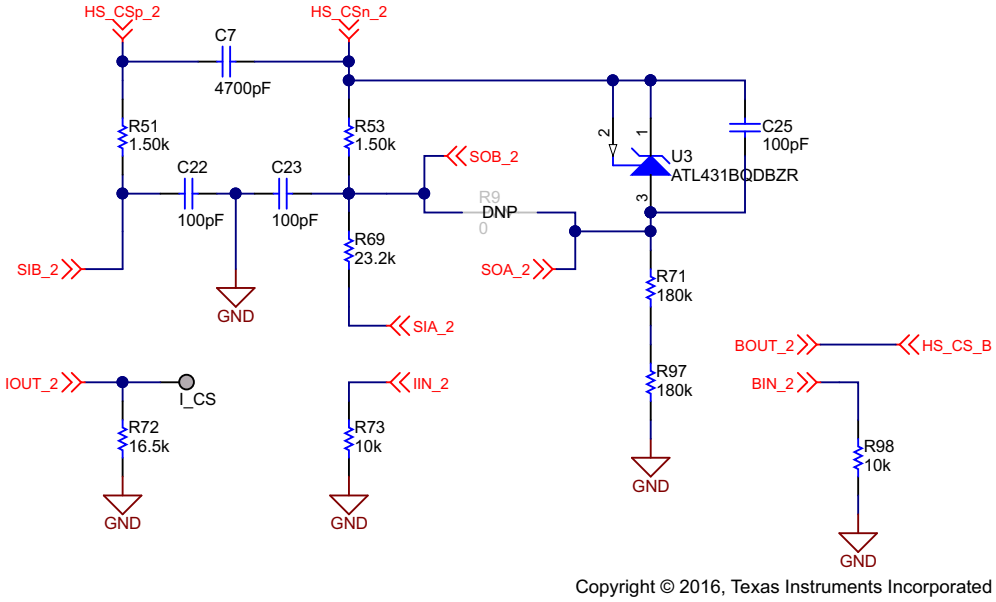


Figure 13. Schematic of Implementing the Bipolar High-Side Current Sense Solution

A few low-pass filters have been placed on the noisy nodes: also for this purpose, R2 and R3 are chosen for the same values.

Due to the excessive size (and cost) of the 2×1206 bias resistor for the TL431, a better choice is to use the ATL431, a bit more expensive than the sufficient TL431, but these require only a minimum current of 35 µA to guarantee regulation.

Assuming then a 50-µA bias current, the correspondent R5 becomes

$$R5 = \frac{(20\ V - 2.5\ V)}{50\ \mu A} = 350\ k\Omega \rightarrow 360\ k\Omega \tag{10}$$

360 kΩ has been chosen as the commercial value. Now at the maximum input voltage, the loss on the bias resistor is only

$$\text{Power over } R5 = \frac{(84 - 2.5\ V)^2}{360\ k\Omega} < 25\ mW \tag{11}$$

meaning a single 0402 resistor (63 mW rated) can do the job.

NOTE: The embedded current sense amplifiers have limited bandwidth (around 400 kHz). This bandwidth also means that the slew rate of the output signal is limited to roughly 0.8 to 1 V/µs, meaning to swing the full range would take 3 to 4 µs (half because the full range has been halved).

Having f_{SW} = 16 kHz leads to a period of about 62 µs. Both of these values provide the minimum duty cycle the system could manage (in closed loop current control), that is, 4/62 ≈ 6.4%, which becomes 3.2% when considering half of the full-range swing. Adding about a 1-µs conversion time of the A/D, it leads to a minimum duty cycle of 3/62 ≈ 4.8% (< % specified as system performances).

This is not a real limitation, since duty cycles < 25% leads to high current into the motor. The switching frequency can be increased to reduce phase current ripple up to eight times the nominal one.

4.3 Protections

Different protections are provided for this stepper driver:

- OCP
- OTP
- OVP
- UVLO

All these protections can be easily implemented using a general purpose open drain output comparator barrier and combining the outputs in wiring OR or AND fashion.

Note that overvoltage is not a real protection, but it basically disables the gate drive as the input voltage overcomes the 85-V nominal.

A constant and well-regulated voltage reference (as a threshold for the comparator) is provided by the most affordable TL431 while phase current, input voltage, and system temperature are scaled down with simple voltage dividers.

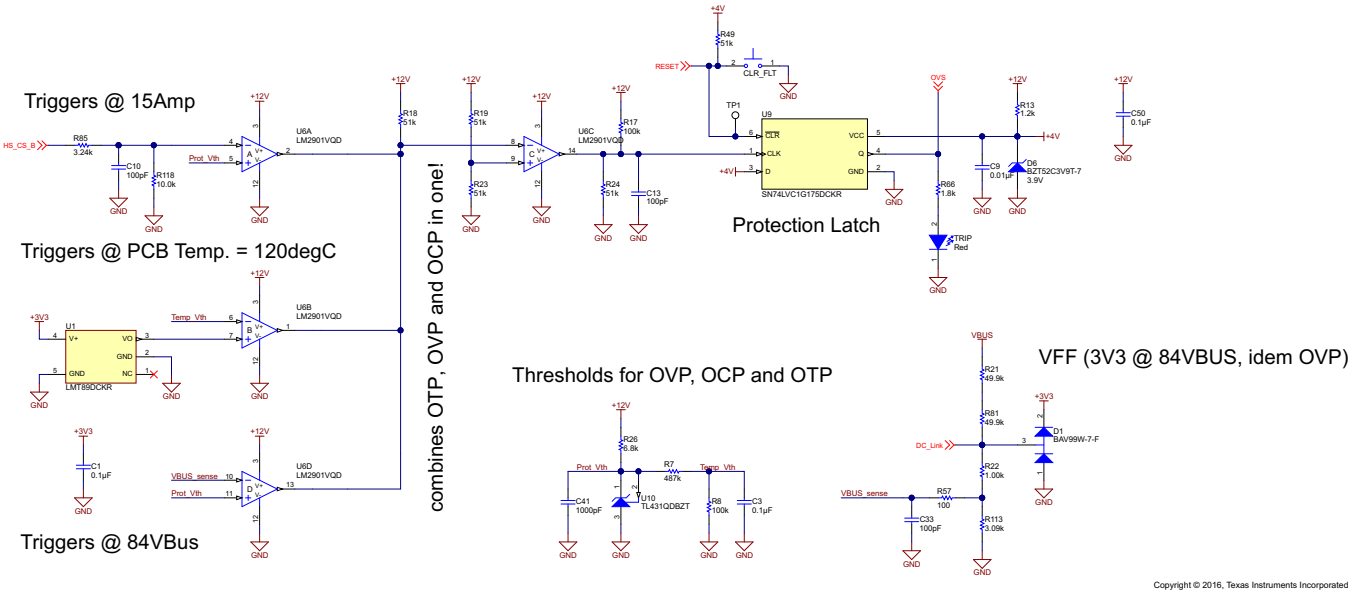


Figure 14. OVP, OCP, and OTP With Latch, Adjacent Thresholds, Voltage Feed Forward (VFF) Network

Finally, UVLO is performed by the LM5018. When the bus or input voltage drops below 18 V, then the LM5018 shuts down, removing the supply to the driver.

4.3.1 Step-by-Step Design

- *Overcurrent*
  The input signal is the HS_CS_x, a voltage signal from 0 to 3.3 V, for a phase current from –15 to 15 A. The comparator U6 compares the voltage HS_CS_x to the reference provided by using a TL431, equal to 2.5 V. This means that to trigger the OCP at 15 A, a voltage divider from 3.3 V to 2.5 V is needed:

$$3.3\ \text{V} \times \frac{\text{R19}}{(\text{R19} + \text{R84})} = 3.3\ \text{V} \times \frac{10\ \text{k}\Omega}{13.24\ \text{k}\Omega} = 2.492\ \text{V} \tag{12}$$

- *Over-temperature*
  The input signal is the output voltage of the precise temperature sensor LMT89. When
  $V_{OUT} \approx 1.8639 - 1.15 \times 10^{-2} \times T \approx 1.001\ \text{V}$
  and then the voltage divider R7 / R8 is used to scale down the 2.5-V reference down to 1 V to trigger the OTP. Act on this divider to move up or down the trip temperature of the protection.
  Setting the threshold at 110°C, for example, leads to

$$V_{OUT} \approx 1.8639 - 1.15 \times 10^{-2} \times T \approx 0.6\ \text{V} \approx 2.5\ \text{V} \times \frac{\text{R8}}{\text{R7} \times \text{R8}} \Rightarrow \text{R8} = 100\ \text{k}\Omega;\ \text{R7} = 316\ \text{k}\Omega$$

  Furthermore, to avoid false OTP tripping at the start-up, a delay is applied on the Temp_Vth signal (see Section 7.1 for details). In particular, C3 is chosen equal to 100 nF and R8 or R7 in the ballpark of tens—even hundreds—of kΩ, depending on the delay necessary to avoid a false OTP trip.

$$V_{OUT} = 1.8639 - 1.15 \times 10^{-2} \times T - 3.88 \times 10^{-6} \times T^2 = 1.8639 - 1.3800 - 0.0559 = 428\ \text{mV} \tag{13}$$

  For example, setting the threshold at 120°C leads to

$$428\ \text{mV} = 2.5\ \text{V} \times \frac{\text{R8}}{\text{R7} + \text{R8}} \Rightarrow \text{R8} = 100\ \text{k}\Omega;\ \text{R7} = 484\ \text{k}\Omega \tag{14}$$

- *Overvoltage indicator*
  OVP threshold is set at VBUS = 84 V through resistor dividers R21 to R113:

$$84\ \text{V} \times \frac{\text{R113}}{(\text{R21} + \text{R82} + \text{R22} + \text{R113})} = 84\ \text{V} \times \frac{3.09\ \text{k}\Omega}{(49.9\ \text{k}\Omega + 49.9\ \text{k}\Omega + 3.09\ \text{k}\Omega + 1\ \text{k}\Omega)}$$
$$= 2.498\ \text{V} \tag{15}$$

  On the same divider, the VBUS sense for the VFF feature is achieved. Indeed:

$$84\ \text{V} \times \frac{(\text{R113} + \text{R22})}{(\text{R21} + \text{R82} + \text{R22} + \text{R113})} = 84\ \text{V} \times \frac{4.09\ \text{k}\Omega}{(49.9\ \text{k}\Omega + 49.9\ \text{k}\Omega + 3.09\ \text{k}\Omega + 1\ \text{k}\Omega)}$$
$$= 3.307\ \text{V} \tag{16}$$

All the outputs of the comparators are OR-wired and feed the OVS pin of the drivers to turn them off. To add a latching feature on the protection (so that a power cycle needs to be performed to clear the protection latch), a D-Type Flip-Flop With Asynchronous Clear (the TI SN74LVC1G175) is adopted. 4 V is selected as the supply voltage of the flip-flop because the internal comparator on the OVS pin of the SM72295 drivers are clamped to VDD; the voltage on these pins has to be higher than VDD itself, meaning it is not recommended to use the 3.3-V rail to supply the flip-flop.

NOTE: The LM2901V is used as a comparator. It is one of the most affordable on the market and, because of that, not the fastest one. This also helps avoid triggering false protection conditions due to potential noise. Also, for the same reason, no hysteresis has been added to the comparator, but a latching protection is preferred.

4.4 3.3-V I/O Host Processor Interface

A host processor is needed to provide the right PWM sequence to the driver and then step the motor. A bunch of I/Os need to be connected to the two TIDA-00365 of which the TIDA-00210 is made; in particular:

- Eight digital inputs (PWMs) for the total eight FET of the two full-bridges (TIDA-00365 digital input, CMOS level)
- Eight analog outputs, four times any TIDA-00365 compiling the TIDA-00210, consisting in:
  - High-side currents in the phases of the stepper motor
  - DC-link voltage for the VFF function
  - Two phase terminal voltages for the BEMF analysis

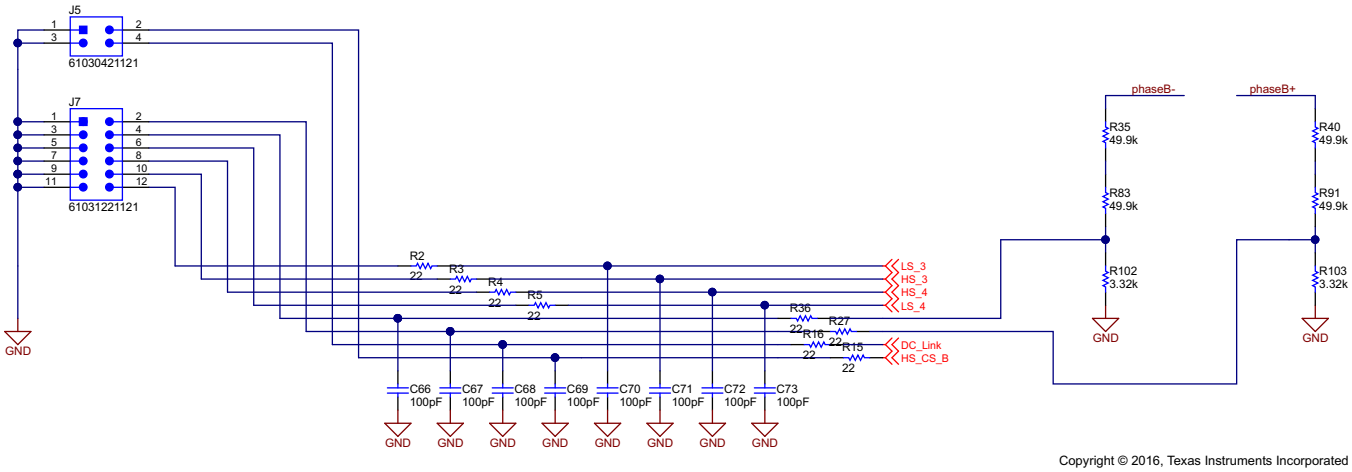


Figure 15. TIDA-00365 Interface and Switch-Nodes Voltage Sensing Network for BEMF Analysis

In Figure 15, the PH_X voltage is 3.3 V when switch node X voltage is equal to 100 V:

$$100\,\text{V} \times \frac{3.4\text{K}}{(49.9\text{K} + 49.9\text{K} + 3.4\text{K})} = 3.295\ \text{V}$$

A typical LP filter 22R/100 pF is applied on all the I/Os to limit the HF noise on these signals.

5 Getting Started

Figure 16 shows an overview of the board and its main functional areas.

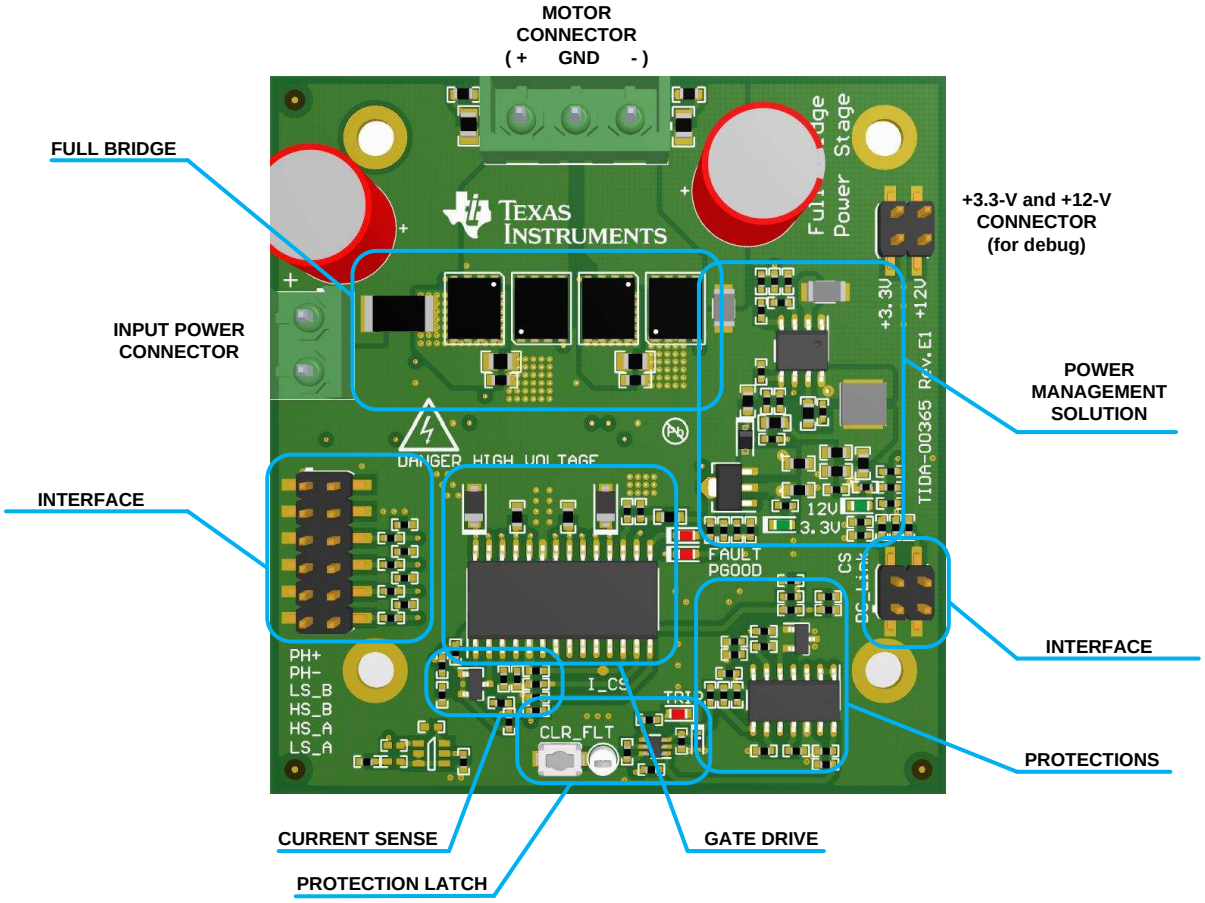


Figure 16. TIDA-00365 Functional Blocks (Top View)

In order to implement a bipolar stepper motor driver, two boards of the TIDA-00365 have to be connected in parallel. In particular, all the IOs are decoupled and independent, except for the GND level that has to be shared between the two TIDA-00365 boards and the FPGA / MCU used to perform the motion control.

Furthermore, note that the four mounting holes have been placed in a relative position to match a potential heat-sink (the Wakefield Engineering 518-95AB) that could be connected on the bottom in case of thermal problems.

A more detailed description of the pin assignment on the interface connectors is showed in Figure 17:

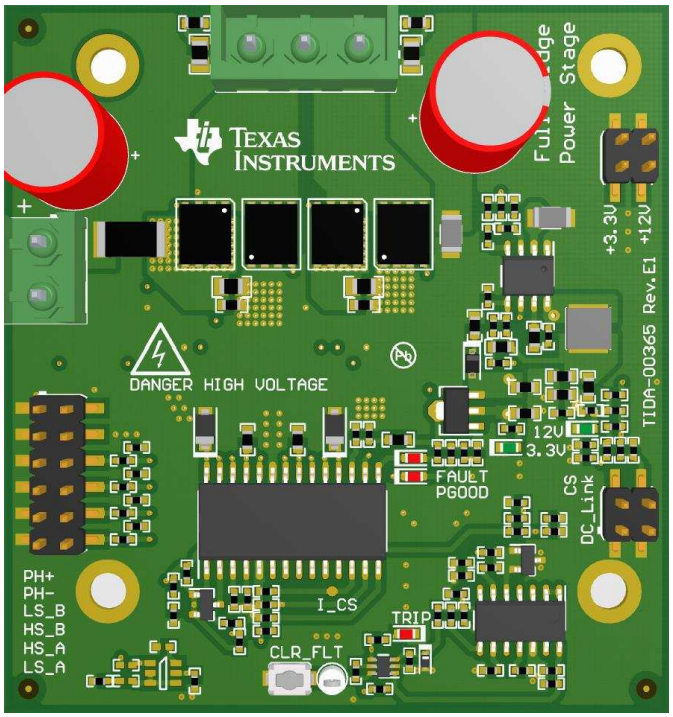


Figure 17. Interface Connector Pin Map

6 Test Results

The test results are illustrated in this section, organized in according with the main functions of the TIDA-00210, as in Section 4.

Table 2 lists the equipment for the test setup:

Table 2. Test Equipment for TIDA-00210

TEST EQUIPMENT	PART NUMBER
Low-speed oscilloscope (suitable for power management tests)	Tektronix TDS2024B
High-speed oscilloscope (suitable for analog signal tests)	Tektronix TDS784C
Adjustable SMPS	Knuerr-Heinzinger Polaris 125-5
True RMS multimeter	Fluke 179
Differential probes	Tektronix P6630
Single ended probes (×2)	Tektronix P6139A
Current probe	Tektronix TCPA300
Current probe	PR30 LEM
Thermal camera	Fluke TI40
Full-bridge driver for DC motor (×2)	TIDA-00365
MCU	C2000 LaunchPad™
Bipolar stepper motor	Bipolar Stepper 42Y312S-LW8 (Anaheim Automation)

Figure 18 shows the setup used for the testing session:

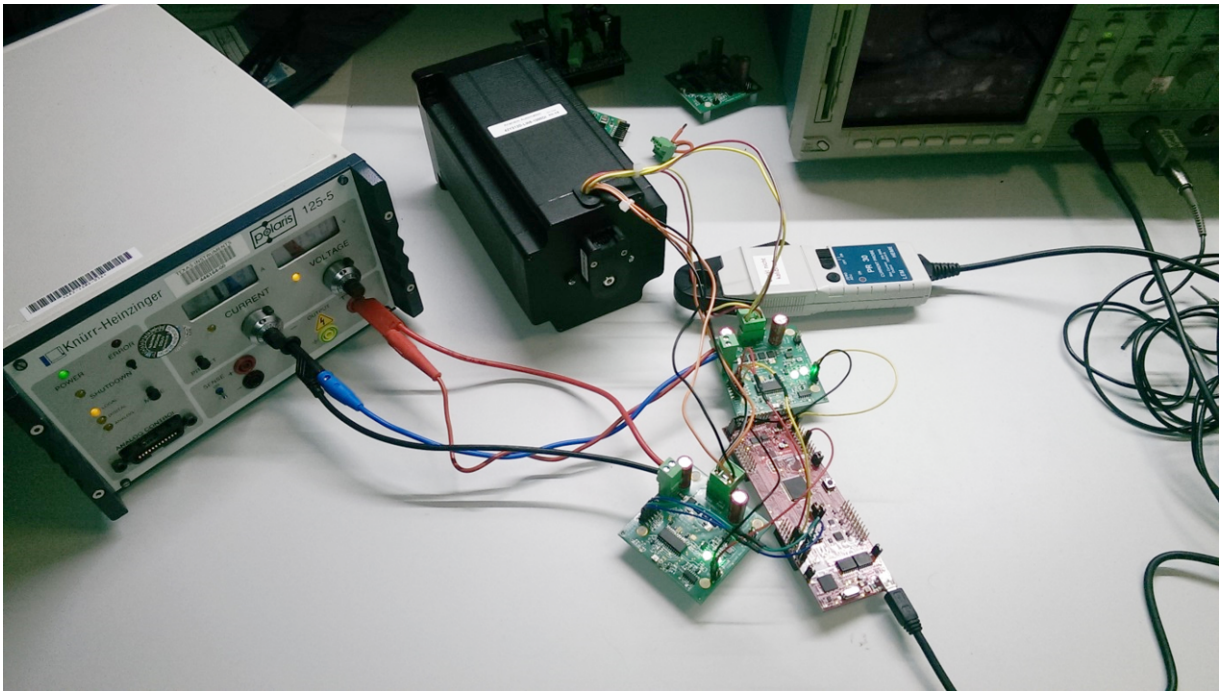


Figure 18. TIDA-00210 Test Setup

6.1 Power Management

A minimum set of tests on the power management solution has been performed. In particular, the performance of LM5018 can be evaluated by looking at its user's guide (SNVA666).

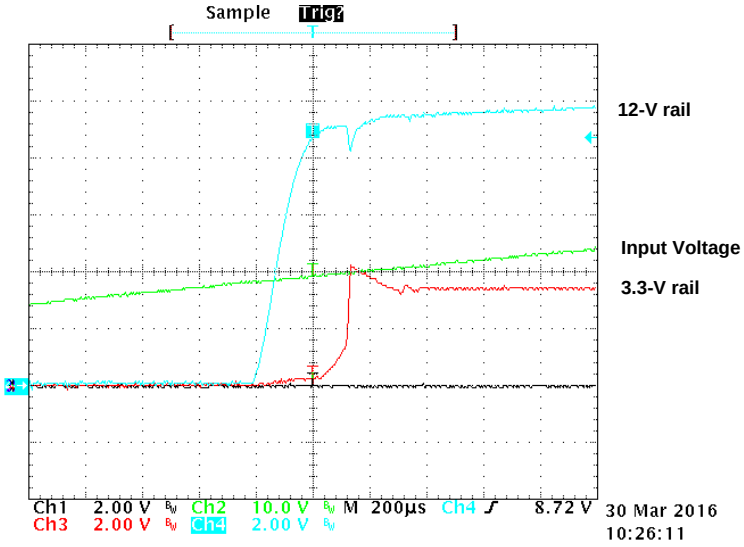


Figure 19. Power Up at 50-V Input (CH2 = V_{IN}, CH4 = 12-V Rail, CH3 = 3.3-V Rail, CH1 = Motor Terminal)

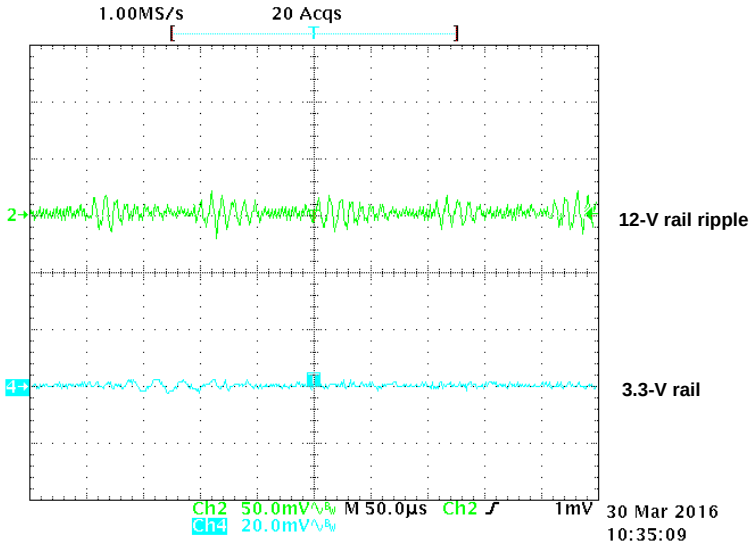


Figure 20. Ripple at 50-V Input (CH4 = 3.3-V Rail, CH2 = 12-V Rail)

Line and load regulations show that the 3.3 V and 12 nV are well regulated at all times, that is, in the range of nominal voltage ±5% consumption on both rails is below 10 mA.

6.2 Full-Bridge Power Stage

6.2.1 Test Setup

The InstaSPIN-MOTION LaunchPad with the TMS320M28069M was used generate the complementary PWM (hard-chopping) for each of the dual TIDA-00365 full-bridge power stages and measure each of the phase currents simultaneously. A closed-loop current control for each of the two phases was implemented as well. Figure 21 shows the corresponding connections.

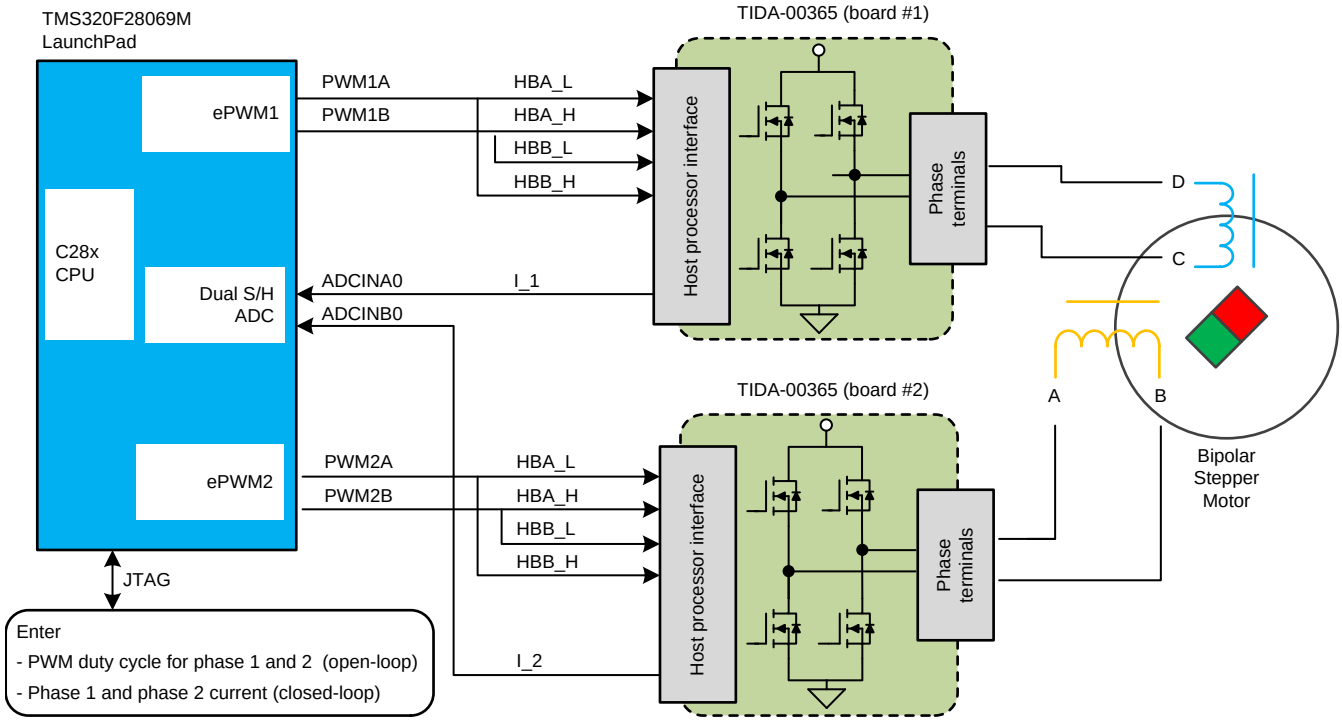


Figure 21. InstaSPIN-MOTION LaunchPad Connection to Dual TIDA-00365 and Bipolar Stepper Motors

The TMS320F28069M was configured as follows:

- PWM1A/PWM1B: Complementary active high symmetric PWM with a 16-kHz period and 120-ns dead-band for both rising and falling edge delay
- PWM2A/PWM2B: Complementary active high symmetric PWM with a 16-kHz period and 120-ns dead-band for both rising and falling edge delay. Phase synchronized to PWM1
- Both phase currents were sampled at 16 kHz at the center of the PWM cycle, when there is no switching
- Dual PI controllers with anti-reset windup for closed-loop phase current control of each phase
- 1/256 microstepping indexer

6.2.2 Full-Bridge Driver

Note that the phase current in the following test pictures has been measured using a current sense probe with voltage output and a trans-impedance gain of 1 V/10 A (ideal).

If not otherwise specified, all the tests have been performed at a 75-V input, 10-A output.

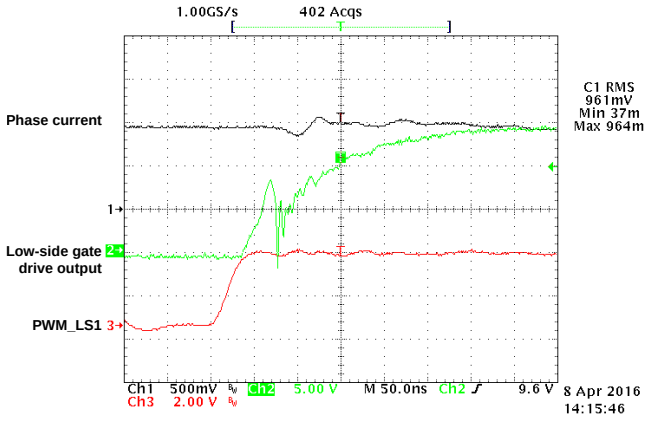


Figure 22. CH2 = Low-Side Gate Drive Output, CH3 = PWM_LS1, CH1 = Phase Current

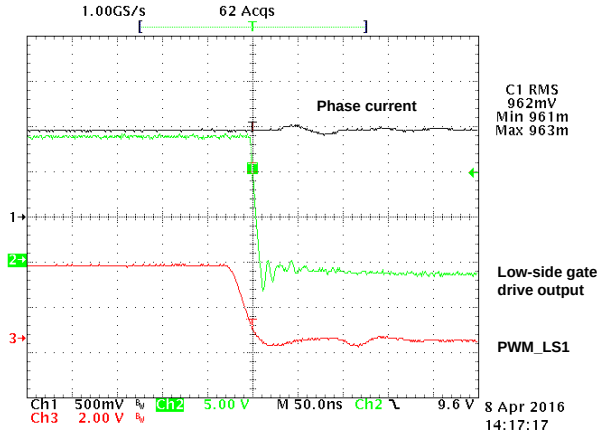


Figure 23. CH2 = Low-Side Gate Drive Output, CH3 = PWM_LS1, CH1 = Phase Current

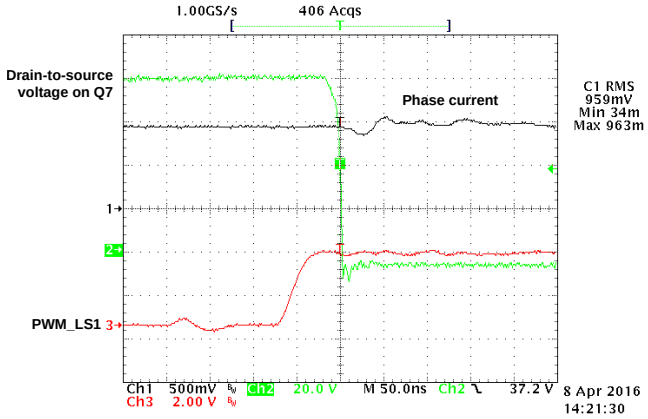


Figure 24. CH2 = Drain-to-Source Voltage of Q7, CH3 = PWM_LS1, CH1 = Phase Current

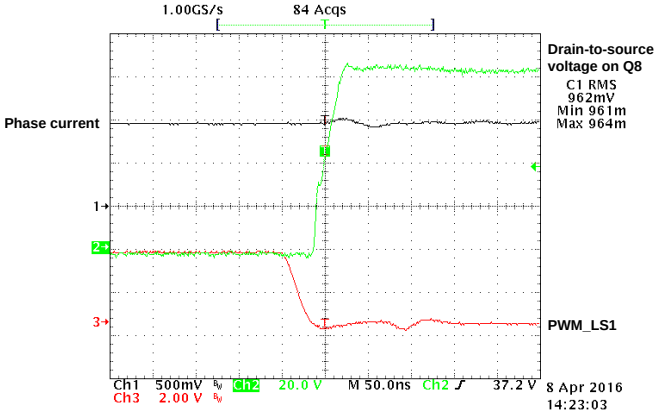


Figure 25. CH2 = Drain-to-Source Voltage of Q8, CH3 = PWM_LS1, CH1 = Phase Current

Figure 22 through Figure 25 clearly show the Miller cap effect on the resulting gate-to-source and drain-to-source voltage of the FETs.

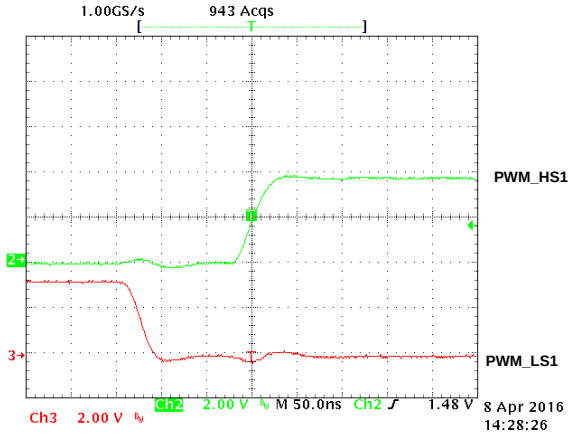


Figure 26. Dead Band Measurement (Falling PWM_LS1, Rising PWM_HS1)

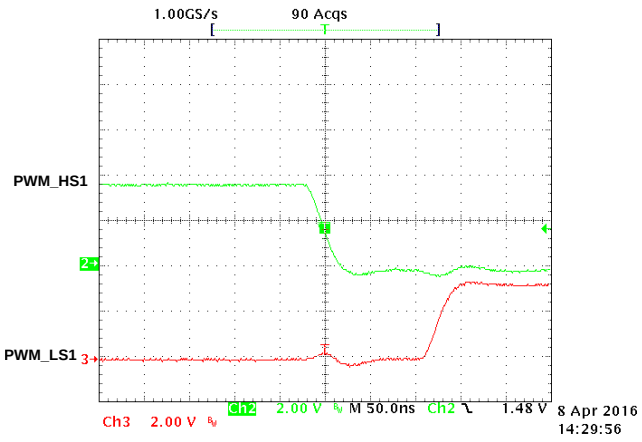


Figure 27. Dead Band Measurement (Falling PWM_HS1, Rising PWM_LS1)

6.2.2.1 (Differential) Phase Voltages versus Phase Current at 75 V, 10 A

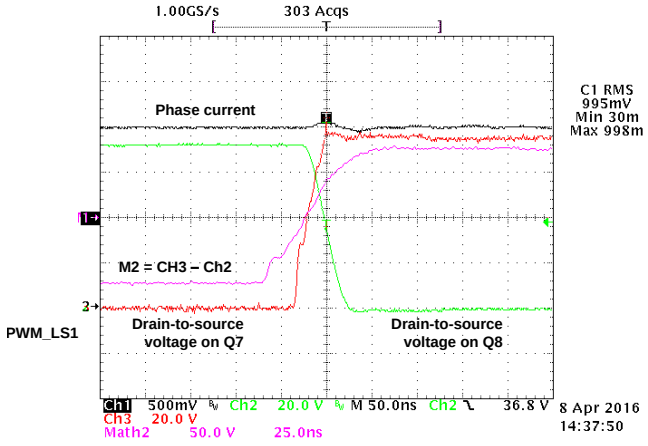


Figure 28. CH2 = Drain-to-Source Voltage of Q8, CH3 = Drain-to-Source Voltage of Q7, CH1 = Phase Current (Black), M2 = CH3 – CH2

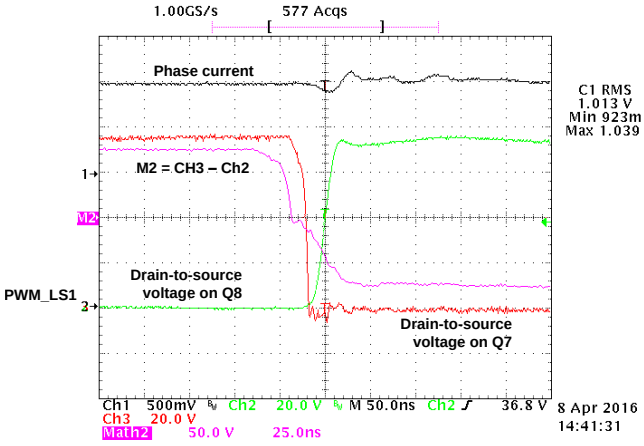


Figure 29. CH2 = Drain-to-Source Voltage of Q8, CH3 = Drain-to-Source Voltage of Q7, CH1 = Phase Current (Black), M2 = CH3 – CH2

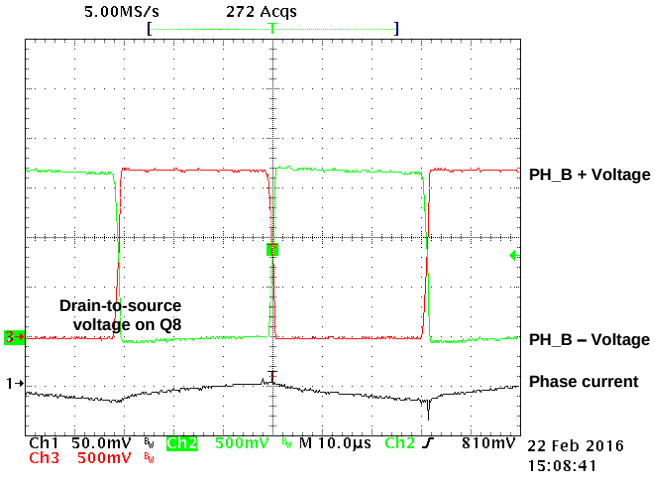


Figure 30. CH2 = PH_B+ Voltage, CH3 = PH_B– Voltage, CH1 = Phase Current (0-A DC), Input Voltage at 50 V

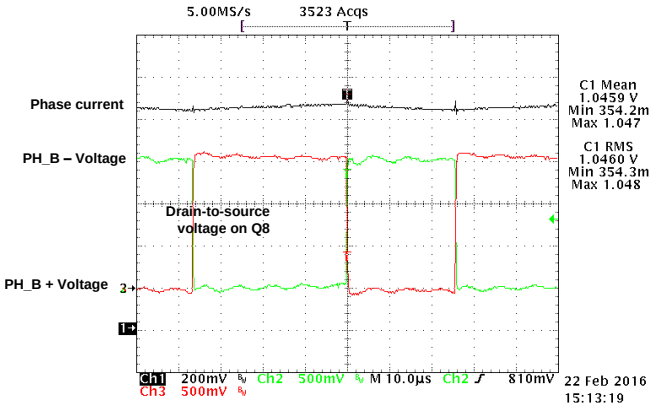


Figure 31. CH2 = PH_B+ Voltage, CH3 = PH_B– Voltage, CH1 = Phase Current (10-A DC), Input Voltage at 50 V

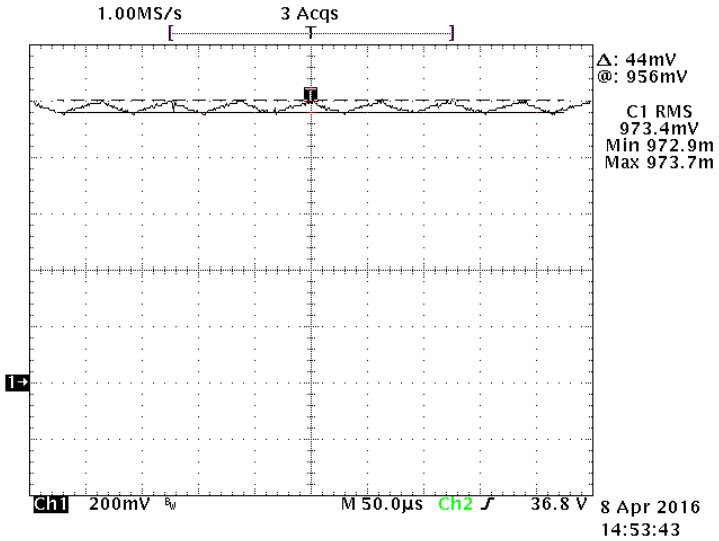


Figure 32. Phase Current Ripple at 75 V, 10 A, 16 kHz

The measured phase current ripple is around 450-mA peak-to-peak at a 16-kHz switching frequency.

6.3 High-Side Current Sense and Phase Voltage Sense

To evaluate the performance of the high-side current sense using the dual high-side amplifiers integrated in the SM72295 full-bridge gate driver, the InstaSPIN-MOTION LaunchPad with the TMS320M28069M was used to sense and control the phase current of the dual TIDA-00365 full-bridge power stages. The following parameters have been used:

- DC-link voltage: V_{DC} = 60 V
- PWM frequency = 25 kHz
- PWM type: Hard-chopping
- PI current control at 25 kHz, phase current measurement triggered at PWM center
- Programmable phase current magnitude (torque)
- Microstep indexer with programmable micro step angle
- Load: Bipolar Stepper 42Y312S-LW8 (Anaheim Automation) with dual phase windings in parallel configuration, no load torque.

The following four figures show the transient response of the high-side current sense amplifier output using the SM72295 dual high-side amplifiers. The analog signal was measured at pin J5-2. Additionally, the phase current of the corresponding stepper winding was measured with a LEM current probe as well as the low-side PWM signal of one half-bridge at pin J7-12 (ePWM1A).

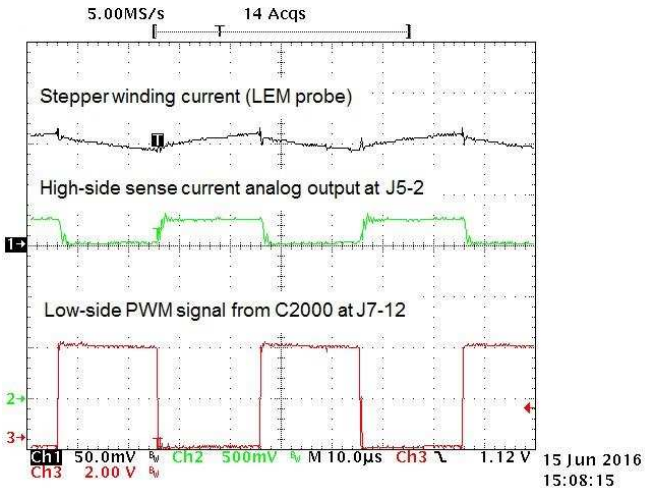


Figure 33. Analog Output Signal From SM72295 Current Sense Amplifier at J5-2 With I_ref 1 A at 25-kHz PWM, 60-V DC

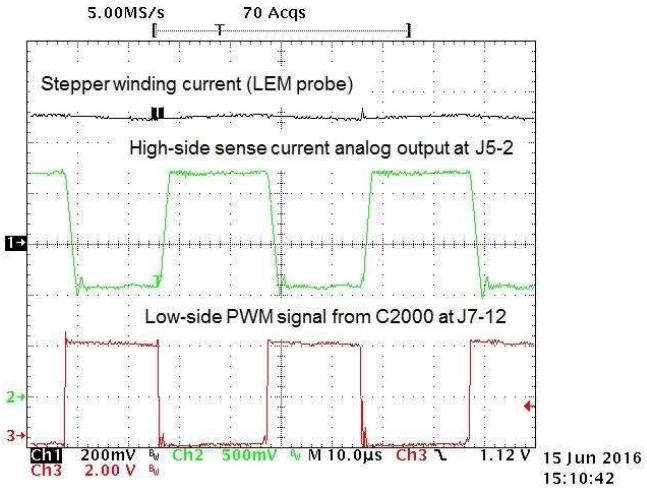


Figure 34. Analog Output Signal From SM72295 Current Sense Amplifier at J5-2 With I_ref 5 A at 25-kHz PWM, 60-V DC

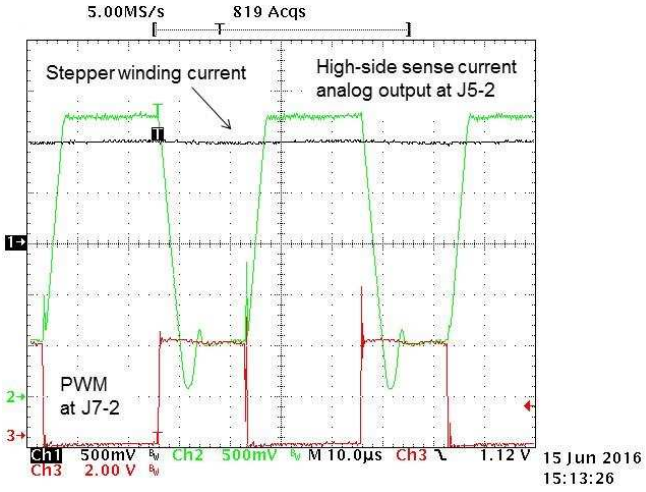


Figure 35. Analog Output Signal From SM72295 Current Sense Amplifier at J5-2 With I_ref 10 A at 25-kHz PWM, 60-V DC

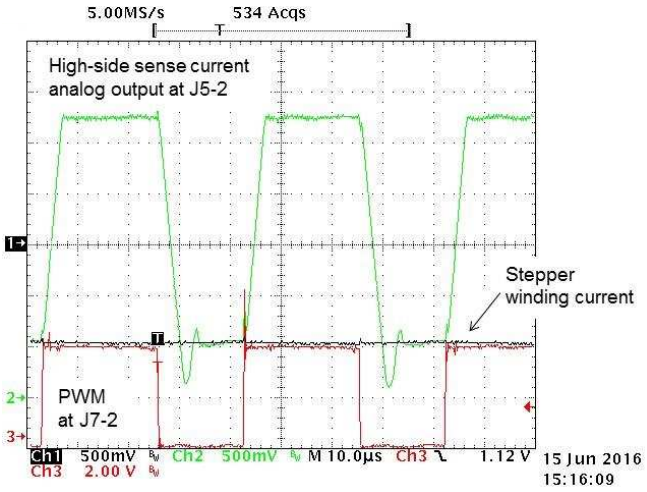


Figure 36. Analog Output Signal From SM72295 Current Sense Amplifier at J5-2 With I_ref –10 A at 25-kHz PWM, 60-V DC

The slew rate of the SM72295 integrated amplifiers of around 2 V/µs will limit the minimum PWM duty cycle to sense the high-side current to around 3 µs (at worst case) to be able to sense maximum current amplitudes. To reduce the minimum PWM duty cycle further, the gain can be reduced, which reduce the voltage swing respectively to mitigate the slew rate. For example, by reducing the gain by 50%, the minimum duty cycle will be reduced to around 1.5 µs; however, the signal-to-noise ratio drops by 6 dB. Hence, it is a trade-off between accuracy and minimum duty cycle.

The following figures show the measured average phase current (using a Fluke ampere meter) versus the high-side current sense output voltage measured at connector J5-2 and sampled center aligned to the PWM on the TMS320F28069M MCU. The absolute error within the ±5-A range for the winding current remains below 100 mA, which is less than 0.4% with respect to the full-scale range of 30 A (–15 to 15 A).

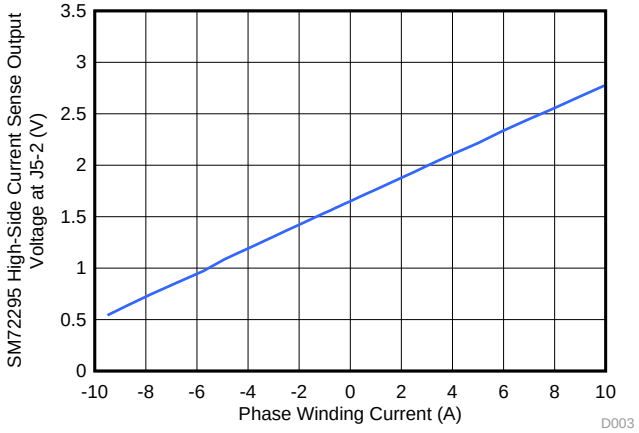


Figure 37. SM72295 Current Sense Amplifier Output Voltage at J5-2 Sampled at PWM Center versus Measured Phase Winding Current (Fluke Ampere Meter)

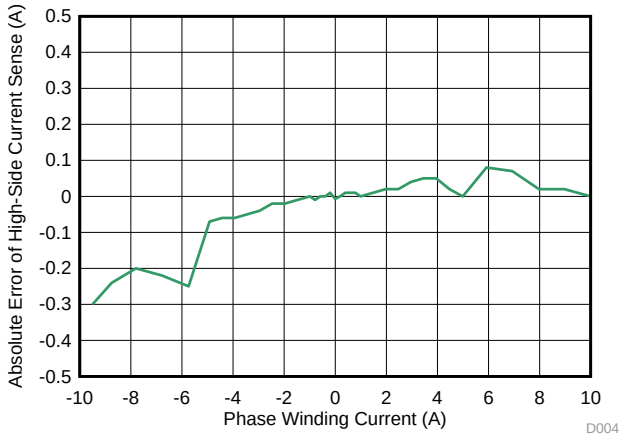


Figure 38. Absolute Error in A of the SM72295 Current Sense Amplifier Output

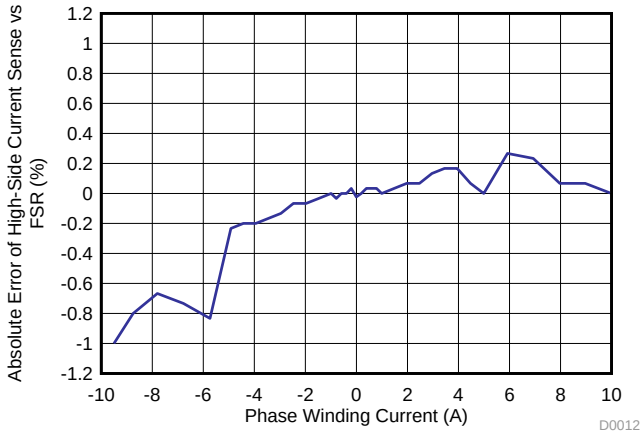


Figure 39. Absolute Error versus FSR (–15 to 15 A) in % of SM72295 Current Sense Amplifier Output

Figure 40 through Figure 42 show the sensed scaled phase+ and phase– to GND voltages measured at the connector J7-2 (phase+) and J7-4 (phase–) to be used for phase-to-phase voltage sensing or back EMF sensing with a 3.3-V ADC embedded in the MCU like the TMS320F28069M.

The winding current reference was set to 1 A, –1 A, and –10 A, respectively. The phase voltages (switch nodes) do not show any overshoot tor ringing, which greatly reduces EMI.

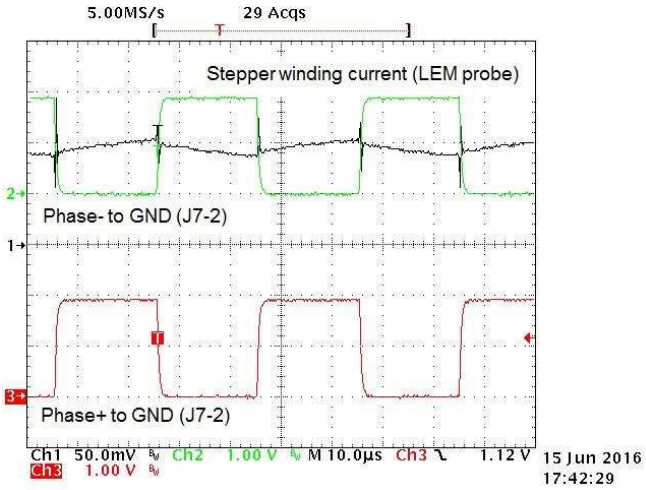


Figure 40. Scaled Phase+ at J7-2 and Phase– at J7-4 versus GND at 1-A Winding Current

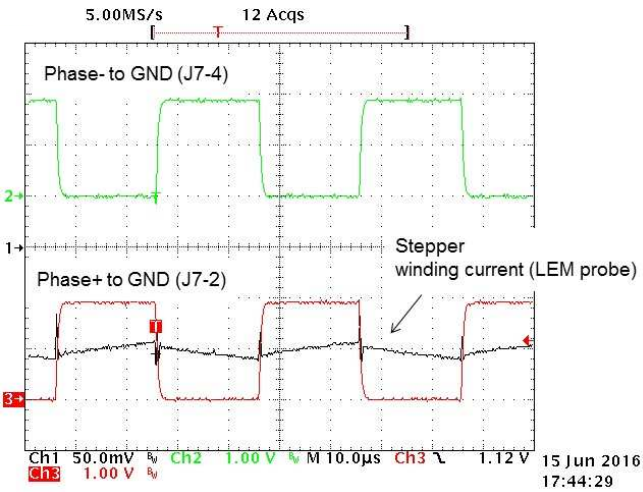


Figure 41. Scaled Phase+ at J7-2 and Phase– at J7-4 versus GND at –1-A Winding Current

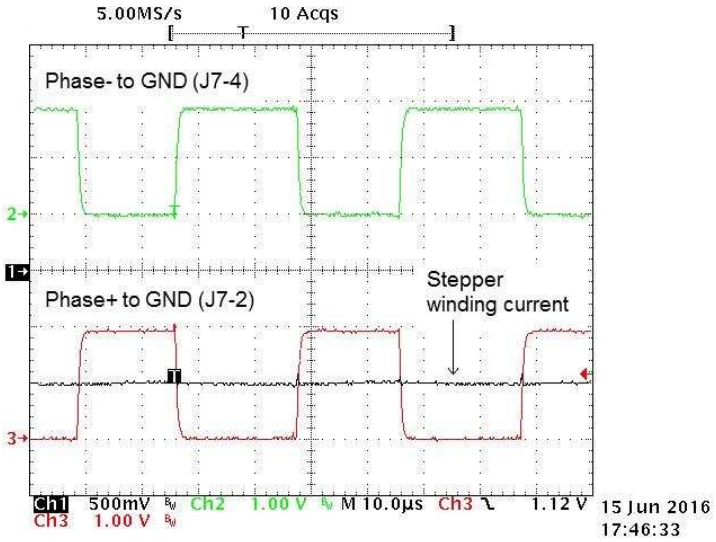


Figure 42. Scaled Phase+ at J7-2 and Phase– at J7-4 versus GND at –10-A Winding Current

6.4 Thermal Performance Without Heat Sink

Due to the limitation in equipment, the efficiency is just estimated. Plus, the following thermal pictures were taken in a worst case scenario (75 V, 10 A).

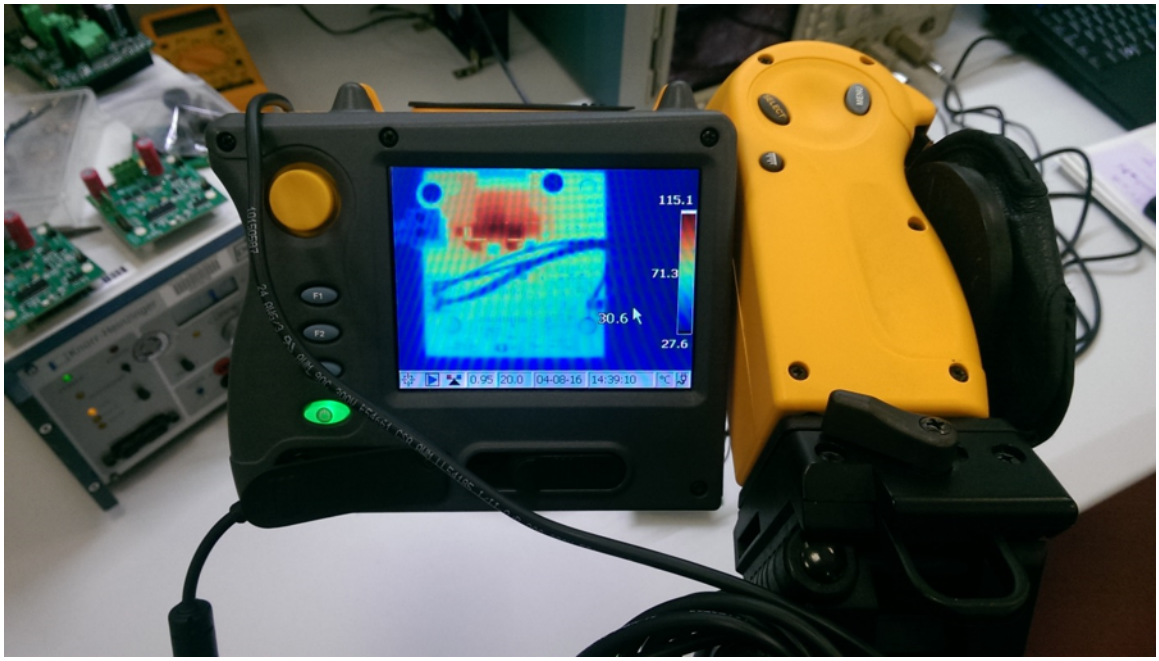


Figure 43. Thermal Picture of TIDA-00210 at 75 V, 10 A, No Air Cooling, No Heat Sink

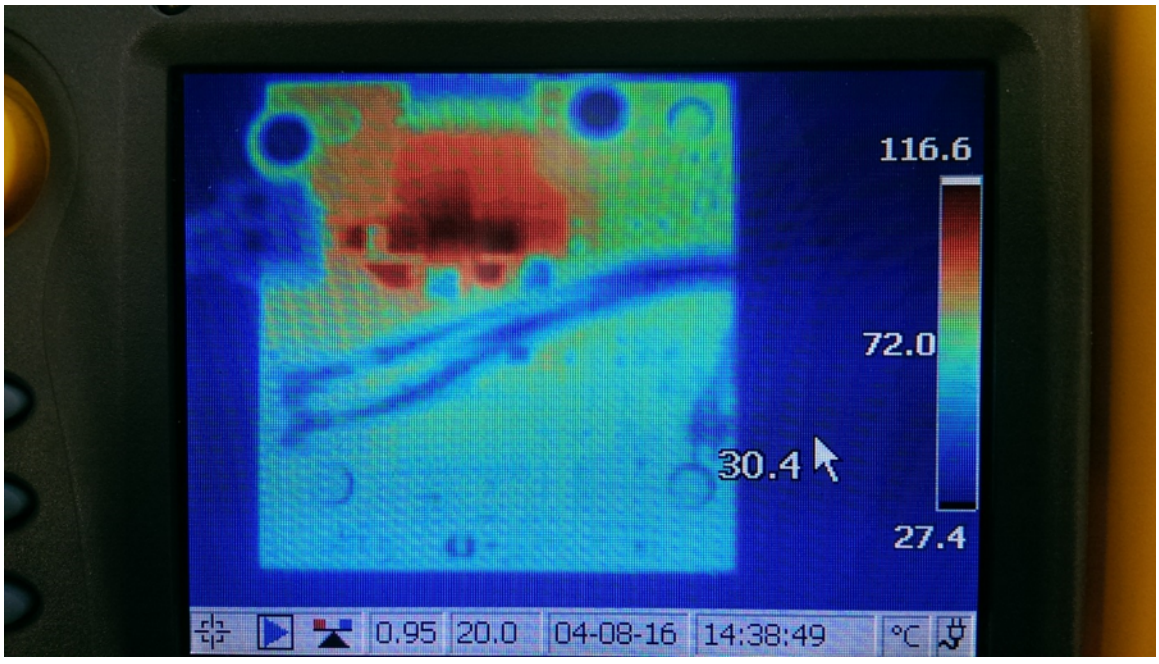


Figure 44. Peak Temperature of TIDA-00210 at 75 V, 10 A, No Air Cooling, No Heat Sink

The peak case temperature detected at 75-V input, 10-A phase current is < 120°C.

Efficiency is estimated as

$$\text{Efficiency} = \frac{P_{OUT}}{P_{IN}} = \frac{\left(P_{IN} - P_{LOSSES}\right)}{P_{IN}} = 1 - \frac{P_{LOSSES}}{P_{IN}} \quad (17)$$

where

- P_{IN} = 75 V × 1.03 A = 77 W
- $P_{LOSSES} \approx 4 \times P_{onFET}$
- $P_{LossOnFET} = P_{Switching} + P_{Conduction} + P_{DeadTime}$

$$= V_{DS} \times I_{PHASE} \times F_{SW} \times \frac{\left(T_{Rise} + T_{Fall}\right)}{2} + R_{DSon} \times I_{PHASE}^2 \times D + V_F \times I_{PHASE} \times F_{SW} \times T_{DeadTime}$$

$$= 75\ V \times 10\ A \times 16\ kHz \times 30\ ns + 23\ m\Omega \times 100\ A^2 \times 0.5 + 1\ V \times 10\ A \times 16\ kHz \times 100\ ns$$

$$= 0.36\ W + 1.15\ W + 0.02\ W = 1.53\ W$$

That is less than half of the package capability.

$P_{LOSSES} \approx 4 \times P_{onFET}$ = 6.12 W

Efficiency = 1 – 6.12 W / 77 W ≈ 92%

At 75 V, the loss of the PMP is around 20 mA x 75 V = 150 mW.

By using external cooling or a heat sink, the total losses can be reduced down to (at best case) 1.03 W x 4 = 4.12 W, plus the losses of the PMP → 4.2 W losses that over a 77-W total power input leads to an efficiency (estimated) of 95% max.

Also using a different MOSFET such as the CSD19533Q5A or the CSD19532Q5A to balance switching and conduction losses can be considered.

6.5 Full-System Evaluation

The following tests where done to evaluate the performance of dual TIDA-00365 full-bridges connected to a high torque, high power bipolar stepper motor. The winding current was measured with the high-side current sense using the dual high-side amplifiers integrated in the SM72295 at constant speed of 256 micro steps per second with a step size of 1/256 degrees. As described earlier, the InstaSPIN-MOTION LaunchPad with the TMS320M28069M MCU was used to sense and control the phase winding currents of the dual TIDA-00365 full-bridge power stages. The following parameters have been used:

- DC-link voltage: V_{DC} = 60 V
- PWM frequency = 25 kHz
- PWM type: Hard-chopping
- PI current control at 25 kHz, phase current measurement triggered at PWM center
- Programmable phase current magnitude (torque)
- Microstep indexer with 256 microsteps (step size 1.40625 degrees)
- Load: Bipolar stepper 42Y312S-LW8 (Anaheim Automation) with dual phase windings in parallel configuration, no load torque

The electrical speed was set to 256 microsteps per second.

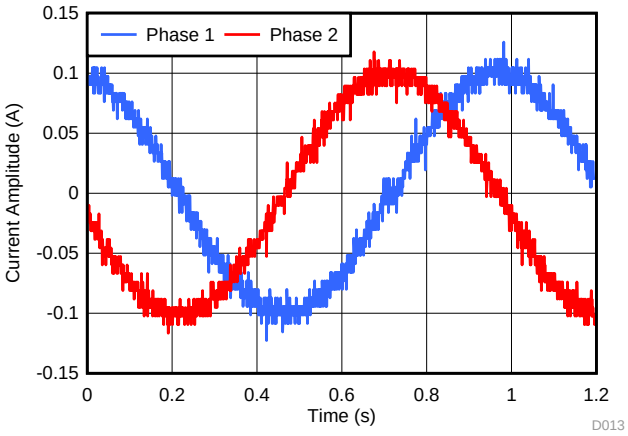


Figure 45. Stepper Phase Winding Currents at 100-mA Current Magnitude and 1/256 Microsteps

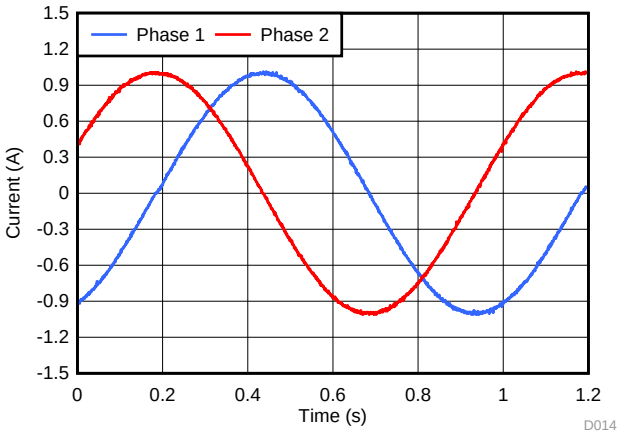


Figure 46. Stepper Phase Winding Currents at 1-A Current Magnitude and 1/256 Microsteps

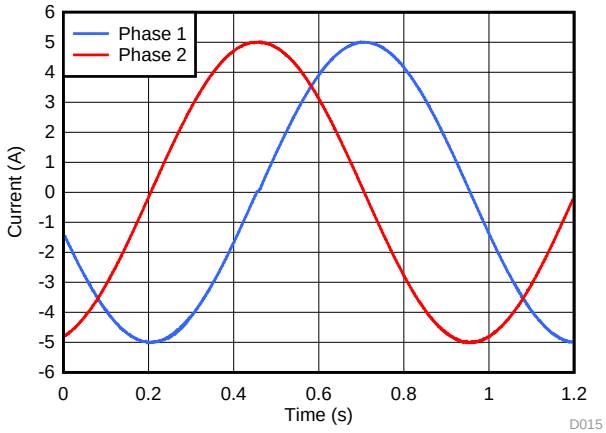


Figure 47. Stepper Phase Winding Currents at 5-A Current Magnitude and 1/256 Microsteps

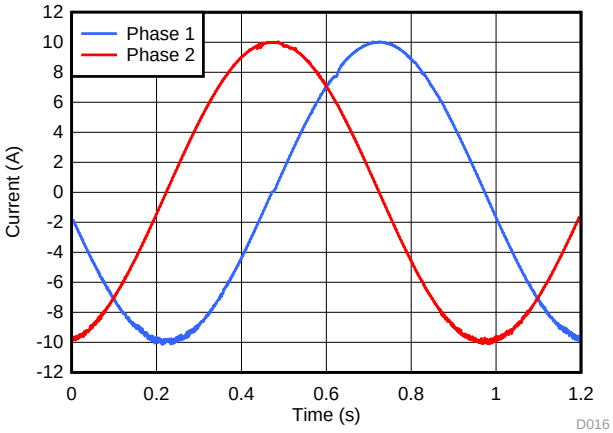


Figure 48. Stepper Phase Winding Currents at 10-A Current Magnitude and 1/256 Microsteps

6.6 Protections

The TIDA-00210 provides a full set of protections such as:

- Undervoltage lockout (UVLO)
- Overvoltage protection (OVP)
- Overcurrent protection (OCP)
- Short-circuit protection (SCP)
- Over-temperature protection (OTP)

Test results are showed in the following subsections.

6.6.1 Undervoltage Lockout (UVLO)

The UVLO has been implemented based on the UVLO feature of the LM501x family. This provides the 12-V rails for the gate driver and also generates the 3.3 V (from the LDO LM317) that enables the host processor interface.

By design, UVLO is set at 18 V (rising input voltage) with an hysteresis of 2 V, meaning that the turnoff threshold (falling UVLO) is around 16 V nominal.

The values measured during the test bench session are 18.2 V and 15.6 V, respectively.

6.6.2 Overvoltage Protection (OVP)

The OVP threshold has been set at 85 V nominal (see Section 7.1).

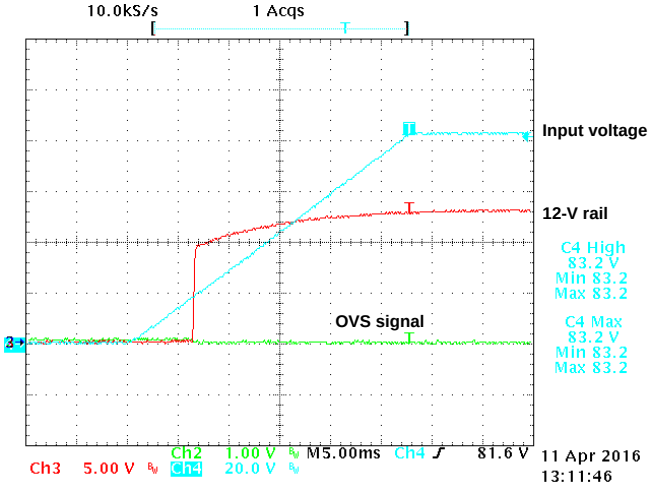


Figure 49. Start-Up Voltage at 84-V Input (CH4 = V_{IN}, CH3 = 12-V Rail, CH2 = OVS Signal)

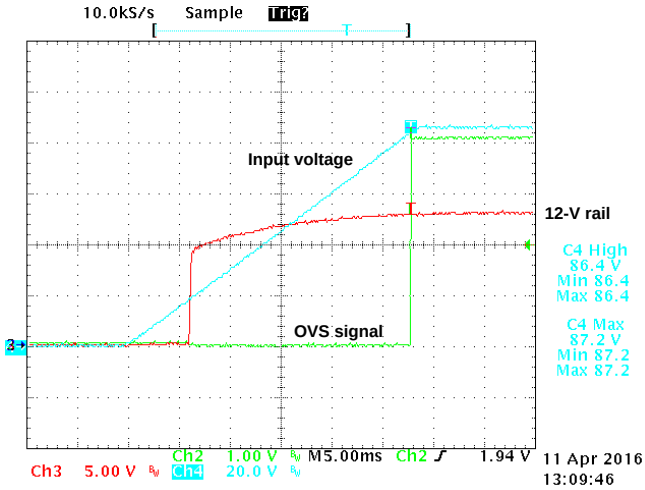


Figure 50. Start-Up Voltage at 86-V Input (CH4 = V_{IN}, CH3 = 12-V Rail, CH2 = OVS Signal)

These waveforms show the input voltage ramp-up (blue trace), the 12-V rail (red) and the OVS signal (green trace; see Section 7.1 for details). These also show that the OVP measured level is between 83.2 and 87.2 V (average of 85.2 V, as expected).

6.6.3 Overcurrent Protection (OCP)

OCP is tested by increasing the duty cycle at the maximum possible in open-loop control.

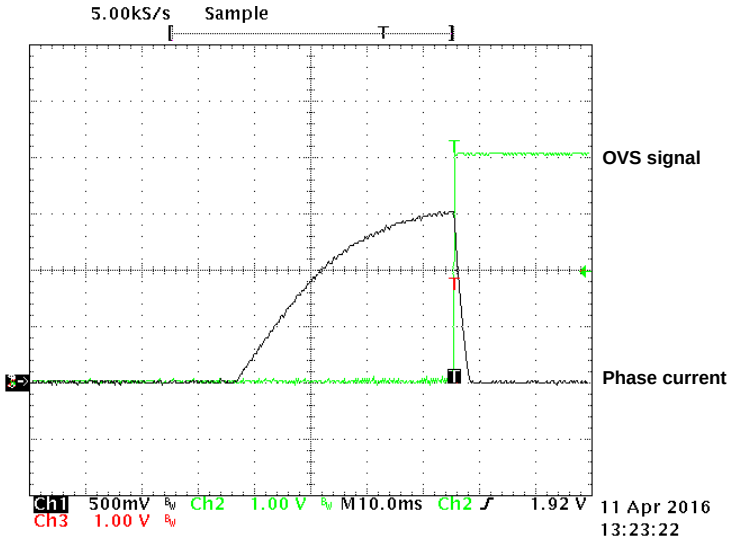


Figure 51. OCP Triggered When Phase Current > 15 A is Forced Into the Motor (CH1 = Phase Current, CH2 = OVS Signal)

Again, in Figure 51, the black trace is the measured current into the phase with a scale of 100 mV/A, and shows a peak current of 15 A when the OVS signal is switched on.

6.6.4 Short-Circuit Protection (SCP)

Having implemented an HS current sense solution, the highest protection level is granted. In particular, the system is able to trigger either phase-to-ground failures or phase-to-ground failures.

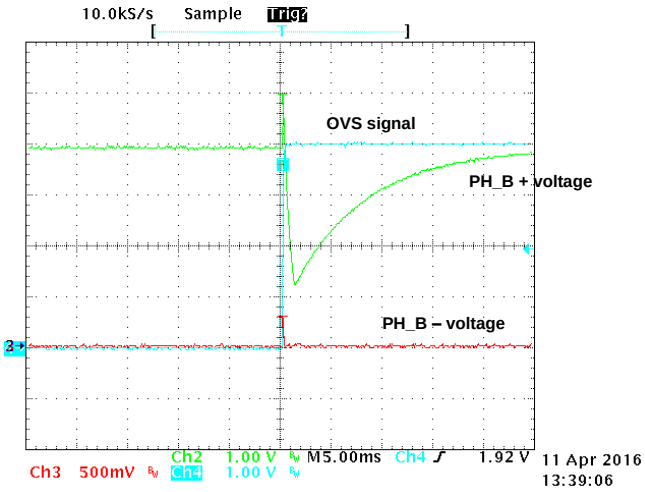


Figure 52. CH2 = PH+, CH3 = PH– (Shunted to GND), CH4 = OVS

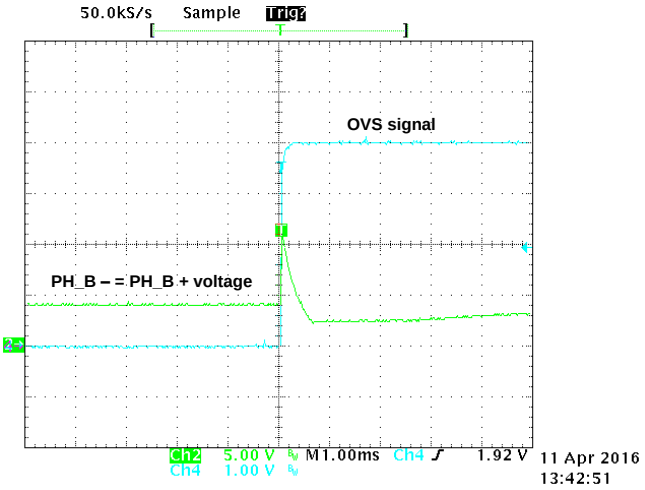


Figure 53. CH2 = PH+ (Shunted to PH–), CH4 = OVS

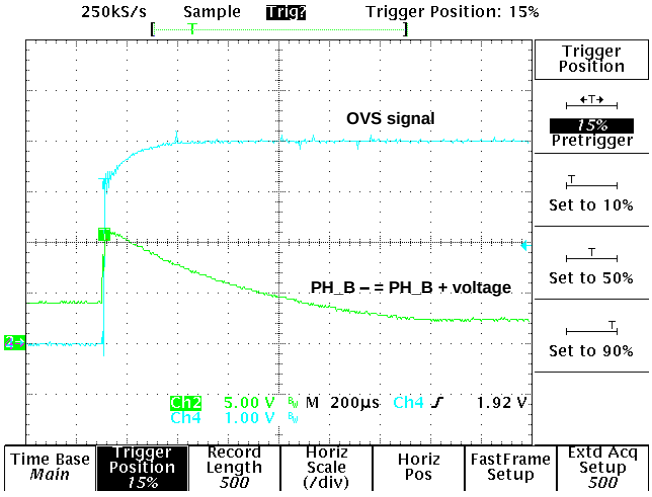


Figure 54. CH2 = PH+ (Shunted to PH–), CH4 = OVS (Zoomed Out)

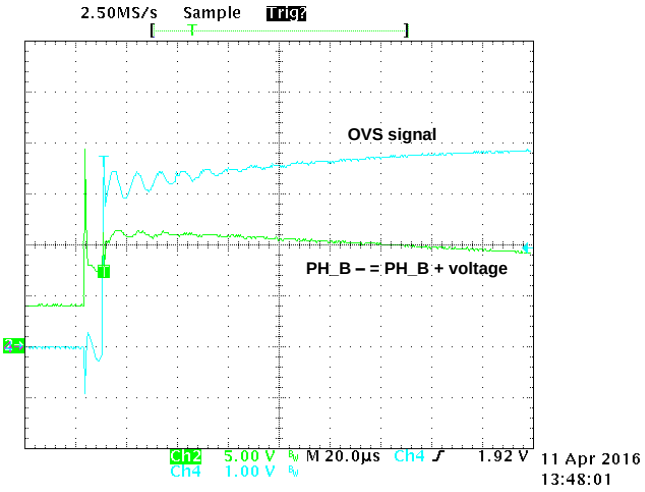


Figure 55. CH2 = PH+ (Shunted to PH–), CH4 = OVS (Zoomed In)

6.6.5 Over-Temperature Protection (OTP)

The OTP is not tested because the protection is assumed to perform properly by design. It has been set at 120°C (PCB temperature) to have both margins from the top (150°C) and bottom (90°C).

7 Design Files

7.1 Schematics

To download the schematics for each board, see the design files at TIDA-00210.

7.2 Bill of Materials

To download the bill of materials for each board, see the design files at TIDA-00210.

7.3 PCB Layout Guidelines

Because of the complexity of the whole system, a complete section is dedicated to the layout design guidelines. The power management stage is not discussed in detail (see the layout guidelines in ICs datasheets) while for the motor drive power stage, see the application notes for the BUs. In particular, see the following application reports:

- *Reducing Ringing Through PCB Layout Techniques* (SLPA005)
- *Class-D Output Snubber Design Guide* (SLOA201)
- *Controlling switch-node ringing in synchronous buck converters* (SLYT465)

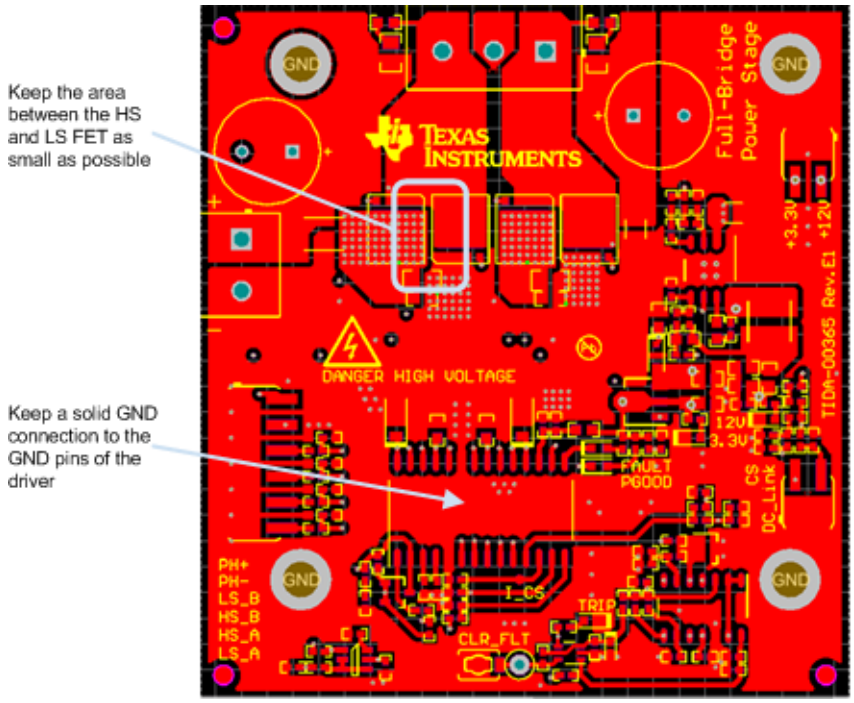


Figure 56. Top Layer

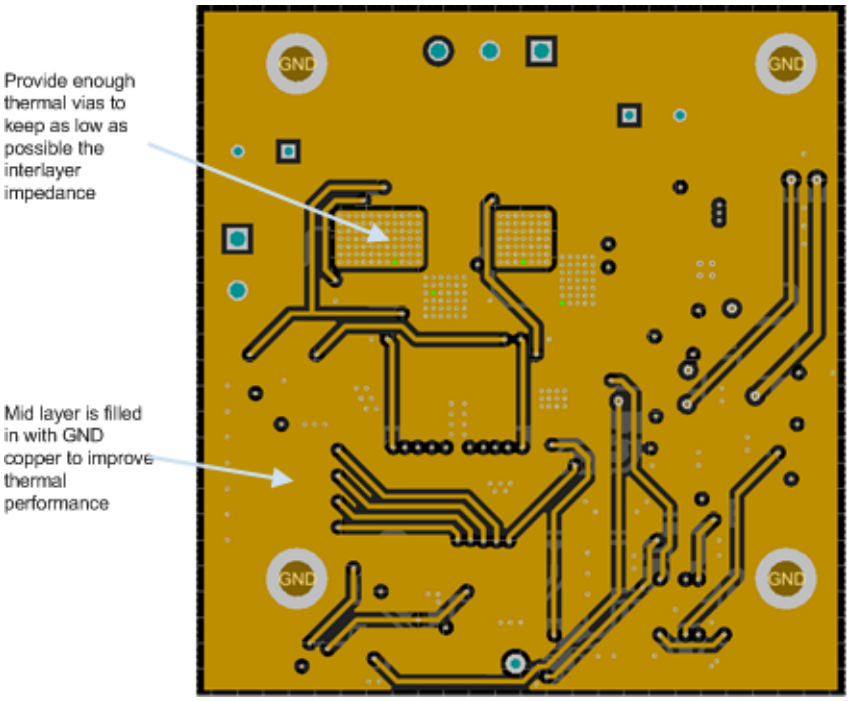


Figure 57. Mid Layer

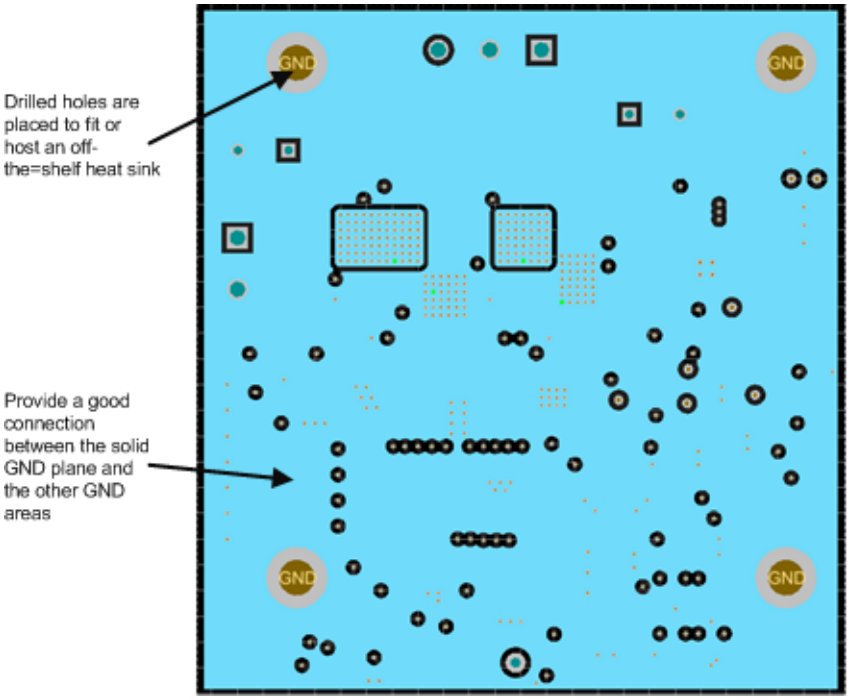


Figure 58. GND Plane

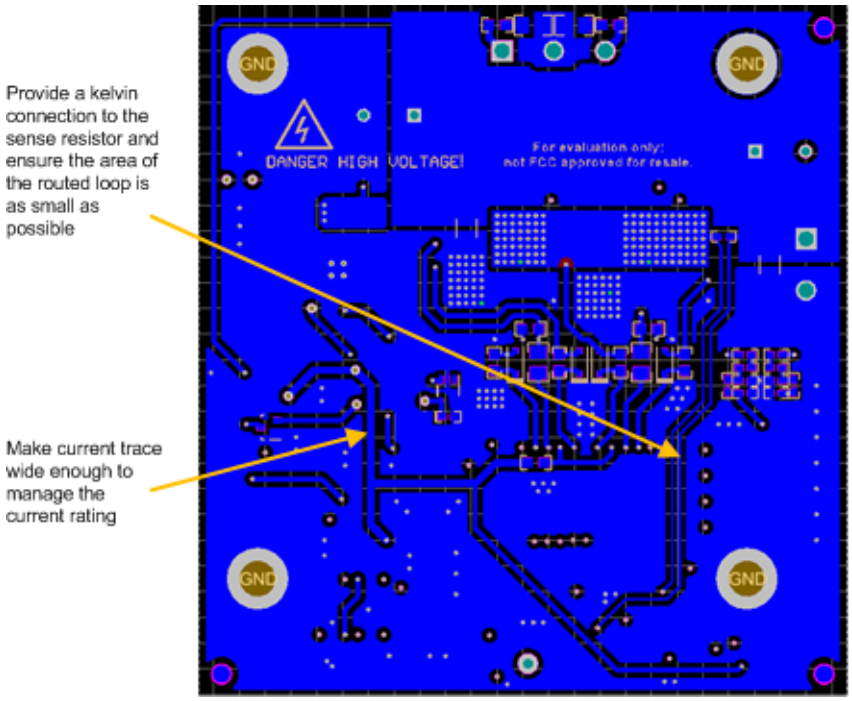


Figure 59. Bottom Layer (Flip View)

7.3.1 Layout Prints

To download the layout prints for each board, see the design files at TIDA-00210.

7.4 Altium Project Files

To download the Altium project files for each board, see the design files at TIDA-00210.

7.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00210.

7.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-00210.

8 Software Files

To download the software files for this reference design, see the link at TIDA-00210.

9 References

1. Texas Instruments, *Stepper Motor System with Medium Torque Drive*, TIDA-00111 Technical Reference (TIDU149)
2. Texas Instruments, *Universal Stepper Motor Driver*, TIDA-00736 Technical Reference (TIDUBC1)
3. Texas Instruments, *Auto-Torque Implementation Reference Design*, TIDA-00740 Design Guide (TIDUAJ4)
4. Texas Instruments, *24V Stepper Motor Controller with Integrated Current Sense Reference Design*, TIDA-00867 Test Report (TIDUBB4)
5. Texas Instruments, *Noise Analysis in Operational Amplifier Circuits*, Application Report (SLVA043)
6. Texas Instruments, *Reducing Ringing Through PCB Layout Techniques*, Application Report (SLPA005)
7. Texas Instruments, *Class-D Output Snubber Design Guide*, Developer's Guide (SLOA201)
8. Texas Instruments, *Controlling switch-node ringing in synchronous buck converters*, Technical Brief (SLYT465)
9. Texas Instruments, WEBENCH® Design Center (http://www.ti.com/webench)

10 Terminology

FSR— Full-scale range

OCT— Overcurrent protection

OTP— Over-temperature protection

OVI— Overvoltage indication

OVP— Overvoltage protection

SCP— Short-circuit protection

UVLO— Undervoltage lockout

UVP— Undervoltage protection

11 About the Authors

VINCENZO PIZZOLANTE is a system engineer in the Industrial Systems-Motor Drive team at Texas Instruments, who is responsible for developing reference designs for industrial drives.

MARTIN STAEBLER is a system architect in the Industrial Systems-Motor Drive team at Texas Instruments, who is responsible for specifying reference designs for industrial drives.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2016) to A Revision	Page
• Changed from preview page	1

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265