TI Designs

Automotive i.MX6 Quad Core Processor Power Reference Design

TI Designs

This design is a low-cost discrete power solution for the i.MX6Q quad core application processor. All of the DCDC regulators operate at frequencies above the AM radio broadcast band to avoid interference with the radio. The DCDC regulators also provide a small solution size due to smaller filter components. The first stage DC-DC converter supports a voltage input range of 6 V to 42 V, allowing the design to support start-stop operation and load dump. The second stage DC-DC converters provide all the necessary power rails to power the i.MX6Q. No power sequencer is necessary for this design. The PWB is a 4-layer board with 2 oz of copper to provide good power dissipation at 85 C ambient.

Design Resources

TIDA-00804	Design Folder
TPS54561-Q1	Product Folder
TPS57114-Q1	Product Folder
LM26420-Q1	Product Folder
TPS54388-Q1	Product Folder
TLV70030-Q1	Product Folder

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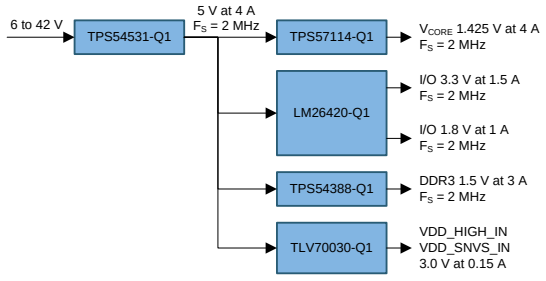


Design Features

- Wide Input Voltage Range: Off-Battery 6-V to 42-V Power Supplies Support Start-Stop System and Load Dump
- The DC-DC Regulators All Operate Above 1.8 MHz to Avoid AM Band Interference
- Small Form Factor: 75 mm × 58 mm Circuit Board Dimensions
- No Power Sequencer Necessary
- Less Than 5% Ripple on All Power Rails

Featured Applications

- Automotive Infotainment Head Unit
- Automotive Instrument Cluster

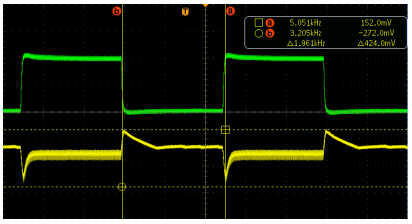
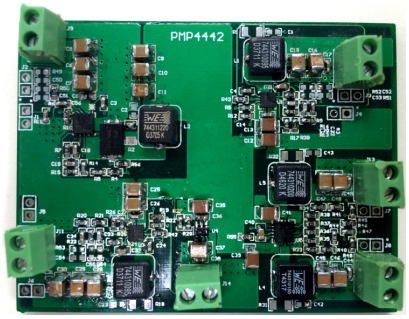


Figure 1. Key Test Result Graph



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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input Voltage Range	5 V to 42 V DC	See Section 2.1.1, Section 3.1, and Section 4.3
Primary Voltage Supply	+ 5 Volts ± 5%	See Section 3.1 and Section 4.3
Primary Supply Load Current	4 A	See Section 3.1 and Section 4.3
Primary Supply Voltage Ripple	Less Than 40 mV p-p	See Section 3.1 and Section 4.3
Primary Voltage Switching Frequency	f(sw) > 1810 kHz	See Section 3.1
VDD_SNVS	3 Volts ± 5%	See Section 2.1.5, Section 3.2, and Section 4.3.3
VDD_SNVS Load Current	0.15 A	See Section 2.1.5, Section 3.2, and Section 4.3.6
Core Supply	1.425 V ± 3%	See Section 2.1.2, Section 3.3, and Section 4.3.3
Core Load Current	4 A	See Section 3.3 and Section 4.3.3
Core Supply Voltage Ripple	Less Than 40 mV p-p	See Section 3.3 and Section 4.3.3
Core Supply Switching Frequency	f(sw) > 1810 kHz	See Section 3.3
DDR Supply	1.5 V ± 5%	See Section 2.1.4, Section 3.4, and Section 4.3.2
DDR Supply Current	3 A	See Section 3.4, and Section 4.3.2
DDR Supply Voltage Ripple	Less Than 40 mV p-p	See Section 3.4, and Section 4.3.2
DDR Supply Switching Frequency	f(sw) > 1810 kHz	See Section 3.4
I/O Supply 1	3.3 V ± 5%	See Section 2.1.3, Section 3.5, and Section 4.3.5
I/O Supply 1 Current	1.5 A	See Section 3.5 and Section 4.3.5
I/O Supply 1 Voltage Ripple	Less Than 40 mV p-p	See Section 3.5 and Section 4.3.5
I/O Supply 1 Switching Frequency	f(sw) > 1810 kHz	See Section 3.5
I/O Supply 2	1.8 V +/- 5%	See Section 2.1.3, Section 3.5, and Section 4.3.4
I/O Supply 2 Current	1 A	See Section 3.5 and Section 4.3.4
I/O Supply 2 Voltage Ripple	Less Than 40 mV p-p	See Section 3.5 and Section 4.3.4
I/O Supply 2 Switching Frequency	f(sw) > 1810 kHz	See Section 3.5

2 System Description

The TIDA-00804 *Automotive i.MX6 Quad Core Processor Power Reference Design* was created as a functional evaluation of a power supply subsystem for an automotive head unit or instrument cluster that uses an i.MX6Q application processor for the main processing unit. The TIDA-00804 uses single and dual-channel step-down converters and an LDO to provide all of the power supply voltages required in a typical i.MX6Q design. No power supply sequencer is required because the supplies are enabled sequentially using the power good and enable pins on the selected devices. All switching power supplies operate at frequencies above 1.8 MHz to ensure that there is no power supply noise interfering with the AM radio broadcast band.

Figure 2 shows an example system block diagram of an Automotive Head Unit. This design represents the Power Supply Subsystem In the upper left corner of the block diagram. Figure 3 shows the block diagram.

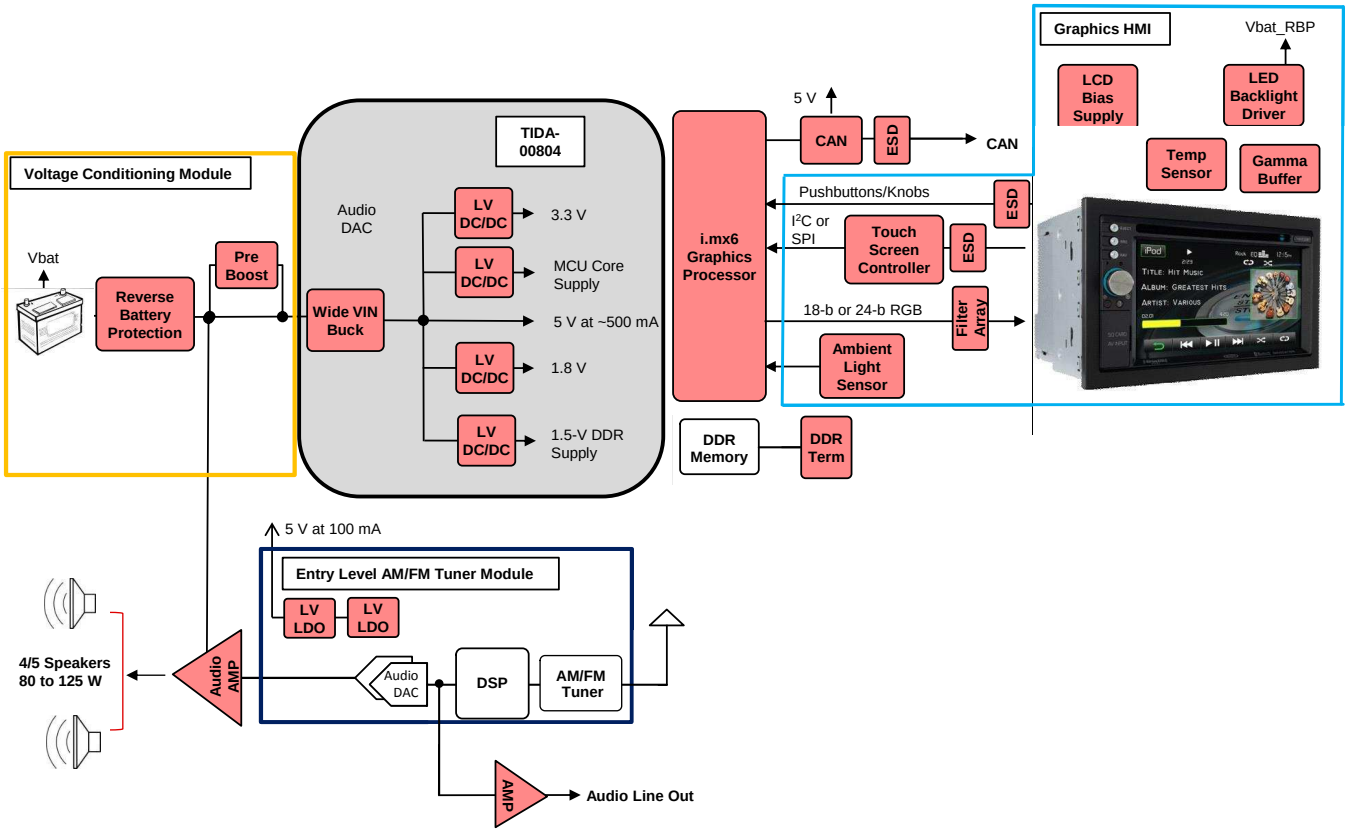

Figure 2. System Level Block Diagram of a Head Unit With a Graphics Display

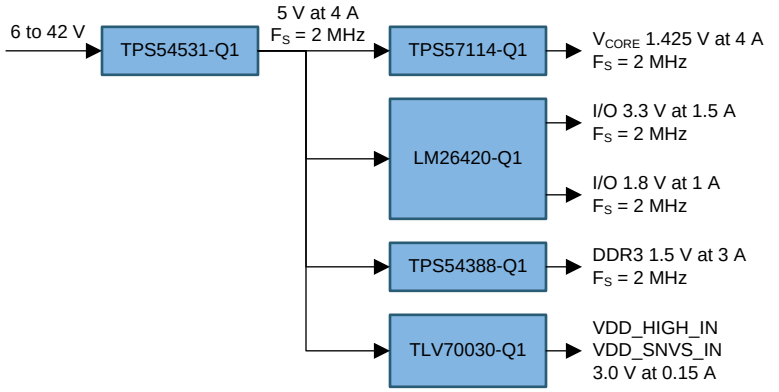

Figure 3. Block Diagram

2.1 Highlighted Products

2.1.1 TPS54561-Q1

The TPS54561-Q1 device is a 60-V, 5-A, step-down regulator with an integrated high-side MOSFET. The device survives load dump pulses up to 65 V per ISO 7637. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode and 152-µA supply current enables high efficiency at light loads. Pulling the enable pin low reduces shutdown supply current to 2 µA .

Undervoltage lockout has an internal 4.3-V setting. Use of an external resistor divider at the EN pin may increase the setting. The soft-start pin controls the output-voltage start-up ramp and also configures sequencing or tracking. An open-drain power-good signal indicates the output is within 93% to 106% of its nominal voltage.

A wide adjustable switching-frequency range allows optimization for either efficiency or external component size. Cycle-by-cycle current limit, frequency foldback, and thermal shutdown protect the device during an overload condition.

The TPS54561-Q1 is available in a 10-pin, 4-mm × 4-mm SON package.

Figure 4 shows the TPS54561-Q1 functional block diagram

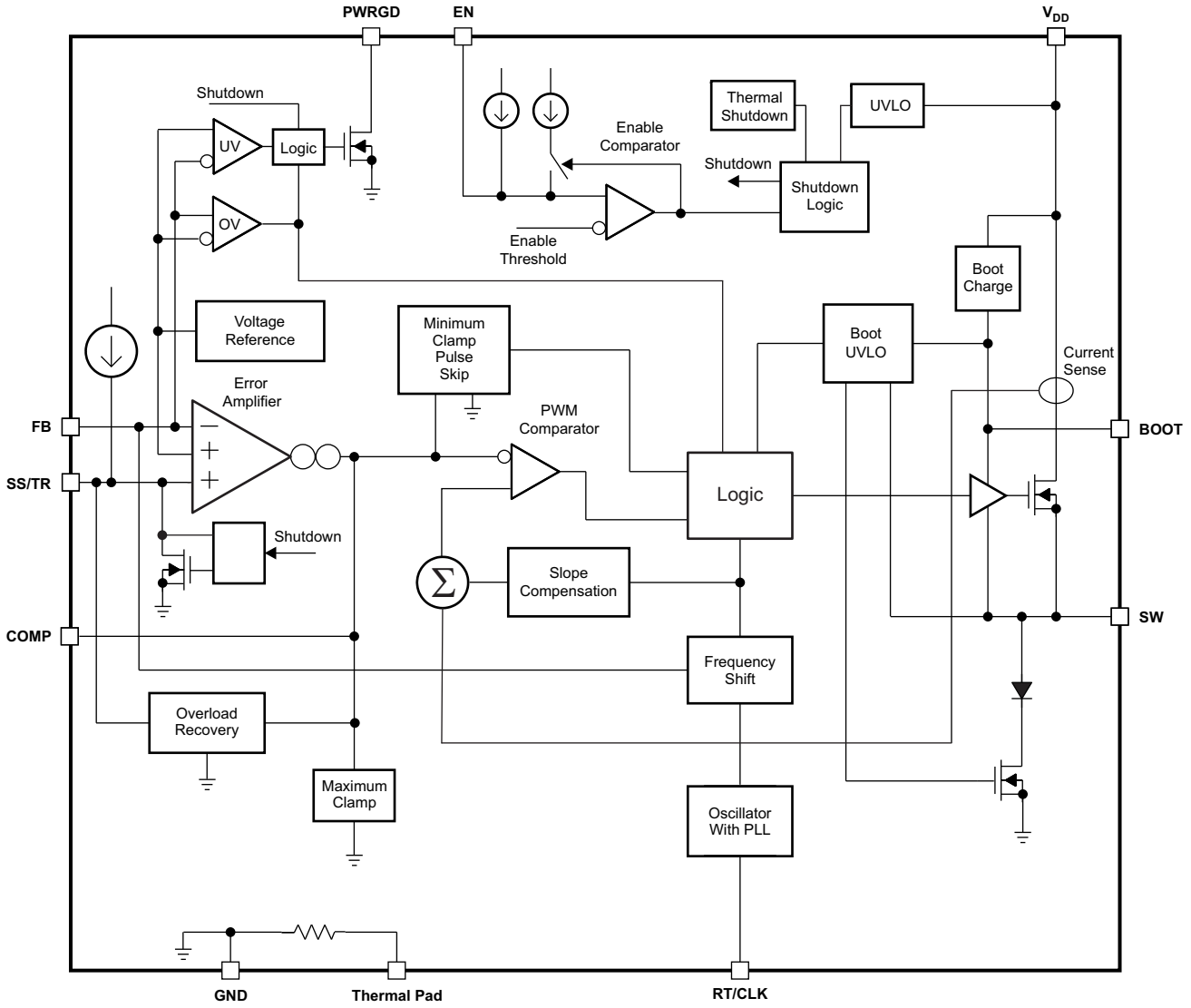

Figure 4. TPS54561-Q1 Functional Block Diagram

2.1.2 TPS57114-Q1

The TPS57114-Q1 device is a full-featured 6-V, 4-A, synchronous step-down current-mode converter with two integrated MOSFETs. The TPS57114-Q1 device enables small designs by integrating the MOSFETs, implementing current-mode control to reduce external component count, reducing inductor size by enabling up to 2-MHz switching frequency, and minimizing the IC footprint with a small 3-mm × 3-mm thermally enhanced QFN package.

The TPS57114-Q1 device provides accurate regulation for a variety of loads with an accurate ±1% voltage reference (V_{ref}) over temperature.

Efficiency is maximized through the integrated 12-mΩ MOSFETs and 515-µA typical supply current. Using the enable pin, shutdown supply current is reduced to 5.5 µA by entering a shutdown mode.

The internal undervoltage lockout setting is 2.45 V, but programming the threshold with a resistor network on the enable pin can increase the setting. The slow-start pin controls the output-voltage start-up ramp. An open-drain power-good signal indicates the output is within 93% to 107% of its nominal voltage.

Frequency foldback and thermal shutdown protect the device during an overcurrent condition.

Figure 5 shows the TPS57114-Q1 functional block diagram.

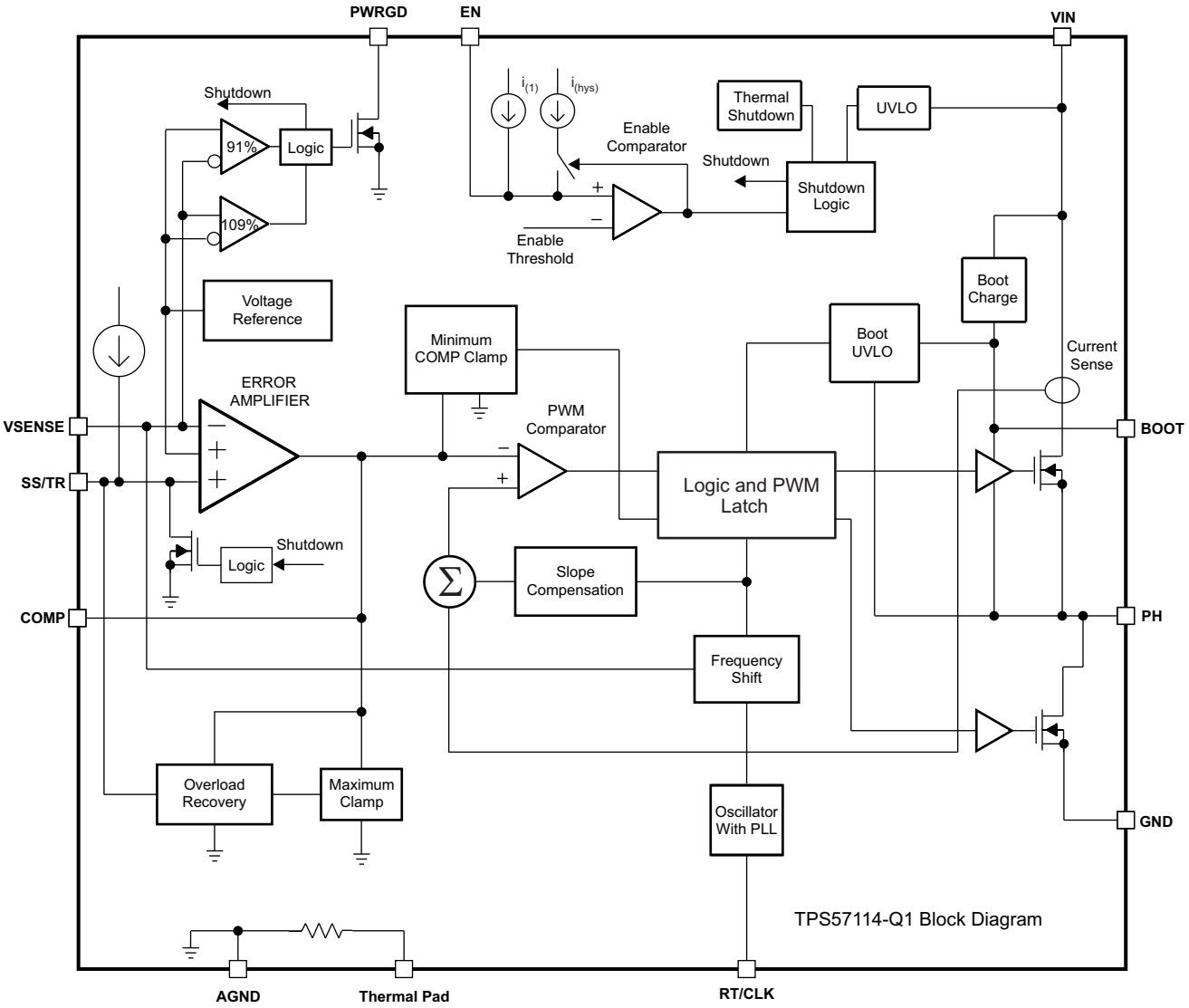

Figure 5. Functional Block Diagram

2.1.3 LM26420-Q1

The LM26420 regulator is a monolithic, high-efficiency dual PWM step-down DC-DC converter. This device has the ability to drive two 2-A loads with an internal 75-mΩ PMOS top switch and an internal 50-mΩ NMOS bottom switch using state-of-the-art BICMOS technology results in the best power density available. The world-class control circuitry allows on times as low as 30 ns, thus supporting exceptionally high-frequency conversion over the entire 3-V to 5.5-V input operating range down to the minimum output voltage of 0.8 V.

Although the operating frequency is high, efficiencies up to 93% are easy to achieve. External shutdown is included, featuring an ultra-low standby current. The LM26420 utilizes current-mode control and internal compensation to provide high performance regulation over a wide range of operating conditions.

Figure 6 shows the LM26420 functional block diagram.

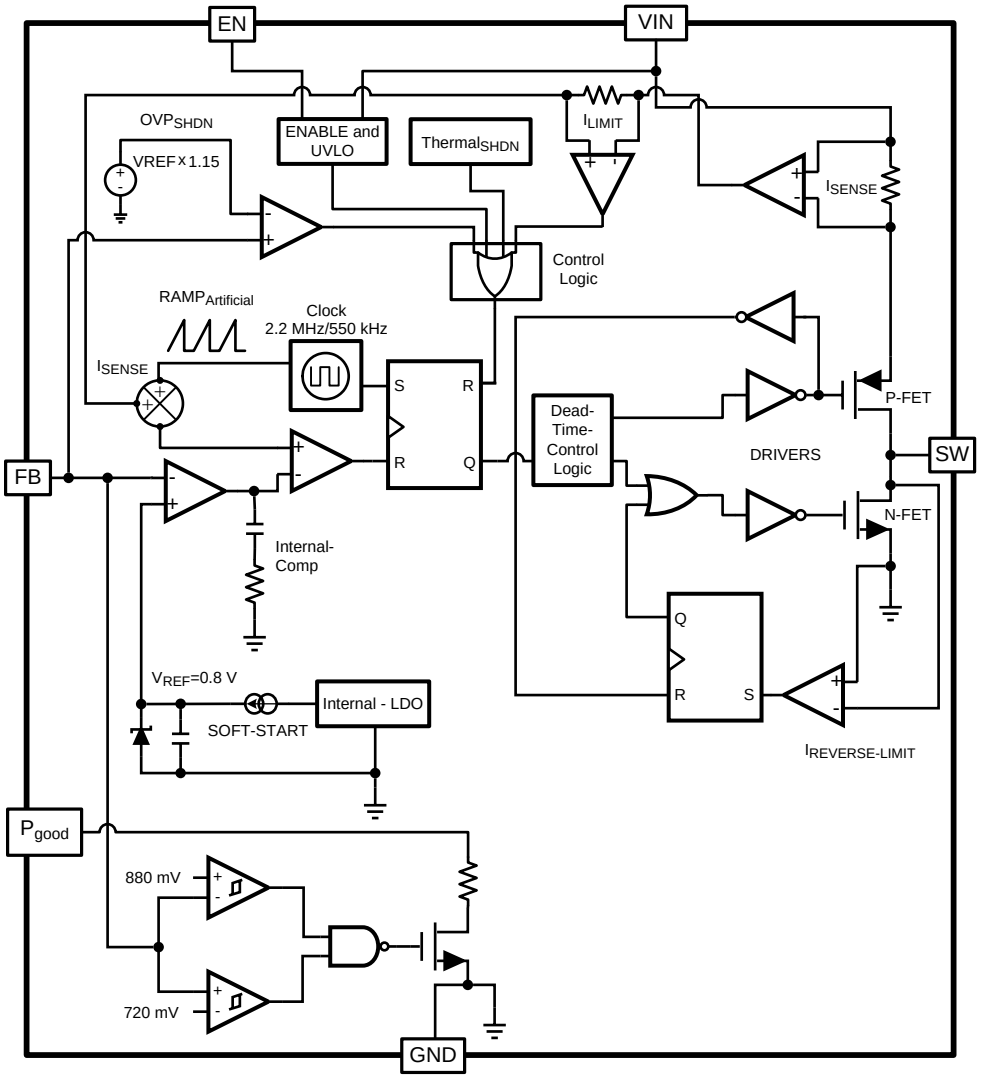

Figure 6. LM26420 Functional Block Diagram

2.1.4 TPS54388-Q1

The TPS54388-Q1 device is a full-featured 6-V, 3-A, synchronous step-down current-mode converter with two integrated MOSFETs.

The TPS54388-Q1 device enables small designs by integrating the MOSFETs, implementing current-mode control to reduce external component count, reducing inductor size by enabling up to 2-MHz switching frequency, and minimizing the IC footprint with a small 3-mm × 3-mm thermally enhanced QFN package.

The TPS54388-Q1 device provides accurate regulation for a variety of loads with an accurate ±1% voltage reference (V_{ref}) over temperature.

The integrated 12-mΩ MOSFETs and 515-µA typical supply current maximize efficiency. Entering shutdown mode using the enable pin reduces shutdown supply current to 5.5 µA, typical.

The internal undervoltage lockout setting is at 2.45 V, but programming the threshold with a resistor network on the enable pin can increase the setting. The slow-start pin sets the output-voltage start-up ramp. An open-drain power-good signal indicates when the output is within 93% to 107% of its nominal voltage.

Frequency fold-back and thermal shutdown protect the device during an overcurrent condition.

Figure 7 shows the TPS54388-Q1 functional block diagram.

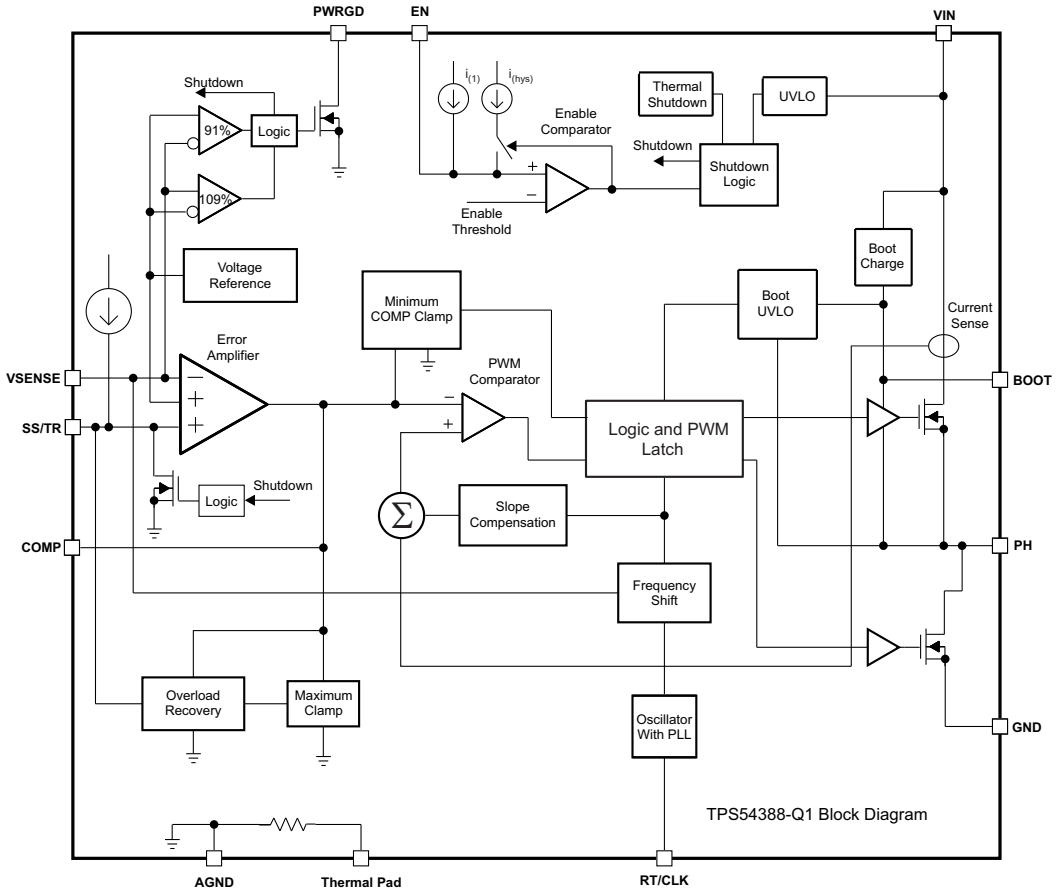

Figure 7. TPS5488-Q1 Functional Block Diagram

2.1.5 TLV70030-Q1

The TLV700xx-Q1 family of low-dropout (LDO) linear regulators are low-quiescent-current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision band-gap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage makes this series of devices ideal for most battery-operated handheld equipment. All device versions have a thermal shutdown and current limit for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV700xx-Q1 LDOs are available in the SOT-5 (DDC) and the SC70-5 (DCK) packages.

Figure 8 shows the functional block diagram.

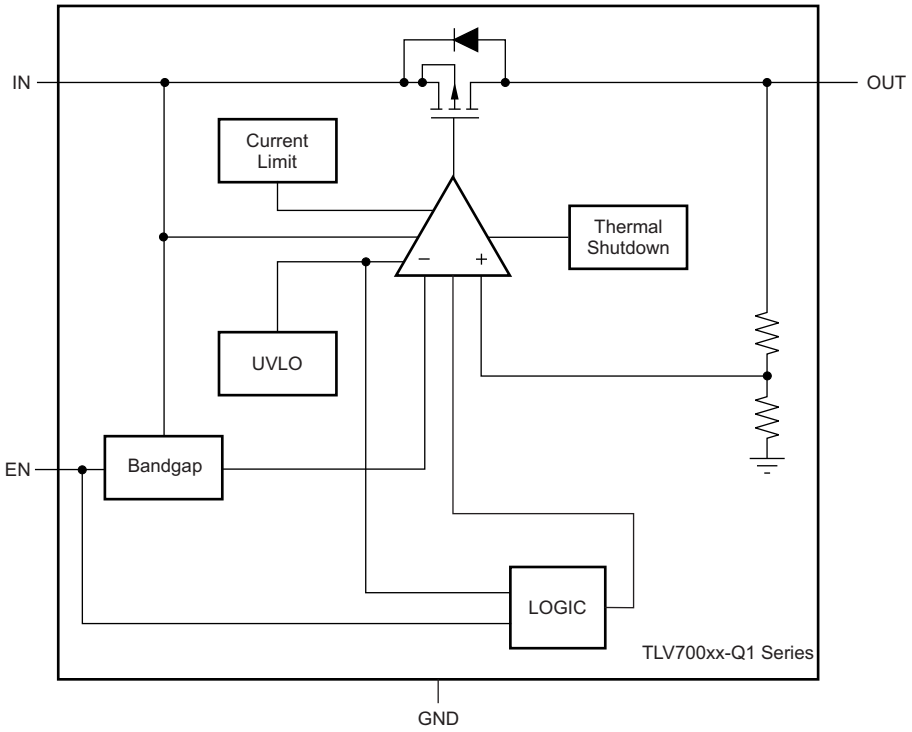

Figure 8. Functional Block Diagram

3 System Design Theory

The circuit organization of TIDA-00804 provides an initial buck regulator from the 6 V to 42 V input voltage to 5 V. The circuit organization allows the subsequent buck regulators to utilize smaller, less expensive components for the filter capacitors and facilitates the use of a linear regulator for VDD_SNVS_IN on the i.MX6Q.

Other than requiring that VDD_SNVS_IN must be applied before any other voltage, the i.MX6 does not require any specific power rail sequence during power-up, and there is no requirement for sequencing during power-down. However, the TIDA-00804 design does cascade the power supply enables by linking the power good signal from one power supply to the enable of the next supply in the sequence. The main 5-V supply powers up when input power is supplied. The 3V ÷ 0.15 A supply is enabled without time delay and it starts to power up as the 5 V rail is coming up. The 1.425 V core supply is enabled by the 3-V VDD_SNVS_IN supply. The 1.5 V DDR supply is enabled by the power good signal from the 1.425 V core supply. The 3.3 V I/O supply is enabled by the power good signal from the 1.5 V supply. Lastly, the 1.8 V supply is enabled by the power good signal from the 3.3 V supply. The I.MX6 does not start the boot process until all power supplies connected have stabilized.

Three of the four switching power supplies in TIDA-00804 have the capability of being synchronized to external clocks and the circuits contain components to facilitate using external clocks. The sync function was not tested in this design, and the parts for testing sync are not populated on the board.

The frequency for each switching power supply in the design may be set by the designer. To ensure that the switching frequencies of the regulators do not produce noise in the AM radio broadcast band, the switching frequencies have been set to values above 1,850 kHz. All of the switching power supply circuits also contain placeholders for snubber network RC circuits, but testing has shown that snubbers are not required.

3.1 TPS54561-Q1

Figure 9 shows the TPS54561-Q1 circuit.

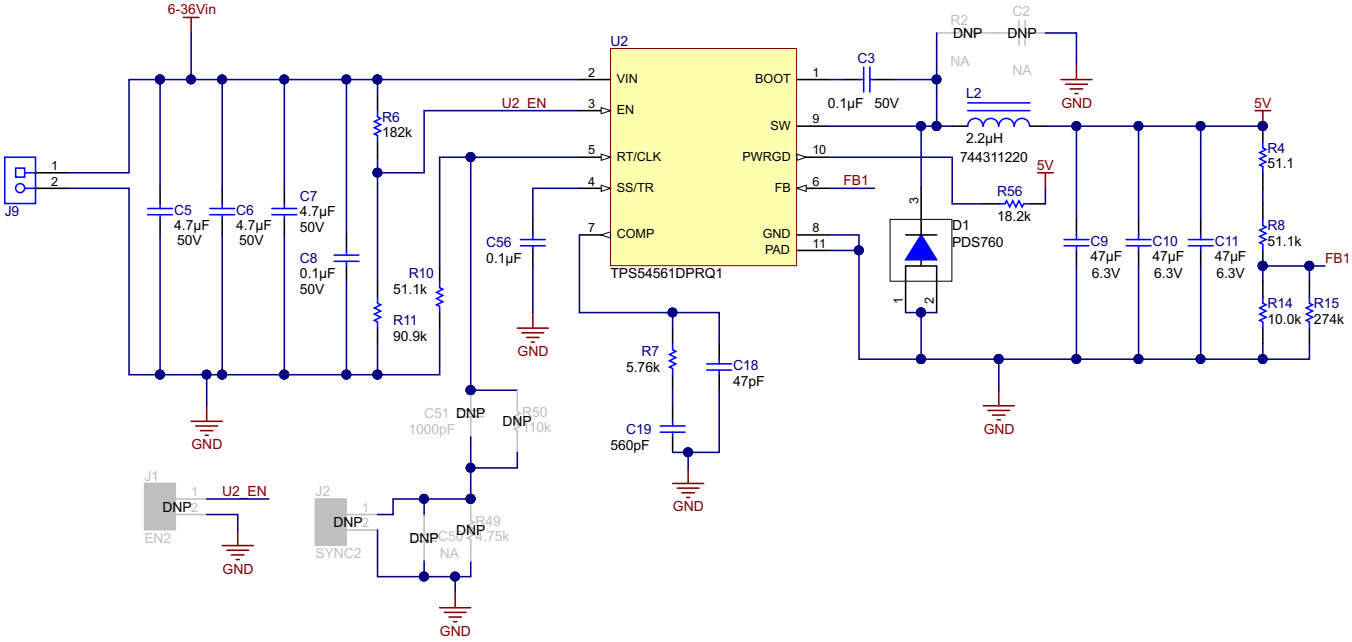

Figure 9. TPS54561-Q1 Circuit

The TPS54561-Q1 Is the primary regulator in the system. All other power rails are derived from the output. The output rating of 4 A is required to provide enough capacity to supply the power required by the other voltage regulators in the design. This regulator was chosen for number of reasons. The regulator has a wide input voltage characteristic, the ability to withstand a load dump from the automobile's charging system, and does not require external FETs for switching. The regulator also has a configurable switching frequency that may be set above the AM radio broadcast band.

The first design consideration for this regulator is the switching frequency. The output frequency is set by the value of resistance at pin RT/CLK. For the TPS54561-Q1 to have a switching frequency above the worldwide AM radio bands, the switching frequency must be set above 1,800 kHz. Choosing a target of 1,900 kHz allows some tolerance in the frequency due to resistance tolerance and drift over temperature. A standard 1% resistor value of 51.1 kΩ is chosen for R10, which is RT in this circuit. The output voltage is set by R4, R8, R14 and R15.

The value for filter inductor, L2, is calculated using equation 31 from the *TPS54561-Q1 4.5-V to 60-V Input, 5-A, Step-Down DC-DC Converter With Eco-mode™* datasheet (SLVSC60). The variable K_{ind} is chosen as 0.3 since ceramic output capacitors will be used. The inductor value is calculated as shown in Equation 1.

$$L_{(O)min} = \left(\frac{V_{Imax} - V_O}{I_O \times K_{(IND)}} \right) \times \left(\frac{V_O}{V_{Imax} \times f_{sw}} \right) = \left(\frac{42\ V - 5\ V}{4\ A \times 0.3} \right) \times \left(\frac{5\ V}{42\ V \times 1{,}900{,}000\ Hz} \right) = 1.88\ \mu H \quad (1)$$

A standard inductor value of 2.2 µH was used. The output capacitors C9, C10, and C11 are each 47 µF and result in a total capacitance of 141 µF. The total capacitance will insure good transient performance and low voltage ripple. The catch diode, D1, has an average current rating of 7A, though the diode will not have to conduct continuously. The diode's reverse withstanding voltage is 60 V. The input capacitors C5, C6, C7 and C8 have a total value of 14.2 µF. C8 is provided for high frequency filtering. The voltage ratings on these capacitors are 50V, which limits the maximum input voltage to 50 V or less. R6 and R11 set the threshold voltage to enable the TPS54561-Q1. The part is enabled once the input voltage is above 3.87 V.

3.2 TLV70030-Q1

Figure 10 shows the TLV70030-Q1 circuit.

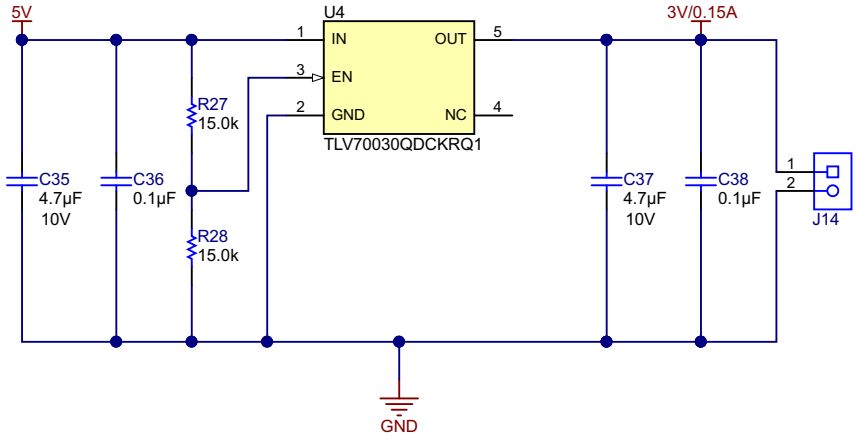

Figure 10. TLV70030-Q1 Circuit

The TLV70030-Q1 supplies VDD_HIGH_IN and VDD_SNVS_IN on the i.MX6Q. The maximum load for these two power rails will not exceed 130 mA, so the load capability of the TLV70030-Q1 is ideal for this application. The design of the TLV70030-Q1 section is simple. The input and output filter capacitors are 4.7 uF and 0.1 uF. The 0.1 uF capacitors provide extra high frequency filtering at both the input and output. 4.7 uF filter capacitors are used to insure there is enough capacity for any power consumption transients.

The TLV70030-Q1 is enabled when its enable pin is above 0.9V. For this design, the enable pin is connected to the junction of a resistor divider connected from net 5V to ground. Since the divider voltage will be one-half the voltage on 5V. Therefore, the TLV70030-Q1 will be enabled once 5V reaches 1.8 V and the 3V output will track the 5V input rise. This is important because VDD_SNVS_IN should be powered up before the other voltage rails are applied to the i.MX6Q.

3.3 TPS57114-Q1

Figure 11 shows the TPS57114-Q1 circuit.

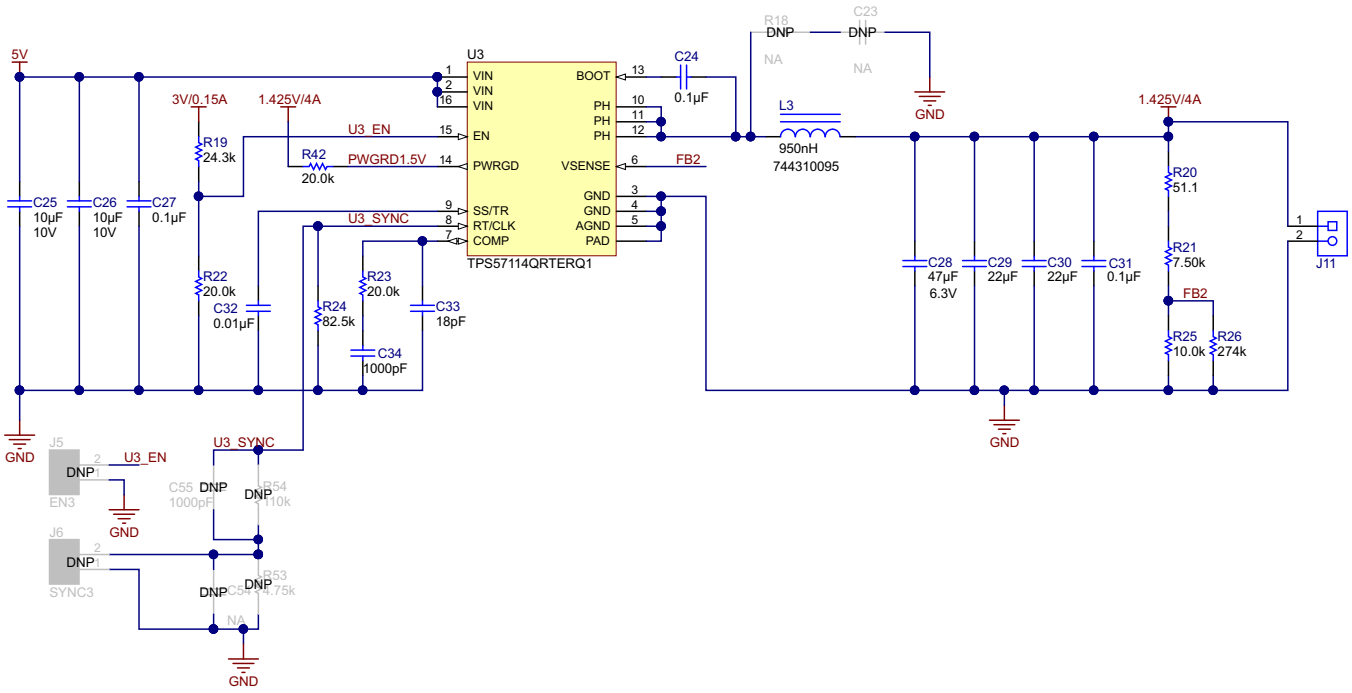

Figure 11. TPS57114-Q1 Circuit

The TPS57114-Q1 was chosen for several reasons. The TPS57114-Q1 has a configurable switching frequency that may be set above 1.8 MHz, out of the AM band. The TPS57114-Q1 also has a high current capacity, a configurable slow start time, a power good signal, and an enable input that are used in power supply sequencing. The TPS57114-Q1 provides the core voltage supply to the i.MX6Q processor, so it has an output current requirement of 4 A at 1.425 V. This power supply is enabled by the 3 V supply. The combination of R19 and R22 form a voltage divider from the 3 V supply that will enable the TPS57114-Q1 when the 3 V supply reaches 2.75 V. In addition, the soft start capacitor, C32 delays the power up by another 4 ms. The combination of the soft start time and the enable voltage allows enough time for VDD_SNVS_IN to reach 2.8 V before the core supply finishes ramping up.

The switching frequency for the TPS57114-Q1 is set to 2MHz by R24. The input filter for the TPS57114-Q1 is composed of C25, C26, and C27. C27 is a 0.1 µF that helps reduce high frequency noise. C25 and C26 create a total of 20 µF. The output section is filtered by inductor L3 and capacitors C28 through C31. The value of L3 is calculated using Equation 2 from the *TPS57114-Q1 2.95-V to 6-V Input, 4-A Output, 2-MHz, Synchronous Step-Down SWIFT™ Switcher* datasheet (SLVSAH5).

$$L3 = \left(\frac{V_{Imax} - V_O}{I_O \times K_{(IND)}}\right) \times \left(\frac{V_O}{V_{Imax} \times f_{sw}}\right) = \left(\frac{5\ V - 1.425\ V}{4\ A \times 0.2}\right) \times \left(\frac{1.425\ V}{5\ V \times 2{,}000{,}000\ Hz}\right) = 0.64\ \mu H \quad (2)$$

A close standard value of 0.95 µH was chosen for L3. For the output filter capacitors, C31 is another 0.1 uF capacitor for filtering high frequencies, and the combination of C28 through C31 totals 91.1 uF for low-voltage ripple and good transient response.

The power good signal from the TPS57114-Q1 is pulled up to the 1.425-V supply with a 20-kΩ resistor. The power good signal is used to enable the next power supply in the chain when the 1.425-V output has settled.

3.4 TPS54388-Q1

Figure 12 shows the TPS54388-Q1 circuit.

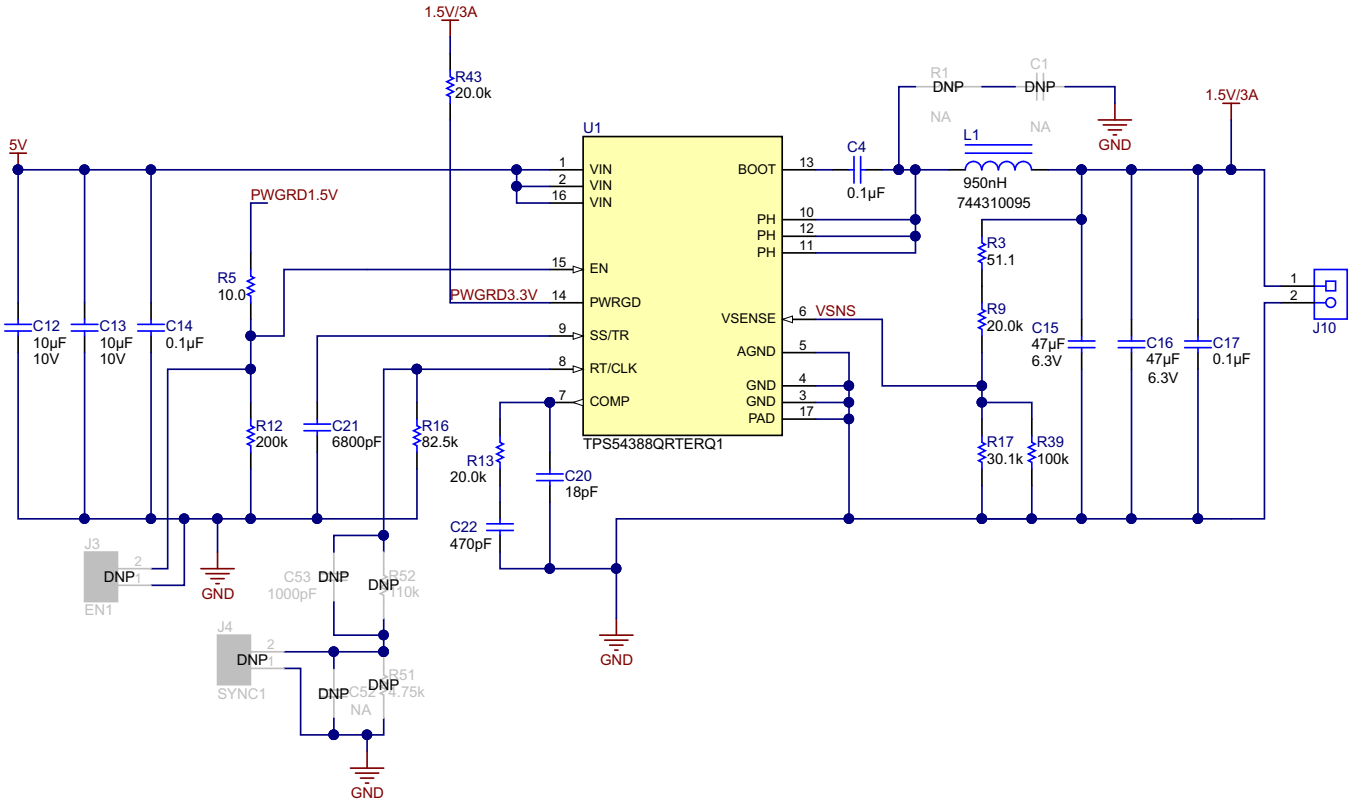

Figure 12. TPS54388-Q1 Circuit

The TPS54388-Q1 was chosen for many of the same reasons as the other switching regulators. The TPS54388-Q1 has a configurable switching frequency that may be set above 1.8 Mhz, a high current capacity, configurable slow start, an enable pin and a power good signal. The TPS54388-Q1 circuit provides the 1.5-V power supply needed for DDR3. The output is rated at 3 A. As mentioned in Section 3.3, the TPS54388-Q1 is enabled when the TPS57114-Q1 power good signal is high. C21 is a 6.8 nF capacitor connected to the SS, or Slow-Start, pin that provides an additional 2.72 ms startup delay.

The switching frequency for the TPS54388-Q1 is set for 2.012 MHz by R16. C12, C13, and C14 provide 20.1 uF of input capacitive filtering. The output inductor, L1, is calculated from Equation 3 in the *TPS54388-Q1 2.95-V to 6-V Input, 3-A Output, 2-MHz, Synchronous Step-Down SWIFT Switcher* datasheet (SLVSAF1).

$$L_1 = \left(\frac{V_{Imax} - V_O}{I_O \times K_{(IND)}}\right) \times \left(\frac{V_O}{V_{Imax} \times f_{sw}}\right) = \left(\frac{5\ V - 1.5\ V}{3\ A \times 0.2}\right) \times \left(\frac{1.5\ V}{5\ V \times 2{,}012{,}000\ Hz}\right) = 0.87\ \mu H \quad (3)$$

Since the value is so close, the same 0.95 µH inductor used for the TPS57114-Q1 circuit is also used here. Output filter capacitance is provided by capacitors C15, C16, and C17. There is a total of 47.1 uF of filter capacitance.

The power good pin is pulled up to the 1.5-V supply output with a 20-kΩ resistor. When the TPS54388-Q1 power is good, the 3.3 V I/O supply is enabled.

3.5 LM26420-Q1

Figure 13 shows the LM26420-Q1 circuit.

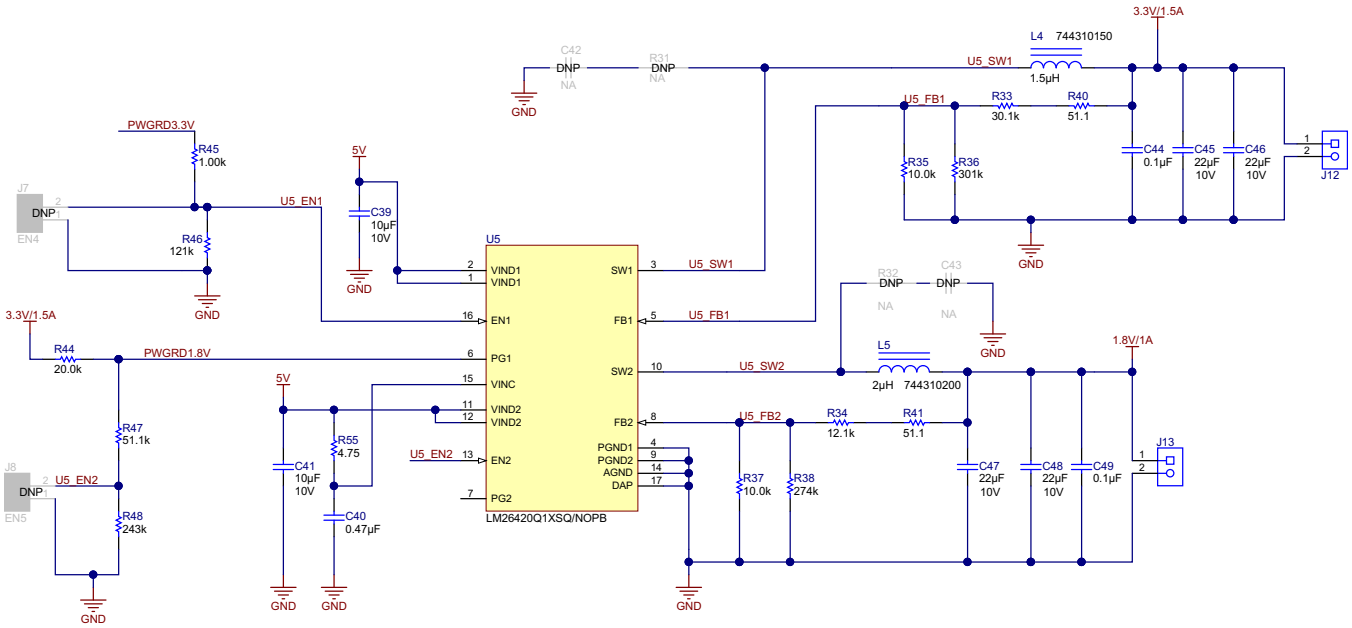

Figure 13. LM26420-Q1 Circuit

The LM26420-Q1 is a dual output buck regulator. It was chosen for this design because it integrates two step-down switching power supplies in one package. The LM26420-Q1 also features a switching frequency that is above the AM radio broadcast band, enable inputs for both power supply sections, and power good signals for use in power sequencing. In this design, output one of the TPS26420-Q1 provides 3.3 V at 1.5 A. Output 2 provides 1.8 V at 1 A. Output 1 is turned on by the power good signal from the TPS54388-Q1 in Section 3.4. Output 2 of the TPS 26420-Q1 is enabled by the power good signal from output one. There are no additional delays in startup for either supply.

The LM26420-Q1 does not have an adjustable operation frequency. Instead, the LM26420-Q1 has a fixed frequency range of 1.85 MHz to 2.65 MHz, which still guarantees that the LM26420-Q1 operates at a frequency above the AM band.

Internal circuitry on the TPS26420-Q1 is powered through pin 15 of the part, which is named VINC. This pin is powered by the 5 V supply through R55, a 4.7 Ω resistor, and is filtered with C40, a 0.47 µF capacitor. This is described in section 8.1.2 of the LM26420-Q1 datasheet. The maximum current into pin 15 is 6.2 mA, so the voltage drop on R55 is only 29 mV. The combination of R55 and C40 create a low pass filter with a cutoff frequency of 72 kHz, which is well below the operating frequencies of all of the power supplies.

Output 1 provides the 3.3 V, 1.5 A power supply. This supply is enabled by the power good signal from the TPS54388-Q1. 10 µF C39 is the input capacitor filter connected to and placed near pins 1 and 2 of the LM26420-Q1. Pins 1 and 2 are the input pins for output one. The output filter consists of L4, C44, C45, and C46. C45 and C46 combined provide 44 µF, and C44 is a 0.1 µF capacitor for high frequency filtering. The inductor values for the LM26420-Q1 are chosen using equations 6 – 13 in the LM26420-Q1 data sheet. For output 1, the inductor is calculated as shown in Equation 4.

$$I_L = \left(\frac{DT_S}{2\Delta i_L}\right) \times \left(V_{IN} - V_{OUT}\right) \tag{4}$$

Where Duty Cycle D is shown in Equation 5.

$$D = \frac{V_{OUT} + \left(I_{out} \times R_{DSon\_BOT}\right)}{V_{IN} + \left(I_{out} \times R_{DSon\_BOT}\right) - \left(I_{out} \times R_{DSon\_TOP}\right)} = \frac{3.3\ V + \left(1.5\ A \times 0.1\right)}{5\ V + \left(1.5\ A \times 0.1\right) - \left(1.5\ A \times 0.135\right)} = 0.697 \tag{5}$$

Δi_L is the difference between the maximum load current and the peak inductor current and is usually about 0.1 I_{out} to 0.2 I_{out}. Taking the worst case of 0.2 I_{out} and substituting into Equation 5,

$$L = \left(\frac{DT_S}{2\Delta i_L}\right) \times \left(V_{in} - V_{out}\right) = \left(\frac{0.697\left(\frac{1}{1{,}850{,}000}\right)}{2(0.2)(1.5\ A)}\right) \times (5 - 3.3) = 1.067 \times 10^{-6}\ H = 1.067\ \mu H \quad (6)$$

The value for L4 is selected as a 1.5 µH, which is close to the calculated value.

Output 2 provides the 1.8 V, 1-A power supply. This supply is enabled by the power good signal from output 1 of the LM26420-Q1. 10 µF C41 is the input capacitor filter connected to and placed near pins 11 and 12 of the LM26420-Q1. Pins 11 and 12 are the input pins for output two. The output filter consists of L5, C47, C48, and C49. C47 and C48 combined provide 44 µF, and C49 is a 0.1 µF capacitor for high frequency filtering, similar to the filter for output 1. L5 is calculated in the same manner shown in Equation 5 and Equation 6.

$$D = \frac{V_{OUT} + \left(I_{out} \times R_{DSon\_BOT}\right)}{V_{IN} + \left(I_{out} \times R_{DSon\_BOT}\right) - \left(I_{out} \times R_{DSon\_TOP}\right)} = \frac{1.8\ V + (1\ A \times 0.1)}{5\ V + (1\ A \times 0.1) - (1\ A \times 0.135)} = 0.383 \quad (7)$$

$$L = \left(\frac{DT_S}{2\Delta i_L}\right) \times \left(V_{in} - V_{out}\right) = \left(\frac{0.383\left(\frac{1}{1{,}850{,}000}\right)}{2(0.2)(1\ A)}\right) \times (5 - 1.8) = 1.65 \times 10^{-6}\ H = 1.65\ \mu H \quad (8)$$

The standard value 2 µH is chosen for L5.

The output power good signal is not connected to a pull-up resistor because it is not used elsewhere in the power supply. This is the last voltage to power up.

4 Test Data

The following sections describe the performance data collected on each power supply.

4.1 Test Equipment Used

- **Multi-meter(current):** Fluke 8845A
- **Multi-meter (voltage):** Fluke 187
- **DC Source:** Chroma 61530
- **Electronic load:** Chroma 63110A module
- One PMP4442 circuit board

4.2 Test Setup

Input power was provided by the Chroma 61530 power supply. The input power was wired to power input connector J9. The input voltage was set for 12 V for all tests. Each supply output was tested individually using the Chroma 63110A Electronic load. The multi meters were used to measure voltage and output current.

4.3 Output Characteristics

4.3.1 TPS54561-Q1 for 5 V at 4 A

4.3.1.1 Output Load Regulation

The output of the TPS54561-Q1 was tested with loads ranging from 0 A to the design target of 4 A. Table 2 lists the output regulation data for the TPS54561-Q1 and the data is graphed in Figure 14. The input voltage was 12 V.

Table 2. Output Regulation Data for the TPS54561-Q1

OUTPUT CURRENT (A)	OUTPUT VOLTAGE (V)
No load	5.057
0.50	5.051
1.00	5.049
1.50	5.048
2.00	5.047
2.50	5.046
3.00	5.045
3.50	5.044
4.00	5.042

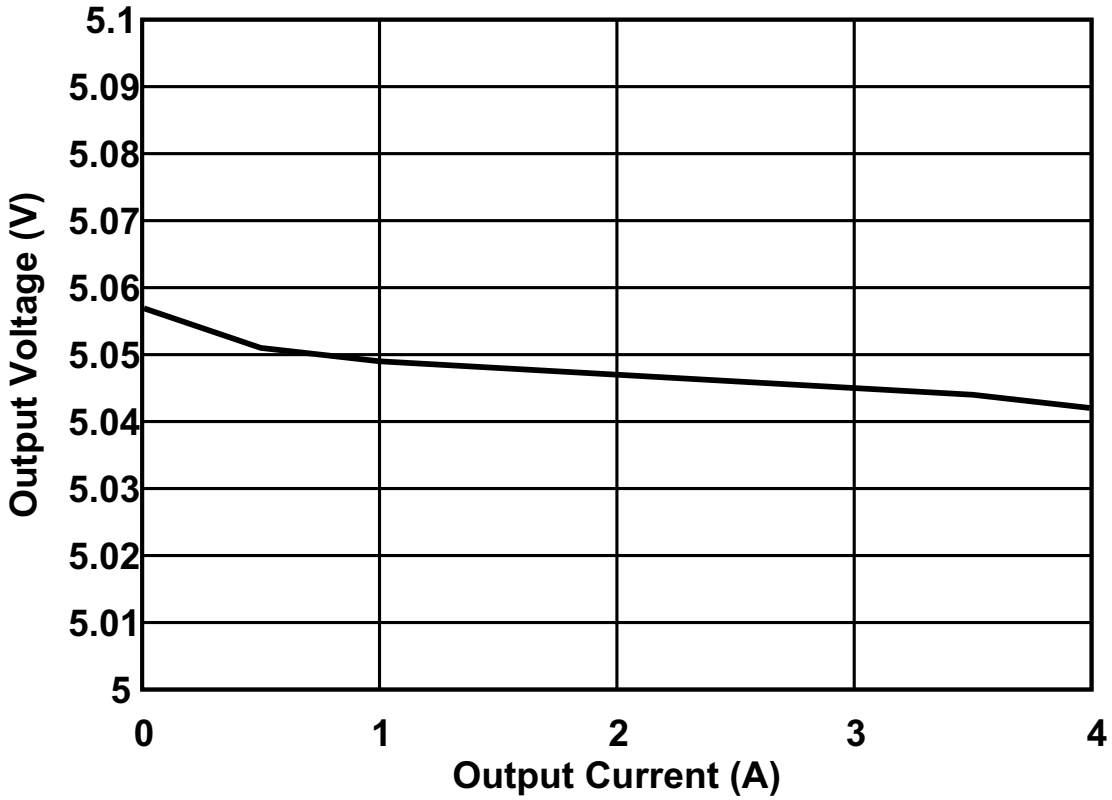

Figure 14. TPS54561-Q1 Load Regulation

The output voltage deviation is only 15 mV between the no load and 4 A of output.

4.3.1.2 Output Ripple Voltage

The TPS54561-Q1 output ripple was measured on an oscilloscope with the circuit conditions with 12 V of input voltage and 4 A load current. The measured ripple was 17 mVp-p, and Figure 15 shows the oscilloscope plot.

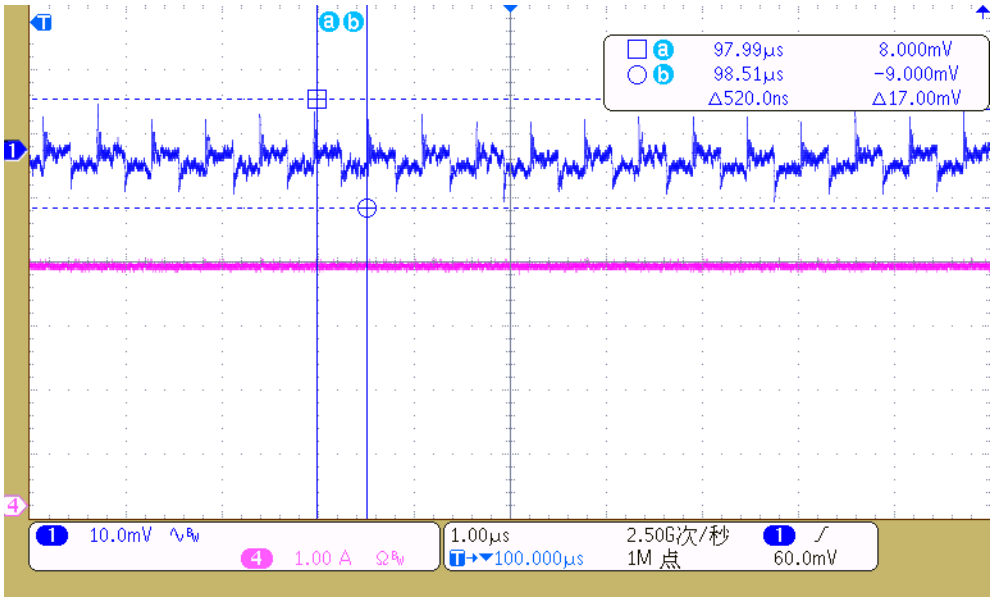

Figure 15. TPS54561-Q1 Output Ripple Voltage

4.3.1.3 Dynamic Response

The output dynamic response of the TPS54561-Q1 was measured with 12 V of input voltage and a load that varied between 0 A and 2 A. The load step pulse width was 516 µs and the rise and fall time was 2.5 A per µs. The load step was controlled by the dynamic load. The maximum voltage deviation was 232 mVp-p as shown in Figure 16.

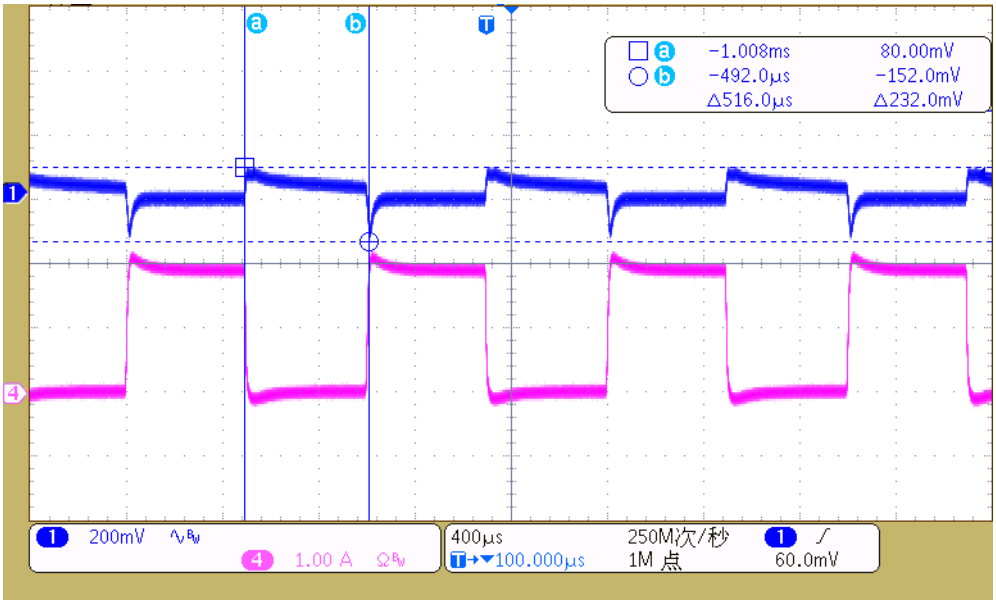

Figure 16. TPS54561-Q1 Load Step Response, 0 A to 2 A

Next, the load step response was measured again with a load step from 2 A to 4 A and a pulse width of 512 µs and the rise and fall time was 2.5 A/ µs. The output voltage deviation was 200 mVp-p as shown in Figure 17.

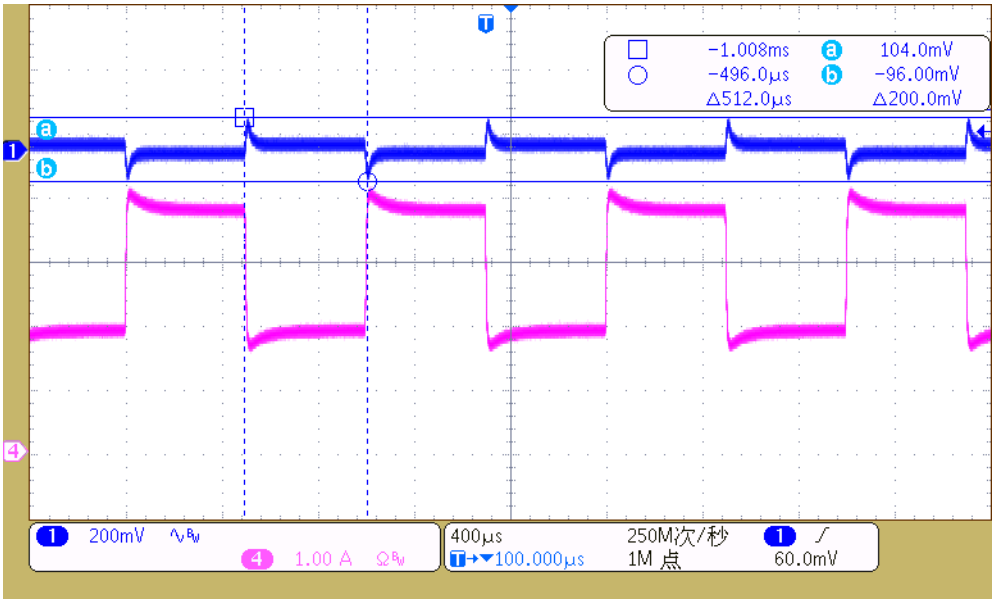

Figure 17. TPS54561-Q1 Load Step Response, 2 A to 4 A

Finally, the load step response was measured with a load step from 0 A to 4 A and a pulse width of 510 µs (1.961 kHz), and the rise and fall time was 2.5 A per µs. The output voltage deviation was 424 mVp-p as shown in Figure 18.

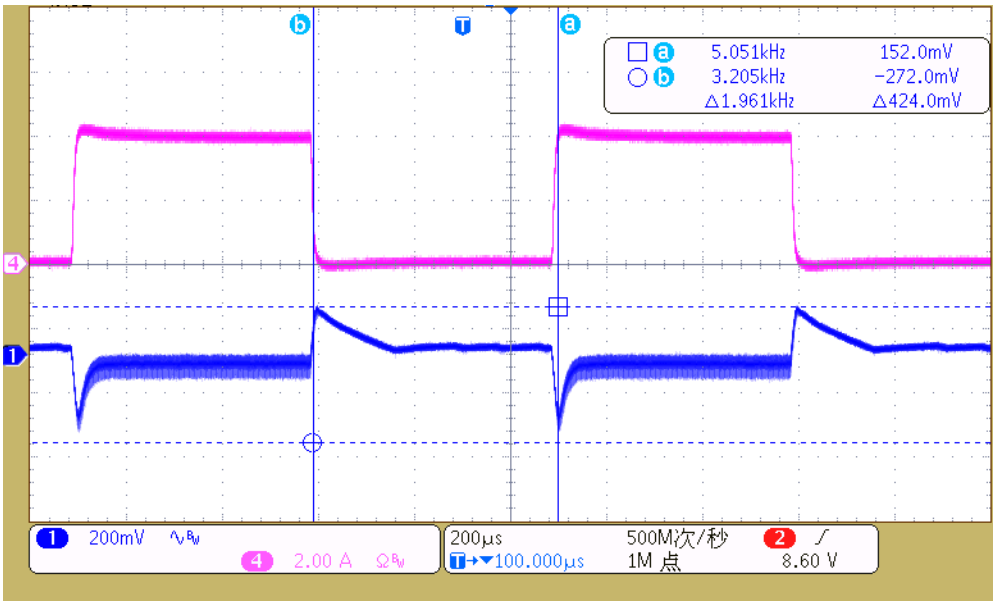

Figure 18. TPS54561-Q1 Load Step Response, 0 A to 4 A

4.3.2 TPS54388 for 1.5 V at 3 A

4.3.2.1 Output Regulation

The output of the TPS54388-Q1 was tested with loads ranging from 0 A to 3 A, and Table 3 lists the results. The data is graphed in Figure 19. The input voltage of 12 V was applied to the input of the TPS54561-Q1 5 V regulator, thus, the input to the TPS54388-Q1 is 5 V.

Table 3. Output Regulation Data for the TPS54388-Q1

OUTPUT CURRENT (A)	OUTPUT VOLTAGE (V)
NO LOAD	1.4975
0.50	1.4948
1.00	1.4930
1.50	1.4915
2.00	1.4900
2.50	1.4885
3.00	1.4871

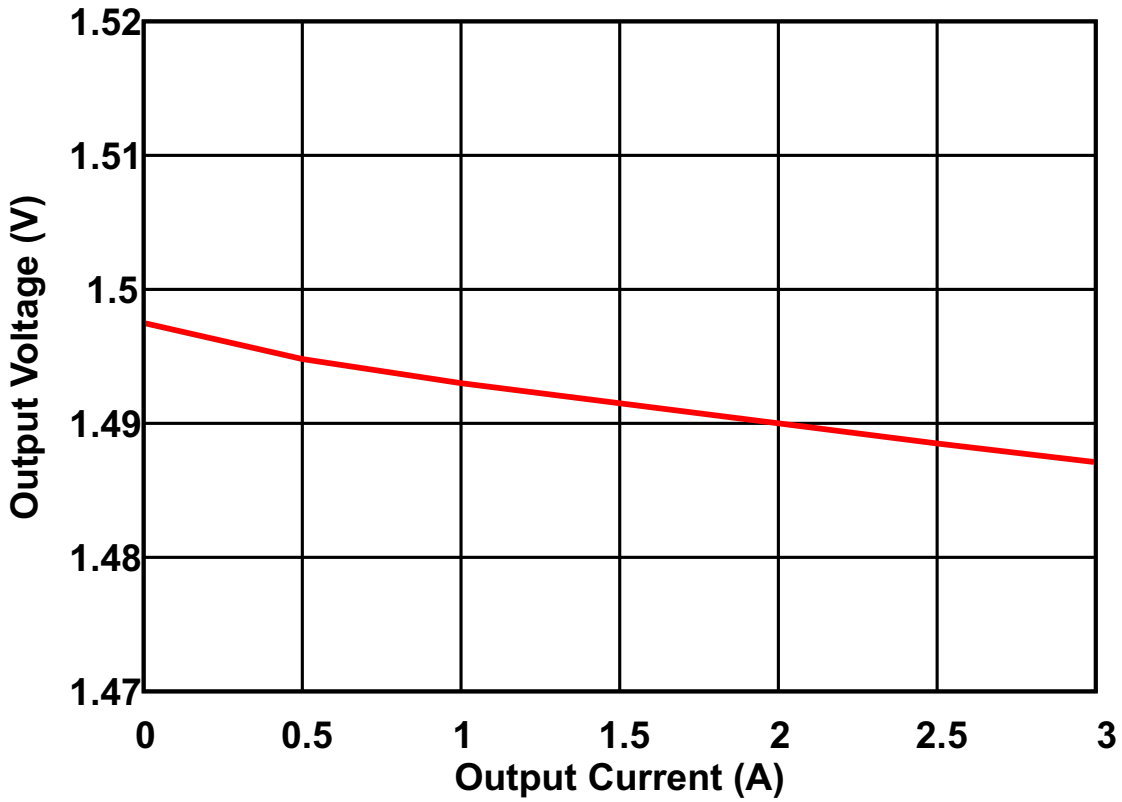

Figure 19. TPS54388-Q1 Load Regulation

The output voltage of the TPS54388-Q1 only varied by 10.4 mV between the no load and the 3 A load conditions.

4.3.2.2 Output Ripple Voltage

The TPS54388-Q1 output ripple was measured with a 3 A load current. The measured ripple was 24.6 mVp-p. Figure 20 shows the oscilloscope plot.

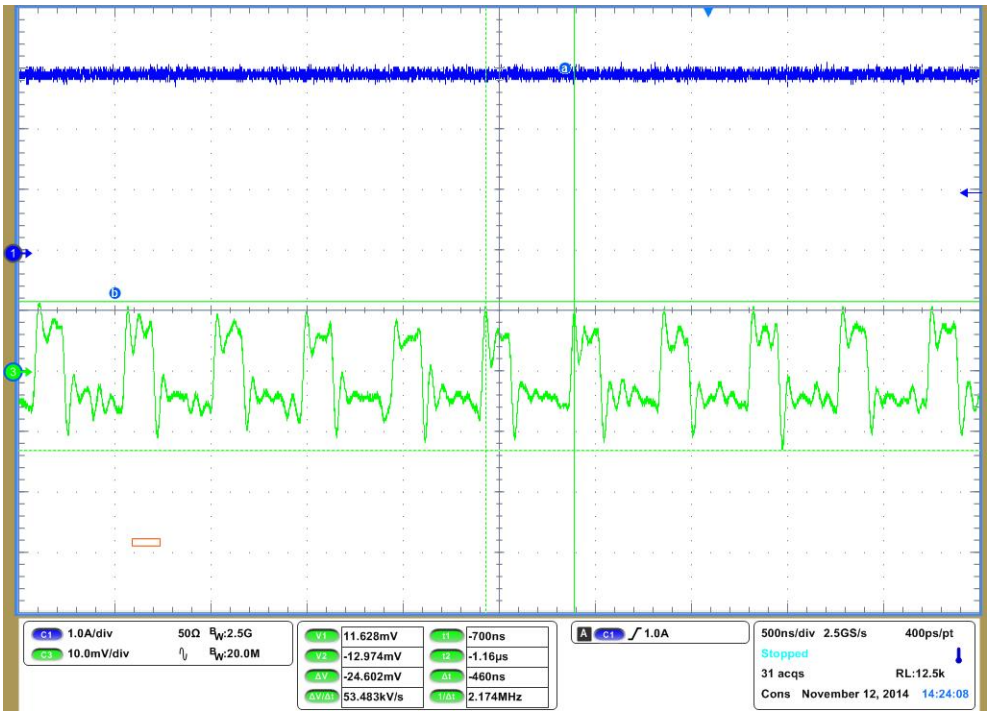

Figure 20. TPS54388-Q1 Output Voltage Ripple

4.3.2.3 Dynamic Response

The output dynamic response of the TPS54388-Q1 was measured with load steps of 0 A to 1.5 A, 1.5 A to 3 A, and 0 A to 3 A. The load step pulse width was between 496 µs and 512 µs. The load step rise and fall time was 2.5 A per µs. For the 0 to 1.5 A load step, the maximum voltage deviation was 87.1 mVp-p as shown in Figure 21.

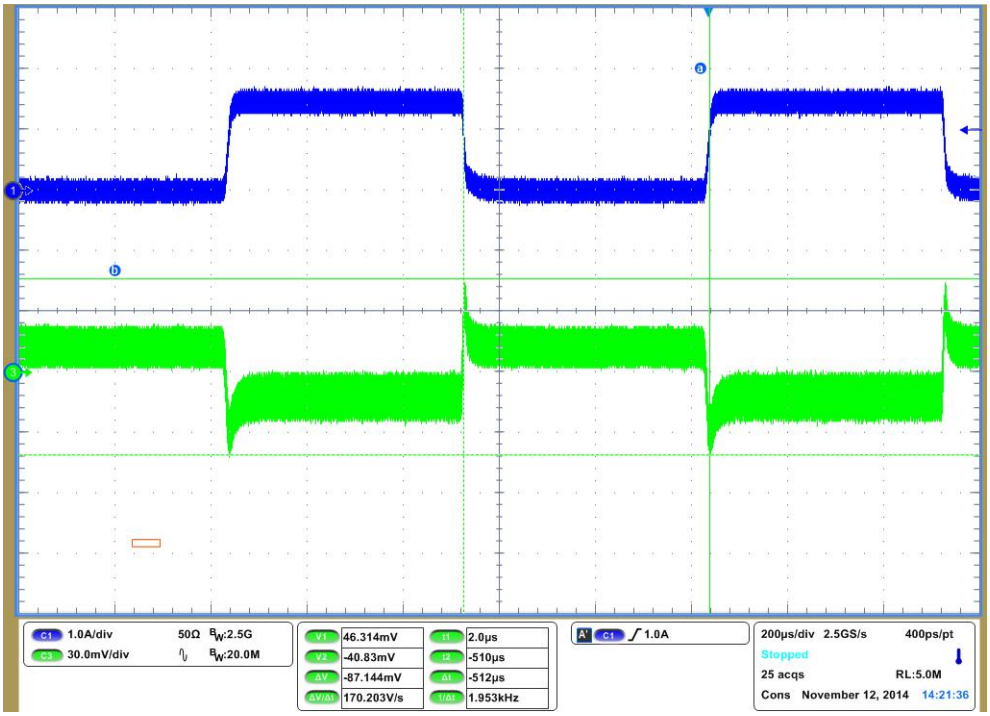

Figure 21. TPS54388 Load Step Response, 0 A to 1.5 A

For the 1.5 A to 3 A load step, the maximum voltage deviation was 108 mVp-p as shown in Figure 22.

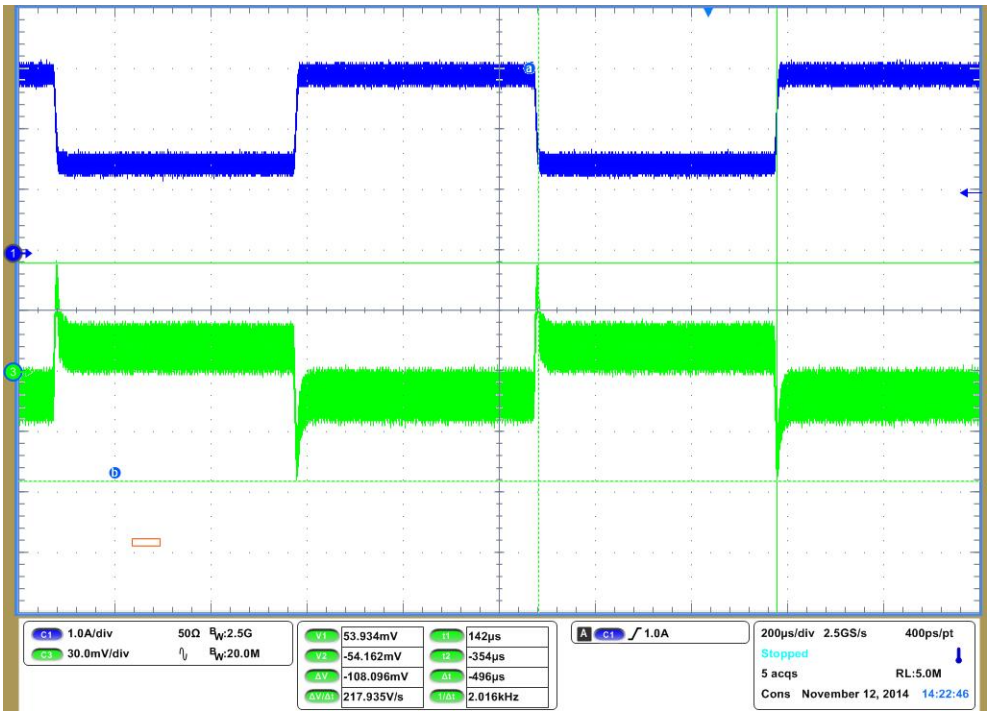

Figure 22. TPS54388 Load Step Response, 1.5 A to 3 A

For the 0 A to 3 A load step, the maximum voltage deviation was 145 mVp-p as shown in Figure 23.

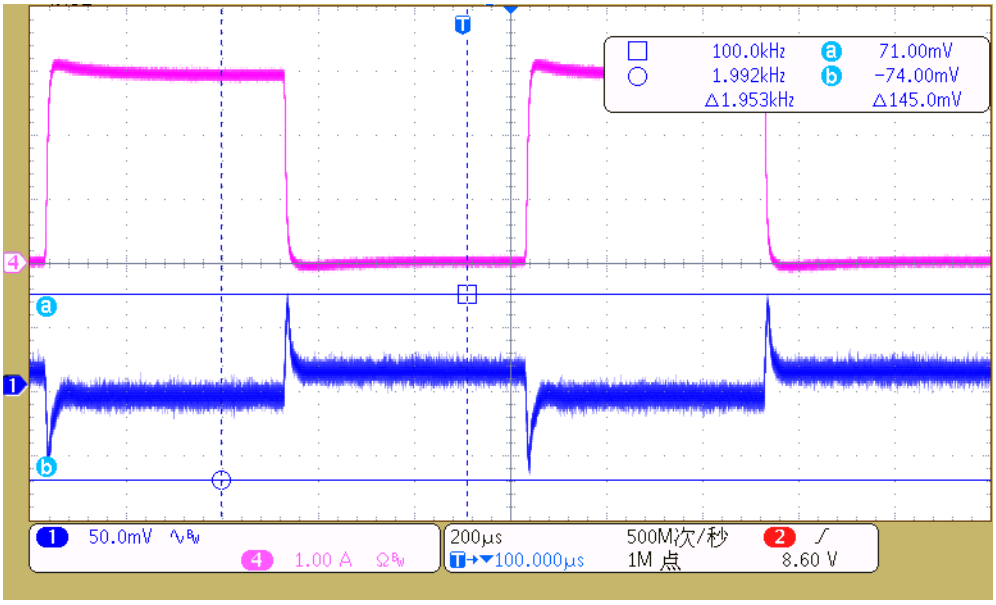

Figure 23. TPS54388 Load Step Response, 0 A to 3 A.

4.3.3 TPS57114 for 1.425 V at 4 A

4.3.3.1 Output Regulation

The output of the TPS57114-Q1 was tested with loads ranging from 0 A to 4 A. The results are listed in Table 4 and the data is graphed in Figure 24 . The input to the TPS57114-Q1 is 5 V.

Table 4. Output Regulation Data for the TPS57114-Q1

OUTPUT CURRENT (A)	OUTPUT VOLTAGE (V)
0	1.4251
0.50	1.4237
1.00	1.4227
1.50	1.4219
2.00	1.4211
2.50	1.4203
3.00	1.4195
3.50	1.4188
4.00	1.4181

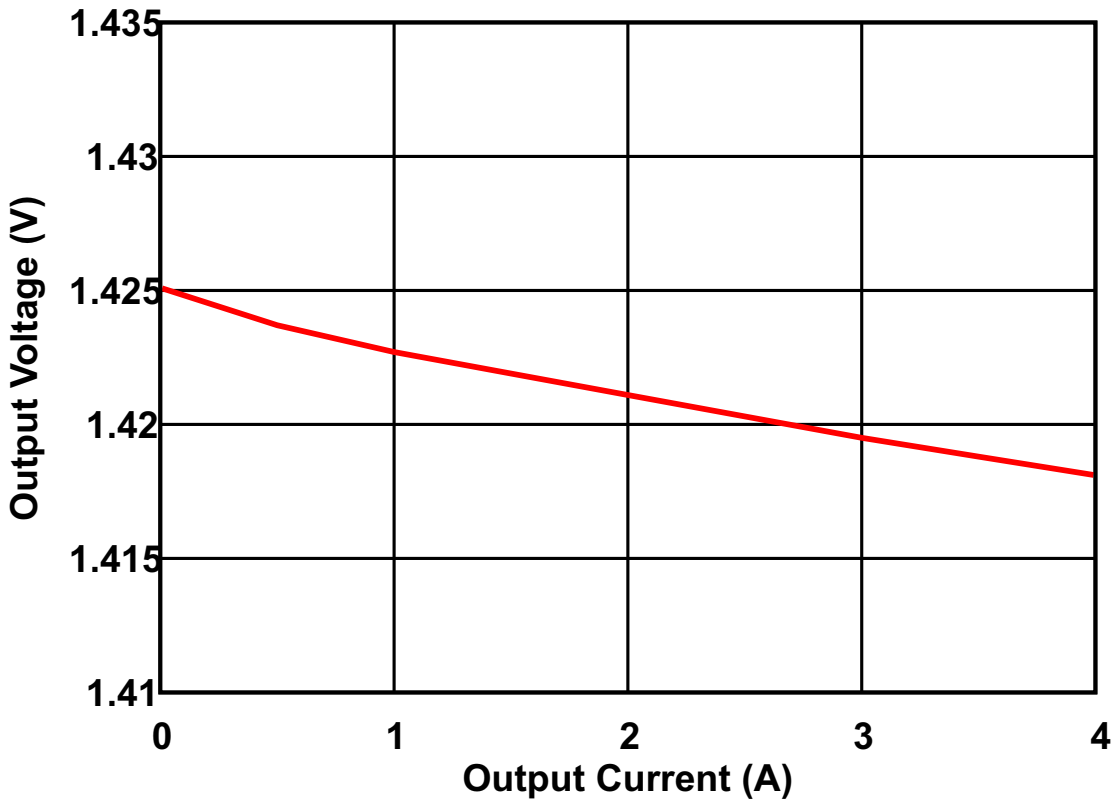

Figure 24. TPS57114-Q1 Load Regulation

The output voltage of the TPS57114-Q1 only varied by 7 mV between the no load and the 4 A load conditions.

4.3.3.2 Output Ripple Voltage

The TPS7115-Q1 output ripple was measured with a 4 A load current. The measured ripple was 23.5 mVp-p. Figure 25 shows the oscilloscope plot.

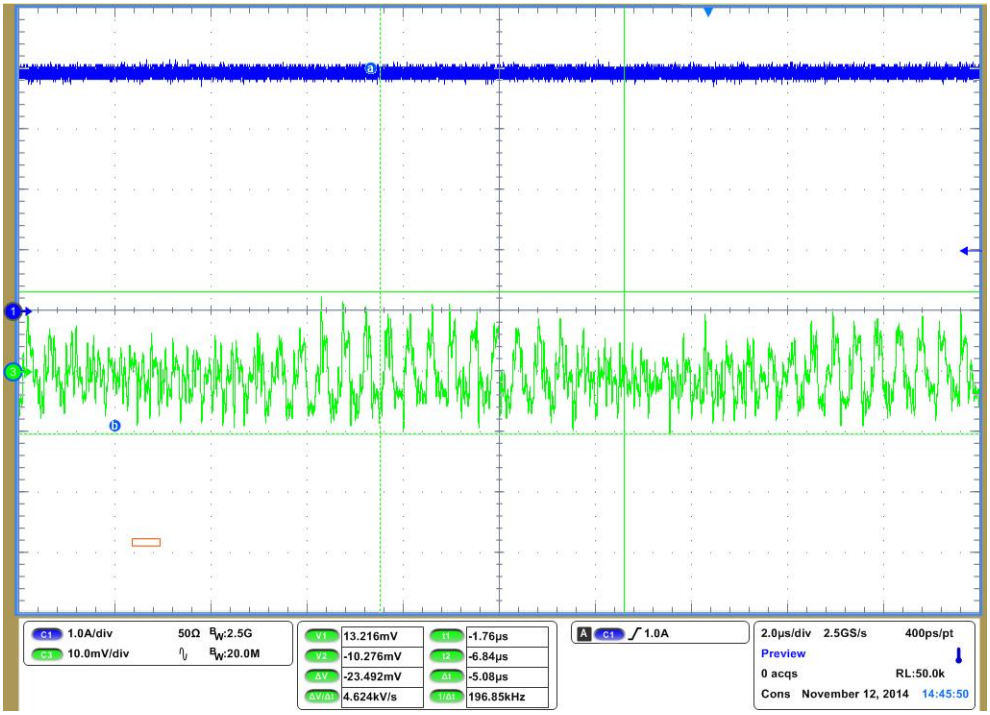

Figure 25. TPS57114-Q1 Output Voltage Ripple With a 4-A Load

4.3.3.3 Dynamic Response

The output dynamic response of the TPS57114-Q1 was measured with load steps of 0 A to 2 A, 2 A to 4 A, and 0 A to 4 A. The load step pulse width was between 504 µs and 508 µs. The load step rise and fall time was 2.5 A/µs. For the 0 to 2 A load step, the maximum voltage deviation was 130 mVp-p, as shown in Figure 26.

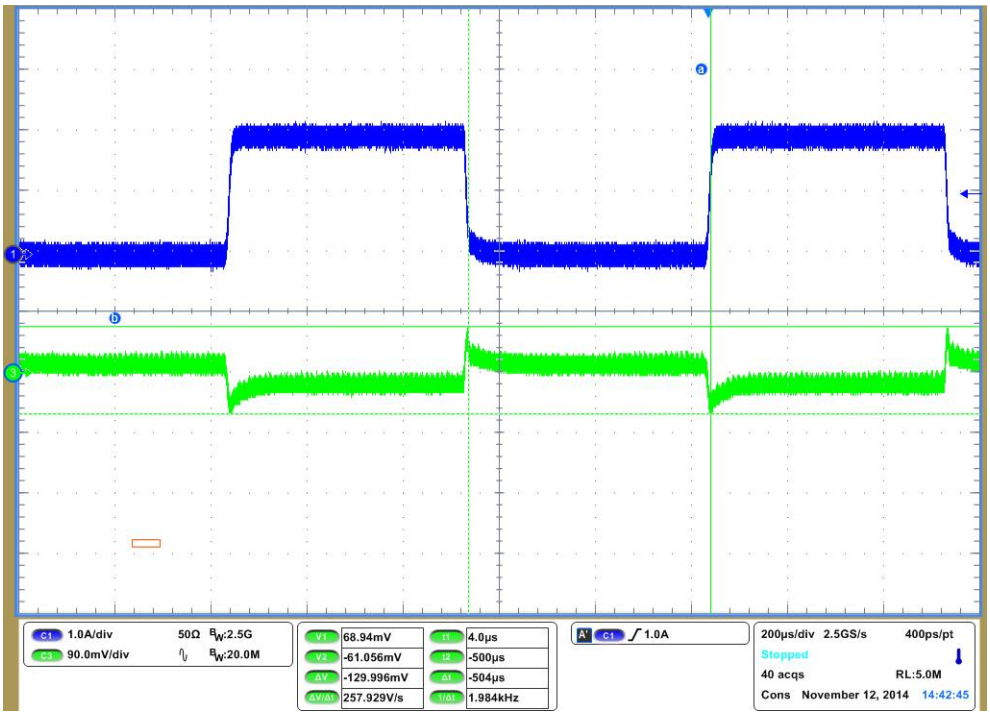

Figure 26. TPS57114-Q1 Load Step Response, 0 A to 2 A

For the 2 A to 4 A load step, the maximum voltage deviation was 142.8 mVp-p, as shown in Figure 27.

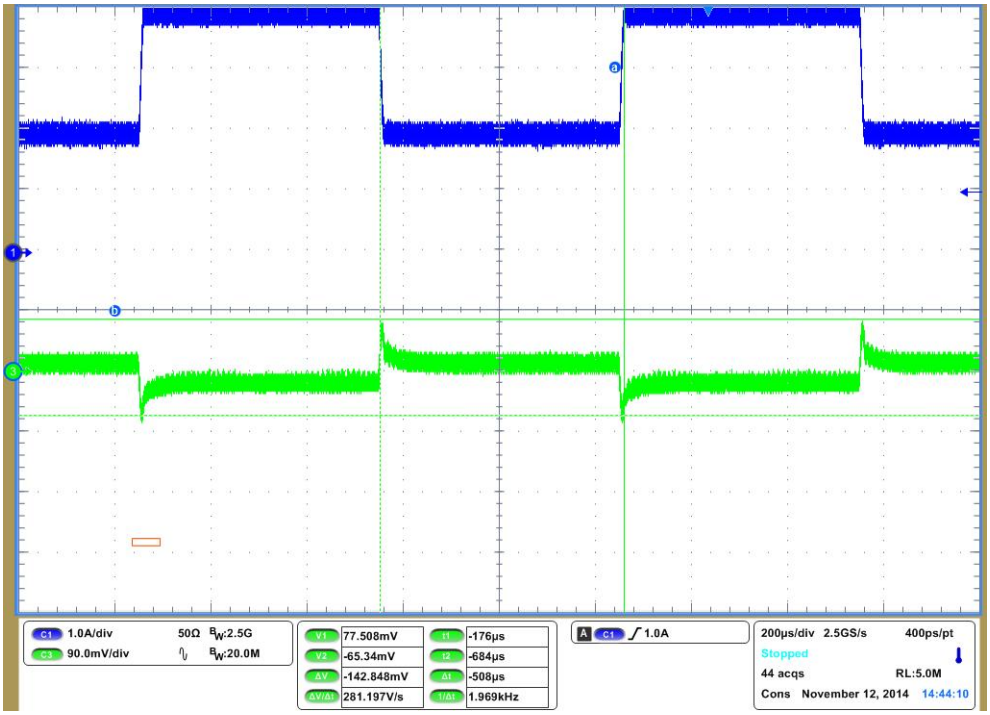

Figure 27. TPS57114-Q1 Load Step Response, 2 A to 4 A.

For the 0 A to 4 A load step, the maximum voltage deviation was 212 mVp-p, as shown in Figure 28.

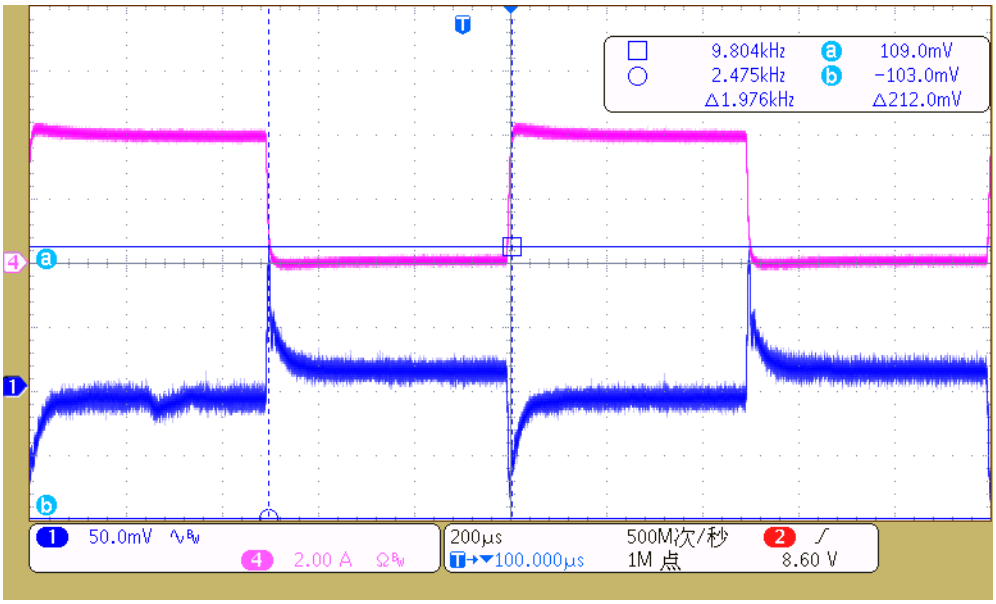

Figure 28. TPS57114-Q1 Load Step Response, 0 A to 4 A

4.3.4 LM26420 for 1.8 V at 1 A

4.3.4.1 Output Regulation

Output two of the LM26420-Q1 was tested with loads ranging from 0 A to 1 A. The results are listed in Table 5 and the data is graphed in Figure 29. The input to the LM26420-Q1 is 5 V.

Table 5. Output Regulation Data for LM26420-Q1, Section Two (1.8 V Output)

OUTPUT CURRENT (A)	OUTPUT VOLTAGE (V)
0	1.8005
0.20	1.8005
0.40	1.8004
0.60	1.8003
0.80	1.8002
1.00	1.8001

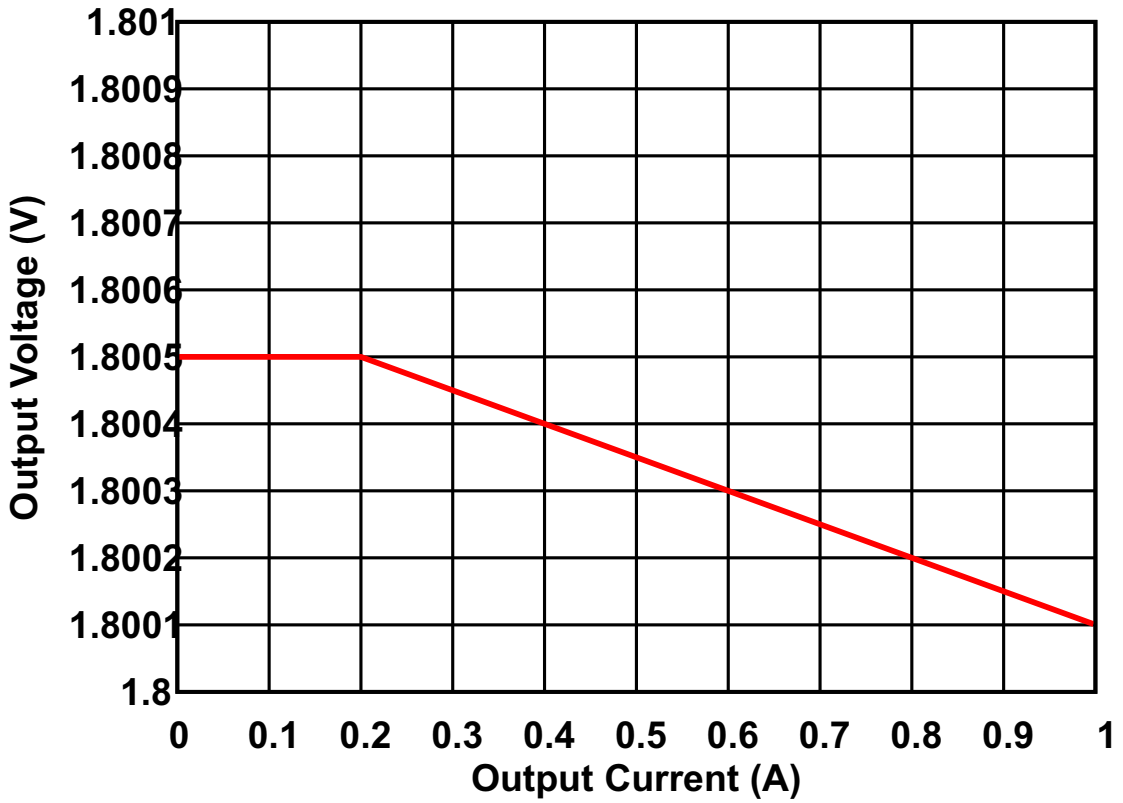

Figure 29. LM26420-Q1 Load Regulation

The 1.8 V output voltage of the LM26420-Q1 varied by less than 1 mV between the no load and the 1 A load conditions.

4.3.4.2 Output Ripple Voltage

The LM26420-Q1 output ripple was measured with a 1-A load current. The measured ripple was 17.3 mVp-p. Figure 30 shows the oscilloscope plot.

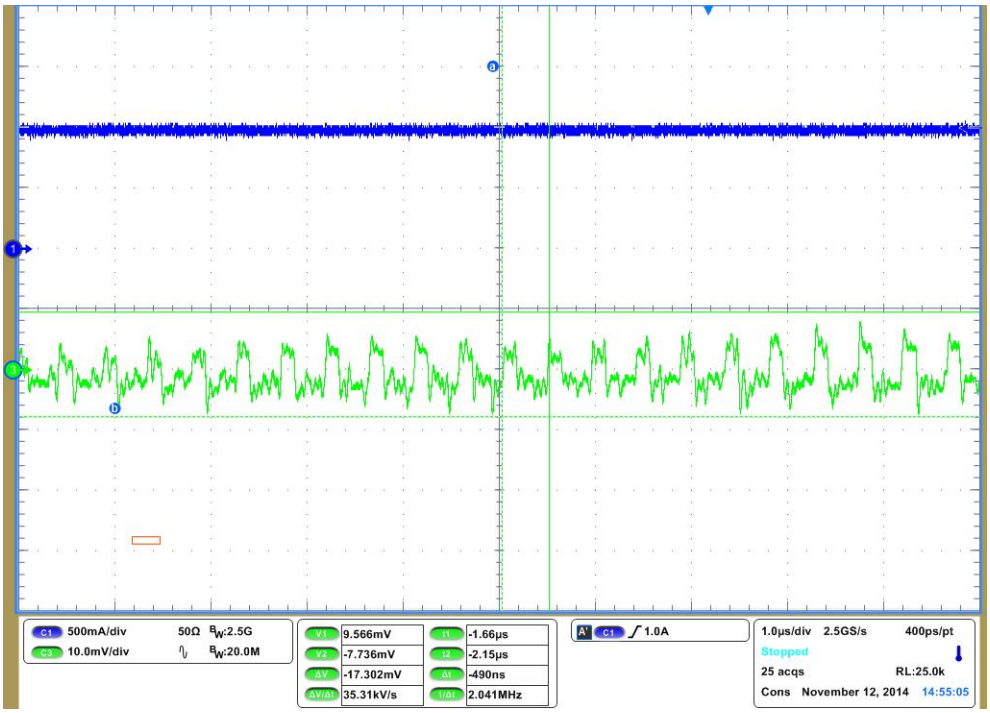

Figure 30. LM26420-Q1 1.8V Output Voltage Ripple with a 1 A Load

4.3.4.3 Dynamic Response

The output dynamic response of the LM26420-Q1 1.8 V output was measured with load steps of 0 A to 0.5 A, 0.5 A to 1 A, and 0 A to 1 A. The load step pulse width was between 480 µs and 512 µs. The load step rise and fall time was 2.5 A per µs. For the 0 to 0.5 A load step, the maximum voltage deviation was 67 mVp-p, as shown in Figure 31.

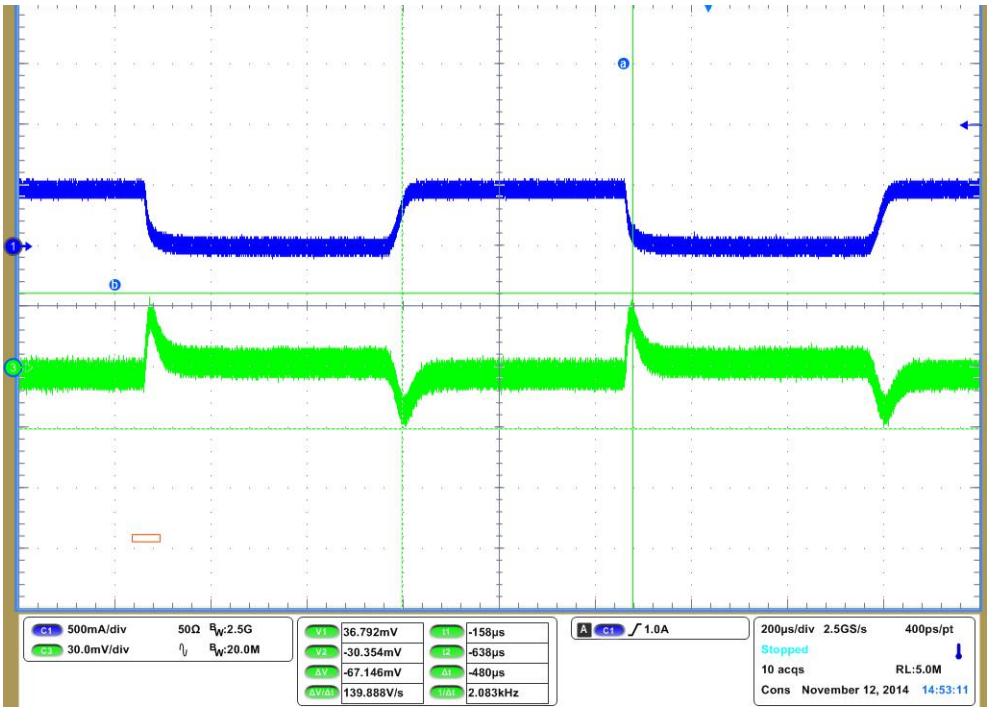

Figure 31. LM26420-Q1 Load Step Response, 0 A to 0.5 A

For the 0.5 A to 1 A load step, the maximum voltage deviation was 90 mVp-p, as shown in Figure 32.

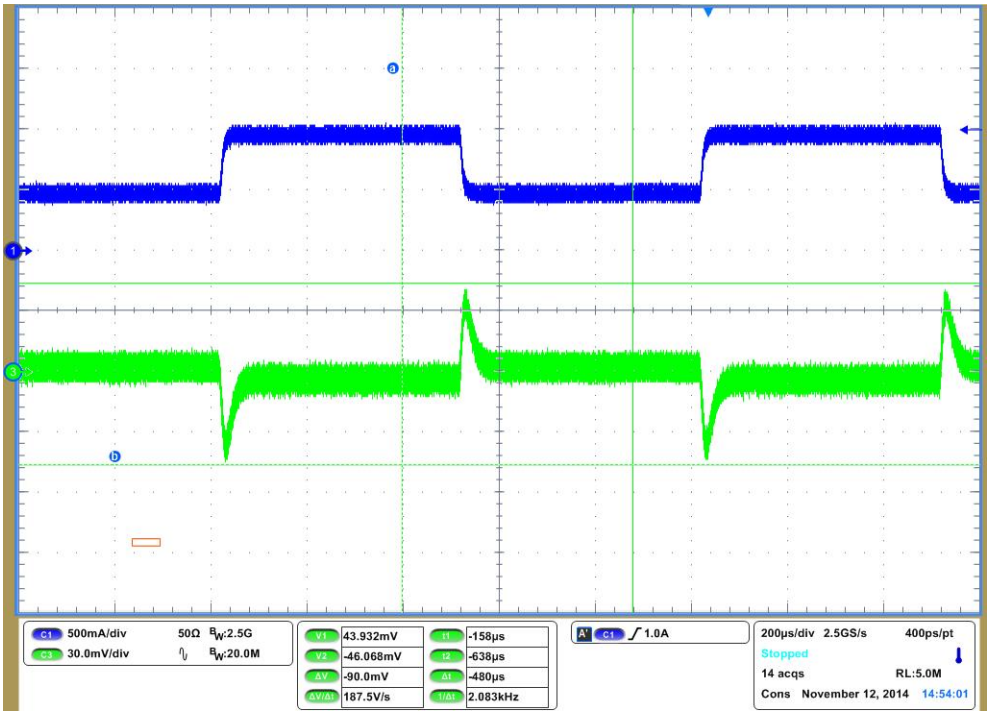

Figure 32. LM26420-Q1 Load Step Response, 0.5 A to 1 A

For the 0 A to 1 A load step, the maximum voltage deviation was 148 mVp-p, as shown in Figure 33.

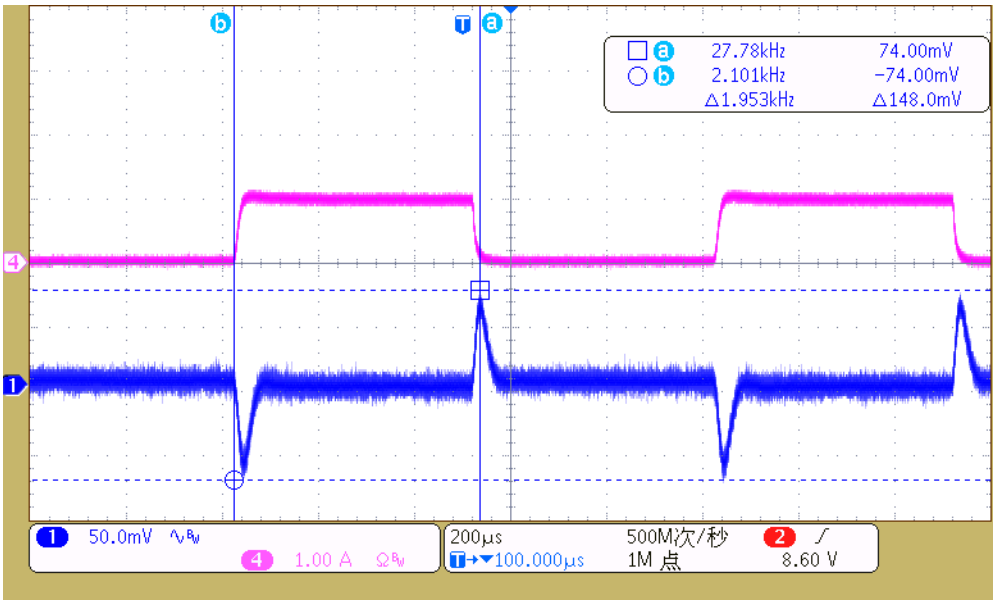

Figure 33. LM26420-Q1 Load Step Response, 0 A to 1 A

4.3.5 LM26420 for 3.3V at 1.5A

4.3.5.1 Output Regulation and Curve

Output one of the LM26420-Q1 was tested with loads ranging from 0 A to 1.5 A. The results are listed in Table 6. The data is graphed in Figure 34. The input to the LM26420-Q1 is 5 V.

Table 6. Output Regulation Data for LM26420-Q1, Section One (3.3 V Output)

OUTPUT CURRENT (A)	OUTPUT VOLTAGE (V)
0	3.3019
0.30	3.3014
0.60	3.3012
0.90	3.3008
1.20	3.3004
1.50	3.3002

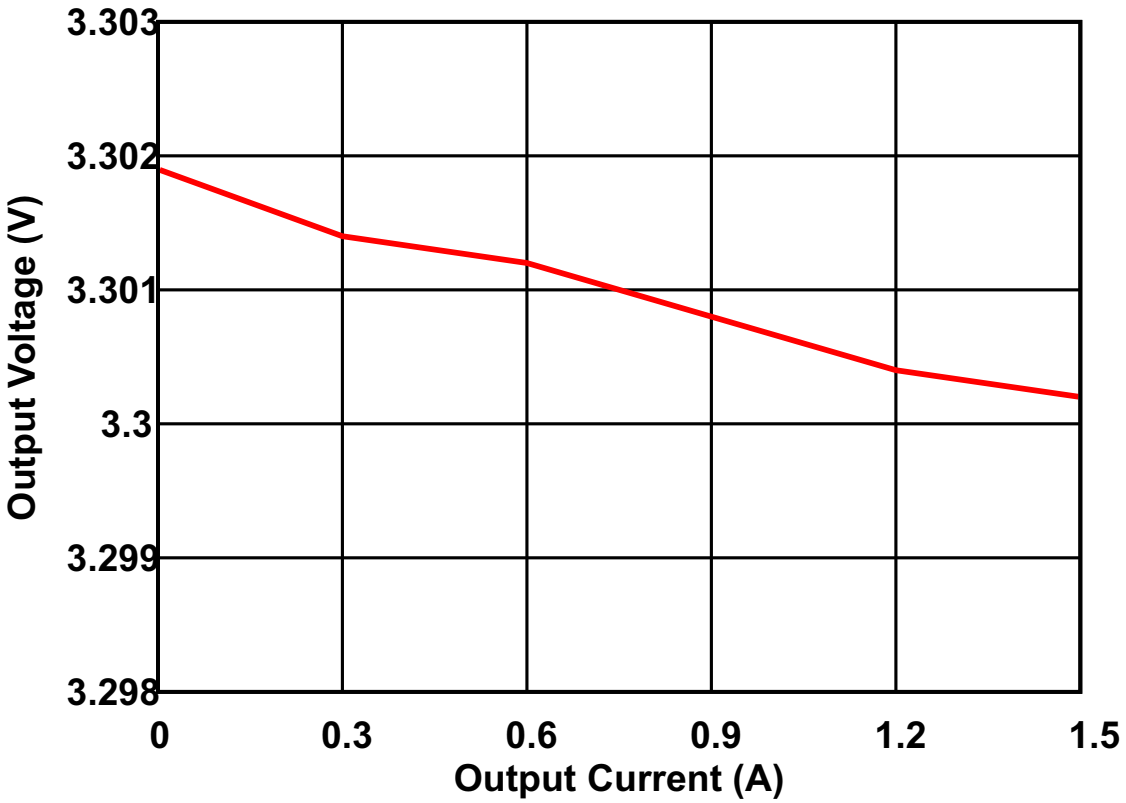

Figure 34. LM26420-Q1 Load Regulation

The 3.3 V output voltage of the LM26420-Q1 varied by less than 1 mV between the no load and the 1.5 A load conditions.

4.3.5.2 Output Ripple Voltage

The LM26420-Q1 3.3 V output ripple was measured with a 1.5 A load current. The measured ripple was 37.1 mVp-p. Figure 35 shows the oscilloscope plot.

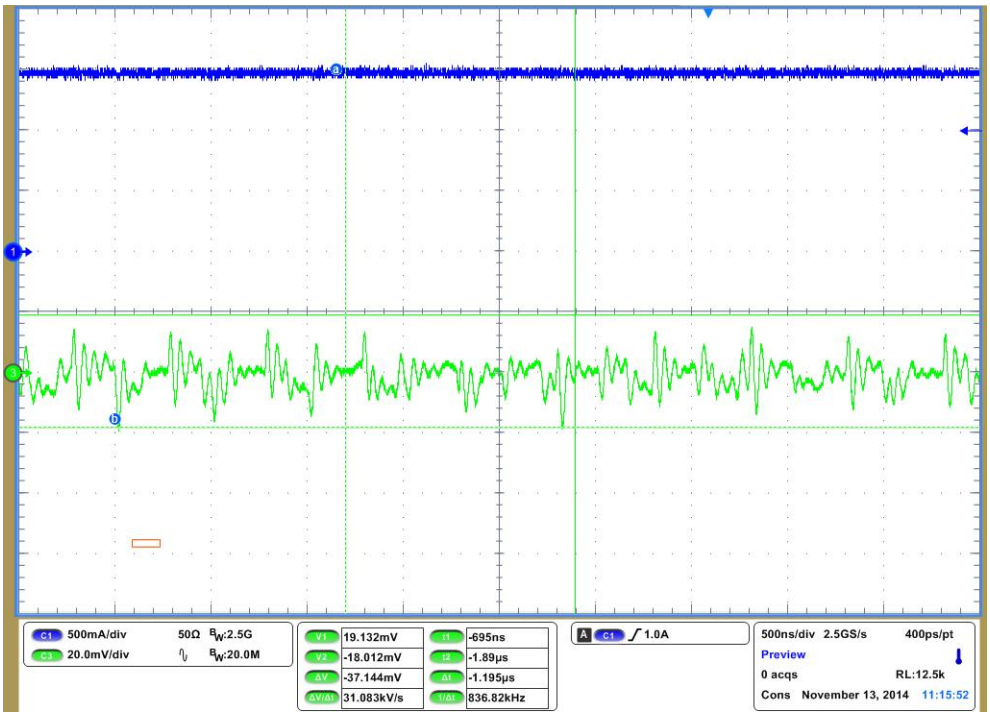

Figure 35. LM26420-Q1 3.3V Output Voltage Ripple with a 1 A Load

4.3.5.3 Dynamic Response

The output dynamic response of the LM26420-Q1 3.3 V output was measured with load steps of 0 A to 0.75 A, 0.75 A to 1.5 A, and 0 A to 1.5 A. The load step pulse width was between 478 µs and 506 µs. The load step rise and fall time was 2.5 A per µs. For the 0 to 0.75 A load step, the maximum voltage deviation was 186 mVp-p, as shown in Figure 36.

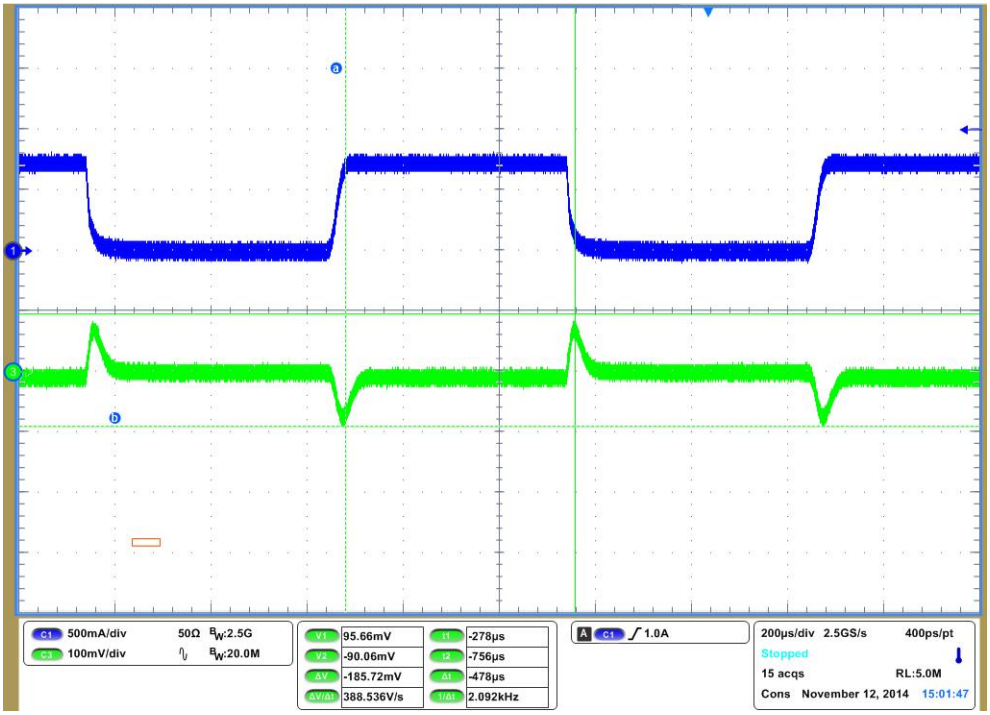

Figure 36. LM26420-Q1 3.3 V Load Step Response, 0 A to 0.75 A

For the 0.75 A to 1.5 A load step, the maximum voltage deviation was 217 mVp-p, as shown in Figure 37.

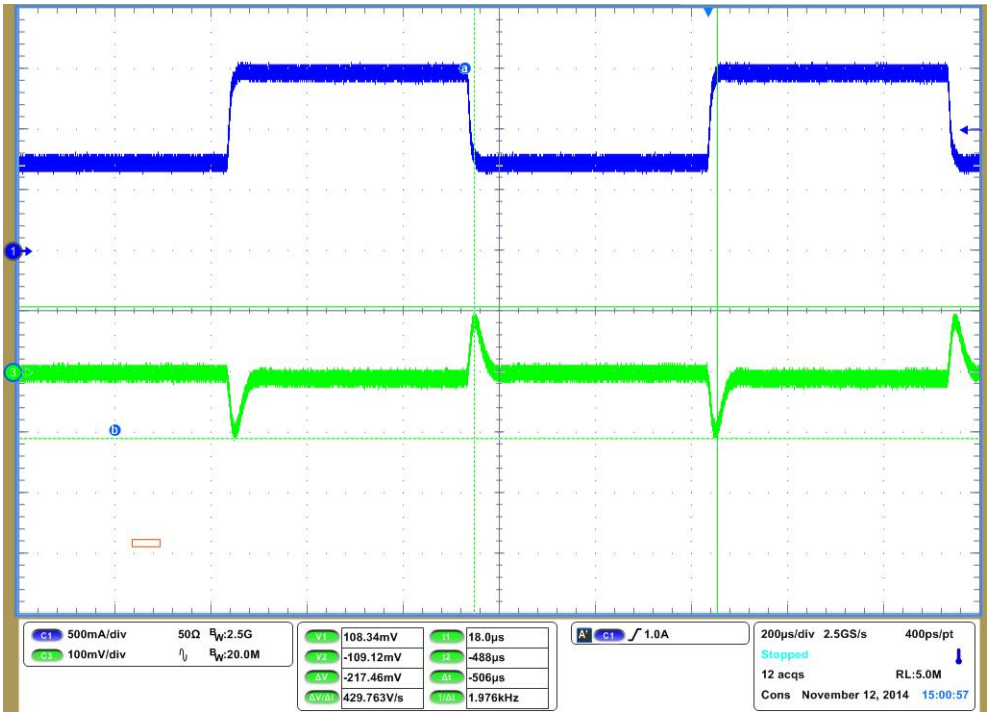

Figure 37. LM26420-Q1 3.3 V Load Step Response, 0.75 A to 1.5 A

For the 0 A to 1.5 A load step, the maximum voltage deviation was 360 mVp-p, as shown in Figure 38.

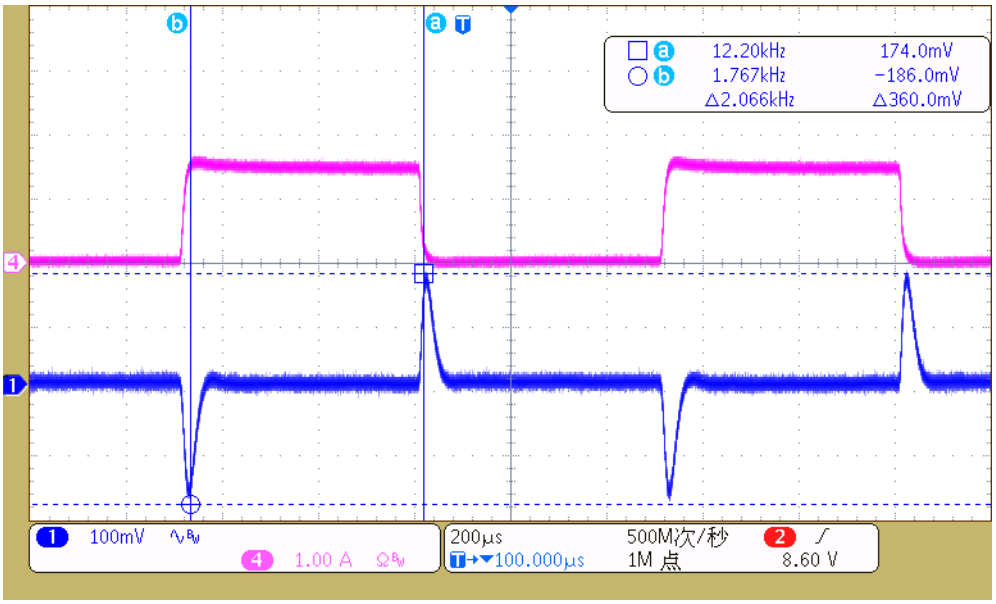

Figure 38. LM26420-Q1 3.3 V Load Step Response, 0 A to 1.5 A

4.3.6 TLV70030 for 3V at 0.15 A

4.3.6.1 Output Regulation and Curve

The TLV70030-Q1 was tested with loads ranging from 0 A to 0.15 A. The results are shown in Table 7 and the data is graphed in Figure 39. The input to the TLV70030-Q1 is 5 V.

Table 7. Output Regulation Data for TLV70030-Q1

OUTPUT CURRENT (A)	OUTPUT VOLTAGE (V)
0	2.9913
0.03	2.9915
0.06	2.9917
0.09	2.9918
0.12	2.9918
0.15	2.9921

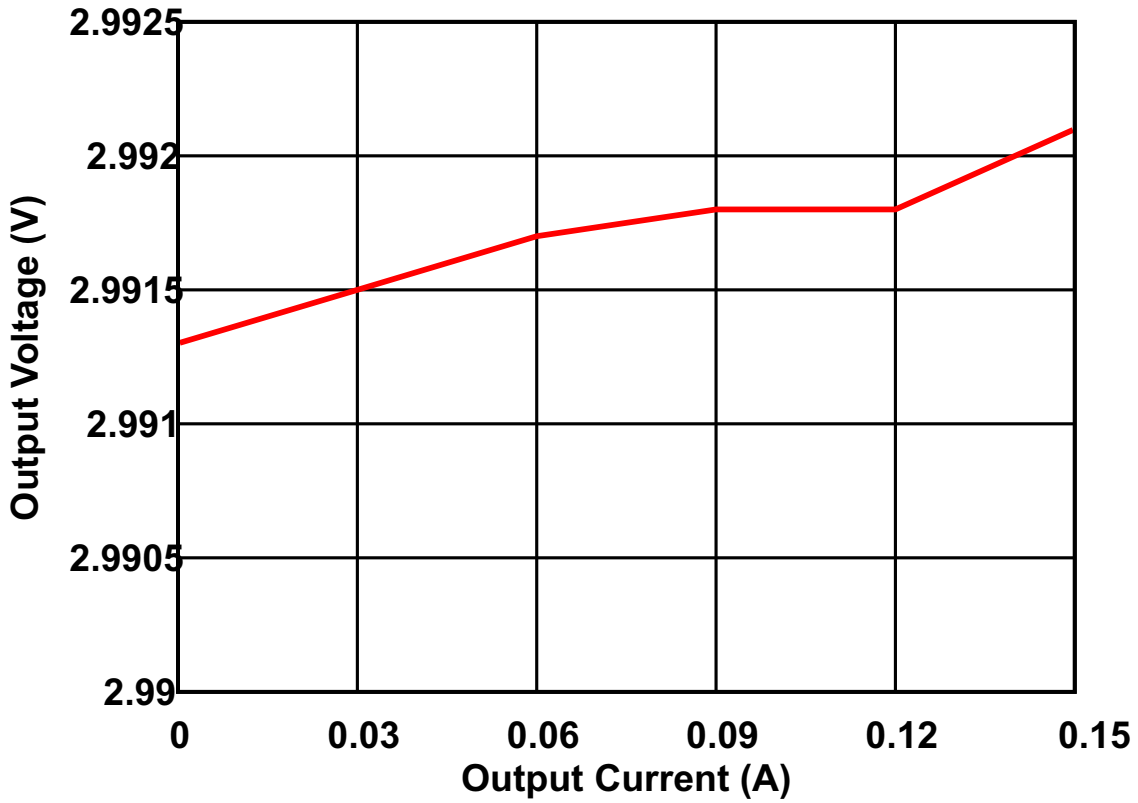

Figure 39. TLV70030-Q1 Load Regulation

The output voltage of the TLV70030-Q1 varied by less than 1 mV between the no load and the 0.15 A load conditions.

4.3.6.2 Output Ripple Voltage

The TLV70030-Q1 output voltage ripple was measured with a 0.15 A load current. The measured ripple was 25.6 mVp-p and Figure 40 shows the oscilloscope plot.

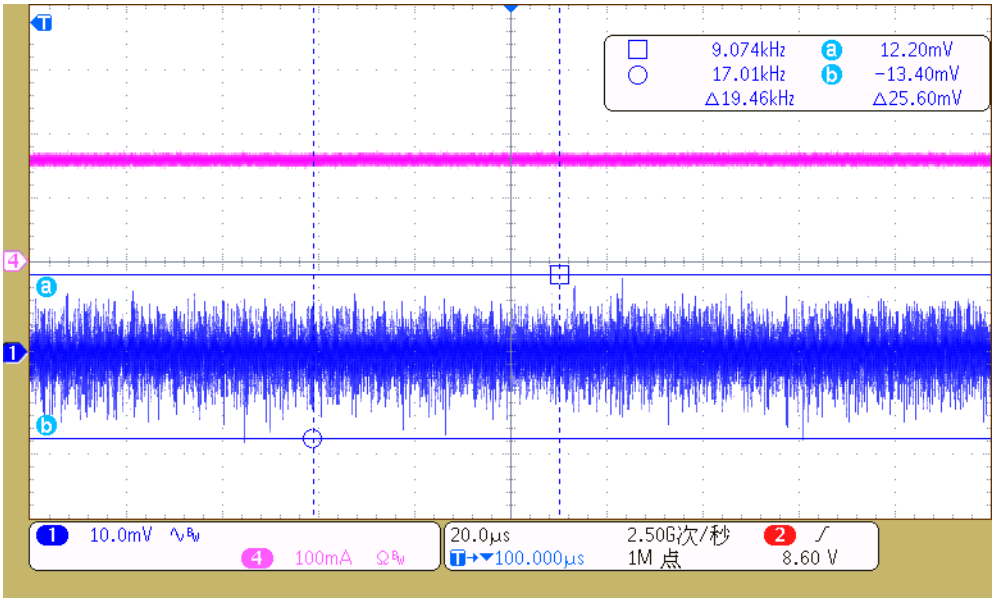

Figure 40. TLV70030-Q1 Output Voltage Ripple With a 0.15 A Load

4.4 Output Voltage Time Sequence

One feature of the TIDA-00804 design is that no voltage sequencer is required. Power sequencing is accomplished by using power good outputs from the various regulators as explained in Section 3. This section measures the actual power supply output timing relationships. For reference, the power supplies power up in this order:

1. TLV70030-Q1 3 V supply
2. TPS57114-Q1 1.425 V supply
3. TPS54388-Q1 1.5 V supply
4. LM26420 section one 3.3 V supply
5. LM26420 section two 1.8 V supply

One oscilloscope was used to measure the output voltage of the different power supplies. Since the oscilloscope has only four measurement channels, the time phasing measurements were made with in two parts. Figure 41 shows the relationships of the 3 V, 1.5 V, 3.3V and 1.425 V supplies.

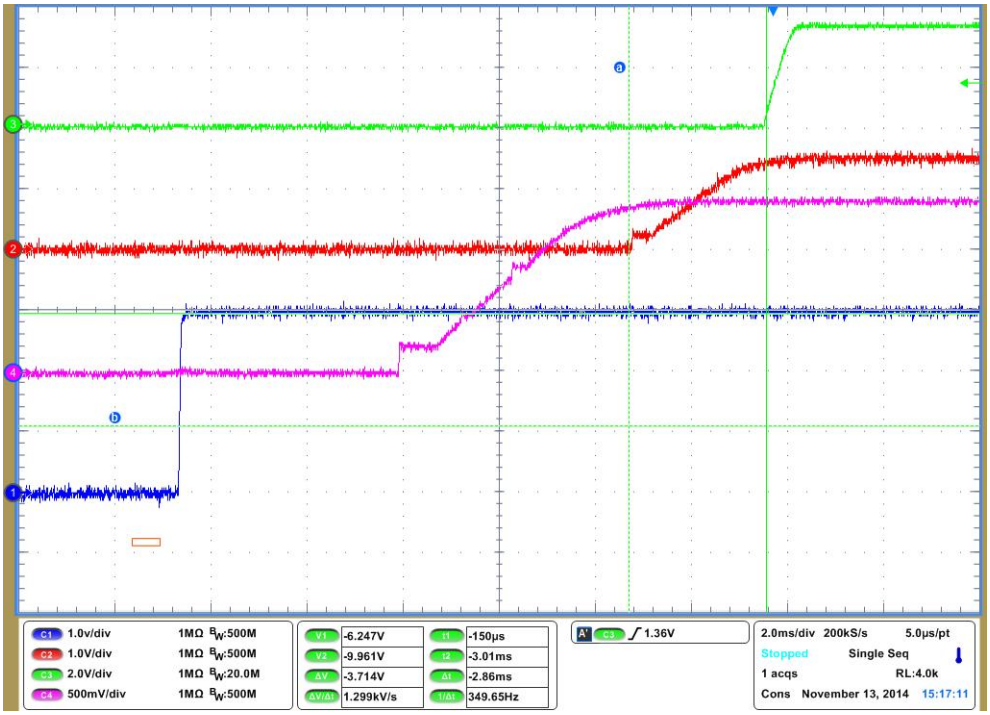

Figure 41. Power-Up Relationships of the 3 V, 1.5 V, 3.3V and 1.425 V Supplies

Ch1: 3V Output Voltage 1V/div

Ch2: 1.5V Output Voltage 1V/div

Ch3: 3.3V Output Voltage 2V/div

Ch4: 1.425V Output Voltage 500mV/div

As expected, the 3 V supply is the first to start. The 3-V supply settles to 3 V in about 0.2 ms. The 1.425 V supply is settled about 8.7 ms after the 3-V power supply rises. The 1.5-V supply starts to rise once the 1.425-V supply is good. The 1.5-V supply settles after 2.9 ms. The 1.5 V power good signal enables the 3.3-V supply, which rises very quickly and settles in 0.3 ms.

Figure 42 shows the relationships of the 1.8 V, 1.5 V, 3.3V and 1.425 V supplies.

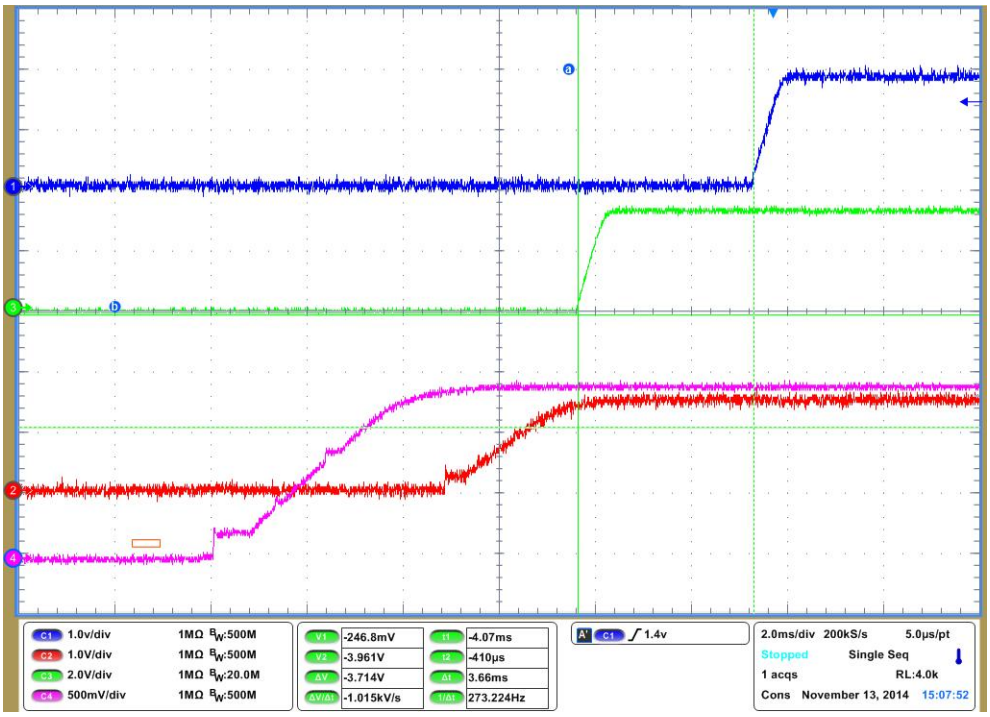

Figure 42. Power-Up Relationships of the 1.8 V, 1.5 V, 3.3V and 1.425 V supplies

Ch1: 1.8V Output Voltage 1V/div

Ch2: 1.5V Output Voltage 1V/div

Ch3: 3.3V Output Voltage 2V/div

Ch4: 1.425V Output Voltage 500mV/div

Figure 42 shows the same relationships for the 1.425 V, 1.5 V, and 3.3 V supplies. The 1.8 V supply is delayed from the start of the 3.3 V supply by 3.7 ms. The 1.8 V supply rises in about 0.3 ms. The total time delay from the start of the 3 V to the settling of the 1.8 V is 16.1 ms. The Table 8 summarizes the power up sequence.

Table 8. Power-Up Sequence Times

STEP	POWER SUPPLY	OUTPUT VOLTAGE (V)	DELAY FROM PREVIOUS SUPPLY UNTIL SUPPLY SETTLES (ms)
1	TLV70030-Q1	3	0.2
2	TPS57114-Q1	1.425	8.7
3	TPS54388-Q1	1.5	2.9
4	LM26420-Q1	3.3	0.3
5	LM26420-Q1	1.8	4
–	–	Total Time (ms):	16.1
–	–		

4.5 Thermal Performance

Figure 43 shows a thermal image of the TIDA-00804 circuit board when all of the power supply outputs are loaded to their maximum design ratings. The ambient temperature is 25 C. The power supplies are allowed to operate long enough for the board to reach thermal equilibrium. Most of the heat is generated in the TPS54561-Q1, D1 and L2, which are all part of the 5 V power supply.

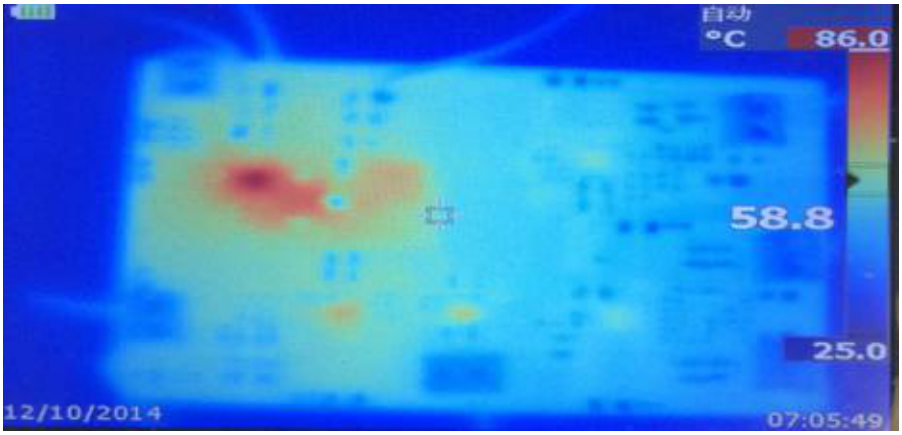

Figure 43. Thermal image of the TIDA-00804 board with maximum loads

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00804.

5.2 Bill of Materials (BOM)

To download the bill of materials (BOM), see the design files at TIDA-00804.

5.3 PCB Layout

5.3.1 PCB Layers

The pictures presented in the board layout figures are screen captures from the PWB layout tool. To see the layout files, gerber files, and odb files refer to http://www.ti.com/tool/TIDA-00804.

Figure 44 shows the top layer.

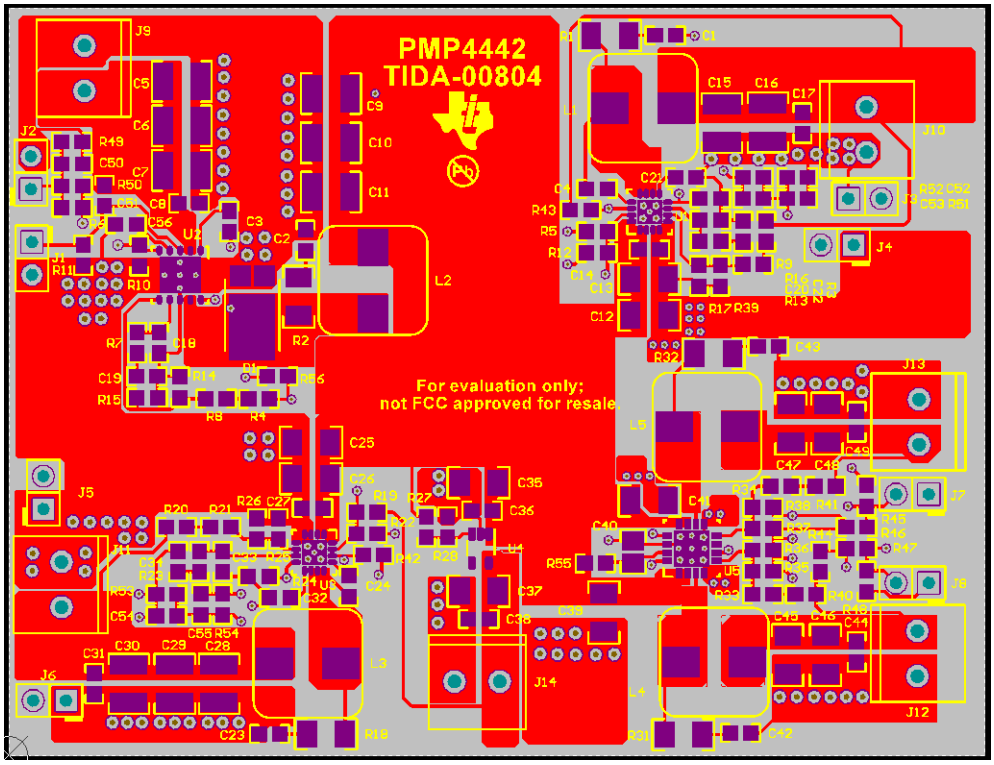

Figure 44. Top Layer

Figure 45 shows the ground plane layer 1.

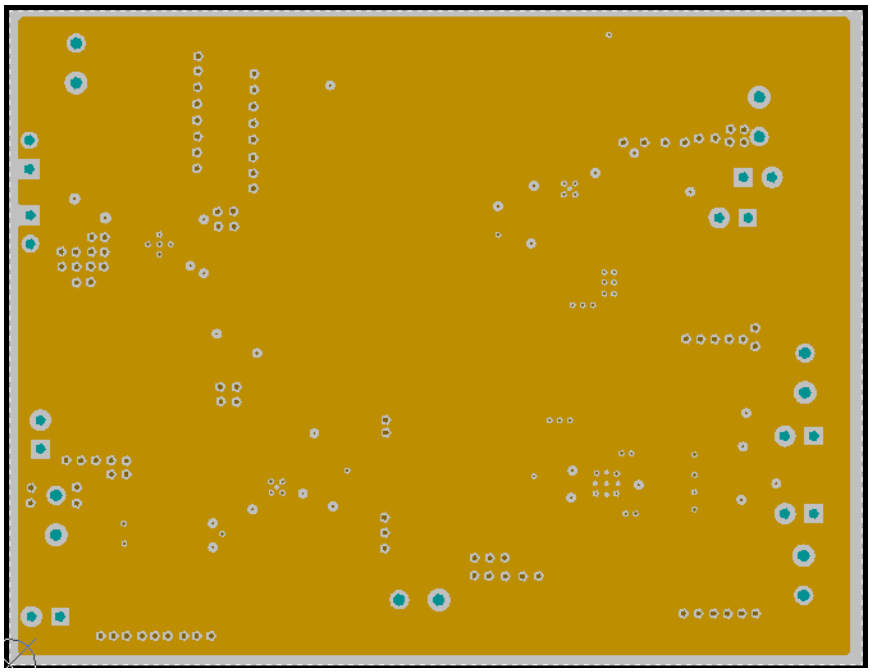

Figure 45. Ground Plane Layer 1

Figure 46 shows the ground plane layer 2.

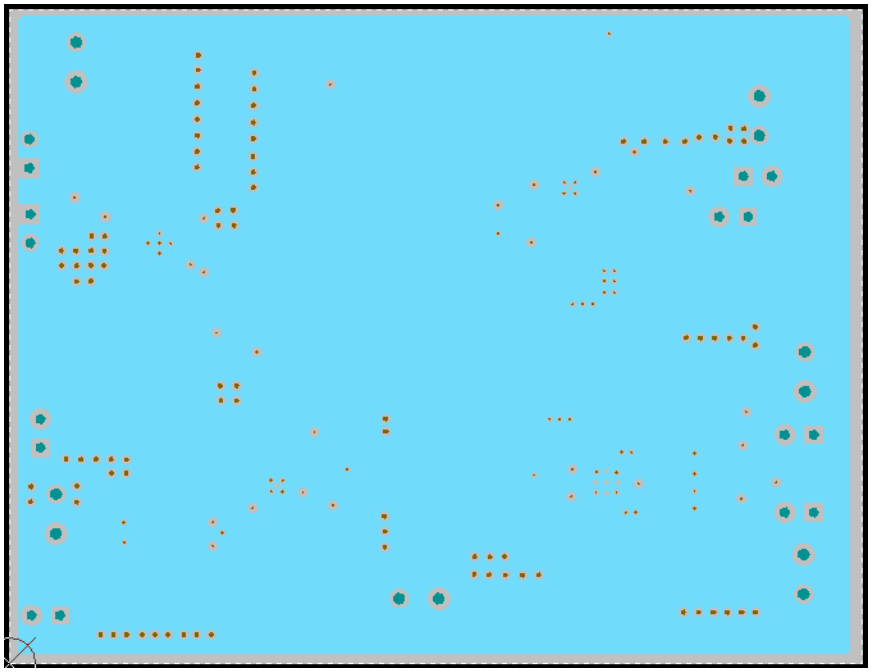

Figure 46. Ground Plane Layer 2

Figure 47 shows the bottom layer.

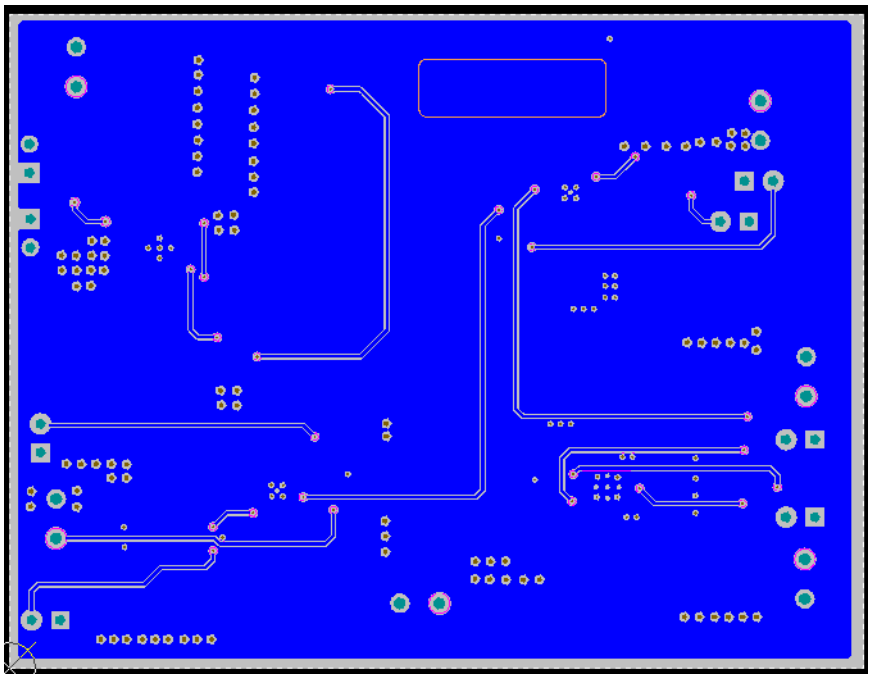

Figure 47. Bottom Layer

5.3.2 PCB Layout Recommendations

Because this is a power supply board, many of the design recommendations are the same for each circuit. Input voltage, output voltage, and ground connections should have very low impedance. Thus, large copper fills were used on the top layer for all of these connections. In addition, there are two interior layers that are ground only, and the bottom layer is mostly filled with ground as well. The regulators with thermal pad packages have vias in the ground plane underneath the part to help spread the heat to the other ground layers. This improves thermal performance. The regulator output switching connections to the filter inductors are kept as short as possible and are also as wide as possible in order to maintain low impedance. Ideally, the input and output filter capacitors ground connections should be made adjacent to each other to insure small loops for the current to flow in, which lowers switching noise. The TPS54561-Q1 circuit is an example of this. Figure 47 shows how the input and output capacitor grounds are placed adjacent to each other to insure a short path for the switching current loop. The input capacitors are C5, C6 , and C7, while the output capacitors are C9, C10, and C11. To highlight the nets, ground is shown in green while + 5 V is shown in yellow.

Figure 48 shows the TPS54561-Q1 input and output capacitor placement ground.

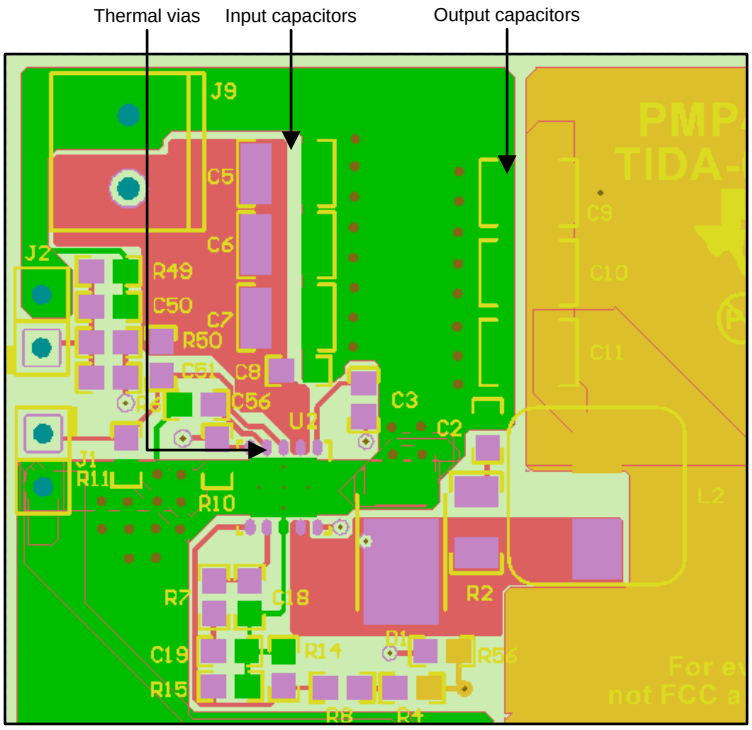

Figure 48. TPS54561-Q1 Input and Output Capacitor Placement Ground = Green, +5 V = Yellow

Keeping the switching loop small is most important on this first regulator stage since it delivers the highest output power. For the other three switching regulators, component placement prevents placing the input and output filter capacitor grounds adjacent to each other, so a large number of ground vias have been provided in the ground connections to insure the lowest possible ground impedance. Figure 49 shows the TPS57114-Q1 circuit layout. C25 and C26 are the input capacitors, while C28, C29, and C30 are the output capacitors.

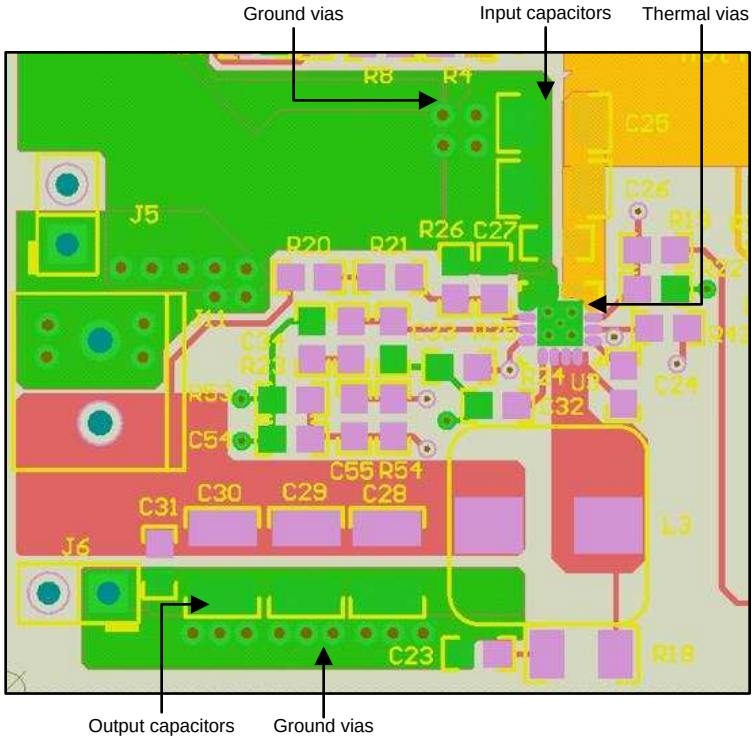

Figure 49. TPS57114-Q1 Input and Output Capacitor Placement Ground = Green, +5V = Yellow

The layouts for the TPS54388-Q1 and the LM26420-Q1 follow the same rules.

5.4 Altium Project

To download the altium project files for each board, see the design files at http://www.ti.com/tool/TIDA-00804.

5.5 Gerber Files

To download the gerber files for each board, see the design files at http://www.ti.com/tool/TIDA-00804.

5.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at http://www.ti.com/tool/TIDA-00804.

6 References

1. TPS54561-Q1 Automotive 4.5 V to 60 V Input 5 A Step-Down DC-DC Converter With Soft-Start and Eco-mode™
2. TPS57114-Q1 Automotive 2.95 V to 6 V Input, 4 A, 2 MHz Synchronous Step-Down SWIFT™ DCDC Converter
3. LM26420-Q1 Dual 2.0 A, High Frequency Synchronous Step-Down DC-DC Regulator
4. TPS54388-Q1 Automotive Catalog 2.95 V to 6 V Input, 3 A, 2 MHz Synchronous Step Down SWIFT DCDC Converter
5. TLV70030-Q1 Automotive 200 mA, Low IQ, Low Dropout Regulator for Portables

7 About the Author

MARK KNAPP is a Systems Architect at TI where he is responsible for developing reference design solutions for the Automotive Infotainment and Cluster segment. He has an extensive background in video camera and infrared imaging systems for Military, Automotive, and Industrial applications. In addition, he has created several Internet of Things designs. Mark earned his BSEE at the University of Michigan-Dearborn and his MSEE at the University of Texas at Dallas.

DAVID JI is a System Application Engineer at TI where he is responsible for developing power reference design solutions for the Automotive Infotainment, Power Delivery, and Appliances segment. In addition, he has supported enterprise switchers and IP phone application. David earned his BSEE at the Qufu Normal University and his MSEE at the South China of University of Technology.

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