

# TI Designs

## Full Duplex RS-485 Over Two Wires Reference Design



### TI Designs

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### Design Resources

<a href="#">TIDA-00862</a>	Tool Folder Containing Design Files
<a href="#">SN65HVD3806E</a>	Product Folder
<a href="#">SN65HVD96</a>	Product Folder
<a href="#">SN74LVC1G97</a>	Product Folder
<a href="#">SN74LVC1G04</a>	Product Folder

### Design Features

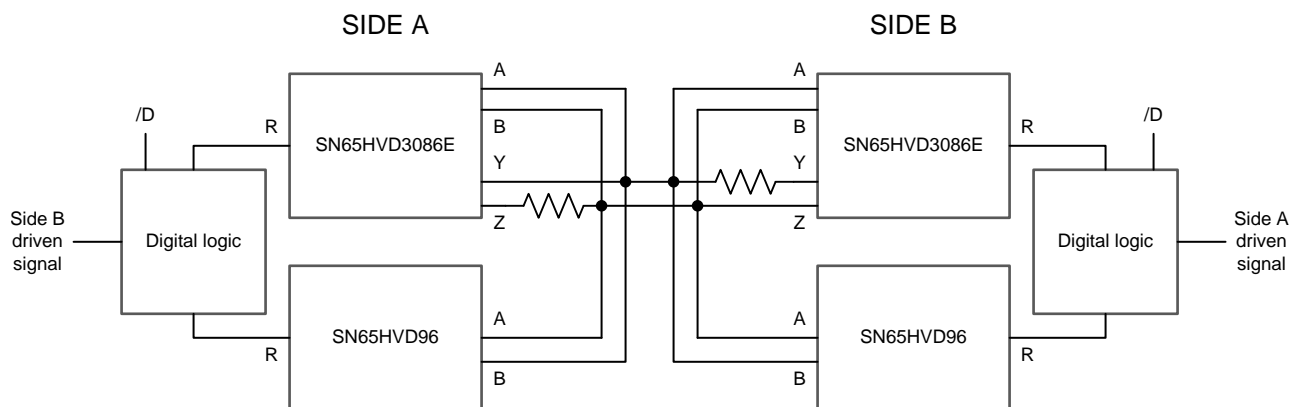
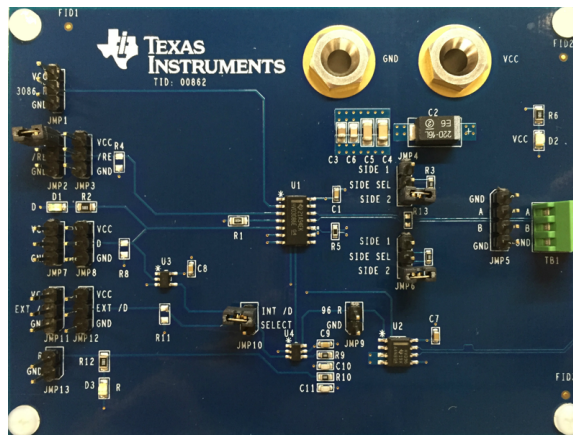
- Physical Level, Full-Duplex Differential Communication Using Only Two Bus Lines
- Ability to Set Link Side Orientation With Ease
- Independent Send and Receive Data Rate Transmission

### Featured Applications

- E-Meters
- Industrial Automation
- Security and Surveillance Equipment
- Encoders and Decoders



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## 1 Design Overview

The RS-485 communication protocol defines one of many physical layer standards for differential signaling in either half- or full-duplex communications channels. Four bus lines are required (a pair of bus lines for each data direction) to implement typical full duplex communication. As cable distances increase, the cost of an additional two bus lines can be substantial. This design enables full-duplex differential signaling using only two bus wires by employing the use of Texas Instrument’s (TI) SN65HVD96 SymPol™ transceiver. The system takes advantage of bus contention (caused by the driving of opposing signals by separate transceivers on the bus) to allow for a tri-stated data line. Using onboard digital logic, the system can detect the logic state of the opposing driver with knowledge of its own driven signal, its received signal, and the output of the SymPol transceiver. The design allows for completely independent sending and receiving data rates.

## 2 RS-485 Standard

The RS-485 communications standard enables highly robust data transmission over long distances and electrically noisy environments by utilizing a balanced differential bus line over twisted pair cable. The standard itself defines only the physical layer implementation of the system, while other standards cover data link layer recommendations. RS-485 signals are carried using twisted pair cable with 120-Ω characteristic impedance. The best practice for RS-485 networks specifies 120 Ω of termination on each end of an RS-485 bus to reduce signal reflections. RS-485 networks can function as multipoint or multidrop systems; however, the focus of this TI Design is a two-node network.

The RS-485 standard specifies the minimum bus signal levels during data transmission. A driver must provide at least 1.5-V differential over a 54-Ω load and a receiver must detect a differential input of at least 200 mV. These specifications allow for robust performance despite the given signal degradation along the bus path. High and low logic states on an RS-485 bus are represented by a positive or negative differential voltage.

Using one pair of bus lines, a typical RS-485 system can achieve half duplex communication between many nodes in a network. Care must be taken from a communications protocol standpoint to prevent bus contention, which is caused when multiple drivers attempt to drive the bus lines at the same time. By adding two more bus lines and full-duplex capable transceivers, the network can allow for bidirectional communication with data being sent to and from a node simultaneously.

## 3 Block Diagram

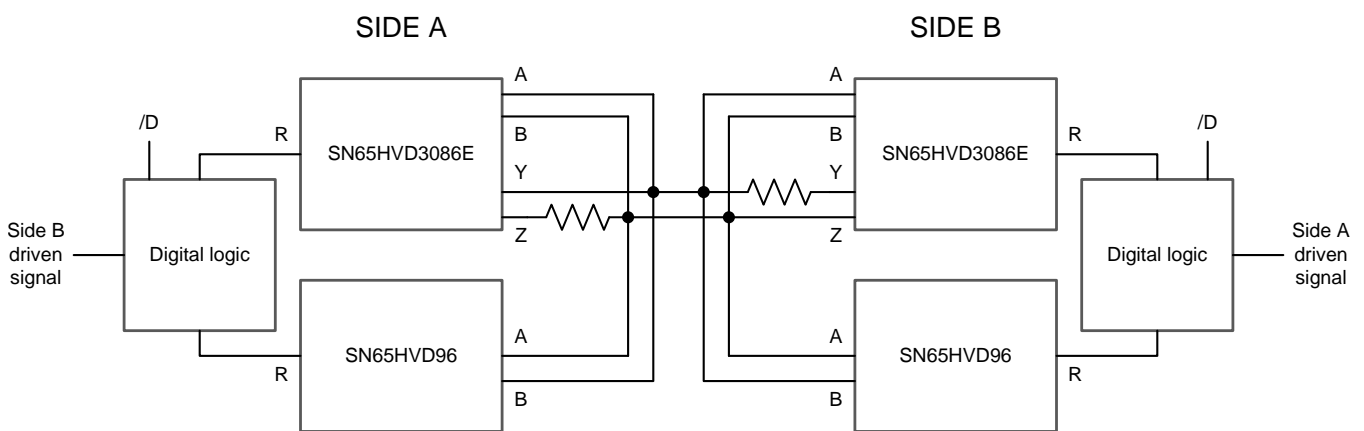


Figure 1. TIDA-00862 Block Diagram

## 4 Highlighted Products

This TIDA-00862 design allows for full duplex differential communication by enabling a third bus state and by utilizing TI's SN65HVD96 SymPol transceiver. The design specifies the use of a SN65HVD3803E full duplex RS-485 transceiver, SN65HVD96 SymPol transceiver, SN74LVC1G97 multipurpose digital logic device, and SN74LVC1G04 single inverter.

### 4.1 SN65HVD3086E Full Duplex Transceiver

The SN65HVD3086E is a 5-V full duplex transceiver designed for RS-485 or RS-422 data bus networks with signaling rates up to 20 Mbps. The device features operation over a wide common mode range, bus fault protection, and fail safe protection.

### 4.2 SN65HVD96 SymPol™ Transceiver

The SN65HVD96 transceiver allows for communication in differential signaling systems regardless of the orientation of the bus lines (normal or reversed). The SymPol device detects two states: passive and active on the bus. When the differential voltage on the bus is between  $\pm 500$  mV, the bus is classified as passive and the receiver outputs logic low. When the differential is greater than  $\pm 900$  mV, the bus is active and the receiver outputs logic high. The SN65HVD96 can operate with data rates up to 5 Mbps.

### 4.3 SN74LVC1G97 Configurable Multiple-Function Gate

The SN74LVC1G97 is a configurable logic gate device with a 3-bit input which can operate over a 1.65- to 5.5-V VCC range. The three-input gate is used to generate the received signal from the opposing transceiver in the system by using the received signal of the full duplex transceiver, the received signal of the SymPol transceiver, and the complement of the driven signal on the receiving side. The device outputs digital logic levels based on the following truth table ([Table 1](#)) from the data sheet:

**Table 1. Function Table**

INPUTS			OUTPUT
In2	In1	In0	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

### 4.4 SN74LVC1G04 Single Inverter

A single inverter is used to generate the complement of the driven signal on each side of the RS-485 system for cases when the user chooses not to generate this signal directly from the MCU. The inverted signal is required as one of the three inputs to the multiple-function gate.

## 5 System Description

The "full duplex over a two-wire" scheme is made possible by taking advantage of bus contention, which is caused when the two drivers attempt to communicate simultaneously on the same set of bus lines. Unlike a typical full duplex system where the driver bus lines of each transceiver are connected to the receiver bus lines of the other, the drivers in this design are connected directly to each other.

The bus is terminated at each end with a standard 120- $\Omega$  termination to match the characteristic impedance of the transmission media. To prevent excess current flow when the transceivers drive opposing states, 30- $\Omega$  current-limiting series resistors are placed in between the driver lines. Next, the bus lines of the SymPol transceiver are connected asymmetrically to the driver bus lines with one line connected on the transceiver side of one of the series resistors and the other connected on the bus side of the other series resistor. For this reason, the printed-circuit board (PCB) design incorporates jumpers to configure each side of the link as "Side 1" or "Side 2." A proper configuration enables each side of the line to have opposite series resistors populated. Finally, the receiver bus lines of the full duplex transceiver are connected to the bus lines of the SymPol transceiver.

The multifunction logic gate is connected to the system with:

- In0 = /D
- In1 = SN65HVD3086E Receiver
- In2 = SN65HVD96 Receiver

The output Y of the logic device is the received signal from the opposing side of the link.

### 5.1 Operational Modes

When using two transceivers each with two possible driving states there are four possible signaling situations that can occur on the bus: both driving high, both driving low, side one high and side two low, and side one low and side two high. For situations where the transceivers drive the same logic level, the differential on the bus simply increases beyond single driver differential levels. Alternatively, when the drivers oppose each other, the voltage on the bus varies based on where the bus is probed. For example, if the Y line has been driven high on side one and low on side two, the logic level matches the driven signal of each transceiver before the series current limiting resistor. Because the SymPol transceiver on each side of the link has one connection before the series resistor and one after, the differential voltage on its bus amounts to zero when the signals are driven opposite of each other. Because bus contention is a key factor for this design, both transceivers must be enabled at all times, which is why the DE pin of the SN65HVD3086E is tied high on the board.

#### 5.1.1 Both Sides Drive High

When both sides of the link drive a high signal, a large positive differential results on the bus, which the full duplex transceiver interprets as a high signal and the SymPol transceiver interprets as a low signal:

In0	L
In1	H
In2	L
Y	H

#### 5.1.2 Both Sides Drive Low

When both sides of the link drive a high signal, a large positive differential results on the bus, which the full duplex transceiver interprets as a high signal and the SymPol transceiver interprets as a low signal:

In0	H
In1	L
In2	L
Y	L

### 5.1.3 Side 1 Drives High, Side 2 Drives Low

The differential is 0 for both sides on the bus lines of the SymPol transceiver and the full duplex receiver bus. This value causes the full duplex receiver and the SymPol receiver to output high:

#### Side 1

In0	L
In1	H
In2	H
Y	L

#### Side 2

In0	H
In1	H
In2	H
Y	H

### 5.1.4 Side 1 Drives Low, Side 2 Drives High

The differential is 0 for both sides on the bus lines of the SymPol transceiver and the full duplex receiver bus. This value causes the full duplex receiver and the SymPol receiver to output high:

#### Side 1

In0	H
In1	H
In2	H
Y	H

#### Side 2

In0	L
In1	H
In2	H
Y	L

## 6 System Design Theory

The configuration described in [Section 5](#) demonstrates the fundamental operation of full duplex communication using two bus lines; however, several other design considerations must be made to achieve optimal performance from this system.

### 6.1 SymPol Switching Glitches

Because of the fact that the RS-485 differential signaling transitions from positive to negative differential voltage, an inevitable small unit of time exists in which the differential voltage residing on the bus is below  $\pm 500$  mV (as the signals cross each other). If both sides of the link transmit identical signals (same data rate, phase, and logic level), then these approximate 0-V differential periods cause the SymPol transceiver to falsely receive a passive level. The receiver of the SN65HVD96 outputs a short high level, causing the final received signal to glitch towards the incorrect logic level.

### 6.2 Delay-Induced Phase Mismatch

An appreciable delay exists between the /D signal and the R inputs from either the full duplex transceiver or the SymPol transceiver. Excess delay between the /D input and either of the other two input signals causes glitches on the output of the multifunction gate because the inputs appear to be different logic levels. These glitches become more apparent as the data rates increase.

#### 6.2.1 Example of Delay Causing Glitch

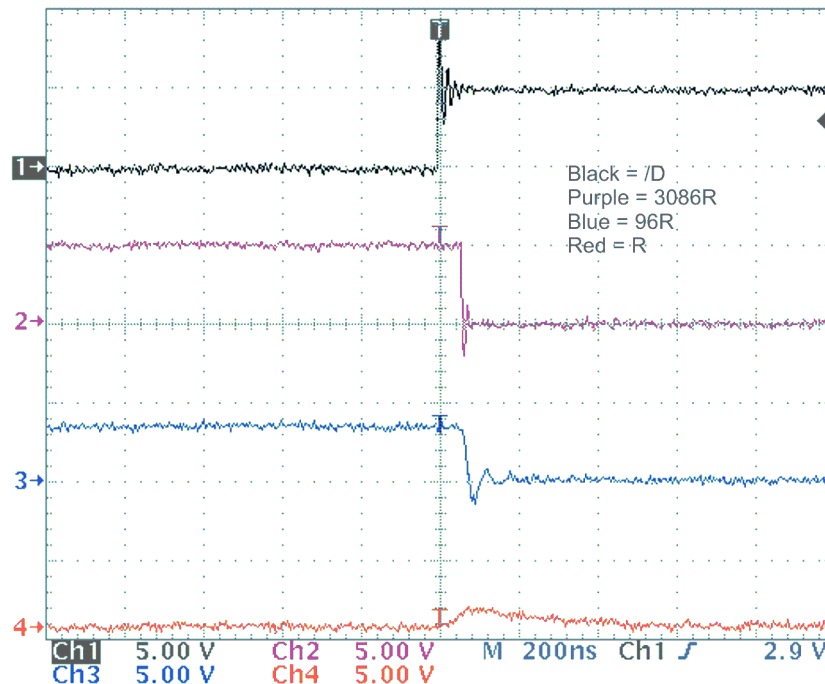


Figure 2. Example of Delay Causing Glitch

### 6.3 Glitch Compensation

#### 6.3.1 Second-Order Passive Low-Pass Filter

To correct for the glitches caused by SymPol switching and phase delay, a second-order passive low-pass filter is used on the output of the multifunction logic device. The use of the low-pass filter limits the data rate of the system to around 1 Mbps as the rise time of the signal is decreased; however, the filter significantly reduces the magnitude of the high frequency glitches, preventing the signal from rising or falling below the anticipated logic voltage threshold.

The second-order low-pass filter is a simple cascade of two first-order low-pass filters, which provides significant attenuation for high frequency glitches while maintaining signal integrity for lower frequency signals in the passband. Figure 3 shows the filter design:

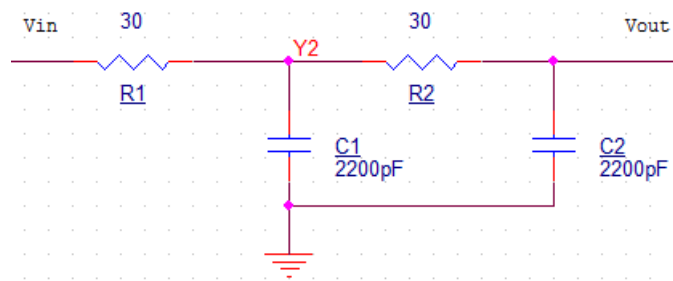


Figure 3. Second-Order Low-Pass Filter

Equation 1 shows the transfer function for the filter:

$$\frac{V_{IN}}{V_{OUT}} = \frac{1}{s^2 + s \times \left( \frac{1}{R1 \times C1} + \frac{1}{R2 \times C1} + \frac{1}{R2 \times C2} \right) + \frac{1}{R1 \times R2 \times C1 \times C2}} \quad (1)$$

The bode plot and step response have been plotted against the first-order passive filter in Figure 4 and Figure 5 to demonstrate the improvement in rolloff and the similarity in step response:

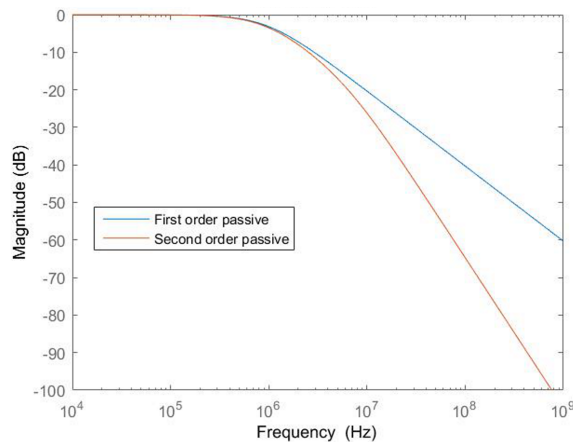


Figure 4. Bode Diagram

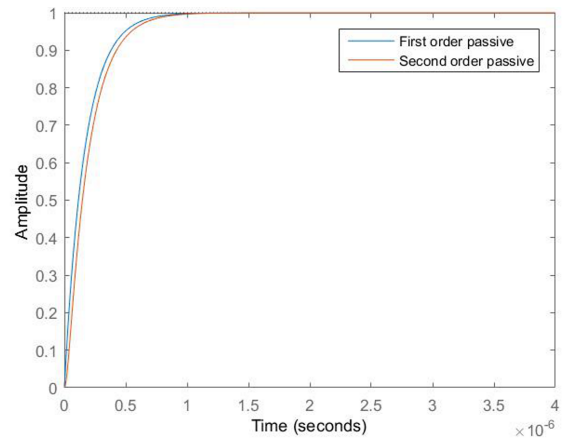


Figure 5. Step Response

### 6.3.2 Example Glitches Before and After Filtering

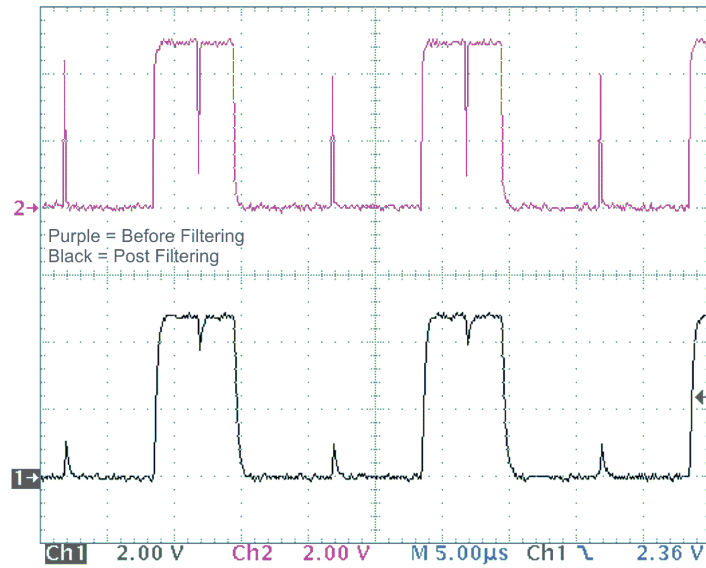


Figure 6. Example Glitches Before and After Filtering

### 6.3.3 Post-Filter Glitch Magnitude ( $\approx 900$ mV)

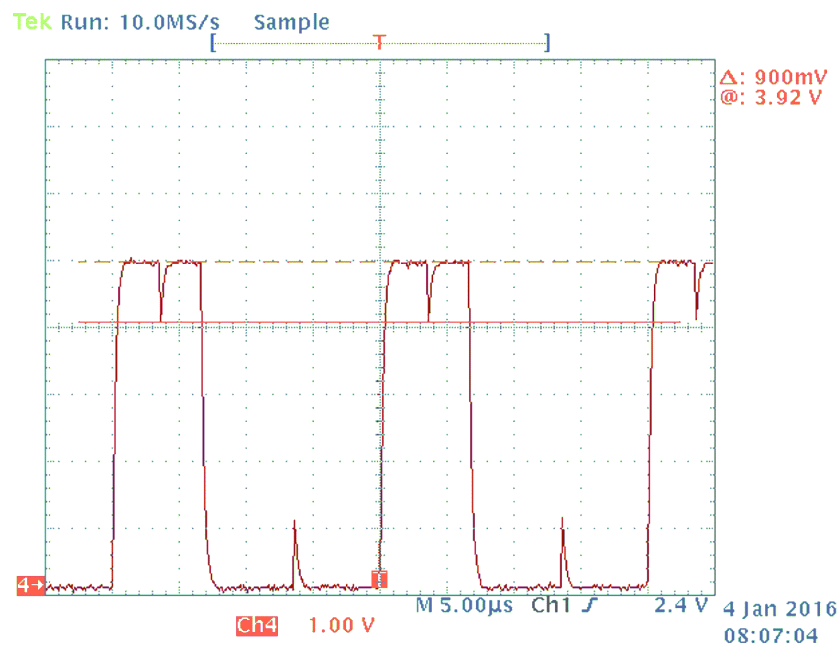


Figure 7. Post-Filter Glitch Magnitude ( $\approx 900$  mV)



### 6.3.4 Phase Compensation

To correct for the delay between the /D signal and the received signal of the full duplex transceiver, intentional phase delay can be introduced to the /D signal on each side. Figure 8 shows an example of an uncompensated setup where side 1 of the link is driving a 215-kHz square wave and the other side is driving a 50-kHz square wave. Glitches can be observed on the received waveform in locations corresponding to the transitions of the driving waveform:

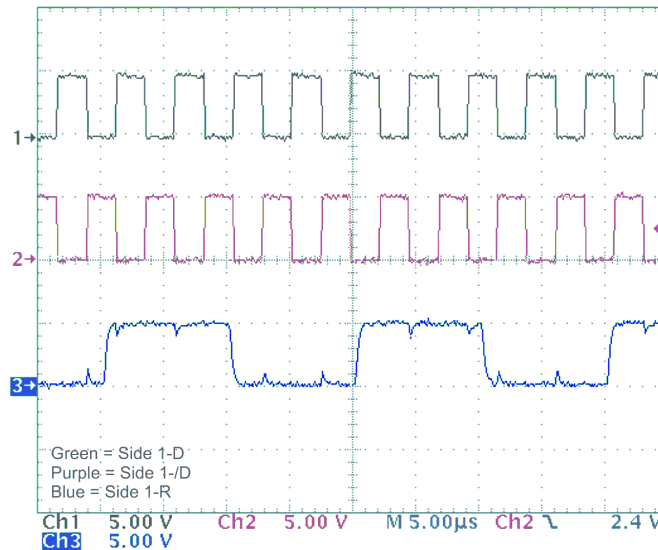


Figure 8. Before Phase Compensation

To correct for the delay between the /D signal and the other two inputs to the multifunction logic device, a  $-8^\circ$  phase delay is implemented on the /D signal (by using an external /D source). This delay effectively removes the glitches from the received signal chain (in Figure 9):

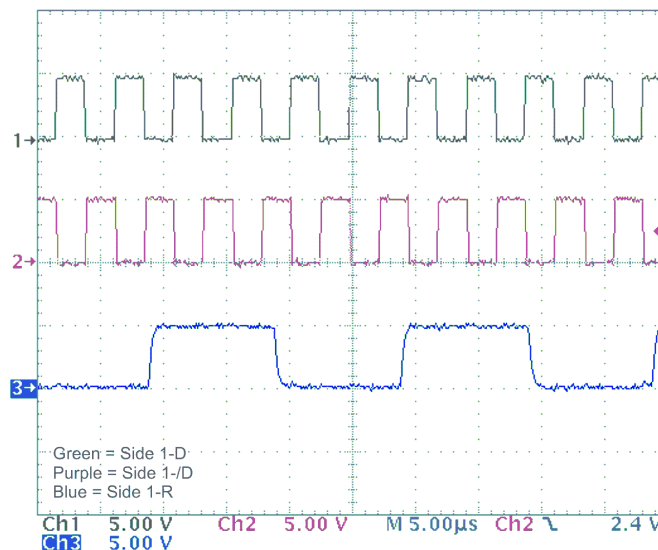


Figure 9. Post Phase Compensation

One important thing to note is that this delay must be fine-tuned for the systems specific data rate, cable length, and so forth. One delay value may not be effective for all setups and can cause signal degradation rather than improvement.

## 6.4 Independent Data Rates

The design does not require data rates or phases of the driven signals to match, allowing for completely independent data rates on each side of the link. If the two sides of the link are synchronized in phase, then any glitches caused by delay occur at a predictable location in the signal chain. Although the low-pass glitch filter should eliminate any erroneous logic transitions as a result of glitches, one consideration worth noting is that the location of the glitches in the signal chain will not be deterministic if the signals have independent data rates.

## 7 Getting Started Hardware

Evaluating both sides of the RS-485 connection requires the use of two boards. The design comes prepopulated with all four of the TI integrated circuits (ICs) that enable the board to function. VCC and GND are connected using the banana jacks in the top-right corner of the boards. The next step is to connect the driver bus lines together using a twisted pair cable. The boards include a terminal block with screw heads to allow for bus cables to be securely attached. The boards must be configured for “Side 1” or “Side 2” for the system to function properly. Identifying marks on the silkscreen direct where to place jumpers on each board to set the link side. For example, to configure the board as Side 1, populate a jumper between the top two pins of JMP4 and JMP6. To configure as Side 2, populate jumpers between the bottom two pins of JMP4 and JMP6. Finally, the /D input selection jumper must be either connected or not connected depending on how the user decides to provide the signal. The onboard inverter IC allows the user to provide the /D signal directly from the D signal if desired. Alternatively, the /D signal can be provided from a signal generator or MCU. The jumper labeled “/D Select” must be populated if the inverter is to be used and must be unpopulated if /D is to be driven externally.

## 8 Test Setup

The system is tested using a dual-channel function generator (or two single-channel function generators) and an oscilloscope to drive signals on each side of the RS-485 bus and measure the received waveforms/bus activity on each side.

First the two boards must be properly powered (see the blue status light-emitting diode [LED]), connected together, configured for the appropriate side, and the “/D Select” pin must either be connected or removed as per the explanation in [Section 7](#). Connect the two outputs of the function generator to the D pins on each board. The function generator outputs must be configured to output square waves with a frequency less than 500 kHz (1 Mbps). Because the driver inputs are high impedance, make sure that the high voltage level is 2.5 V and the low level is 0 V or ensure that the function generator outputs have been configured for high impedance. The boards also contain unpopulated pads that allow for the placement of 50- $\Omega$  resistors from the inputs to ground if desired.

The RS-485 bus lines can be connected together with twisted pair cable using the terminal block TB1.

If the /D signal is to be provided externally, make sure that the “/D Select” pin has been removed and the appropriate signal has been connected. To monitor the INT /D signal of the board, simply probe the EXT /D header while the INT /D SELECT jumper is populated.

Take note that the receiver may be disabled if required; however, for the scheme to function properly, both drivers must be enabled at all times. For this reason, the DE pins are pulled with a resistor to VCC on the PCB.

To monitor the received signal at each board, connect an oscilloscope probe to the R pin. Status LEDs indicate activity on the driver and receiver. The board also contains jumpers which allow for easy monitoring of the bus lines if desired. Because the board contains double headers for the input signals, injecting a signal and monitoring it with a scope is simple.

## 9 Test Data

### 9.1 100-kbps Complimentary Signals

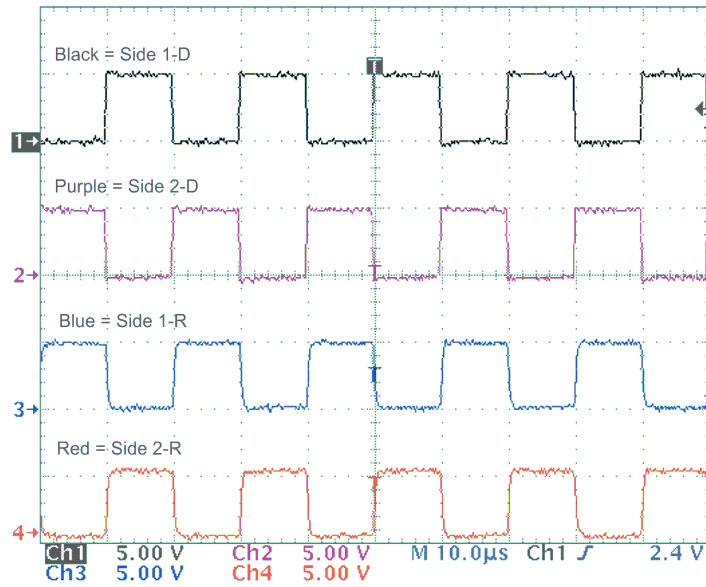


Figure 10. 100-kbps Complimentary Signals

### 9.2 100-kbps Independent Phase and Duty Cycle

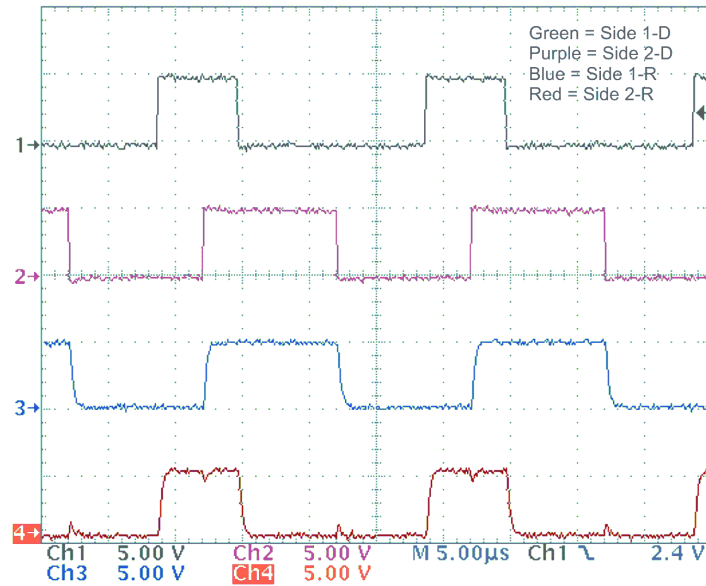


Figure 11. 100-kbps Independent Phase and Duty Cycle

### 9.3 Independent Data Rate and Phase

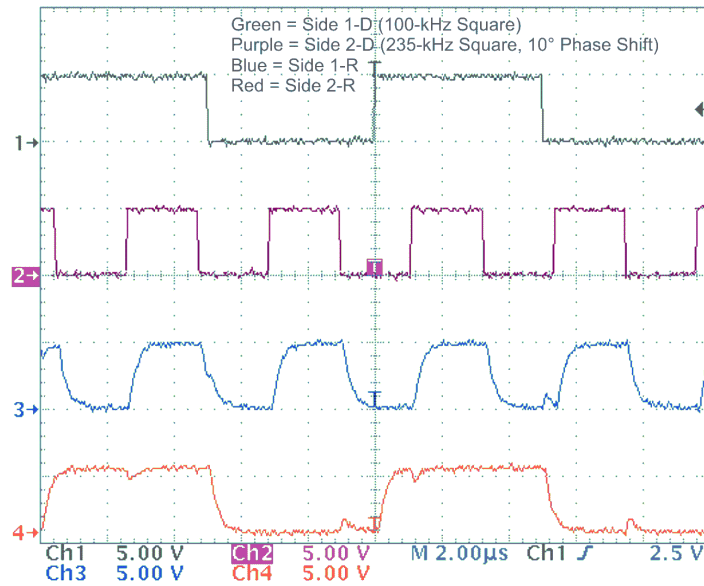


Figure 12. Independent Data Rate and Phase

### 9.4 100-kbps Bus Lines

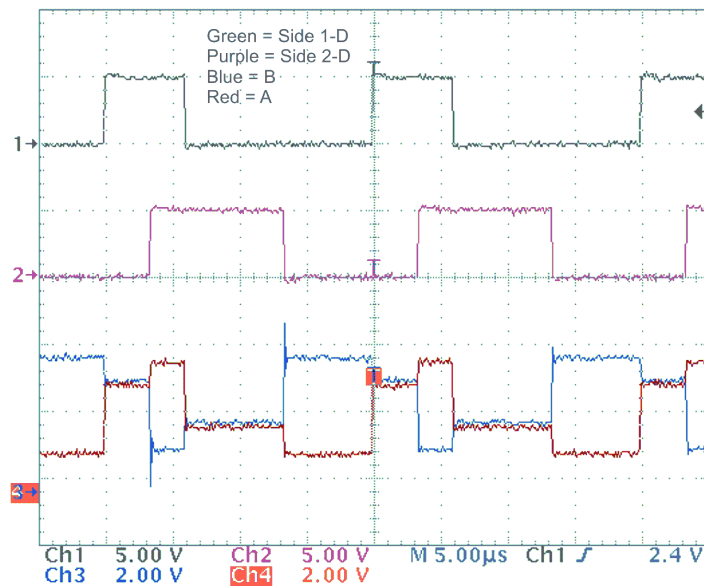


Figure 13. 100-kbps Bus Lines

### 9.5 100-kbps Logic Inputs and R Output

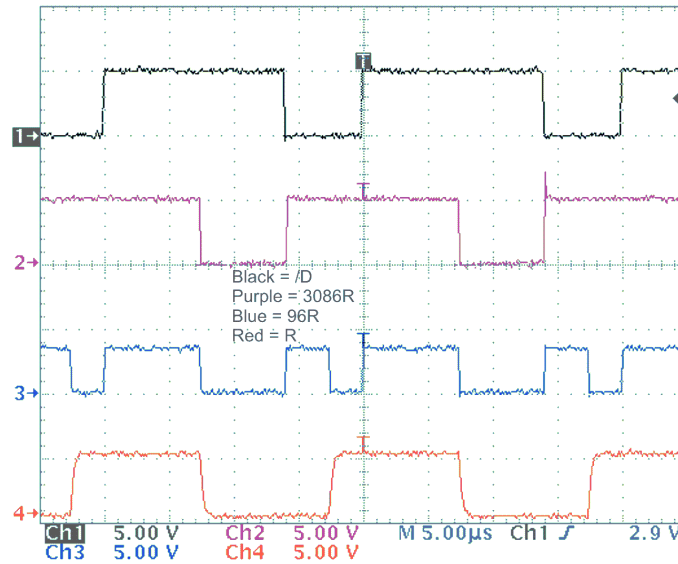


Figure 14. 100-kbps Logic Inputs and R Output

### 9.6 1-Mbps Signaling

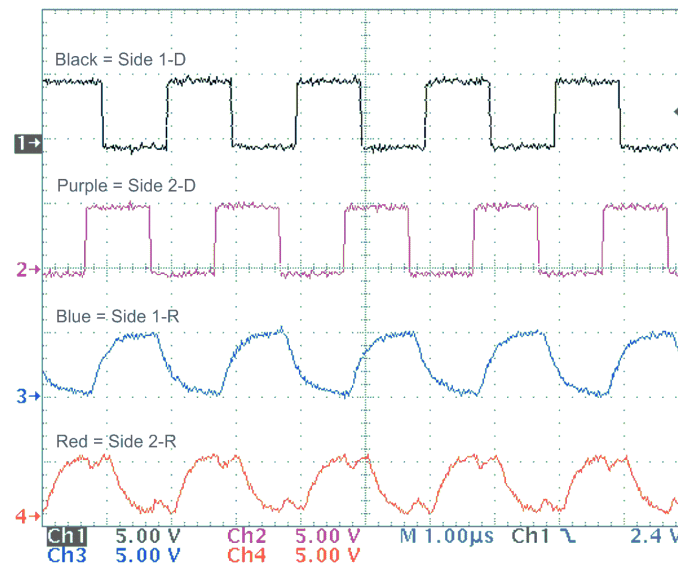


Figure 15. 1-Mbps Signaling

From a system design standpoint, the filtering technique can be modified to allow for further glitch reduction if the data rate of the system is reduced as a trade-off. Decreasing the rolloff frequency of the filter or increasing the rate of the rolloff in the stop band can reduce the magnitude of the high frequency glitches; however, this action negatively impacts the signal integrity of the intended signal, especially for higher data rates.

## 10 Design Files

### 10.1 Schematics

The download the schematics, see the design files at [TIDA-00862](http://TIDA-00862).

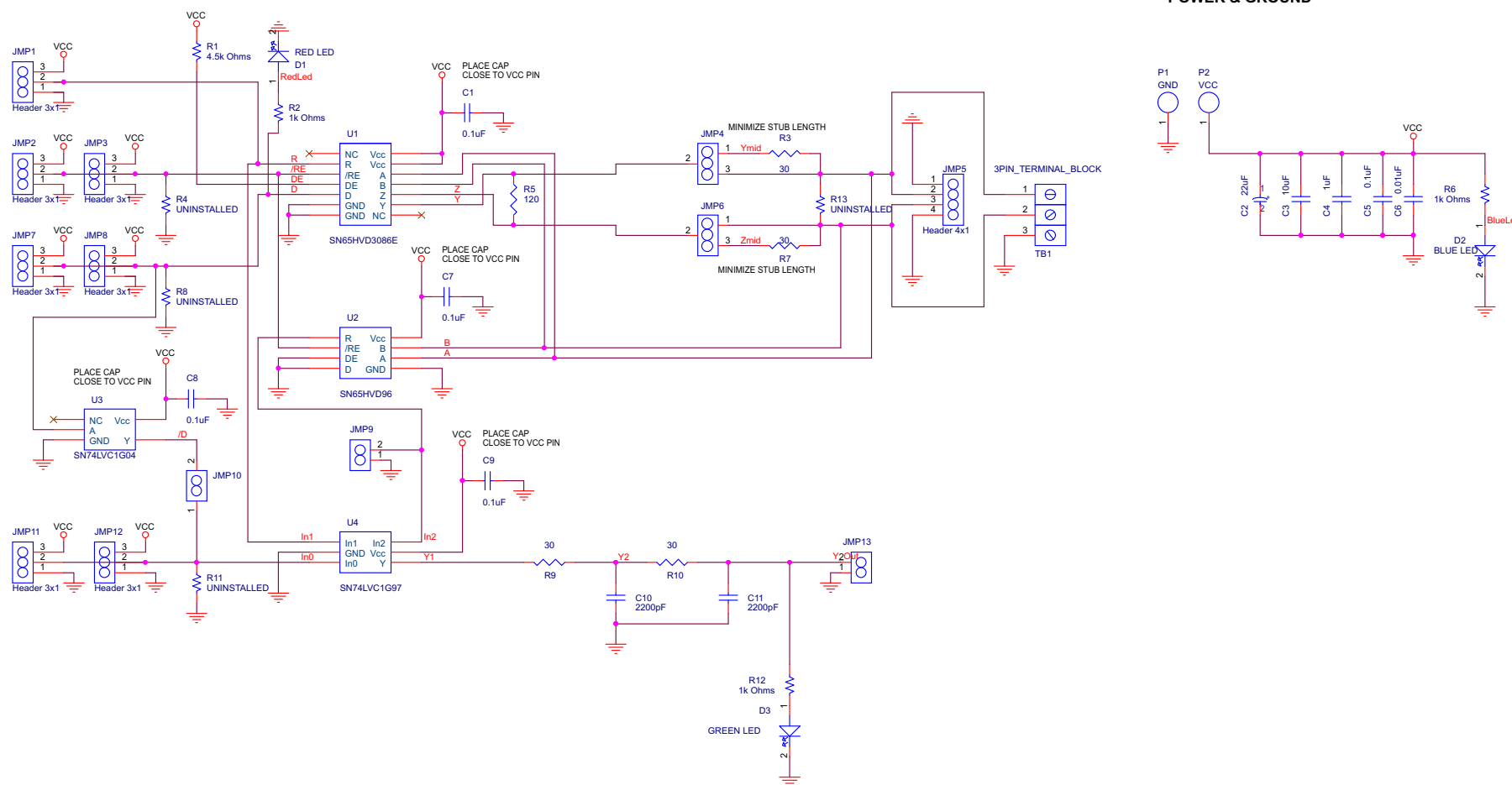


Figure 16. TIDA-00862 Schematic

## 10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00862](https://www.ti.com/lit/zip/TIDA-00862).

## 10.3 PCB Layout Recommendations

- Use VCC and ground planes to provide low-inductance.

**NOTE:** High-frequency currents follow the path of least inductance and not the path of least impedance.

- Apply 100- to 220-nF bypass capacitors as close as possible to the VCC pins of the transceiver, UART, and controller ICs on the board.
- Use at least two vias for VCC and ground connections of bypass capacitors to minimize effective via-inductance.
- Use 1- to 10-k $\Omega$  pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Minimize the stub length for the bus-series resistor selection path.
- Route the ground plane below the bus path.
- Route the single-ended signals 60  $\Omega$  and differential signals 120  $\Omega$ .

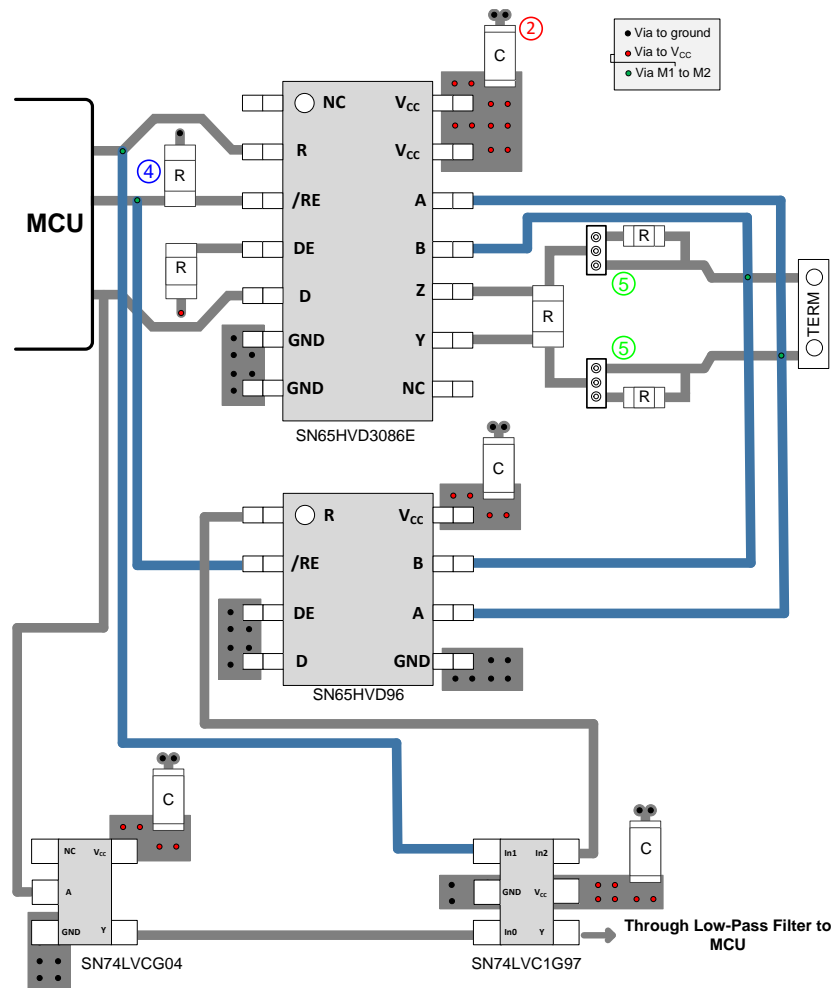


Figure 17. PCB Layout Recommendations

## 10.4 Layout Prints

To download the layout prints, see the design files at [TIDA-00862](https://www.ti.com/lit/zip/TIDA-00862).

## 10.5 Layout Guidelines

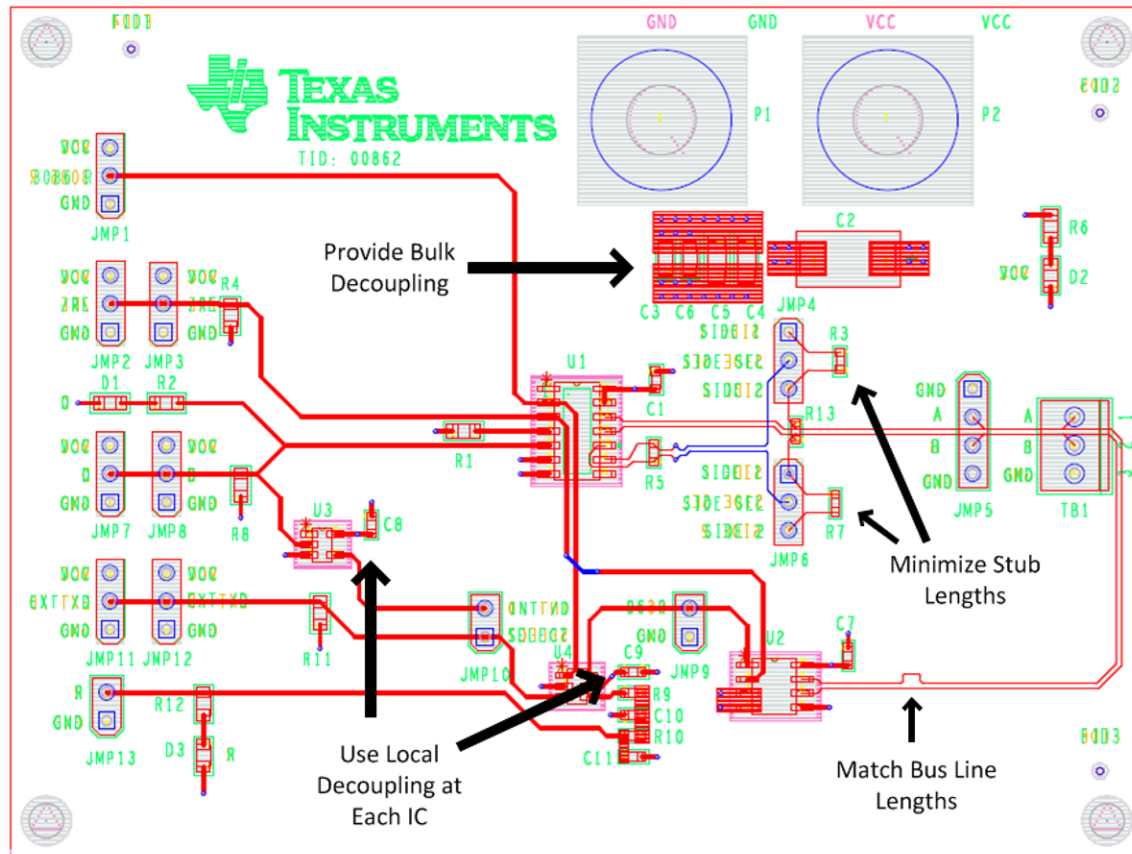


Figure 18. Layout Guidelines

## 10.6 Gerber Files

To download the Gerber files, see the design files at [TIDA-00862](https://www.ti.com/lit/zip/TIDA-00862).

## 10.7 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-00862](https://www.ti.com/lit/zip/TIDA-00862).

## 11 References

1. Texas Instruments, *The RS-485 Design Guide*, Application Report ([SLLA272](https://www.ti.com/lit/zip/SLLA272))

## 12 About the Author

**CASEY MCCREA** is an applications engineer at Texas Instruments, currently in the Industrial Interface group. Casey supports several wired interface product families including RS-485, IO-Link, CAN, and LVDS. He provides assistance with the creation of technical content for data sheets, internal part characterization, and EVM board design. Casey also supports numerous customer issues directly and via the E2E forum. Casey earned his Bachelors of Science in Electrical Engineering (BSEE) from the University of Maryland, College Park.



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