TI Designs: TIDA-00730
IEC ESD RS-485 Bus Protection

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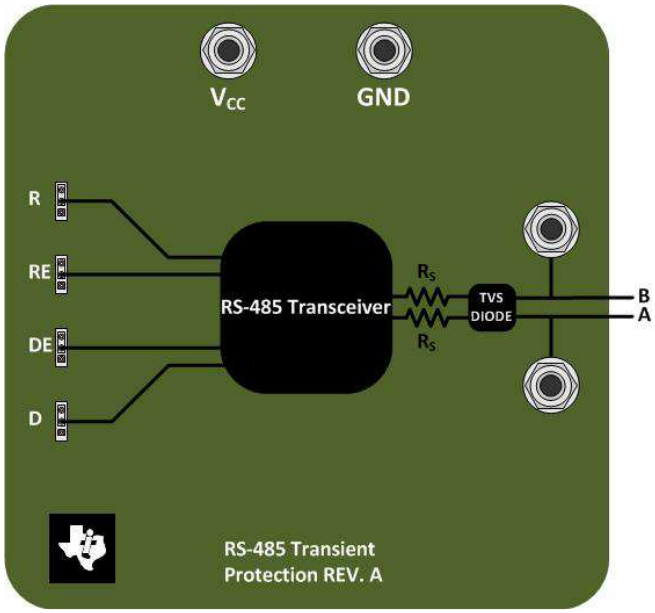
Design Features

- Board Level IEC ESD Evaluation
- Easy control of transceivers logic I/O pins
- PAD Site Evaluation Of Multiple TVS Diode Structures
- Series Pulse Proof Resistor Pads
- General Purpose Evaluation Module For Half-Duplex RS-485 Transceivers

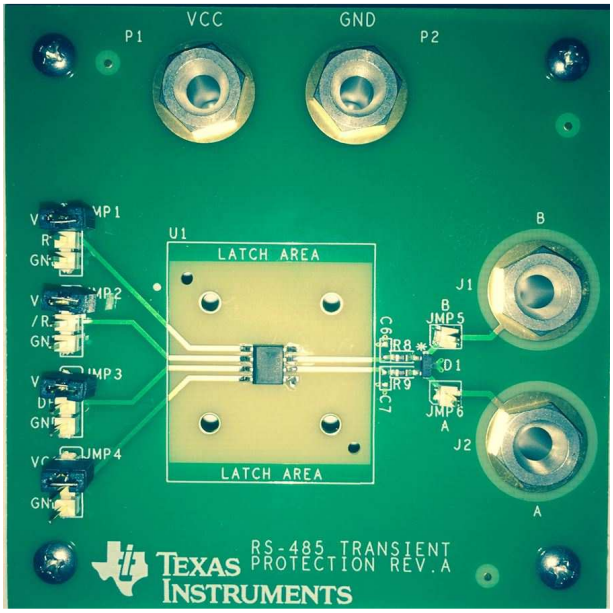
Featured Applications

- E-Meters
- Industrial Automation
- Security and Surveillance Equipment
- Encoders and Decoders

Block Diagram



Board Image



1 Design Overview

Industrial networks such as RS-485, RS-422, RS-232, CAN, and Profibus are expected to withstand harsh system-level transients in their end applications without being damaged. These events can be caused by electrostatic discharge during handling, interruption of inductive loads, relay contact bounce, and/or lightning strikes. Designing to meet these requirements can be challenging without the proper tools and knowledge about the standards that the design requires.

TI design *TIDA-00730* shows a practical example of how to protect the most sensitive components against these lethal transients. This documentation walks through the TIA/EIA-485 standard, the IEC 61000-4-x transient test standards, the implementation of system level protection against the transient and overall schematic design/layout.

2 Standards

There are many standards that can be referenced by engineers looking to ensure ESD robustness in their end design. Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM) are the most common ESD standards in industry, as most vendors provide data on these parameters in the supporting documentation for a given device. These traditional ESD models do not take into account system-level ESD events and are solely meant as device level specs. These specifications ensure that the device can make it through the handling and assembly process without being damaged by ESD.

HBM, MM, and CDM are sufficient models for many industrial applications but some industrial applications are subjected too much greater stresses. In the real world the transients that a system can be subjected to are much more severe than the levels covered by the aforementioned ESD standards. The next three sections will discuss the IEC 61000-4-2 Electrostatic Discharge Immunity Test, IEC 61000-4-4 Electrical Fast Transient/Burst Immunity Test, the IEC 61000-4-5 Surge Immunity Test standards and the expected levels of energy the industrial system can see.

2.1 IEC 61000-4-2 Electrostatic Discharge Immunity Test

The IEC 61000-4-2 ESD immunity test is a system-level ESD test that imitates a charged operator discharging onto an end system. The characteristics of the IEC ESD test differ from that of other ESD standards in rise times, the amount of energy delivered during the strike, and the number of strikes administered during the testing. There are two types of testing methods involved with the IEC ESD; contact discharge and air discharge. The contact ESD test discharges an ESD pulse from an IEC ESD gun directly onto the device under test (DUT). The air ESD discharge test involves moving the charged ESD gun towards the DUT until the air breaks down enough to allow conduction of the ESD strike between the ESD gun and the DUT. The IEC ESD testing is performed with both positive and negative polarities, and a passing score is not achieved unless both polarities at a single level are survived. Table 1 shows the IEC 61000-4-2 ESD test voltage levels and the peak current levels:

Table 1: IEC 61000-4-2 ESD Test Voltage Levels

Contact Discharge			Air Discharge	
Level	Test Voltage (kV)	Peak Current (A)	Level	Test Voltage (kV)
1	2	7.5	1	2
2	4	15	2	4
3	6	22.5	3	8
4	8	30	4	15
*	Special	Special	*	Special

* is an open level. The level has to be specified in the dedicated equipment speciation. If higher voltages than those shown are specified, special test equipment may be needed.

Figure 1 depicts the basic shape of the IEC ESD pulse and shows the timing sequence of the test pulses.

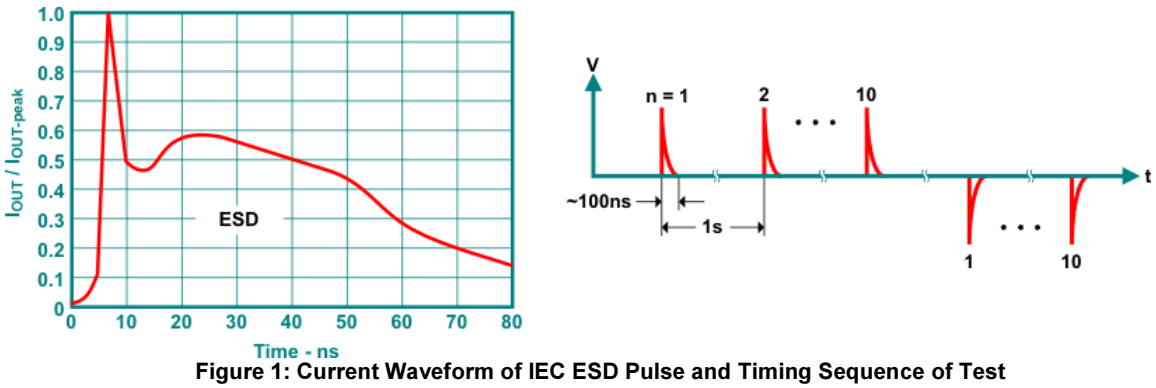


Figure 1: Current Waveform of IEC ESD Pulse and Timing Sequence of Test

2.2 IEC 61000-4-4 Electrical Fast Transient/Burst Immunity Test

The IEC 61000-4-4 electrical fast transient (EFT) or burst immunity test is meant to simulate the switching transients caused by the interruption of inductive loads, relay contact bounce, etc. The EFT test is performed on power lines, I/O data lines, I/O control lines and earth wires. The EFT test is a burst of pulses that have predetermined amplitude and limited duration. The typical duration of a burst is 15 ms at a repetition rate of 5 kHz, although 100 kHz repetition is a more realistic test. The burst period, which is the time from the start of one burst to the start of the next burst, is 300 ms. The test requires the application of six burst frames of ten seconds duration with ten second pauses between frames. In a typical EFT test sequence 3 million pulses will be delivered to the DUT via a capacitive clamp which couples the energy into the system. Table 2 below shows the IEC 61000-4-4 EFT test voltage levels and repetition rates:

Table 2: IEC 61000-4-2 ESD Test Voltage Levels

	On Power Port, PE		On I/O Signal, data and control ports	
Level	Test Voltage (kV)	Repetition Rate (kHz)	Test Voltage (kV)	Repetition Rate (kHz)
1	0.5	5 or 100	0.25	5 or 100
2	1	5 or 100	0.5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
*	Special	Special	*	Special

*Is an open level. The level has to be specified in the dedicated equipment specification.

Figure 2 below depicts the basic shape of the IEC EFT pulse and shows the timing sequence of the test pulses.

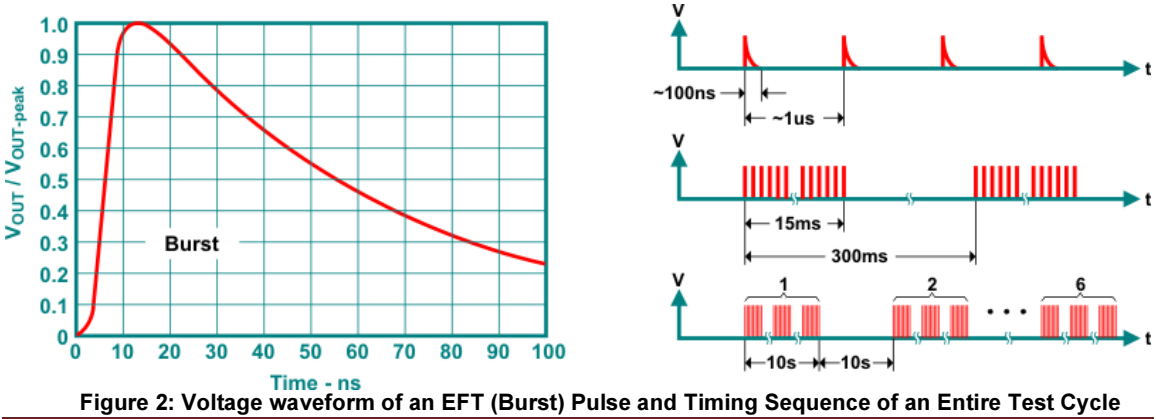


Figure 2: Voltage waveform of an EFT (Burst) Pulse and Timing Sequence of an Entire Test Cycle

2.3 IEC 61000-4-5 Surge Immunity Test

The IEC 61000-4-5 Surge immunity test is the most severe transient immunity test in terms of current and duration. This test is meant to simulate transients caused by direct or indirect lightning strikes as well as the switching of power systems including load changes and short circuits.

The surge generator's output waveforms are specified for open and short circuit conditions. Characteristics for this test are high current (due to low generator impedance) and long pulse duration. Pulse duration for the surge immunity test is approximately 1000 times longer than that of IEC ESD and IEC EFT, resulting in high-energy pulses.

This test requires five positive surge pulses and five negative surge pulses with a time interval between pulses of one minute. Typically though, this time interval is reduced to something shorter than one minute to help reduce overall test time.

Table 3: IEC Surge Open Circuit Voltage Test Levels

Level	Open-circuit voltage ±10% (kV)
1	0.5
2	1
3	2
4	4
*	Special

* Can be any level above, below, or in between the other levels. This level can be specified in the product standard.

Figure 3 below depicts the basic shape of the IEC surge pulse and shows the timing sequence of the test pulses.

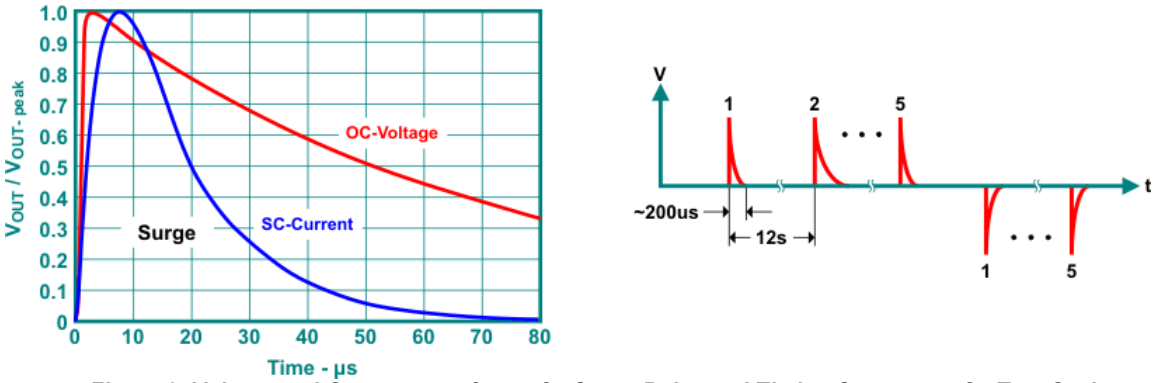


Figure 3: Voltage and Current waveform of a Surge Pulse and Timing Sequence of a Test Cycle

3 System Description

In this TI Design, a TVS diode is implemented on each bus line along with series pulse proof resistors to protect the RS-485 transceiver from lethal ESD, EFT (burst), and surge transients. The TVS diode acts as a clamping circuit to redirect the transient energy to ground while the pulse proof resistors act as a current limiter to protect the bus lines from dangerous overvoltage conditions. Figure 4 shows the TI Design with all of its components:

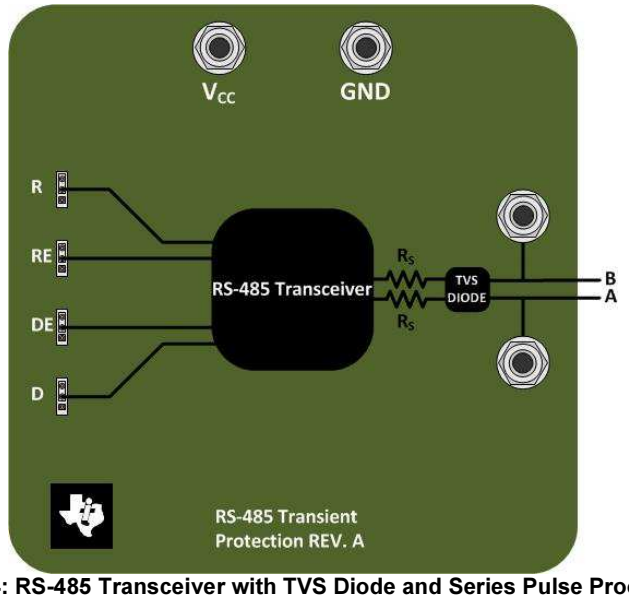


Figure 4: RS-485 Transceiver with TVS Diode and Series Pulse Proof Resistors

4 TIA/EIA-485 Standard and Transceivers

4.1 TIA/EIA-485 Standard

TIA/EIA-485 is a differential signaling standard which defines the electrical characteristics of drivers and receivers used to implement a balanced, multi-point transmission line. A compliant TIA/EIA-485 transceiver must support a differential signal of 1.5 V across a 54 Ω load as well as a -7 V-to-+12 V common mode voltage range. RS-485 transceivers are designed to support a wide range of serial data transmission data rates over very long distances (up to ~1000 meters).

Texas Instruments RS-485 transceivers meet or exceed the requirements set by the TIA/EIA-485 standard and support other features like automatic polarity correction, receiver equalization, 1.8 V I/O levels, and integrated IEC ESD protection. While all of these features are nice to have, this TI Design only focuses on the SN65HVD3082E (a standard 5-V RS-485 transceiver), and the SN65HVD82 (a 5-V transceiver with integrated IEC ESD protection).

4.1.1 SN65HVD3082E

The SN65HVD308xE family of transceivers support half-duplex operation and are designed for RS-485 data bus networks. They are powered by a 5-V supply, support data rates up to 20 Mbps, and are fully compliant to the TIA/EIA-485 standard.

4.1.2 SN65HVD82

The SN65HVD82 transceiver supports half-duplex operation and is designed for RS-485 data bus networks in demanding industrial applications. The SN65HVD82 is powered by a 5-V supply, is optimized for data rates up to 250 kbps, and is fully compliant to the TIA/EIA-485 standard. The bus pins, A and B, have integrated ESD protection making them robust to ESD events with high levels of protection against HBM, Air-Gap Discharge, CDM, IEC 61000-4-2,

and IEC 61000-4-4. The SN65HVD82 supports ±12 kV of IEC ESD protection, ±16 kV HBM protection, and ± 4kV IEC EFT protection on die.

5 System Design Theory

This TI Design features the CDSOT23-SM712 TVS diode from Bourns Inc., series pulse proof resistors, a pad site for an 8 pin SOIC RS-485 transceiver with the SN65HVD82 installed, and banana jacks for injecting the ESD, EFT, and surge test pulses. The concept behind the design is to protect the RS-485 transceiver from lethal transients that can occur in real world applications caused by electrostatic discharge during handling, interruption of inductive loads, relay contact bounce, and/or lightning strikes. If the energy that is delivered during one of these transient events is large enough in amplitude it can permanently damage the device.

The TVS is placed very close the board connector where the bus lines enter the design to ensure that any transient energy coupled onto the bus is minimized at the point of origin. The TVS acts as a clamping circuit to redirect any high energy pulses to ground and away from the transceiver. The diode needs to be rated for the type of energy levels that are expected per the design. This design was done with the IEC 61000-4-2 standard in mind, and the CDSOT23-SM712 is rated for this application.

The series pulse-proof resistors on the A and B bus lines limit the residual clamping current the transceiver sees if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors are typically very low in value (~10-20Ω) and should be selected to accommodate the appropriate power levels.

6 Getting Started Hardware

The reference design is a simple design that includes pulse proof resistors, a CDSOT23-SM712 TVS diode from Bourns, and a SN65HVD82 RS-485 transceiver from Texas Instruments. V_{CC} and GND are connected to the reference design via the banana jacks that can be identified via the silkscreen on the board. The device can be placed into drive mode by pulling the driver enable (DE) pin high via the three pin berg header labeled DE. Pulling DE low disables the driver. The board can be placed into receive mode by pulling the receiver enable pin low (/RE) via the three pin berg header labeled /RE. Pulling /RE high disables the receiver. Once the proper mode is enabled, the device functionality can be checked via the three pin berg header labeled R which is the receiver pin, the three pin berg header labeled D which is the driver pin, and the bus pins via single terminal berg pins labeled A and B.

Once device functionality is verified, the transient testing can be done via the two banana jacks connected to the bus pins. The IEC ESD contact test pulses can be injected onto the bus pins by directly touching the banana jacks and discharging the pulses. The IEC ESD air test pulses can be injected onto the bus pins by using either the banana jacks or the single pole berg headers by approaching the contact point slowly until the ESD gun discharges. Care should be taken to ensure that the appropriate bus pin is struck during the air testing as the ESD pulse can jump from pin to pin if the ESD gun is close to both the A and B pins. The EFT test can be performed by connecting your bus wire to the A and B pins and inserting it into the capacitive clamp defined by the IEC 61000-4-4 standard. The surge generator uses shielded banana jacks to couple the energy onto the bus pins directly.

When performing these types of compliance tests, the test methods should be followed as it is laid out in the standards documentation. After each test level is completed the leakage current should be observed as this is a clear indication that something broke in the device.

The device should be checked for general functionality in both the driver and receiver directions. Figure 5 shows an overview of the board with descriptions of each point.

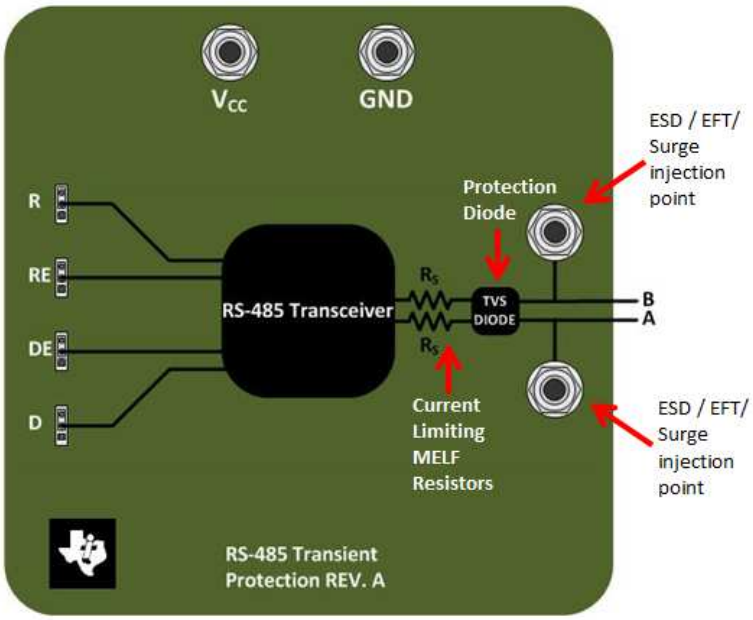


Figure 5: RS-485 Transient EVM Overview

7 Test Setup

Figures 5, 6, and 7 below show the test setups used in the IEC immunity compliance testing for this RS-485 design. Figure 5 shows the IEC ESD setup. The setup used for this testing is fully compliant to the IEC ESD specification. Figure 6 shows the EFT and surge generator box. The EFT/surge generator box is made by EMC-Partner and is model number CDN-UTP. Figure 7 shows the complete test setup with the capacitive clamp defined in the IEC 61000-4-4 standard as well as the protective cases used to encase the DUTS during testing. Figure 8 shows a close up image of the capacitive clamp used to couple the EFT pulses onto the bus cable.

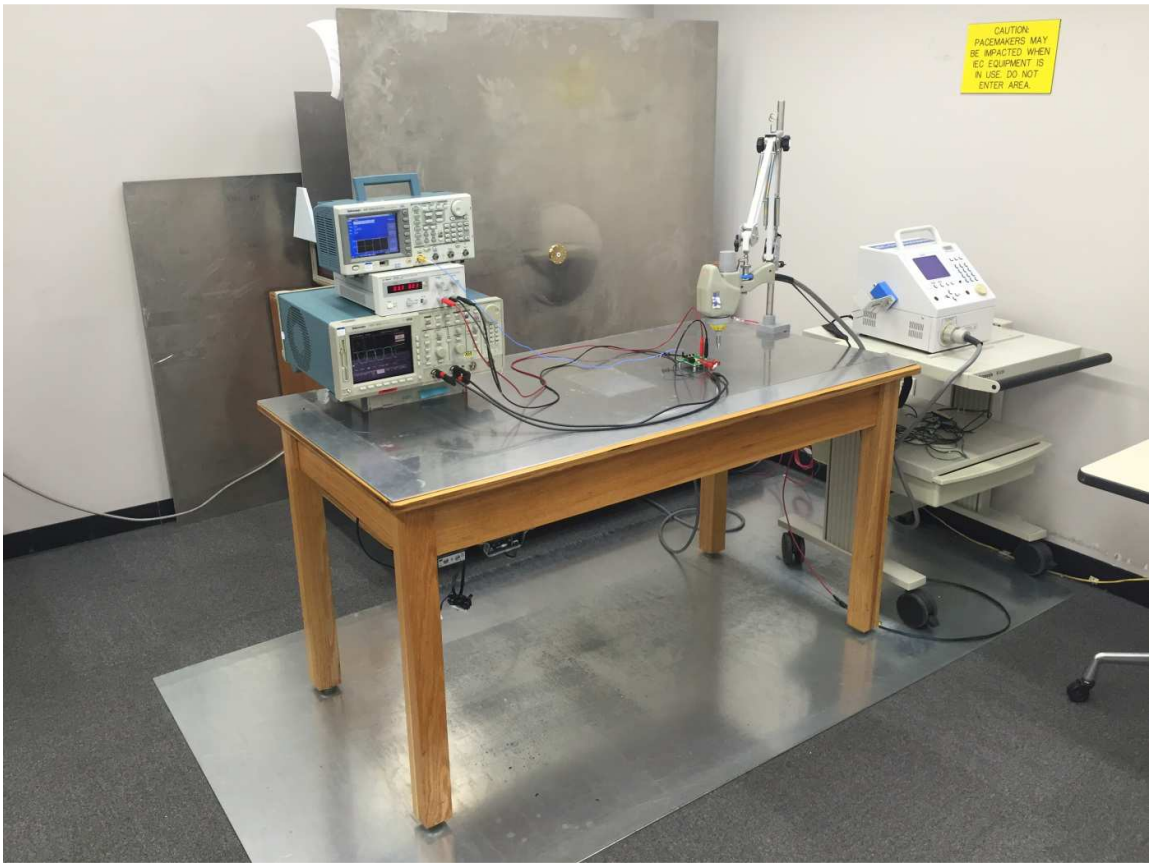


Figure 6: IEC ESD Compliant Test Setup

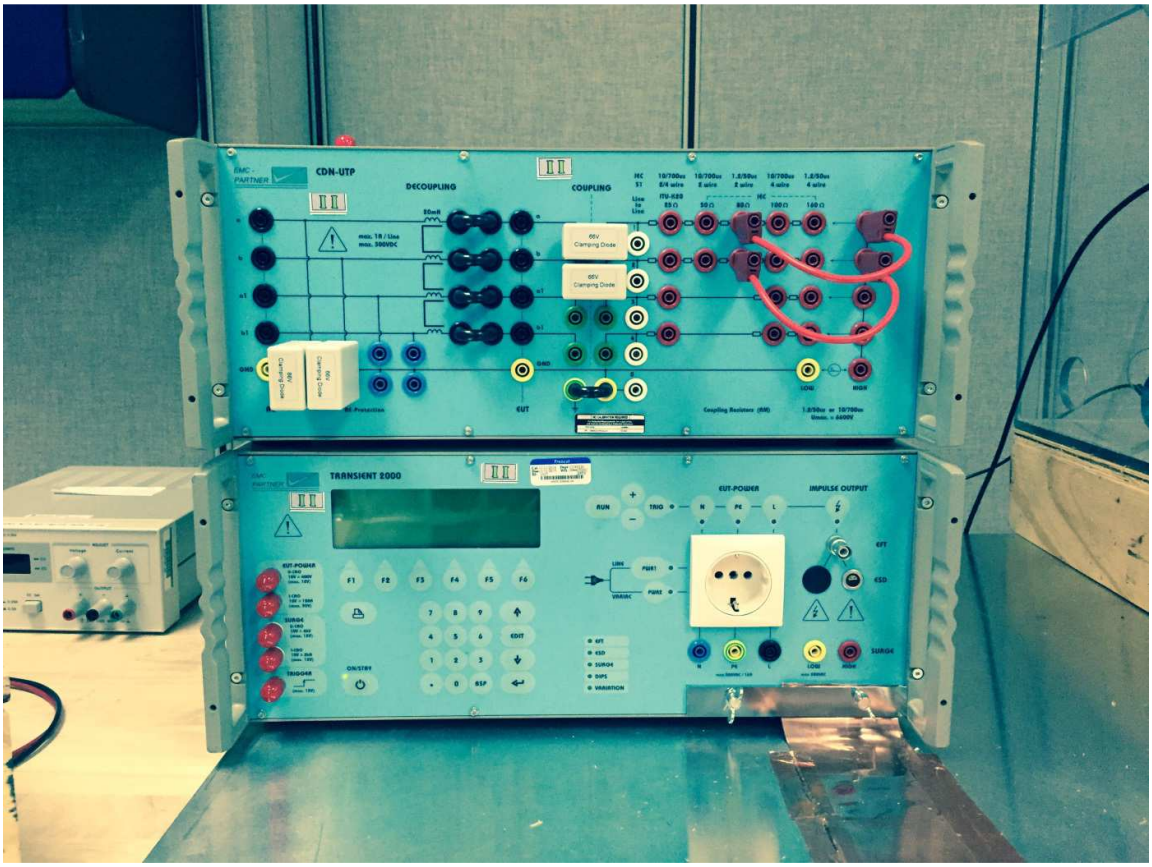


Figure 7: Electrical Fast Transient (EFT) and Surge Generator

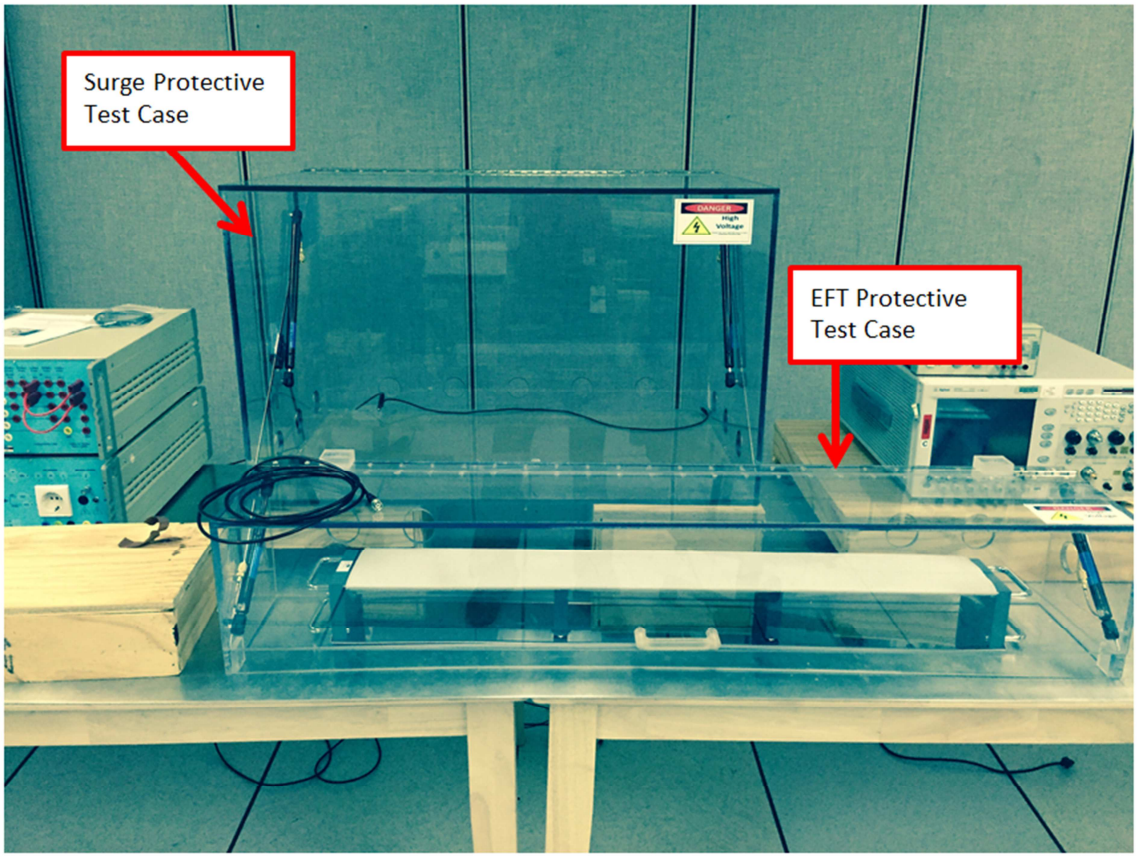


Figure 8: EFT and Surge Test Setup

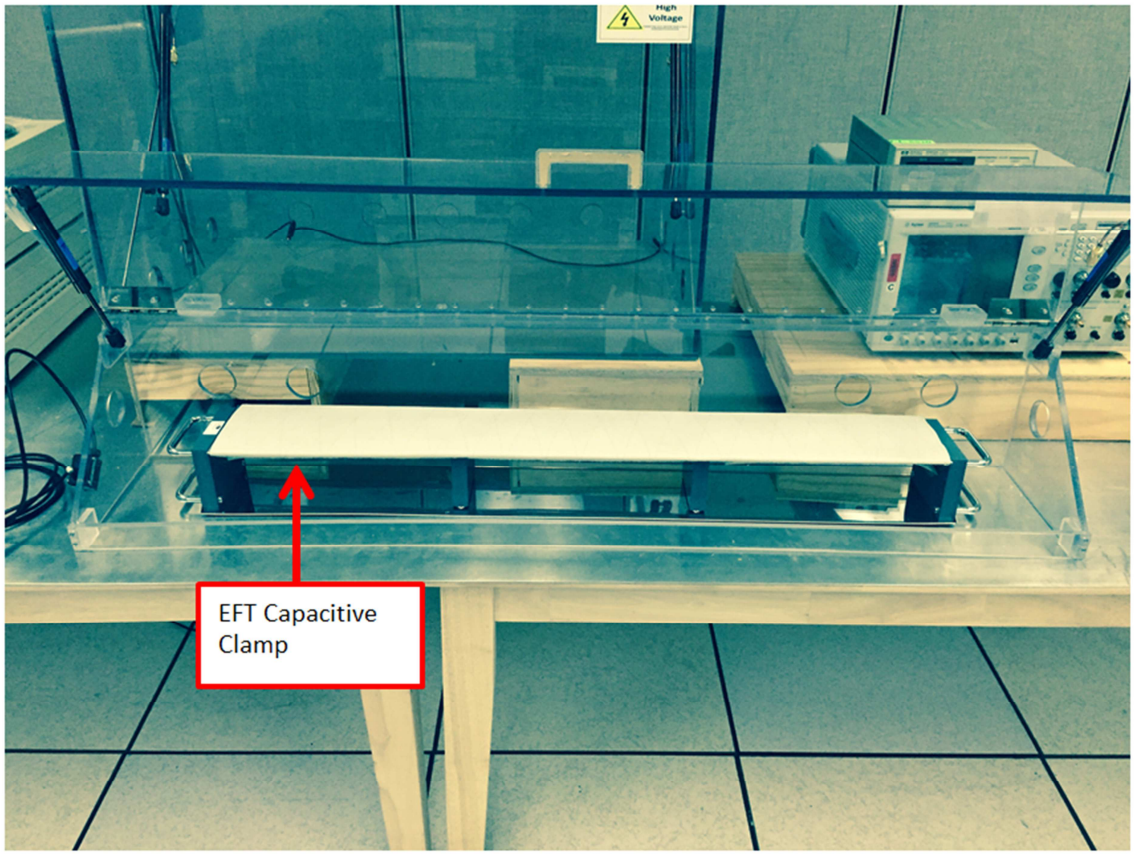


Figure 9: EFT Capacitive Clamp

8 Test Data

Below the test results for the SN65HVD3082E and the SN65HVD82 are summarized for the IEC 61000-4-2 ESD immunity test, the IEC 61000-4-4 EFT immunity test, and the IEC 61000-4-5 surge immunity test.

Table 4: Summary of Test Results

Protection Scheme	IEC ESD (kV)	IEC EFT (kV)	IEC Surge (kV)
SN65HVD82			
TVS	±30 Contact ±30 Air	±4	±1
SN65HVD3082E			
TVS	±14 Contact ±30 Air	±4	±1

Table 5: IEC ESD Contact Discharge Test Results

RS-485 IEC ESD Test Results						
Positive Contact ESD Strikes						
IEC ESD Level	**SN65HVD82**			SN65HVD3082		
	Board 1	Board 2	Board 3	Board 1	Board 2	Board 3
+4kV	✓	✓	✓	✓	✓	✓
+5kV	✓	✓	✓	✓	✓	✓
+6kV	✓	✓	✓	✓	✓	✓
+7kV	✓	✓	✓	✓	✓	✓
+8kV	✓	✓	✓	✓	✓	✓
+9kV	✓	✓	✓	✓	✓	✓
+10kV	✓	✓	✓	✓	✓	✓
+11kV	✓	✓	✓	✓	✓	✓
+12kV	✓	✓	✓	✓	✓	✓
+13kV	✓	✓	✓	✓	✓	✓
+14kV	✓	✓	✓	✓	✓	✓
+15kV	✓	✓	✓	×	×	×
+16kV	✓	✓	✓	NT	NT	NT
+17kV	✓	✓	✓	NT	NT	NT
+18kV	✓	✓	✓	NT	NT	NT
+19kV	✓	✓	✓	NT	NT	NT
+20kV	✓	✓	✓	NT	NT	NT
+21kV	✓	✓	✓	NT	NT	NT
+22kV	✓	✓	✓	NT	NT	NT
+23kV	✓	✓	✓	NT	NT	NT
+24kV	✓	✓	✓	NT	NT	NT
+25kV	✓	✓	✓	NT	NT	NT
+26kV	✓	✓	✓	NT	NT	NT
+27kV	✓	✓	✓	NT	NT	NT
+28kV	✓	✓	✓	NT	NT	NT
+29kV	✓	✓	✓	NT	NT	NT
+30kV	✓	✓	✓	NT	NT	NT
IEC ESD Level	Negative Contact ESD Strikes					
	Board 1	Board 2	Board 3	Board 1	Board 2	Board 3
-4kV	✓	✓	✓	✓	✓	✓
-5kV	✓	✓	✓	✓	✓	✓
-6kV	✓	✓	✓	✓	✓	✓
-7kV	✓	✓	✓	✓	✓	✓
-8kV	✓	✓	✓	✓	✓	✓
-9kV	✓	✓	✓	✓	✓	✓
-10kV	✓	✓	✓	✓	✓	✓
-11kV	✓	✓	✓	✓	✓	✓
-12kV	✓	✓	✓	✓	✓	✓
-13kV	✓	✓	✓	✓	✓	✓
-14kV	✓	✓	✓	✓	✓	✓
-15kV	✓	✓	✓	✓	✓	✓
-16kV	✓	✓	✓	✓	✓	✓
-17kV	✓	✓	✓	✓	✓	✓
-18kV	✓	✓	✓	✓	✓	✓
-19kV	✓	✓	✓	✓	✓	✓
-20kV	✓	✓	✓	✓	✓	✓
-21kV	✓	✓	✓	✓	✓	✓
-22kV	✓	✓	✓	✓	✓	✓
-23kV	✓	✓	✓	✓	✓	✓
-24kV	✓	✓	✓	✓	✓	✓
-25kV	✓	✓	✓	✓	✓	✓
-26kV	✓	✓	✓	✓	✓	✓
-27kV	✓	✓	✓	✓	✓	✓
-28kV	✓	✓	✓	✓	✓	✓
-29kV	✓	✓	✓	✓	✓	✓
-30kV	✓	✓	✓	✓	✓	✓

Table 6: IEC ESD Air Discharge Test Results

RS-485 IEC ESD Test Results						
Positive Air ESD Strikes						
IEC ESD Level	**SN65HVD82**			SN65HVD3082		
	Board 1	Board 2	Board 3	Board 1	Board 2	Board 3
+4kV	✓	✓	✓	✓	✓	✓
+5kV	✓	✓	✓	✓	✓	✓
+6kV	✓	✓	✓	✓	✓	✓
+7kV	✓	✓	✓	✓	✓	✓
+8kV	✓	✓	✓	✓	✓	✓
+9kV	✓	✓	✓	✓	✓	✓
+10kV	✓	✓	✓	✓	✓	✓
+11kV	✓	✓	✓	✓	✓	✓
+12kV	✓	✓	✓	✓	✓	✓
+13kV	✓	✓	✓	✓	✓	✓
+14kV	✓	✓	✓	✓	✓	✓
+15kV	✓	✓	✓	✓	✓	✓
+16kV	✓	✓	✓	✓	✓	✓
+17kV	✓	✓	✓	✓	✓	✓
+18kV	✓	✓	✓	✓	✓	✓
+19kV	✓	✓	✓	✓	✓	✓
+20kV	✓	✓	✓	✓	✓	✓
+21kV	✓	✓	✓	✓	✓	✓
+22kV	✓	✓	✓	✓	✓	✓
+23kV	✓	✓	✓	✓	✓	✓
+24kV	✓	✓	✓	✓	✓	✓
+25kV	✓	✓	✓	✓	✓	✓
+26kV	✓	✓	✓	✓	✓	✓
+27kV	✓	✓	✓	✓	✓	✓
+28kV	✓	✓	✓	✓	✓	✓
+29kV	✓	✓	✓	✓	✓	✓
+30kV	✓	✓	✓	✓	✓	✓
IEC ESD Level	Negative Air ESD Strikes					
	Board 1	Board 2	Board 3	Board 1	Board 2	Board 3
-5kV	✓	✓	✓	✓	✓	✓
-6kV	✓	✓	✓	✓	✓	✓
-7kV	✓	✓	✓	✓	✓	✓
-8kV	✓	✓	✓	✓	✓	✓
-9kV	✓	✓	✓	✓	✓	✓
-10kV	✓	✓	✓	✓	✓	✓
-11kV	✓	✓	✓	✓	✓	✓
-12kV	✓	✓	✓	✓	✓	✓
-13kV	✓	✓	✓	✓	✓	✓
-14kV	✓	✓	✓	✓	✓	✓
-15kV	✓	✓	✓	✓	✓	✓
-16kV	✓	✓	✓	✓	✓	✓
-17kV	✓	✓	✓	✓	✓	✓
-18kV	✓	✓	✓	✓	✓	✓
-19kV	✓	✓	✓	✓	✓	✓
-20kV	✓	✓	✓	✓	✓	✓
-21kV	✓	✓	✓	✓	✓	✓
-22kV	✓	✓	✓	✓	✓	✓
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-25kV	✓	✓	✓	✓	✓	✓
-26kV	✓	✓	✓	✓	✓	✓
-27kV	✓	✓	✓	✓	✓	✓
-28kV	✓	✓	✓	✓	✓	✓
-29kV	✓	✓	✓	✓	✓	✓
-30kV	✓	✓	✓	✓	✓	✓

Table 7: IEC Electrical Fast Transient Test Results

RS-485 IEC EFT Test Results			
Positive EFT Strikes			
IEC EFT Level	SN65HVD82 Board 1	SN65HVD82 Board 2	SN65HVD82 Board 3
+0.5kV	✓	✓	✓
+1kV	✓	✓	✓
+2kV	✓	✓	✓
+4kV	✓	✓	✓
Negative EFT Strikes			
IEC EFT Level	SN65HVD82 Board 1	SN65HVD82 Board 2	SN65HVD82 Board 3
-0.5kV	✓	✓	✓
-1kV	✓	✓	✓
-2kV	✓	✓	✓
-4kV	✓	✓	✓
Positive EFT Strikes			
IEC EFT Level	SN65HVD3082E Board 1	SN65HVD3082E Board 2	SN65HVD3082E Board 3
+0.5kV	✓	✓	✓
+1kV	✓	✓	✓
+2kV	✓	✓	✓
+4kV	✓	✓	✓
Negative EFT Strikes			
IEC EFT Level	SN65HVD3082E Board 1	SN65HVD3082E Board 2	SN65HVD3082E Board 3
-0.5kV	✓	✓	✓
-1kV	✓	✓	✓
-2kV	✓	✓	✓
-4kV	✓	✓	✓

Table 8: IEC Surge Test Results

RS-485 IEC Surge Test Results			
Positive Surge Strikes			
IEC EFT Level	SN65HVD82 Board 1	SN65HVD82 Board 2	SN65HVD82 Board 3
+0.5kV	✓	✓	✓
+1kV	✓	✓	✓
+2kV	✗	✗	✗
+4kV	NT	NT	NT
Negative Surge Strikes			
IEC EFT Level	SN65HVD82 Board 1	SN65HVD82 Board 2	SN65HVD82 Board 3
+0.5kV	✓	✓	✓
+1kV	✓	✓	✓
+2kV	✗	✗	✗
+4kV	NT	NT	NT
Positive Surge Strikes			
IEC EFT Level	SN65HVD3082E Board 1	SN65HVD3082E Board 2	SN65HVD3082E Board 3
+0.5kV	✓	✓	✓
+1kV	✓	✓	✓
+2kV	✗	✗	✗
+4kV	NT	NT	NT
Negative Surge Strikes			
IEC EFT Level	SN65HVD3082E Board 1	SN65HVD3082E Board 2	SN65HVD3082E Board 3
+0.5kV	✓	✓	✓
+1kV	✓	✓	✓
+2kV	✗	✗	✗
+4kV	NT	NT	NT

8.1 Test Results

The test results show that by adding a TVS diode to the A and B bus lines of both the SN65HVD3082E and SN65HVD82 transceivers, the transient immunity increases significantly. The designs pass IEC ESD level 4 criteria, IEC EFT level 4 criteria, and IEC surge level 2 criteria. Both designs also fall into the “special” characteristic per the IEC ESD standard as the SN65HVD3082E passes IEC ESD up to ±14kV while the SN65HVD82 passes up to ±30kV IEC ESD, surpassing the level 4 ESD voltage.

Not every design or application will require ±30kV of ESD protection, but for those applications that do, the SN65HVD82 coupled with the CDSOT23-SM712 TVS diode from Bourns will provide this. For designs that do not require this level of protection but need to be rated up to level 4 IEC ESD (±8kV), coupling the SN65HVD3082E with the same CDSOT23-SM712 diode takes a standard RS-485 transceiver with no integrated IEC ESD protection to ±14kV IEC ESD protection.

9 9. Design Files

9.1 Schematics

To download the Schematics for each board, see the design files at
http://www.ti.com/tool/tidu00730

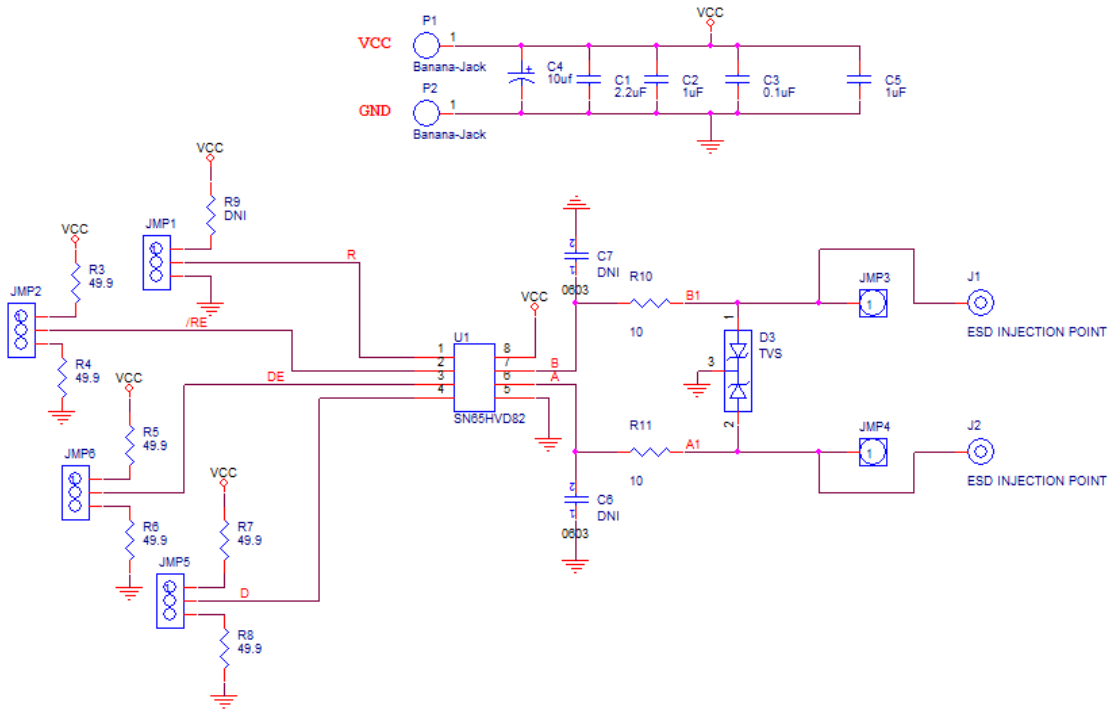

Figure 10: IEC ESD RS-485 Bus Protection Schematic

9.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at
http://www.ti.com/tool/tidu00730

Table 1: TIDA-00730 BOM

Bill Of Materials

TIDA-00730 – IEC ESD RS-485 Bus Protection

Item	Qty	Reference	Value	Manufacturer	Manufacturer Part Number	PCB Footprint
1	1	C1	2.2uF	Any	Any (5V+ Rating)	1206
2	1	C2	1uF	Any	Any (5V+ Rating)	0805
3	1	C3	0.1uF	Any	Any (5V+ Rating)	0603
4	1	C4	10uf	Any	Any (5V+ Rating)	7343
5	1	C5	1uF	Any	Any (5V+ Rating)	0402
6	3	C6,C7,R9	DNI	Any	Any (5V+ Rating)	0603
7	1	D3	TVS	Bourns	CDSOT23-SM712	SOT_23_321
8	4	JMP1,JMP2,JMP5,JMP6	Header 3x1	Samtec	HTSW-150-08-G-S	berg1x3
9	2	JMP3,JMP4	Header 1x1	Samtec	HTSW-150-08-G-S	berg1x1
10	2	J1,J2, P1, P2	Solderless Banana Jack	Emerson Network Power Co	108-0740-001	
11	6	R3,R4,R5,R6,R7,R8	49.9	Any	Any (1% Tolerance)	0603
12	2	R10,R11	10	Any	Any (1% Tolerance)	0603
13	1	U1	8D Half-Duplex	Texas Instruments	SN65HVD82	8Pin D

9.3 PCB Layout Recommendations

1) Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.

2) Use V_{CC} and ground planes to provide low-inductance.
   i. **NOTE:** High-frequency currents follow the path of least inductance and not the path of least impedance.

3) Design the protection components into the direction of the signal path. Do not force the transient's currents to divert from the signal path to reach the protection device.

4) Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC pins of transceiver, UART, and controller ICs on the board.

5) Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.

6) Use 1-kΩ to 10-kΩ pull up or pulldown resistors for enable lines to limit noise currents in these lines during transient events.

7) Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

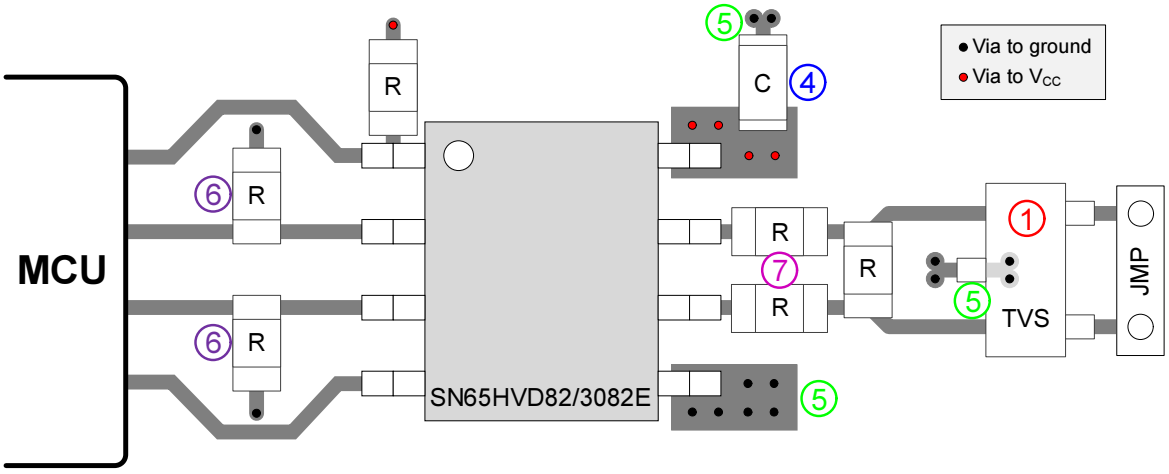

Figure 11: Layout Example

9.3.1 Layout Prints

To download the Layout Prints for each board, see the design files at http://www.ti.com/tool/tidu00730

TOP SILKSCREEN

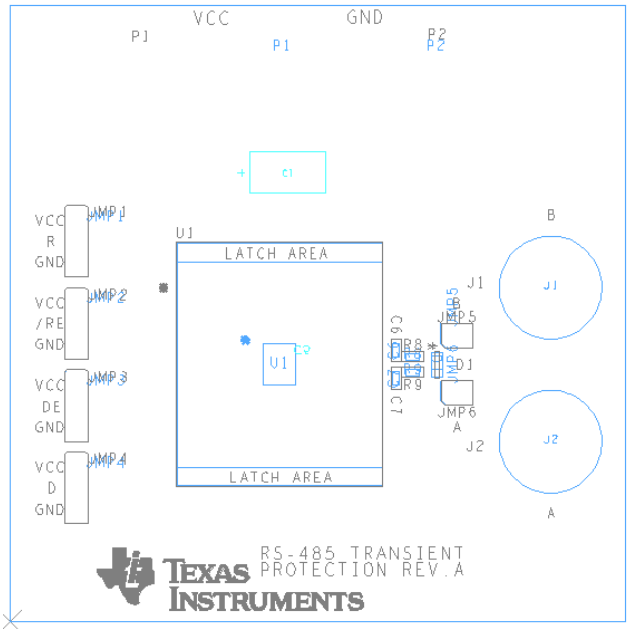

Figure 12: Top Silkscreen

TOP SOLDER MASK

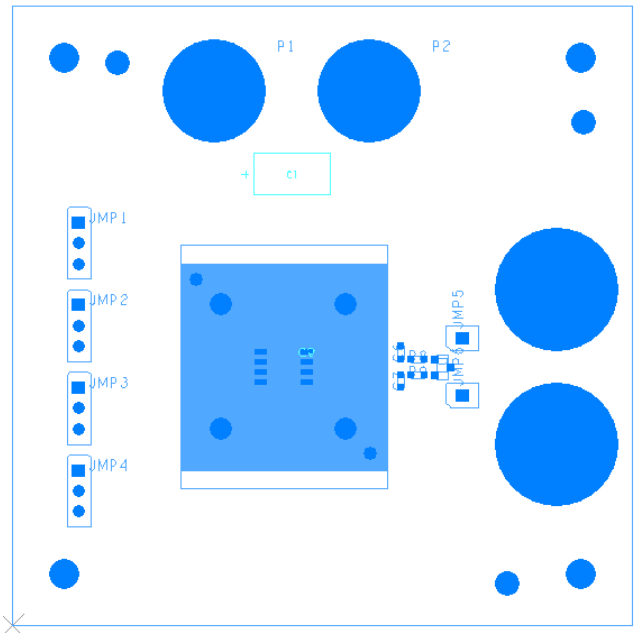

Figure 13: Top Solder Mask

TOP LAYER

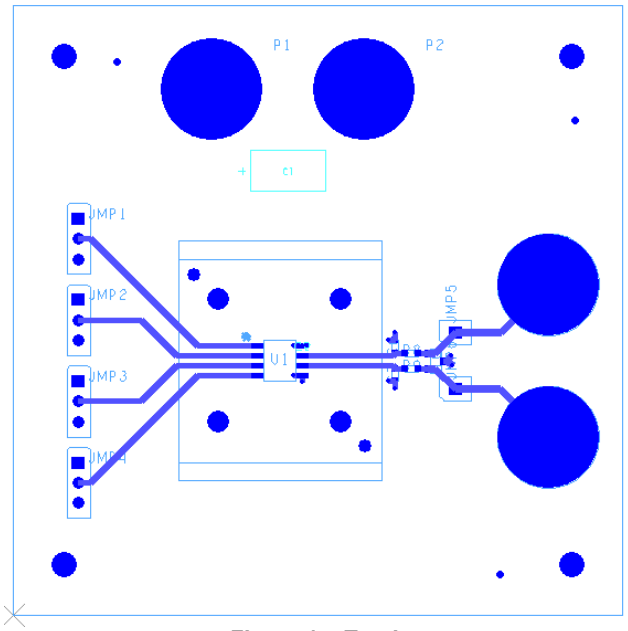

Figure 14: Top Layer

BOTTOM LAYER

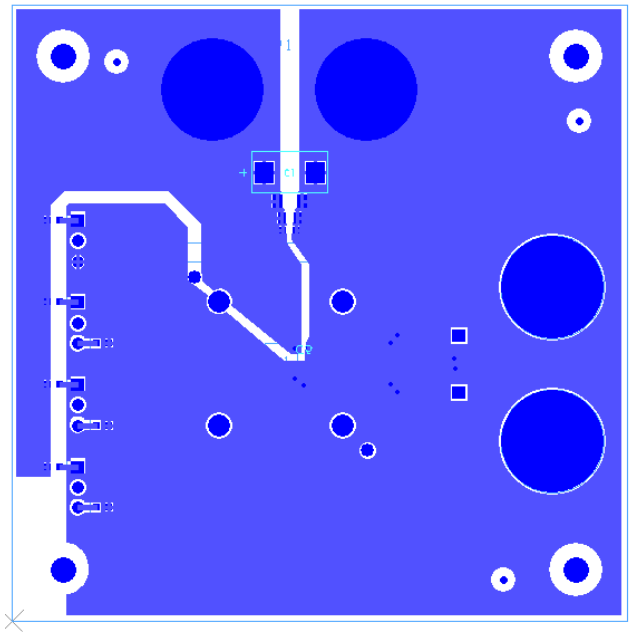

Figure 15: Bottom Layer

BOTTOM SOLDER MASK

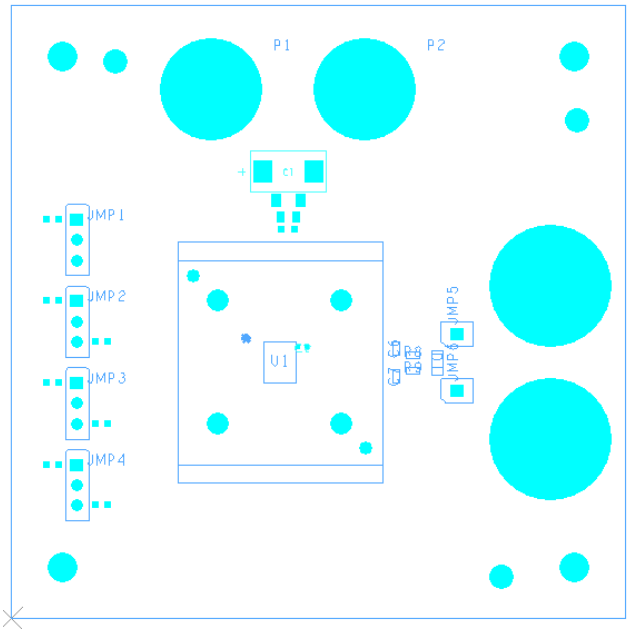

Figure 16: Bottom Solder Mask

BOTTOM SILKSCREEN

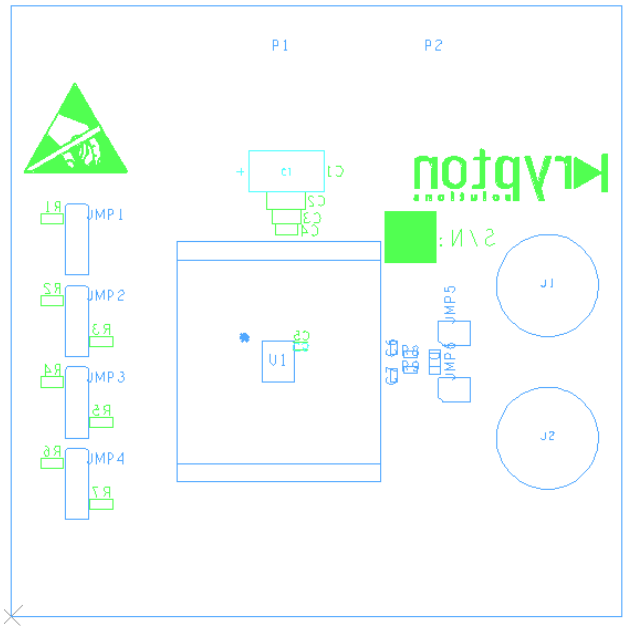

Figure 17: Bottom Silkscreen

MECHANICAL DIMENSIONS

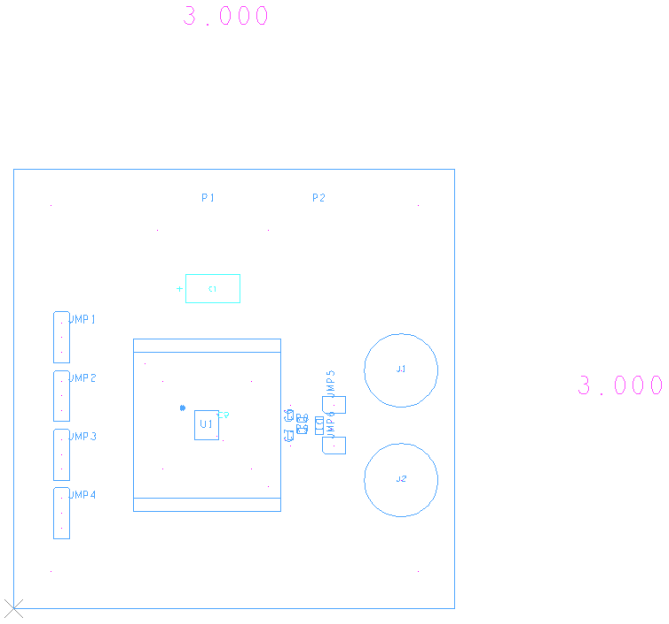

Figure 18: Mechanical Dimensions

9.4 Layout Guidelines

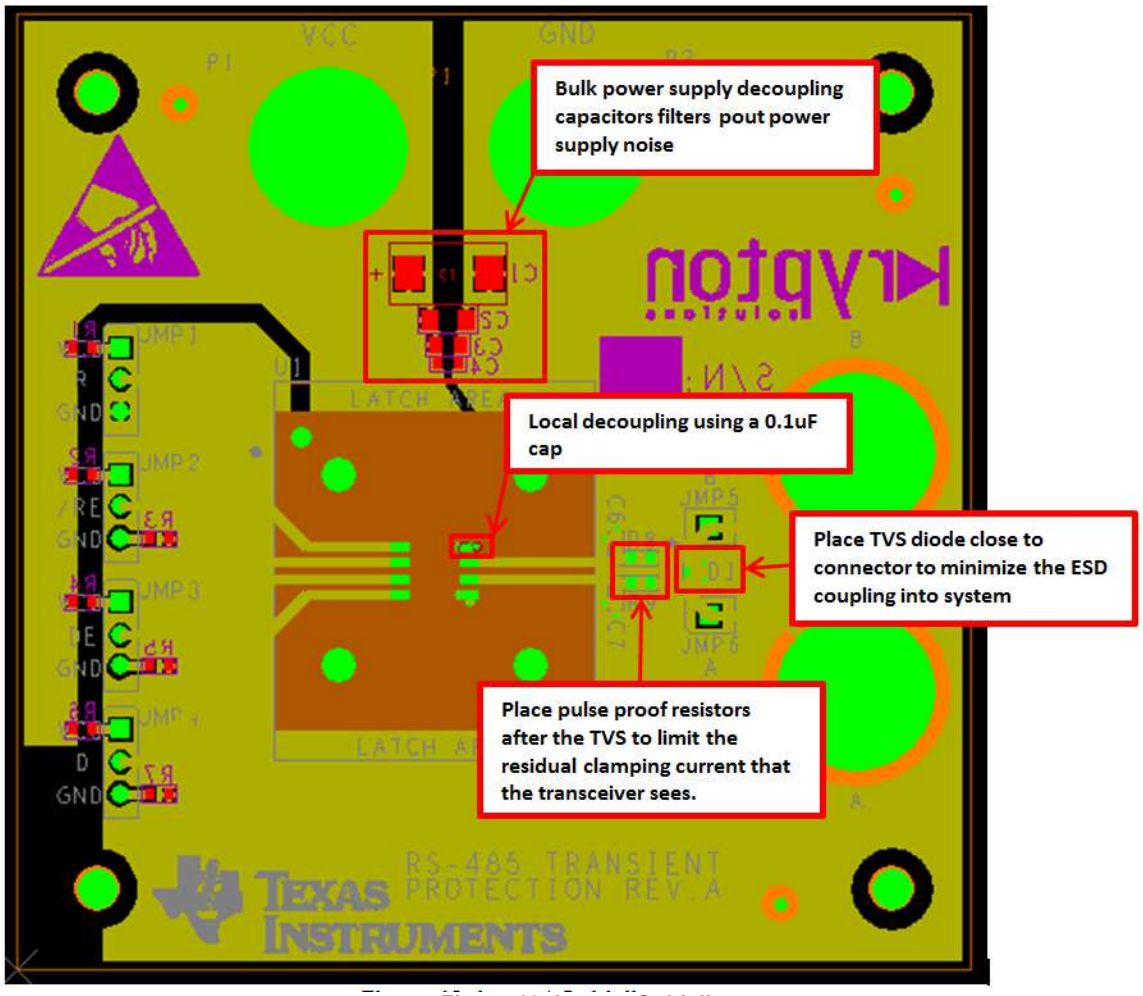

Figure 19: Layout Guidelines

9.5 Gerber files

To download the Gerber files for each board, see the design files at http://www.ti.com/tool/tidu00730

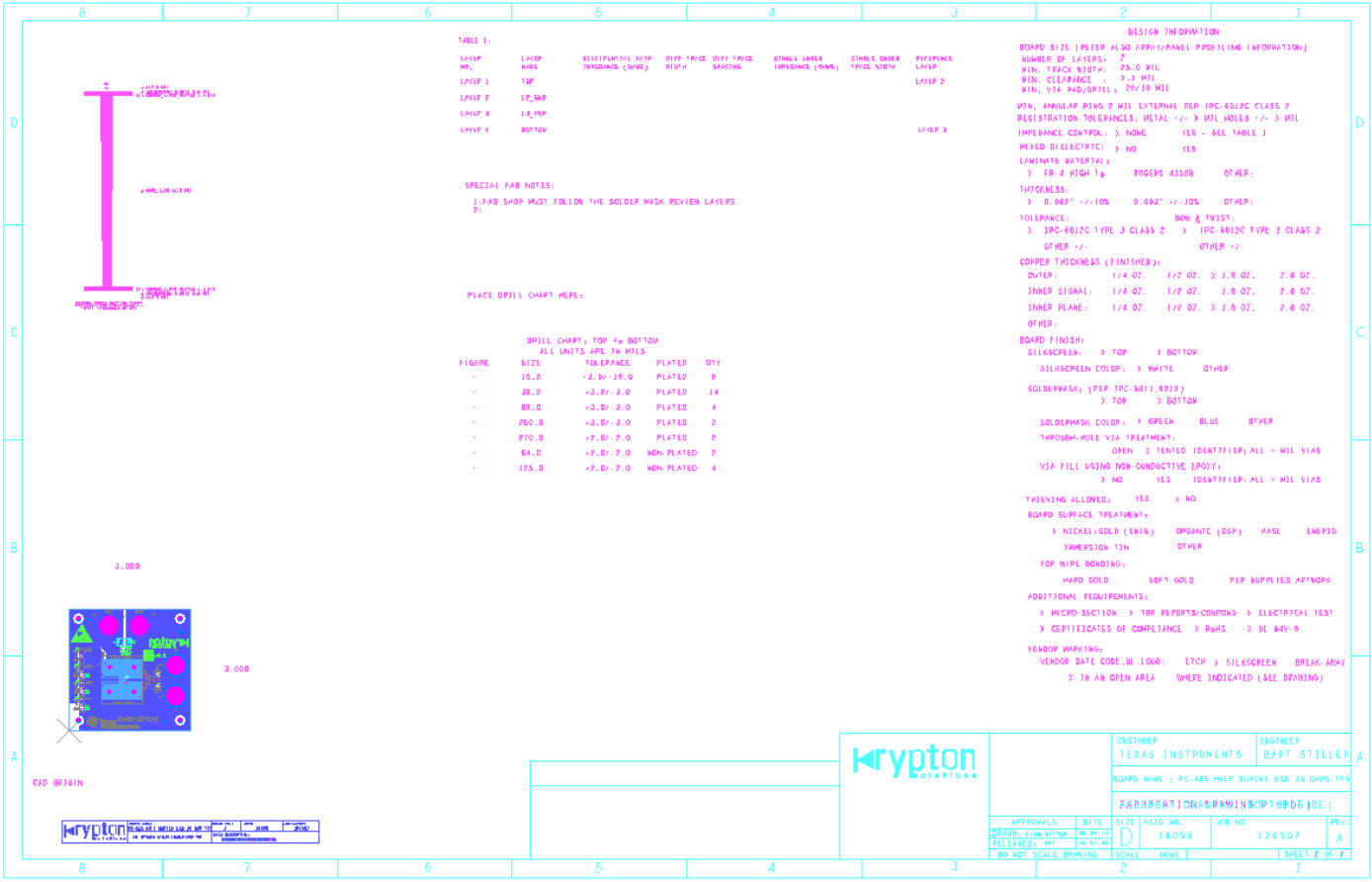

Figure 20: Gerber File

9.6 Assembly Drawings

To download the Assembly Drawings for each board, see the design files at http://www.ti.com/tool/tidu00730

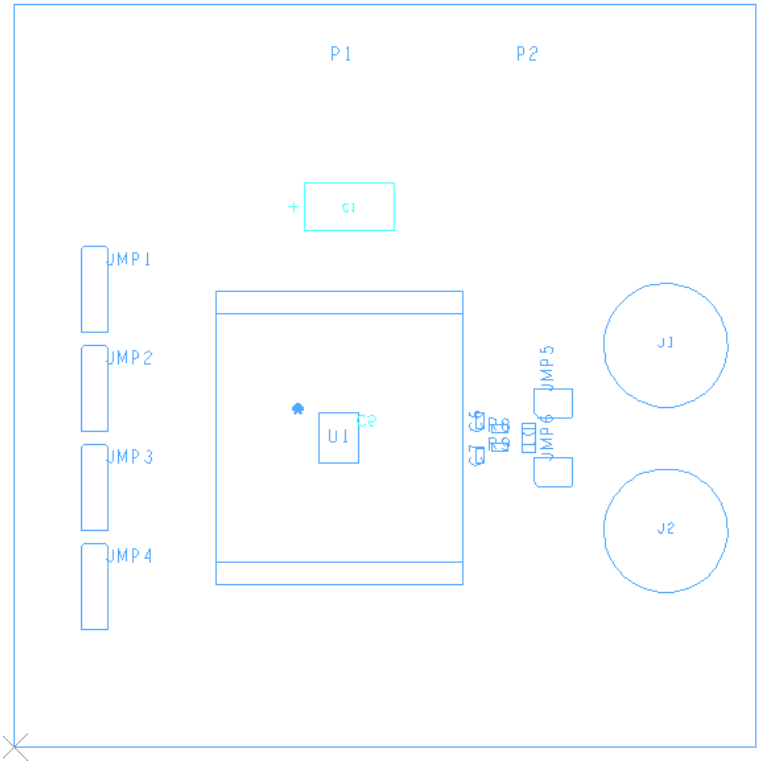

Figure 21: Assembly Drawing

10 References

1. Texas Instruments Application Report, Protecting RS-485 Interfaces Against Lethal Electrical Transients, SLLA292A, 2009

11 About the Author

Michael Peffers is an applications engineer at Texas Instruments supporting the RS-485, LVDS, PECL, CAN, LIN, IO-Link, and Profibus interface products. Michael is responsible for developing reference designs solutions for the industrial segment and direct customer support including onsite support as well as onsite training. Michael is also responsible for producing technical content such as application notes, datasheets, white papers, and is the author of a recurring blog on the Texas Instruments E2E forum called Analog Wire: Get Connected. Michael brings to this role his experience in high-speed SERDES applications as well as experience in the optical transceiver space. Michael earned his Bachelors of Science in Electrical Engineering (BSEE) from the University of Central Florida (UCF).

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