Kevin Duke, Neeraj Gill

TI Designs – Precision: Verified Design

Voltage Mode Multiplying DAC Reference Design

TI Designs – Precision

TI Designs – Precision are analog solutions created by TI's analog experts. Verified Designs offer the theory, component selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

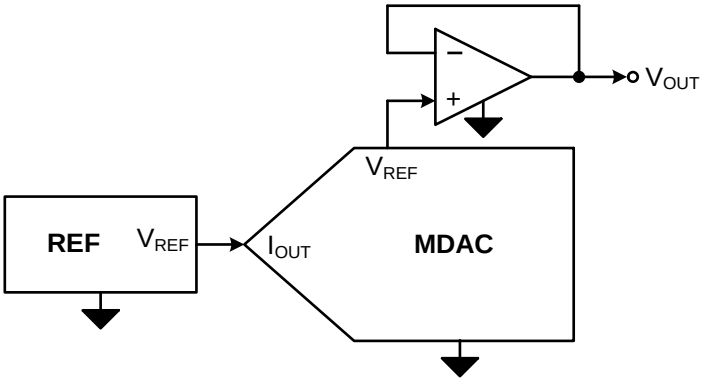
TIPD159	All Design files
TINA-TI™	SPICE Simulator
DAC7811	Product Folder
OPA192	Product Folder
REF5025	Product Folder

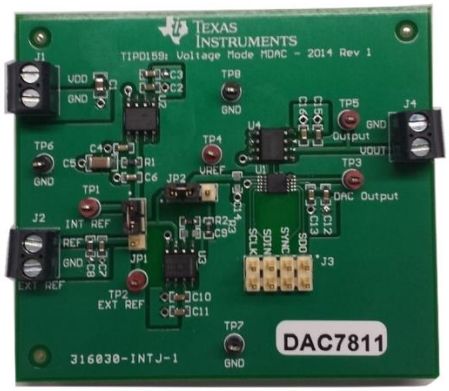
Circuit Description

This multiplying DAC (MDAC) circuit creates a unipolar voltage output from 0 V to 2.5 V. This design does not require dual supplies to realize a unipolar, positive output voltage as with typical MDAC circuits. This design removes the need for a negative rail by using the MDAC in "reverse" to form a binary weighted voltage divider.

TI E2E™ Community

Ask The Analog Experts
WEBENCH® Design Center
TI Designs – Precision Library





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

TINA-TI is a trademark of Texas Instruments
WEBENCH is a registered trademark of Texas Instruments

1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5.5 V
- Input: 3-wire, 16-bit SPI
- Output: 0 – 2.5 V

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Calculated, and Measured Performance

	Goal	Calculated	Measured
Total Unadjusted Error (%FSR)	0.1	0.07481	0.05351

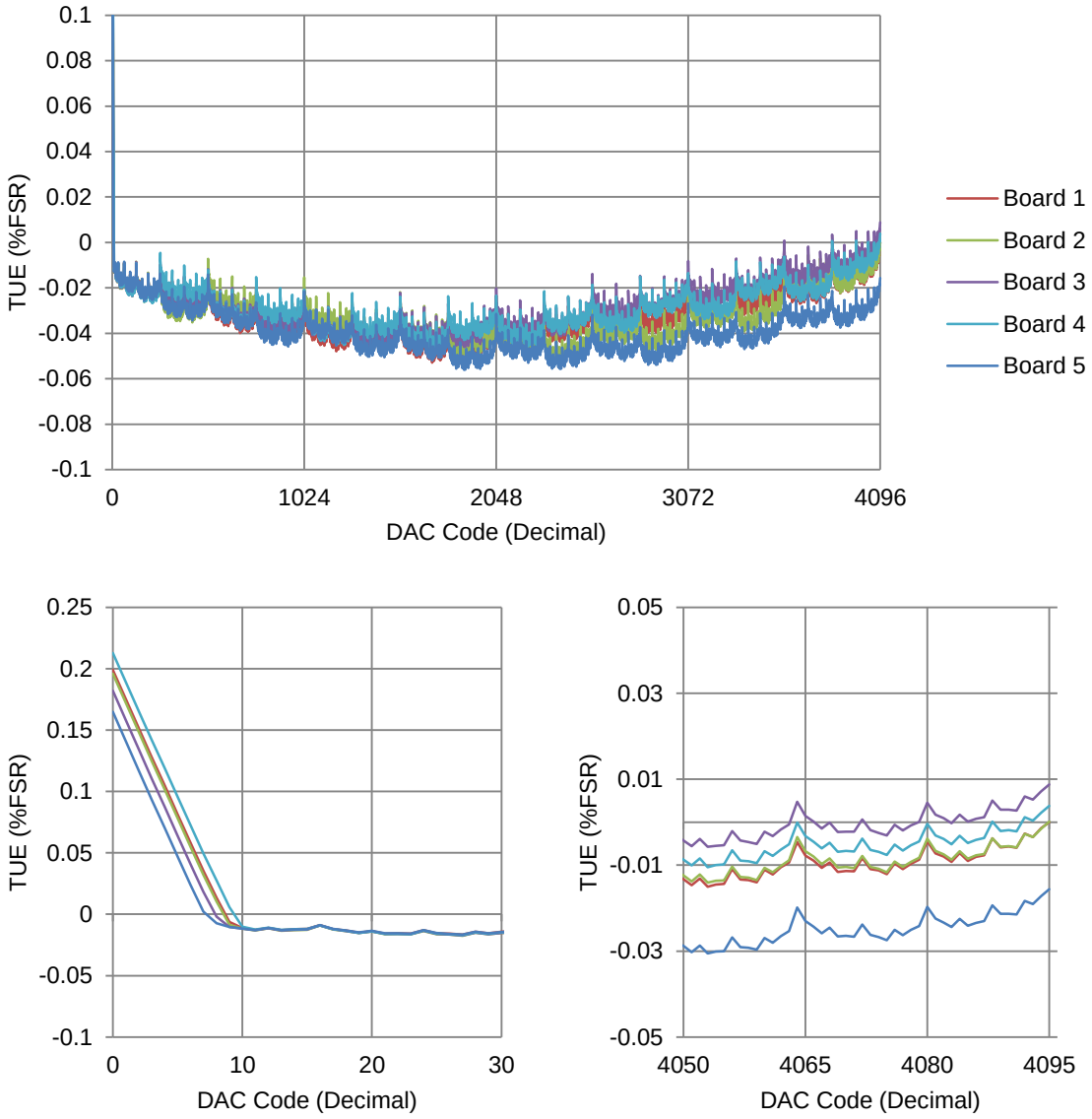


Figure 1: Measured Transfer Function Total Unadjusted Error

2 Theory of Operation

A multiplying DAC (MDAC) is a current output digital-to-analog converter. Typically the output current is converted into a voltage by including an op-amp in a transimpedance configuration at the MDAC current output terminal. The transimpedance stage creates an output voltage with opposite polarity to that of V_{REF} and subsequently the design requires dual supplies, as is discussed in TIPD137. This circuit removes the need of dual power supplies and uses a single supply to power the circuit.

A more detailed schematic for this design, including an optional buffer stage for designs that require optimized settling time, is shown in Figure 2.

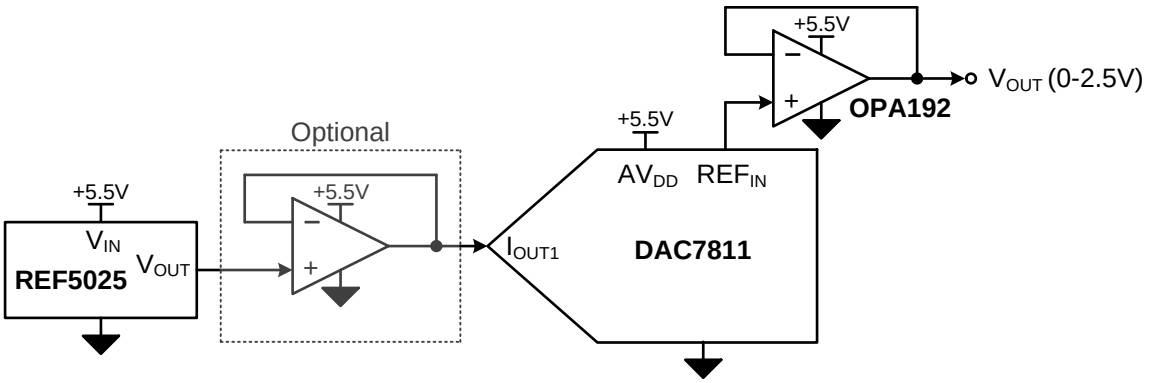


Figure 2: Detailed Circuit Schematic

The transfer function from digital code to output voltage is shown in Equation (1).

$$V_{OUT}(Code) = \frac{V_{REF}}{2^{bits}} * Code \quad (1)$$

2.1 Typical MDAC Configuration

A simplified illustration of the MDAC R-2R ladder architecture is shown in Figure 3. Each 2R leg of the ladder can either be connected to the I_{OUT1} or I_{OUT2} terminal. In normal operation the I_{OUT2} terminal of the MDAC is connected to the non-inverting input terminal of an op amp and ground, while the I_{OUT1} terminal is connected to the inverting input terminal and R_{FB}, as shown in Figure 3. Current flow out of I_{OUT1} develops a voltage across R_{FB}. Through negative feedback the op amp creates a voltage of equal magnitude but opposite polarity to the voltage across R_{FB} at its output to drive the inverting terminal to the non-inverting input tied to ground. In this configuration the R-2R ladder behaves as a binary weighted current divider, allowing the digital input codes to control the current flow into the transimpedance stage. Refer to TIPD137 for more details.

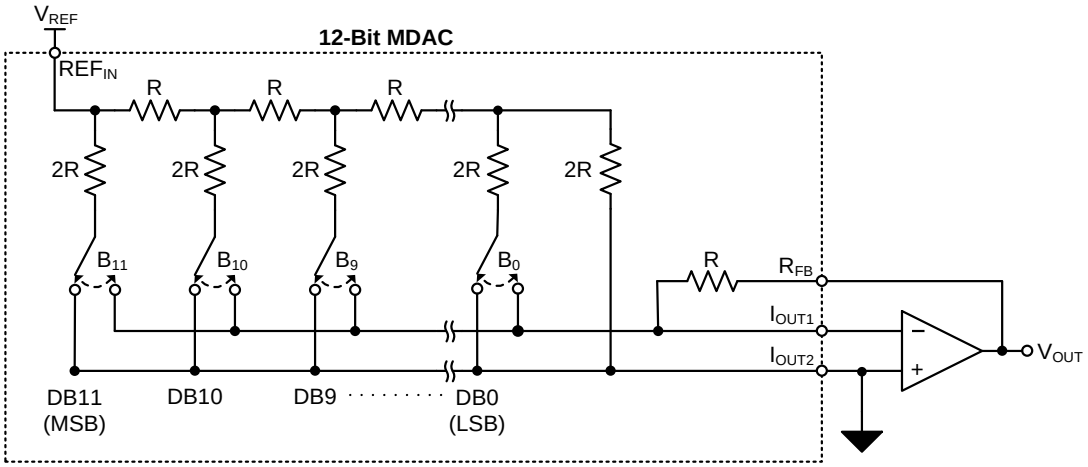


Figure 3: Typical MDAC Application

2.2 Modifications for Single-Supply Operation

In this design the reference voltage is applied at the I_{OUT1} pin and the output voltage is taken from the REF_{IN} pin. In this configuration the R-2R ladder behaves as a binary weighted voltage divider, instead of a current divider, and the high impedance input of the amplifier input keeps the divider isolated from the load.

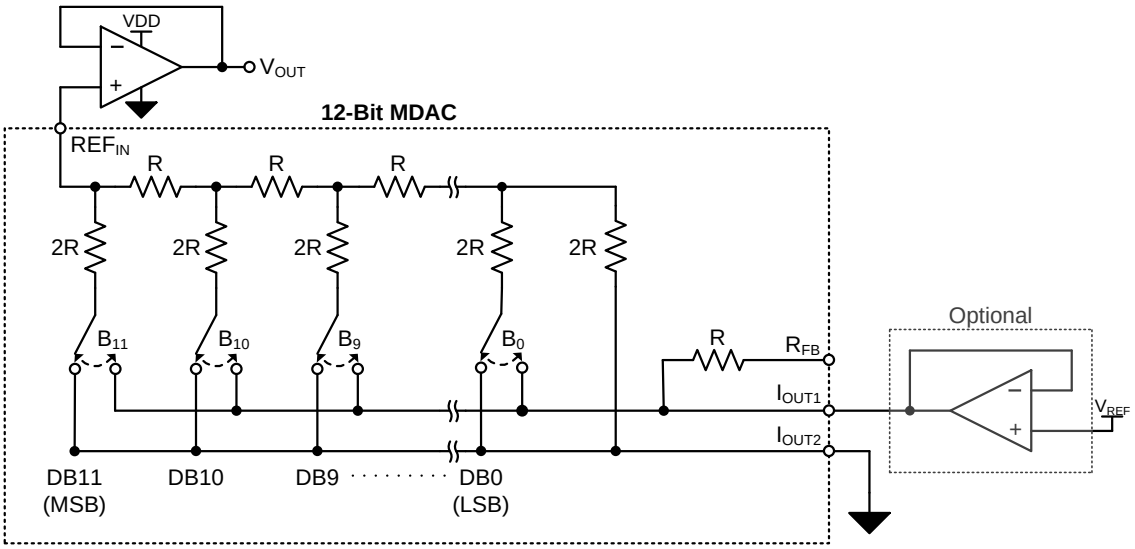


Figure 4: MDAC with offset voltage

2.3 Circuit Requirements & Limitations

N-channel MOSFETs are used in the R-2R DAC ladder to construct the switches. Figure 5 shows a simplified diagram of the circuit used to create one of these switches, with the switch connected to I_{OUT2} and each node connected to the voltages used in this design.

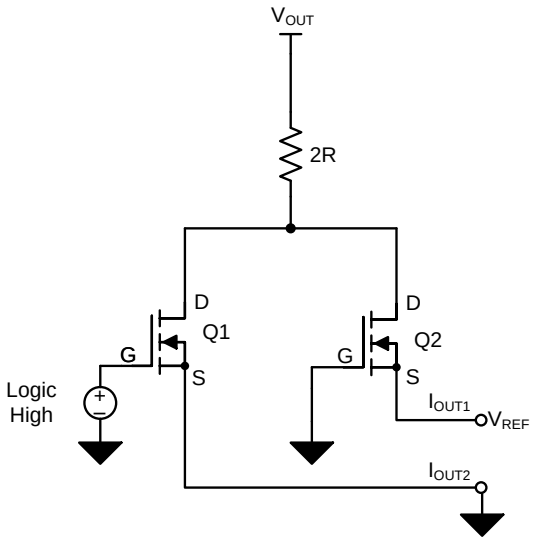


Figure 5: MOSFET Switch

There are three limitations that should be kept in mind when choosing to implement this design: that the digital block of the DAC can still control the DAC switches, minimizing error contributions to DAC linearity caused by R_{ON} mismatches in the switch MOSFETs, and choosing devices that use a trim structure does not create additional error sources.

In order for the digital block of the DAC to control the DAC switches, the gate-source voltage, V_{GS}, must be greater than the threshold voltage, V_{TH}, of the switch MOSFETs. The logic high voltage applied by the digital block of the DAC to the gate of the MOSFETs in the switches should be approximately 2.0 V higher than the bias voltage applied at the source in order to ensure control of the switches over all operating corners for a typical MDAC. In the I_{OUT2} case the MOSFET source is connected to ground, meanwhile the I_{OUT1} MOSFET source is connected to V_{REF}. Therefore, the digital supply voltage should be greater than or equal to V_{REF} + 2 V.

In order to also reduce additional errors to the DAC linearity, the V_{GS} voltage will need to be higher than 2.0 V. Mismatched impedances in the “2R” legs of the R-2R ladder create linearity errors at the DAC output. The 2R resistors are often trimmed to match one another and ideally the MOSFETs in each of the DAC switches is exposed to the same biasing scheme and therefore exhibit matched R_{ON}. In this design one MOSFET in each switch will always be biased differently than the other and therefore the design will inherently display worse linearity than a typical MDAC design. In order to enhance R_{ON} matching, it is helpful to exceed the minimum V_{GS} voltage, 2.0 V, for the MOSFETs in the switches.

This design uses 5.5 V for the analog supply voltage to meet the first condition and minimize the impact of R_{ON} mismatching without approaching the absolute maximum supply rating for the device.

Internal knowledge of the trim architecture of the device is required to understand if the trim scheme will impact the accuracy of this design. For inquiries about applying this design to other devices, please create a post at e2e.ti.com in the precision data converters forum.

3 Component Selection

3.1 MDAC Selection

MDAC selection for this design is based on dc accuracy goals while understanding that there will be additional linearity error created as a result of using the device in this particular configuration. The linearity of higher resolution devices will be impacted more than lower resolution devices due to their dependency on stronger matching in the R-2R ladder. This approach could be applied to any MDAC, though dc accuracy may suffer more or less with other devices.

The DAC7811 was chosen for this design because it is a low resolution device whose linearity will suffer minimal degradation and the internal trim scheme will not create additional error sources when used in this configuration.

3.2 Amplifier Selection

Only one amplifier is required in this design to buffer the voltage output of the MDAC ladder from the load. An additional optional amplifier may be included to buffer the reference voltage input to the DAC ladder. When using the MDAC in the configuration described in this document, the reference voltage input will be exposed to a load transient on code transitions. In order to minimize the impact of this load transient on settling time it is beneficial to include an operational amplifier and/or a “charge well” capacitor to provide this instantaneous current and maintain the output settling time.

For the output amplifier, low input offset voltage as well as input/output swing to the negative rail are the most important parameters for delivering strong dc accuracy. Output voltage swing to the positive rail is not as imperative for this design because the positive supply will have plenty of head-room over the maximum input and output voltage.

Similar dc concerns are applicable to the reference buffer though input/output swing to the negative rail is not as important since the reference input voltage will have enough foot-room over the negative rail.

The OPA192 was chosen as the output amplifier in this design because it delivers low input offset voltage and good input/output swing to rail capability.

3.3 Reference

Reference initial accuracy in this design contributes to both offset and gain errors for the system output and is an important parameter for device selection. The REF5025 2.5 V reference was chosen for this design which delivers strong initial accuracy at 0.05%.

4 Calculations

According to the datasheet, the DAC7811 has an integral non-linearity (INL) of 1 LSB at 12 bits of resolution. The INL error is converted to % FSR by using Equation (2).

$$INL_{DAC}(\%FSR) = \frac{INL(LSB)}{2^{DAC\_RESOLUTION}} * 100 \quad (2)$$

$$INL_{DAC}(\%FSR) = \frac{1LSB}{2^{12}} * 100 = 0.024414\% \quad (3)$$

The gain error for the DAC7811 is also obtained from the datasheet. The gain error is specified as full-scale gain error of ±5 mV with 10 V reference voltage. The gain error is converted to % FSR by using Equation (4).

$$GainError_{DAC}(\%FSR) = \frac{GainError}{FullScaleRange} * 100\% \quad (4)$$

$$GainError_{DAC}(\%FSR) = \frac{5mV}{10V} * 100\% = 0.05\% \quad (5)$$

The DAC7811 does not include an input or output amplifier and therefore does not exhibit any offset error. The only contributor for offset error in this design is the input offset voltage of the output amplifier, the OPA192. The OPA192 datasheet specifies input offset voltage of 5 µV. This offset error is converted into % FSR using Equation

$$OffsetError_{OPA}(\%FSR) = \frac{V_{OS}}{FullScaleRange} * 100\% \quad (6)$$

$$OffsetError_{OPA}(\%FSR) = \frac{5\mu V}{2.5V} * 100\% = 0.0002\% \quad (7)$$

The total unadjusted error (TUE) is obtained by computing the root sum square (RSS) of the error terms as shown in Equation

$$TUE = \sqrt{INL_{DAC}{}^2 + GainError_{DAC}{}^2 + OffsetError_{OPA}{}^2} \quad (8)$$

$$TUE = \sqrt{0.024414^2 + 0.05^2 + 0.0002^2} = 0.0555584\% \quad (9)$$

All of the calculations done above are computed by using an ideal reference of 2.5 V. To better understand the overall system performance the errors computed above are represented with four parameters: INL error, gain error, offset error, and TUE. Table 2 summarizes the performance with an ideal reference.

Table 2: System performance with ideal reference

Parameter	Calculated Value
V_{REF}	2.5 V
INL Error	0.02441%
Gain Error	0.05000%
Offset Error	0.00020%
TUE	0.05556%

The datasheet of the REF5025 indicates that it has initial accuracy of 0.05% at 25ºC. Table 3 shows another set of calculated results that include the effects of reference accuracy.

Table 3: System performance with REF5025 reference

Parameter	Calculated Value
V_{REF}	2.5 V ±0.05%
INL Error	0.02441%
Gain Error	0.07071%
Offset Error	0.00020%
TUE	0.07481%

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

For optimal performance of this design follow standard PCB layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. For high speed applications or applications that value fast settling time, the PCB design includes an optional footprint and jumper options to include a reference buffer amplifier.

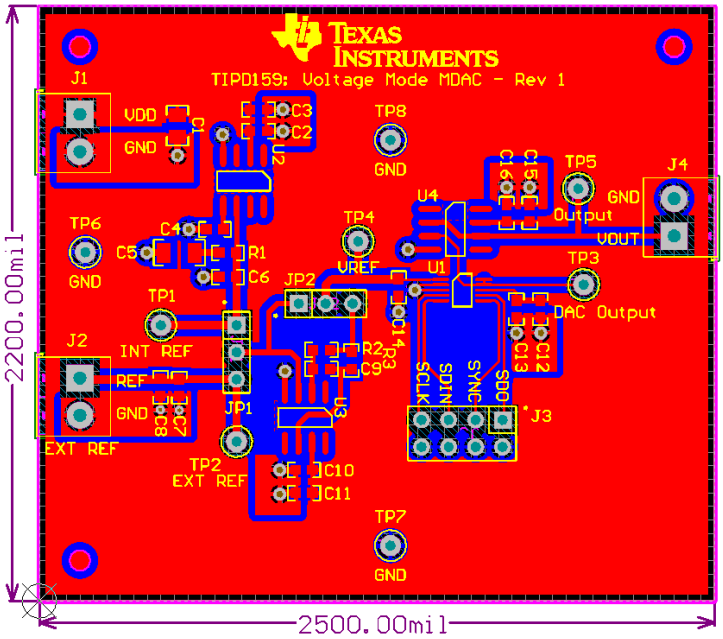


Figure 6: PCB Layout Top Layer

6 Verification & Measured Performance

6.1 Transfer Function

DC transfer function data for the system voltage output was collected using an 8 ½ digit digital multi-meter while driving the input terminals (high-impedance) of the DMM directly. The measured results, including performance at positive and negative full-scale end points, are shown in Figure 7.

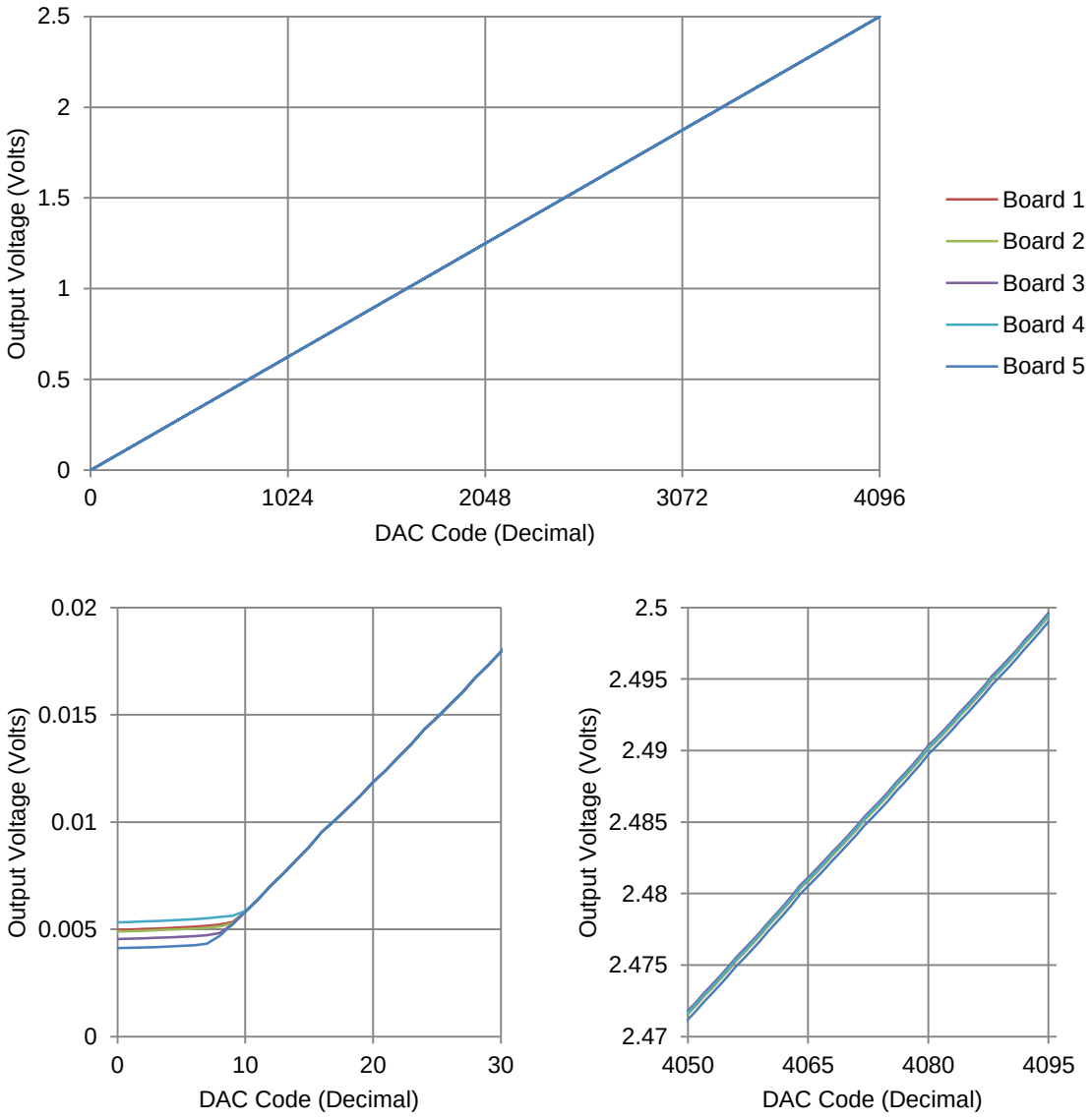


Figure 7: Output Voltage vs. Input Code

The calculated total unadjusted output voltage error in % FSR is shown in Figure 8. The worst-case measured results show TUE of less than 0.6% FSR. Table 4 compares accuracy goals, calculated accuracy, and measured accuracy.

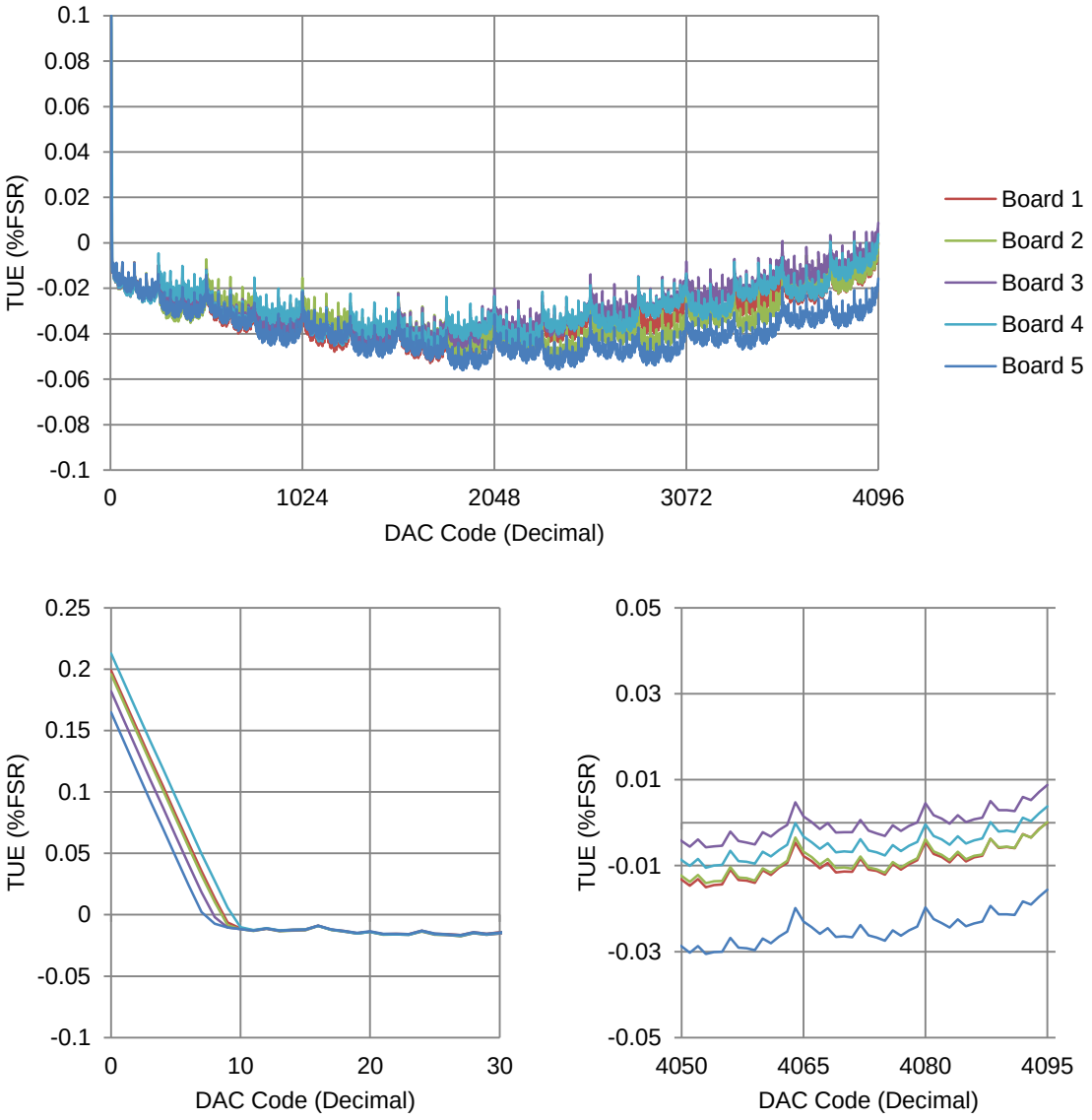


Figure 8: Output Voltage TUE vs. Input Code

Table 4. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Calculated	Measured
Total Unadjusted Error (%FSR)	0.1	0.07481	0.05351

As discussed in section 2.3 of this document, using the MDAC in this configuration causes the internal MOSFET switches to be biased in conditions that are non-ideal for maintaining integral non-linearity (INL) and differential non-linearity (DNL) performance of the MDAC. Figure 9 shows the measured INL and DNL data for this design. The DNL performance maintains monotonic performance with no missing codes, however the INL performance has decayed, as expected, to ~1.5 LSBs compared to the 1 LSB specification in the DAC7811 datasheet.

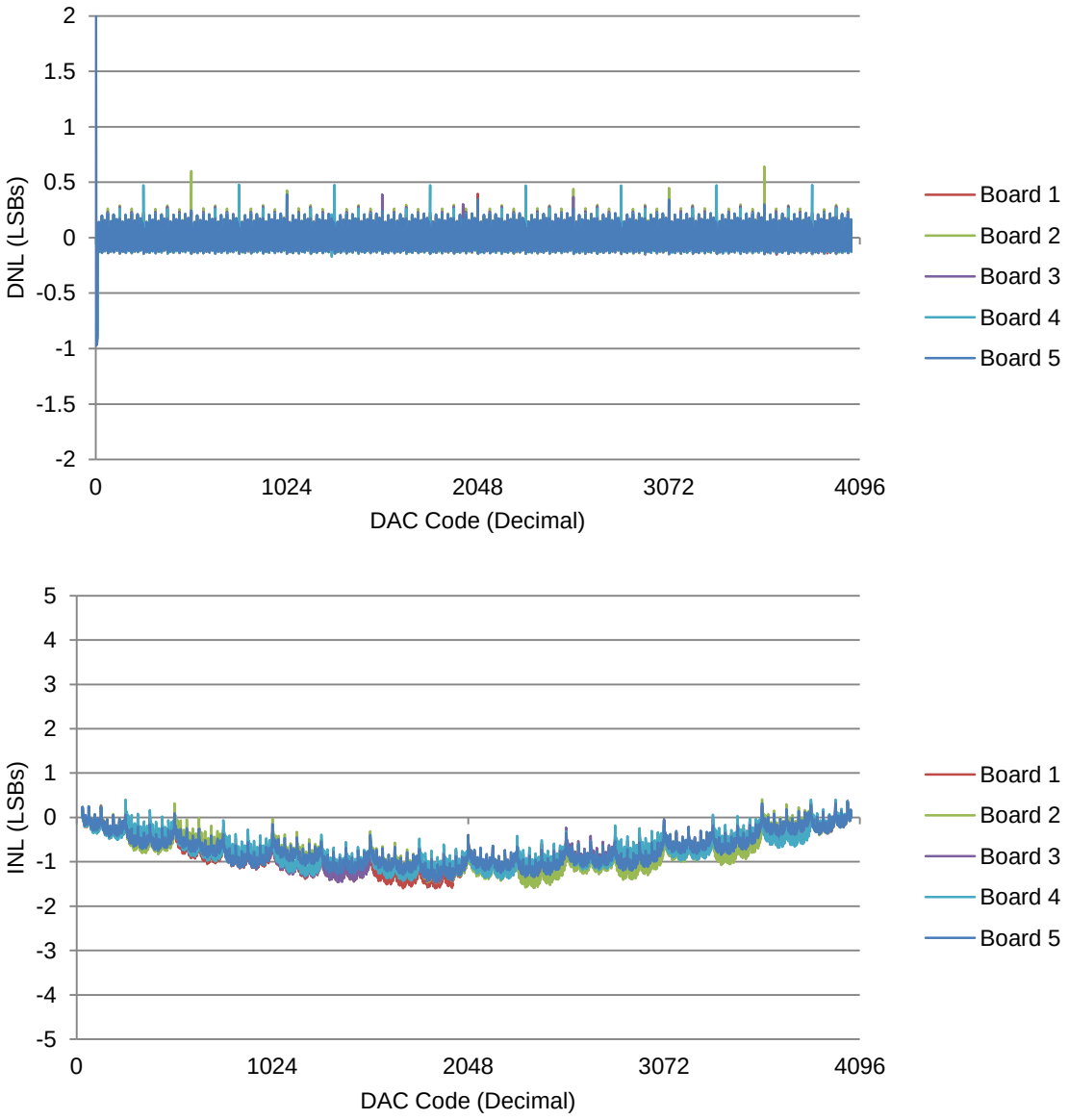


Figure 9: DNL & INL vs. Input Code

7 Modifications

Any MDAC could be used in the configuration discussed in this document. For some devices, however, proprietary internal architectures that are not discussed in the datasheet may contribute additional errors of various magnitude when using the MDAC in this configuration. Before implementing an MDAC in this configuration, please consult the precision data converters forum at e2e.ti.com.

8 About the Author

Kevin Duke is a Systems Engineer in the precision digital to analog converters group at Texas Instruments where he supports industrial automation products and applications. Kevin received his BSEE from Texas Tech University in 2010.

Neeraj Gill was an analog applications rotation engineer at Texas Instruments. He received his BSEE from the University of New Hampshire in 2011 and his Masters in Electrical Engineering, also from the University of New Hampshire, in 2013.

Appendix A.

A.1 Electrical Schematic

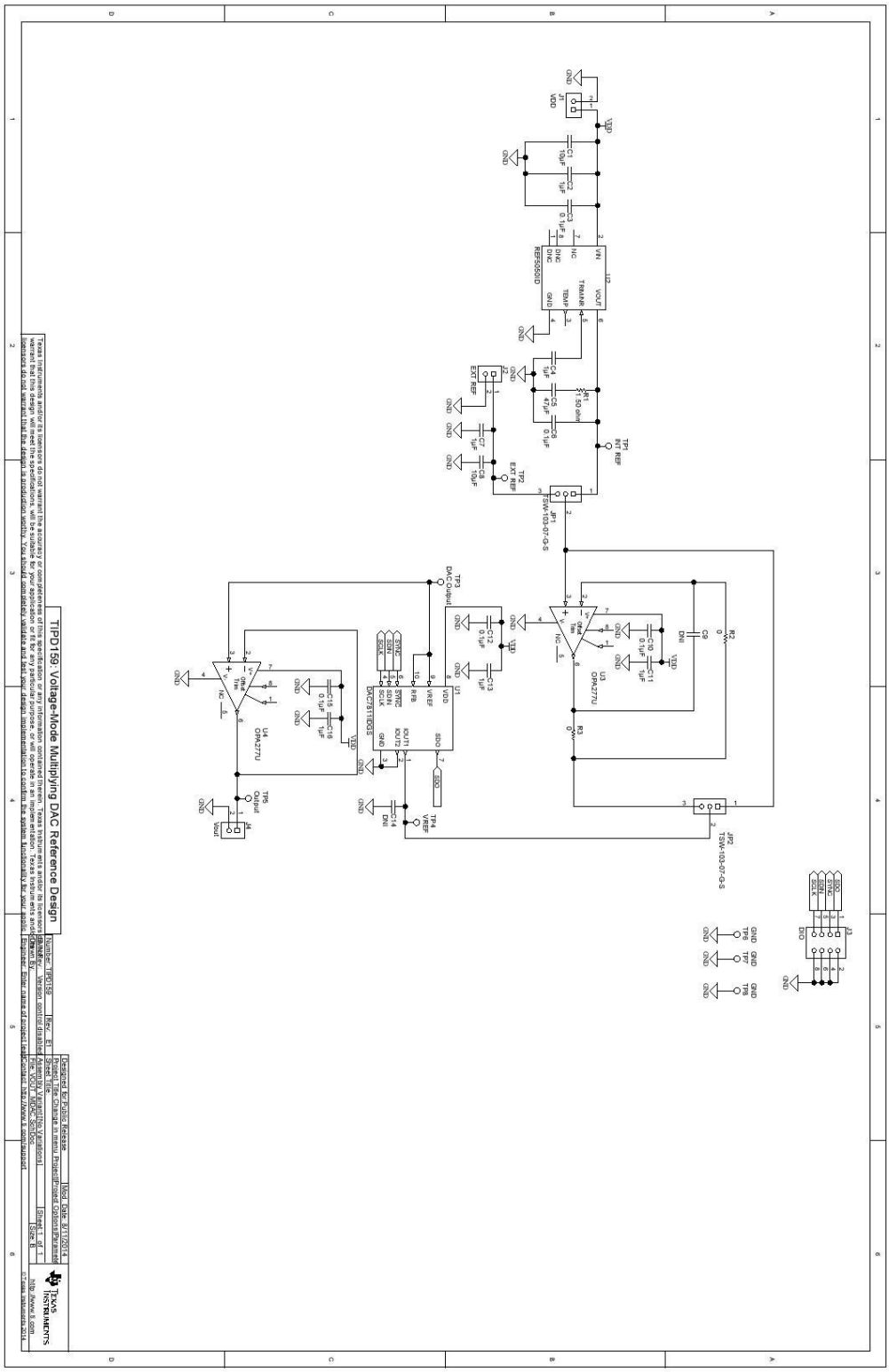


Figure A-1: Electrical Schematic

A.2 Bill of Materials

Texas Instruments

Bill of Materials

TI DESIGNS

TIPD159: Voltage-Mode Multiplying DAC Reference Design

Item #	Quantity	Value	Designator	Description	Manufacturer	Part Number
1	1	10uF	C1	CAP, CERM, 10uF, 25V, +/-10%, X5R, 0805	TDK	C2012X5R1E106K125AB
2	6	1uF	C2, C4, C7, C11, C13, C16	CAP, CERM, 1 µF, 25 V, +/- 10%, X5R, 0603	MuRata	GRM188R61E105KA12D
3	5	0.1uF	C3, C6, C10, C12, C15	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X5R, 0603	MuRata	GRM188R61E104KA01D
4	1	47uF	C5	CAP, CERM, 47uF, 25V, +/-20%, X5R, 1206	TDK	C3216X5R1E476M160AC
5	1	10uF	C8	CAP, CERM, 10 µF, 25 V, +/- 20%, X5R, 0603	TDK	C1608X5R1E106M080AC
6	2		C9, C14	Not Installed		
7	3		J1, J2, J4	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
8	1		J3	Header, TH, 100mil, 4x2, Gold plated, 230 mil above insulator	Samtec	TSW-104-07-G-D
9	2		JP1, JP2	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S
10	1	1.50 ohm	R1	RES, 1.50 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031R50FKEA
11	2	0	R2, R3	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA
12	5		TP1, TP2, TP3, TP4, TP5	Test Point, Miniature, Red, TH	Keystone	5000
13	3		TP6, TP7, TP8	Test Point, Miniature, Black, TH	Keystone	5001
14	1		U1	12-Bit, Serial Input, Multiplying Digital-to-Analog Converter, DGS0010A	Texas Instruments	DAC7811IDGS
15	1		U2	Low-Noise, Very Low Drift, Precision Voltage Reference, D0008A	Texas Instruments	REF5050ID
16	2		U3, U4	High Precision OPERATIONAL AMPLIFIER, D0008A	Texas Instruments	OPA277U

Figure A-2: Bill of Materials

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265