TI Designs

Generating the AVS SmartReflex Core Voltage for the K2E Using the TPS544C25 and the LM10011

Design Overview

The K2E requires the use of AVS SmartReflex control for the CVDD core voltage. This design provides a method of generating the proper voltage without needing software. The circuit is currently implemented on the XEVMK2EX.

Design Resources

K2EVM	K2 EVM Information
66ak2e05	Product Folder
66ak2e02	Product Folder
am5k2e04	Product Folder
am5k2e02	Product Folder
TPS544C25	Product Folder
LM10011	Product Folder

Circuit Description

The 66AK2Ex and AM5K2E0x SOCs requires automatic voltage scaling (AVS) for the core voltage. The SmartReflex controller in the SOC uses the VCNTL interface to direct the voltage needed by the device to the power supply. The LM10011 generates a control current to the TPS544C25, adjusting the voltage generated by that device.

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1 Design Summary

The 66AK2E0x and AM5K2E0x SOCs use SmartReflex technology to decrease both static and dynamic power consumption while maintaining the performance of the device. To achieve this, the SmartReflex controller adjusts the core voltage to an optimized level based on the process corner of the device. This requires a separate core power supply for each SOC configured by the SmartReflex controller circuit. This design uses the LM10011 to communicate with the SOC, using the VCNTL interface and the TPS54C25 to generate the core voltage CVDD.

1.1 Introduction to the LM10011 and the TPS544C25

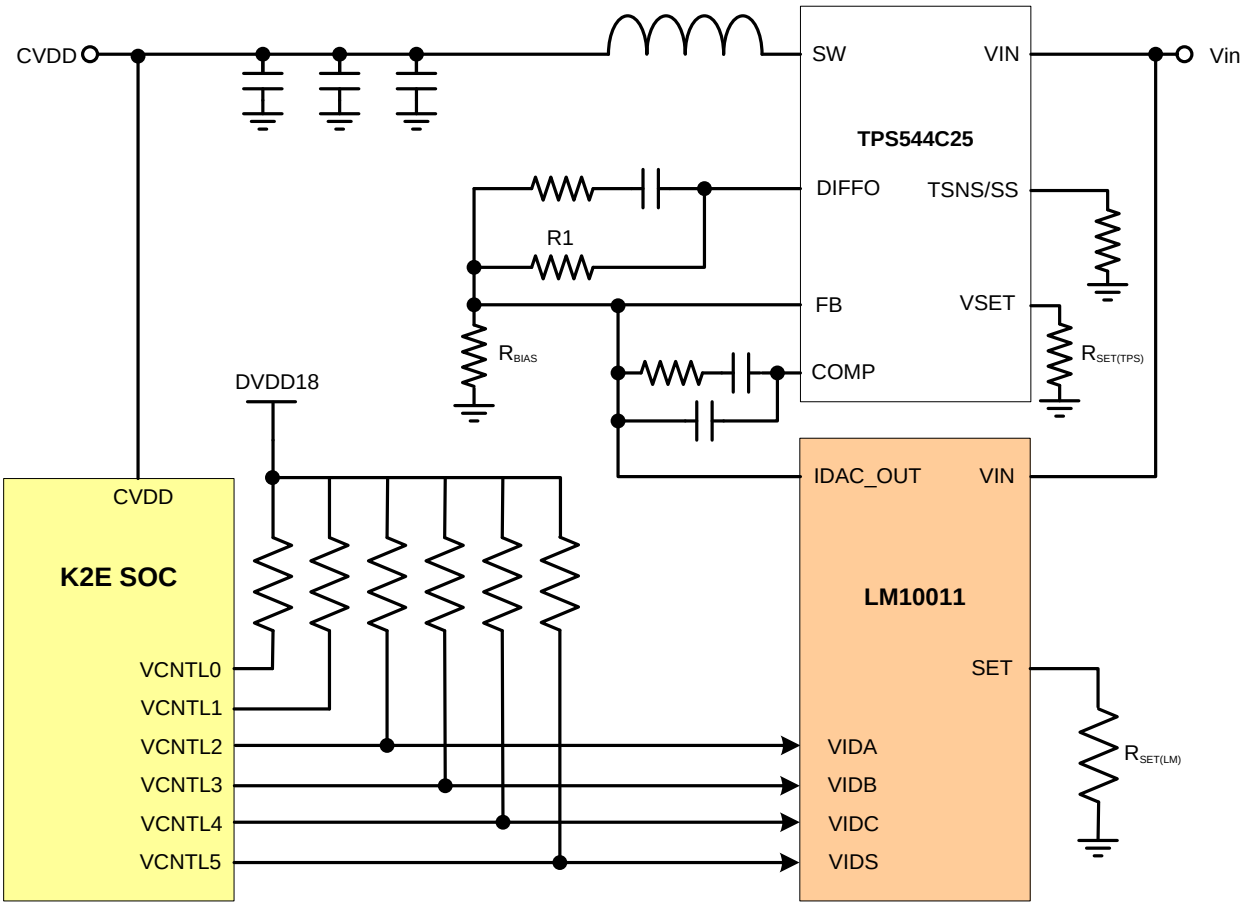


Figure 1. CVDD Power Circuit Using the LM10011 and the TPS544C25

The TPS544C25 is a synchronous buck converter with integrated FETs capable of a 30-A current output. Two methods are available for dynamically setting the output voltage of the TPS544C25. The first is the use of the PMBus interface, which will be discussed in a separate design. The second is the use of the feedback pin FB. Normally a set of resistors including R1, R_{BIAS}, and $R_{SET\ (RSET(TPS))}$ in Figure 1) configure the output voltage for the TPS544C25.

In this design, the LM10011 is also connected to the FB pin. The LM10011 provides a connection to the VCNTL interface of the K2E, which allows the SOC to select a precision DC current output on the IDAC_OUT pin. This current is used to adjust the output voltage of the TPS544C25 to meet the AVS voltage level required by that particular K2E SOC.

1.2 TPS544C25 Basics

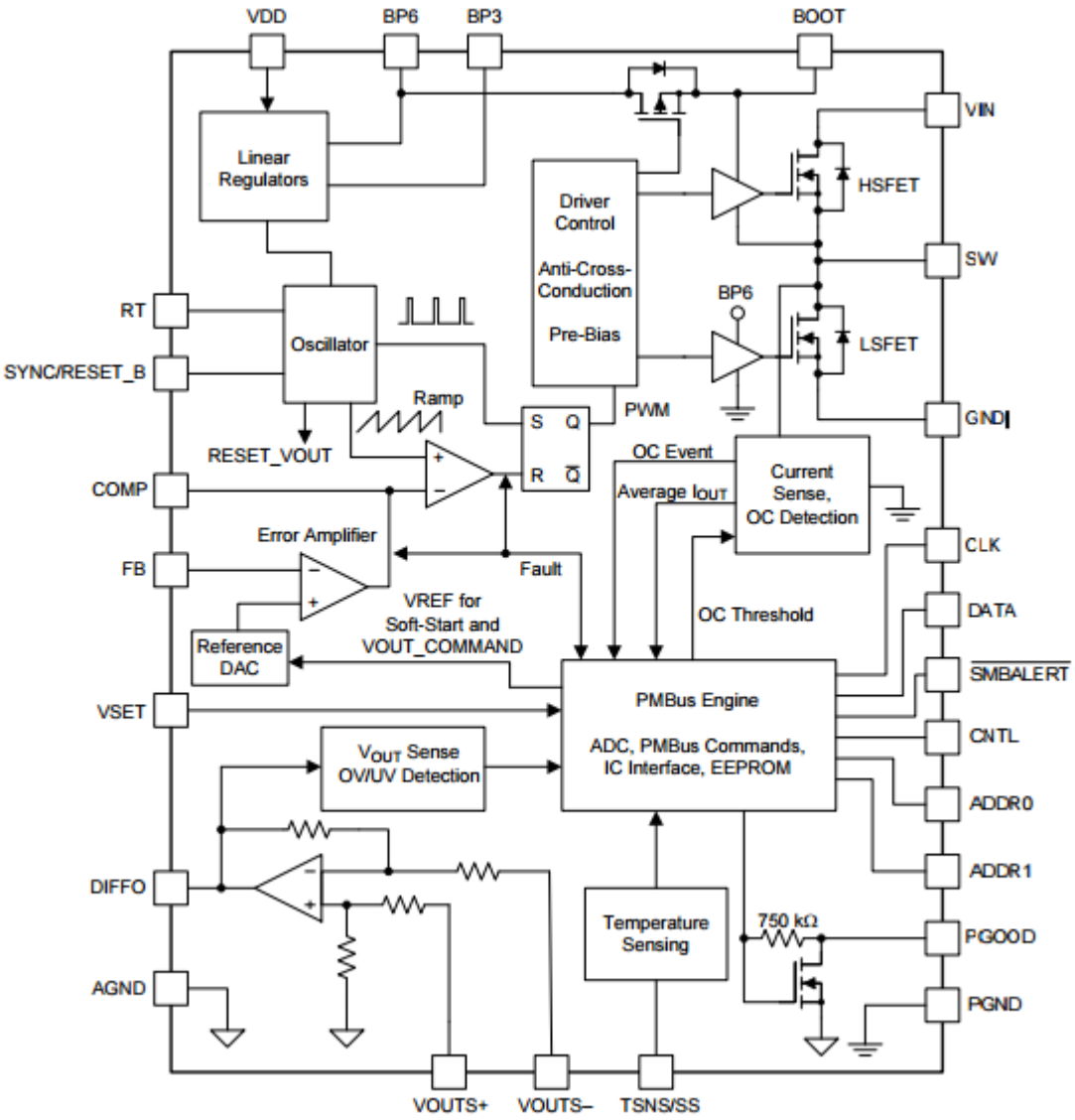


Figure 2. TPS544C25 Functional Block Diagram

For a full understanding of the operation of the TPS544C25, study the data manual (SLUSC81) and the associated design collateral. A brief discussion of the basic operation of the device is provided here as context for understanding the design. The TPS544C25 provides the DC-DC converter for the CVDD core voltage of the K2E SOC. The K2E requires the use of an AVS power supply that configures the output voltage based on the need of the SOC. The TPS544C25 is implemented on the K2E EVM to provide that capability. Two methods of setting the AVS voltage are supported by the TPS544C25. Both methods can be supported by the K2E EVM with the installation of different components. The first uses the LM10011 and the VCNTL interface to control the AVS voltage level. This is the default mode and the component values shown in the EVM schematic enable this method. This TIDesign only describes this default mode. The second method uses the PMBus interface to modify the output voltage. Changes to the components installed and software running on the SOC are required to support this method. A separate TIDesign will be released later to describe the changes needed to support PMBus operation.

To understand the interaction between the LM10011 and the TPS544C25, it is necessary to have some basic information about setting the output voltage for the part. Buck converters use an error amplifier to compare a reference voltage to feedback voltage based on Vout. Generally the reference voltage is fixed and the feedback voltage is created using a resistor divider. In Figure 2, the resistors generating the feedback voltage are called R1 and R_{bias}. The values of these resistors are selected to ensure that the voltage at the FB pin equals the reference voltage for the desired Vout.

The TPS544C25 uses a reference DAC to allow the reference voltage to be modified. By changing the reference voltage, the output voltage can be modified without replacing the resistors on the board. The reference DAC has a range of 0 V to 1.5 V. If the value of Vout is within this range, a voltage divider at the FB pin is no longer necessary and R_{bias} can be removed. The TPS544C25 uses R_{bias} to scale Vout for higher voltage ranges than are supported by the 0-V to 1.5-V range reference DAC, but this isn't necessary for this design. The current at the FB pins, I_{fb}, is no more than 75 nA. Because the FB pin is connected to Vout through R1, the voltage drop between Vout and the FB pin is less than 1 mV. The voltage at the FB pin is equal to Vout = R1*75 nA.

The output voltage is defined by the VOUT_COMMAND register and supports a 1-V swing from 0.5 V to 1.5 V using the values 256 to 768. The output voltage is set to the value of VOUT_COMMAND × 1.953 mV, and the default value of VOUT_COMMAND is 486, which produces a Vout of 0.95 V.

The initial voltage of the device is based on the default value of the VOUT_COMMAND unless an $R_{set(TPS)}$ resistor is connected to the VSET pin of the device. The table in section 7.3.6.3 of the TPS544C25 data manual (SLUSC81) provides a correlation between the resistor connected to the VSET pin and the initial VOUT voltage generated by the part. In this design a 121K resistor is used to generate a VOUT_COMMAND value for 1.10 V. This value is generated as a reference voltage to the error amplifier.

1.3 LM10011 Basics

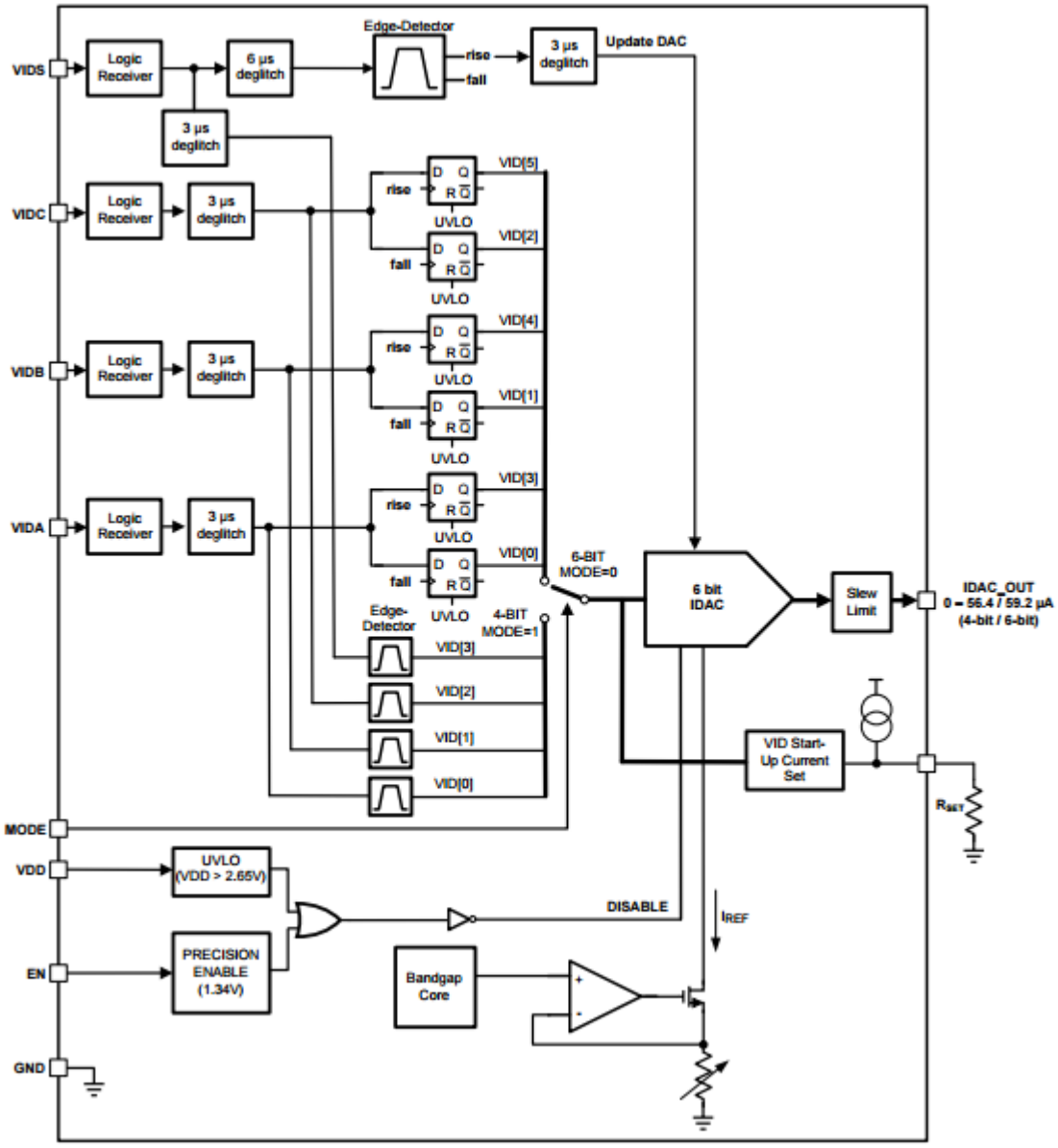


Figure 3. LM10011 Functional Block Diagram

For a full understanding of the operation of the LM10011, study the data manual (SNVS822) and the associated design collateral. A brief discussion of the basic operation of the device is provided here as context for understanding the design. The LM10011 provides a precision DC current-based on a six-bit VID value in steps of approximately 1 uA. The six-bit VID value is provided by the K2E SOC using the VCNTL interface. The IOs for the VCNTL interface are compatible with the 1.8-V open-drain output drivers used in the K2E, if pull-up resistors are included on each of the four VCNTL lines. The LM10011 also uses a $R_{set(LM)}$ resistor to set an initial current output. The TPS544C25 uses this to create an initial voltage level.

1.4 Implementation

Although the operation and implementation of the LM10011 and the TPS544C25 are described in the associated data manuals, this design uses these devices in a slightly different way. This section describes how the two devices generate the commanded voltage.

1.4.1 Output Voltage Control

The CVDD voltage range for the K2E SOC is within the 0.5-V to 1.5-V range of the V_{REF} DAC using the VOUT_SCALE_LOOP value of 1. The SmartReflex range for the K2E is 1.103 V to 0.7 V in 64 steps, with each step separated by approximately 6.396 mV. The TPS544C25 uses the VOUT_COMMAND register to modify the VREF reference voltage to the error ampifier, but this design does not have access to that register. The VREF voltage is set to the maximum voltage in the SmartReflex range, 1.103 V, and the LM10011 is used to step the voltage down. As described above, a reference voltage of 1.1 V at the error amplifier causes the TPS544C25 to generate 1.1 V at VOUT, eliminating the voltage difference at the error amplifier. The voltage at the FB pin, V_{FB}, would normally be V_{DIFFO} + V_{R1}. The power supply circuit attempts to regulate VOUT such that V_{FB} is equal to V_{REF}, or 1.1 V in this example. Because the current flow through R1 is normally in the nA range, a 10K resistor for V_{R1} results in a uV drop, and V_{OUT} would closely approximate V_{DIFFO}.

In this design, the IDAC_OUT of the LM10011 is connected to the FB pin and to one side of R1. The other side of R1 is connected to DIFFO. The current generated by the IDAC in the LM10011 flows through R1, resulting in a voltage across the resistor. The TPS544C25 reduces the output voltage equivalent to the voltage across R1, to return the voltage at the FB pin to the 1.1-V reference value. Each of the VID values generated by the K2E results in a current step, with each step separated by 0.93873 uA. To generate the proper SmartReflex voltages, the value of R1 must result in 6.369-mV steps as the current increases, thus R1 = 6.369 × 10^{-3} V/0.93873 × 10^{-6} A = 6.784 Kohms. The closest 1% value is 6.81 Kohms, resulting in steps of 6.3927 mV.

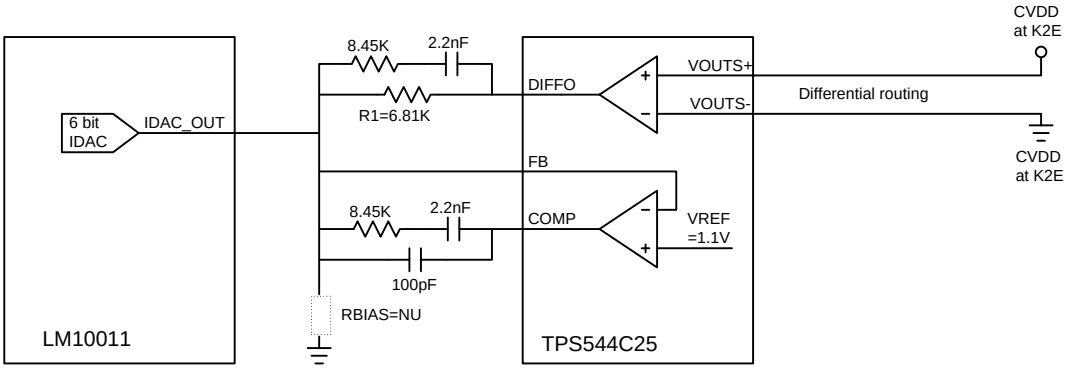


Figure 4. Output Voltage Control Diagram

1.4.2 Input Voltage

The VIN used on the K2E EVM is 12 V, based on the source voltage for AMCC-compliant platforms. The TPS544C25 supports input voltages ranging from 4.5 V to 18 V, and is more efficient with lower voltages. If an input voltage other than 12 V is desired, check with the data manual (SLUSC81) and design collateral for the TPS544C25 to choose the correct support components.

1.4.3 Initial Voltage Control

The initial voltage needed for the K2E is 1.05 V, based on the recommended operation conditions listed in the data manual. Normally, the TPS455C25 uses a resistor connected to the VSET pin to determine the initial voltage level of the part. In this design, VOUT is stepped down from the maximum, using the current generated by the LM10011. Thus, the $R_{SET(TPS)}$ resistor sets the maximum voltage, and not the initial voltage required by the K2E. Because of this, a 121-Kohm resistor is connected between the VSET pin and ground to generate the VOUT_COMMAND for 1.1 V. That 1.1-V reference voltage to the error amplifier does not change during operation.

The initial voltage for the K2E is set by the $R_{SET(LM)}$ resistor connected between the LM10011 SET pin and ground. The 215K resistor causes the LM10011 to generate 7.59 uA until a command is received from the VCNTL interface. 7.59 uA is equivalent to the VID value of 55, which generates a VOUT value of 1.052 V. This meets the initial voltage requirement for the K2E. After the RESETFULLz has been released, the K2E sends the VID value required by this particular SOC over the VCNTL interface.

1.4.4 Sense Voltage

The K2E includes two sets of pins to monitor the CVDD voltage. These pins are connected to CVDD and GND as close to the die as possible, to give the best possible representation of the voltage levels at the processing elements of the SOC. Either pair of pins can be used for the VOUTS+ and VOUTS- inputs to the TPS544C25. The traces for VOUT+ and VOUT- should be routed as a tightly coupled differential pair. The design includes 10-ohm series resistors, as well as a 100-ohm resistor to CVDD and a 100-ohm resistor to ground placed on the far side of the SOC. The 100-ohm resistors are included to insure that the sense lines cannot be floating due to an improper connection to the ball under the SOC.

2 Software Requirements

The K2E device uses SmartReflex class 0 with temperature compensation to set the optimum core voltage level for each individual device. The K2E has a SmartReflex controller, which is enabled once the device is removed from reset by releasing both the PORz and the RESETFULLz. The SmartReflex controller sends the necessary VID values to the power supply using the VCNTL interface. The advantage of this power supply design is that no application software for the K2E is required to operate the SmartReflex interface.

3 PCB Layout Considerations

As with any high-current power supply design, the PCB layout must be correct to insure the proper operation of the circuit, and to minimize the switching noise introduced to the board. The schematic for this design highlights a number of layout considerations, but does not include all of the recommendations listed in the TPS544C25 data manual (SLUSC81). Review those requirements carefully. Some of the requirements are highlighted in Figure 5.

3.1 Capacitor Placement

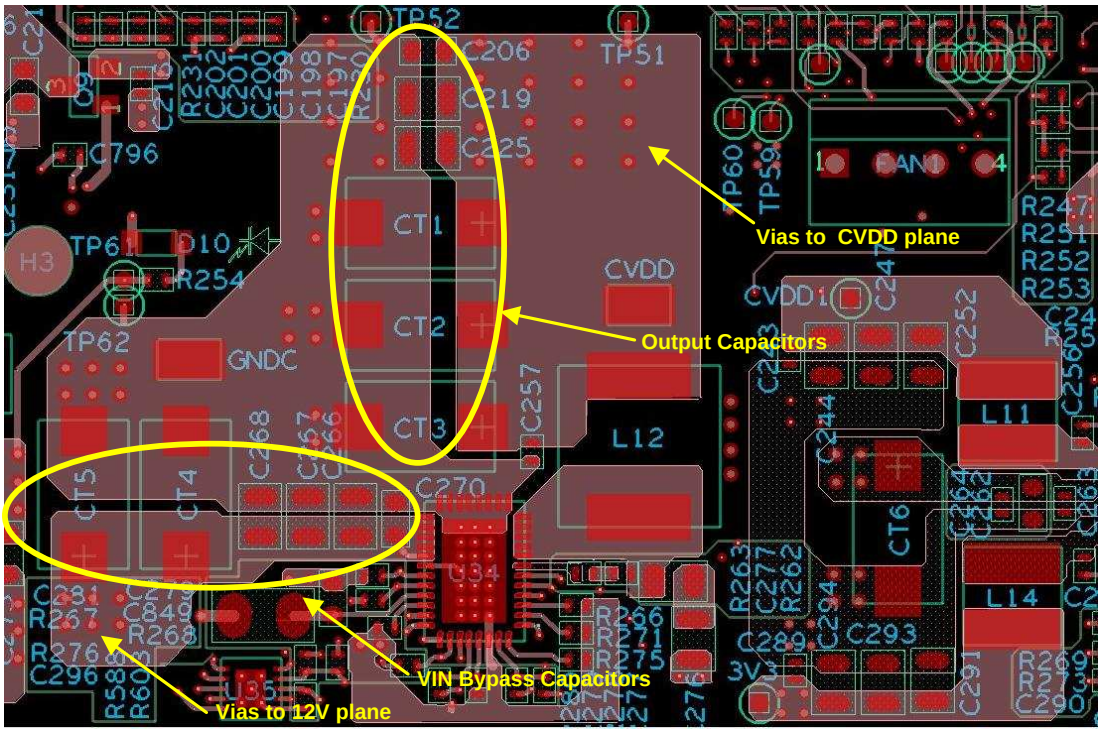
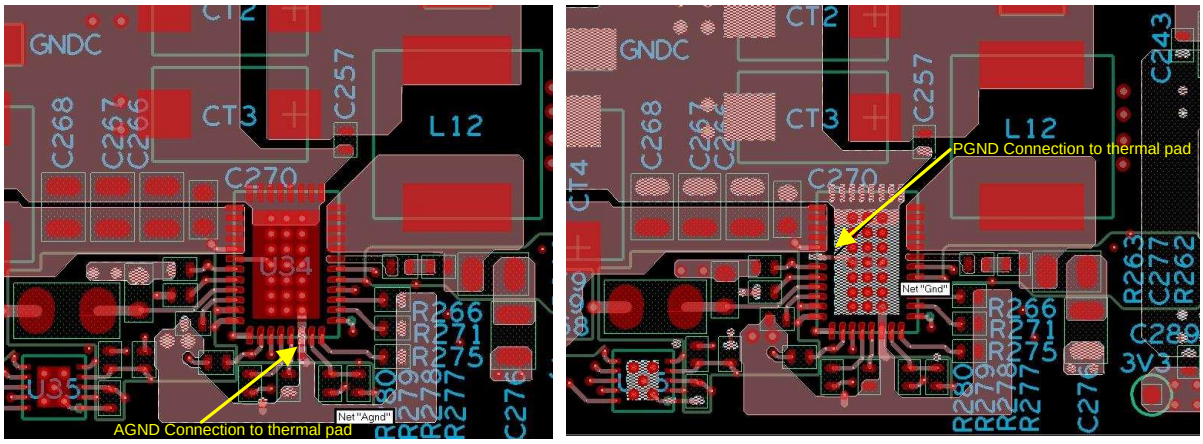


Figure 5. K2E EVM PCB Top Layer

Proper placement of the VIN bypass capacitors and the output capacitors reduces the loop inductance and minimizes noise. All capacitors found on the schematic page for the TPS544C25 are necessary for the proper operation of the power supply, and should be placed based on the layout guidelines provided in the data manual (SLUSC81). All capacitors associated with VIN are on the top layer of the board, with the high-frequency capacitors closest to the VIN pins of the TPS544C25. Local 12-V and ground planes are included for the capacitors on the top layer, to reduce the loop inductance and to keep any ripple off of the internal planes. Vias connect the local top layer planes with the internal planes. Multiple vias are needed to support the necessary current flow. The output capacitors are connected in a similar fashion with local ground and CVDD planes on the top layer of the board.

3.2 Ground Layer Connections



Analog Ground Ground

Figure 6. Analog Ground and Ground Planes

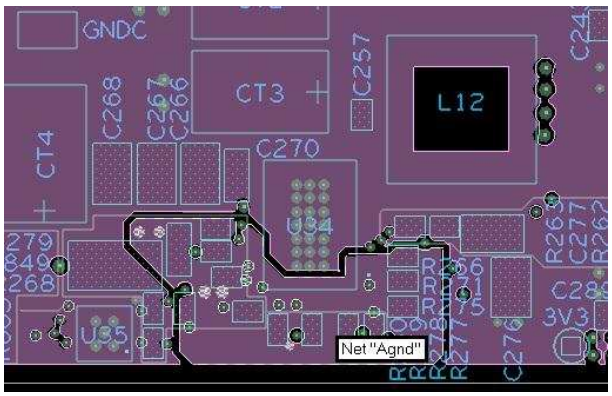


Figure 7. Analog Ground on Layer 2

The TPS544C25 includes pins labeled AGND and PGND. These separate grounds should be routed as different planes and attached at a single point. The device uses a thermal pad under the body to dissipate heat to the PCB. The thermal pad is connected to a similar shape on the bottom of the board, and to the ground planes with an array of vias. The top layer ground plane used for the input and output capacitors should be connected to pins 13 to 20, and to the thermal pad on the top layer. Include a single trace on the top layer between the thermal pad and pin 26.

The analog ground is used by components on one side of the TPS544C25. A small plane is included to connect these components on the top layer. This is connected to a small cutout AGND plane on layer 2. A single point of connection to the board ground is made between the thermal pad and pin 38, using a trace on the top layer. Note that AGND and PGND are not shorted in the schematic provided. A line and a layout note are included to represent the single connection point between the thermal pad and the AGND pin 38, but AGND and GND appear as different nets in the netlist.

3.3 Bypass for BP3, BP6, and VDD

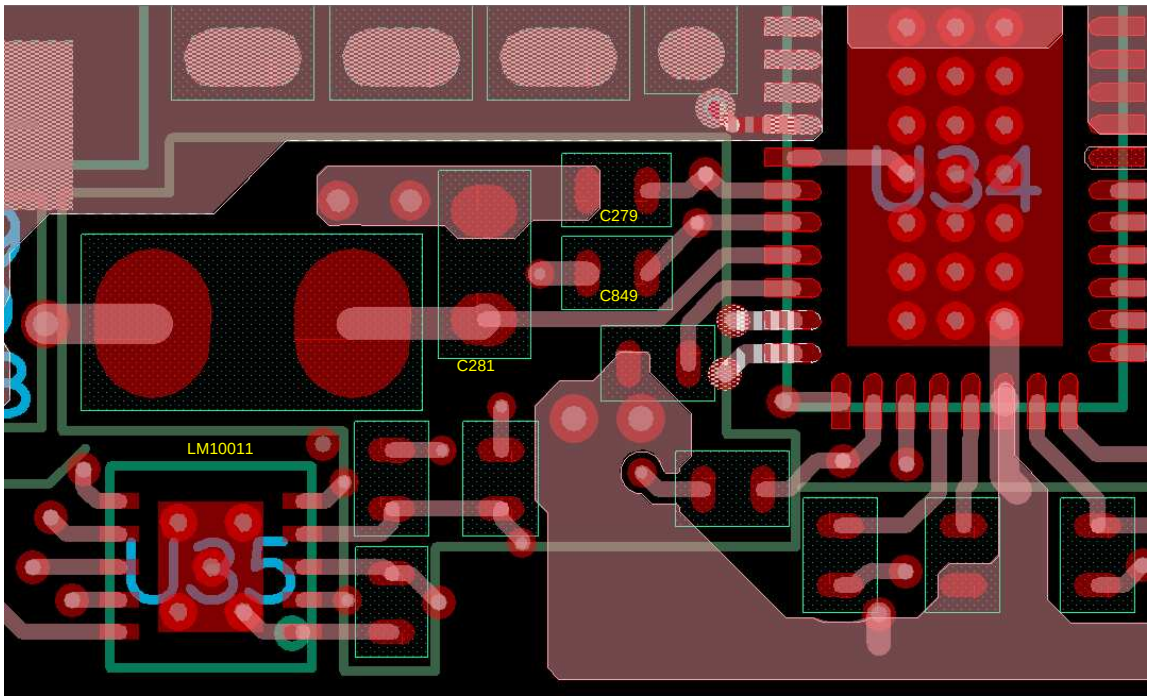


Figure 8. BP3, BP6, VDD Bypass, and LM10011 Position

The TPS544C25 has two internal regulators to provide power for the internal circuitry of the device. A bypass capacitor is required for each of these internal regulators on pins BP3 and BP6. A 2.2-uF capacitor is connected between BP6 and board ground. This capacitor is place directly adjacent to the pin. A 2.2-uF capacitor is connected between BP3 and analog ground. This capacitor is also place directly adjacent to the pin. The VDD pin is the supply pin for the internal regulators. This is connected to the top layer 12-V VIN plane through a resistor and a bypass capacitor. The capacitors are also connected to analog ground. These components are also placed close to the TPS544C25.

3.4 LM10011 Placement

The constant current path between the LM10011 and the 6.81K resistor is kept as short as possible by placing the LM10011 close to the TPS544C25. The VCNTL interface operates at a very slow rate, so longer traces to the SOC are used.

3.5 Sense Line Routing

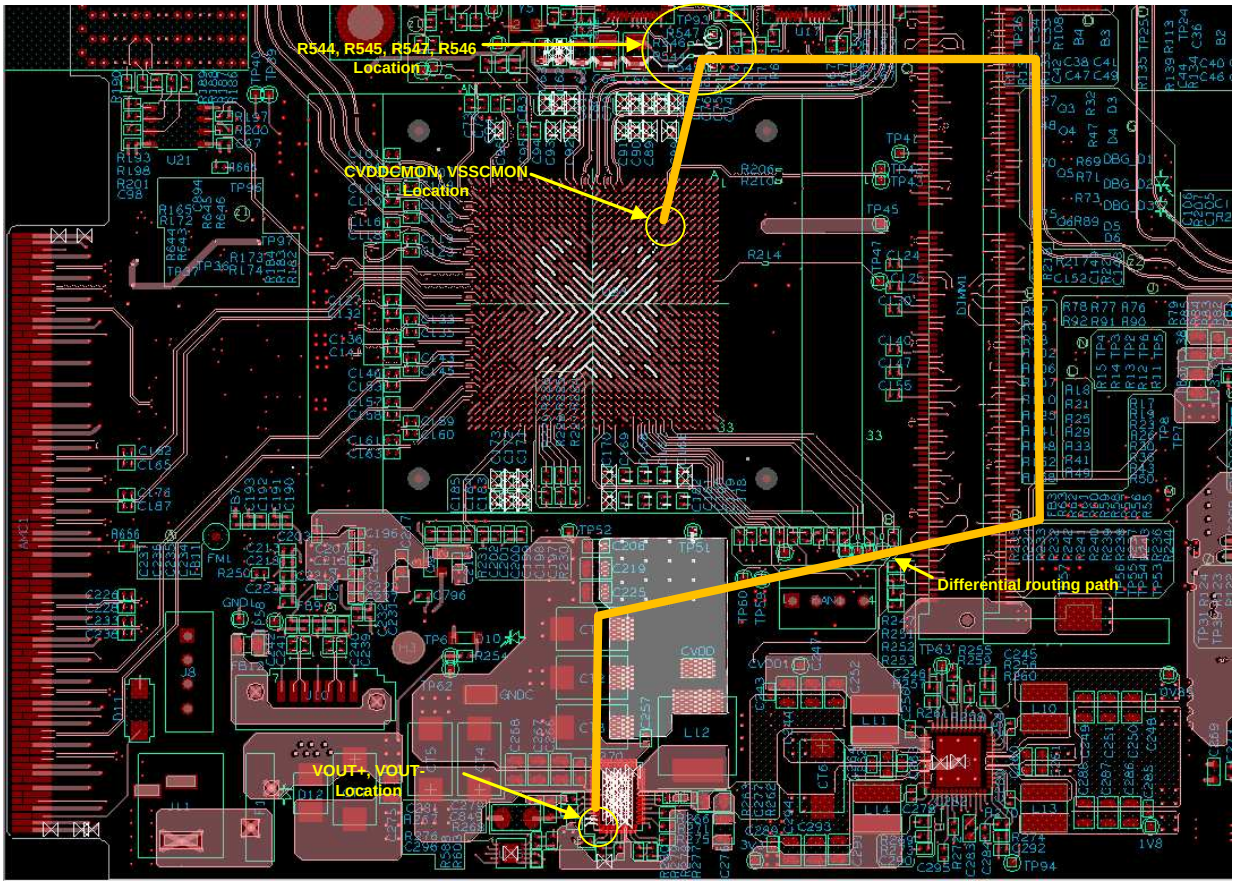


Figure 9. Sense Line Routing

The sense lines terminating at VOUTS+ and VOUTS- are connected to the CVDDCMON (J10) and VSSCMON (J9) pins on the K2E. The series resistors, R545 and R547, as well as the protection resistors, R544 and R546, are located above the K2E. A tightly coupled differential trace pair is routed on inner layers, approximately on the path shown in Figure 9. Note that the sense line is routed around an area of the board used for DDR3 routing.

4 References

1. *TPS544x25 4.5-V to 18-V, 20-A and 30-A SWIFT™ Synchronous Buck Converters with PMBus™ and Frequency Synchronization* (SLUSC81)
2. *LM10011 6/4-Bit VID Programmable Current DAC for Point of Load Regulators with Adjustable Start-Up Current* (SNVS822)
3. *66AK2E05, 66AK2E02 Multicore DSP+ARM KeyStone II System-on-Chip (SoC)* (SPRS865)
4. *AM5K2E04, AM5K2E02 Multicore ARM KeyStone II System-on-Chip (SoC)* (SPRS864)

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