66AK2L06 DSP+ARM® Processor JESD204B Attach to ADC12J4000/DAC38J84 Design Getting Started Guide

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1 Overview

The TI 66AK2L06 system-on-chip (SoC) is the industry's first JESD204B-compliant multicore DSP+ARM® SoC that can interface with high-performance JESD204B data converters. The device also includes a digital front end (DFE) that can process TX and RX signals, forming a system-optimized alternative to FPGAs.

This demonstration focuses on the JESD attach and DFE signal-processing capabilities of the SoC interfaced with TI's high-performance ADC12J4000 and DAC38J84 wideband-data converters. The demonstration consists of transmitting a sample file from the SoC through the DAC38J84 and looping it through the ADC into the SoC. The sample data files include dual-tone and multi-tone test patterns.

1.1 System Description

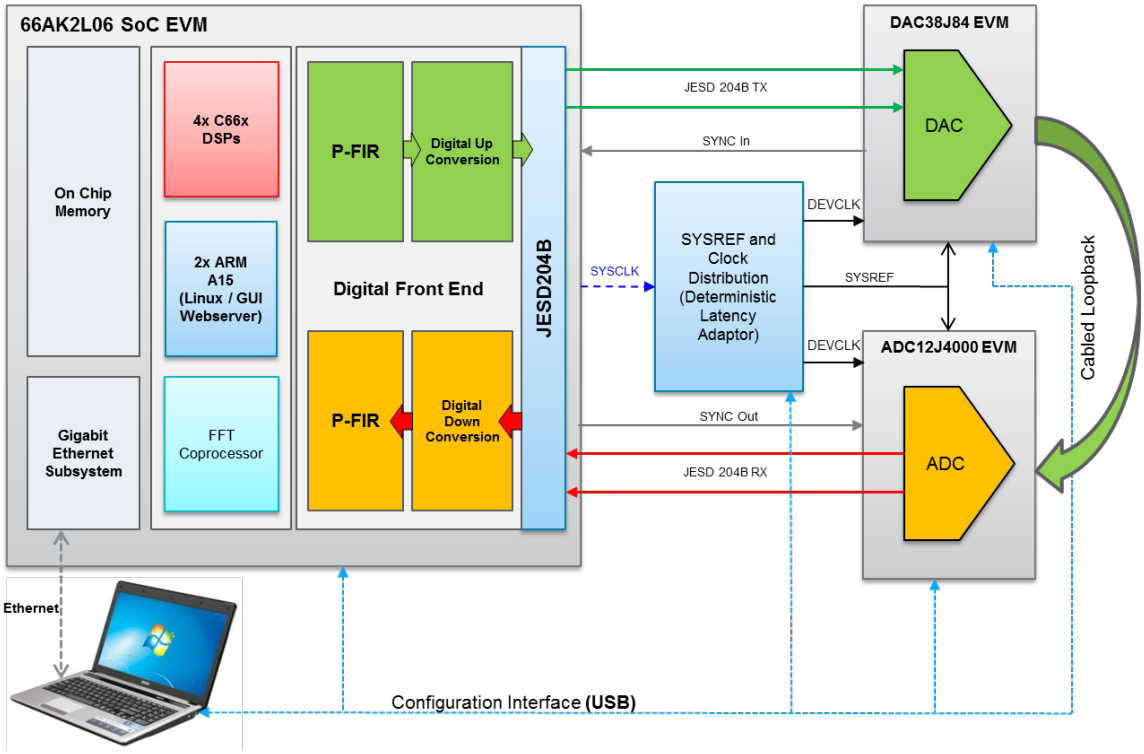

Figure 1. System Block Diagram

The DSP provides baseband data for two 75-MHz antenna carriers (FS = 92.16 Msps/carrier) to the DFE of the 66AK2L06 SoC. In the downlink path, one carrier is up-shifted by 43.5 MHz and the other is down-shifted by 43.5 MHz, giving a total bandwidth of 162 MHz. Carrier data is up-sampled from 92.16 Msps at baseband to provide 368.64 Msps at the JESD interface. The two carriers are combined onto one antenna and packed in parallel IQ format at the JESD204B SerDes. Although there are 4 JESD lanes on the 66AK2L06 SoC, only two are used (one lane for I and one lane for Q. The JESD204B SerDes link rate is 7.3728 Gbps).

DAC38J84 gets its input over JESD as parallel IQ data with a byte clock of 368.64 MHz. The DAC output rate is 737.28 Msps with an interpolation ratio of 2. The output of the DAC38J84 is centered at 184.32 MHz.

TI recommends using a spectrum analyzer to check the DAC output before running the loopback test. In the loopback case, the DAC output signal of the device is sent through a low-pass filter to the ADC12J4000. The DEVCLK of the ADC12J4000 is 2949.12 MHz. The ADC12J4000 is configured in Decimate-by-8 DDR P54 mode. It sends IQ data to the DFE over JESD in parallel IQ format with a byte clock of 368.64 MHz.

In RX side, the DFE inside 66AK2L06 SoC down-samples the data steam and shifts the two carriers back to a center frequency of zero.

2 Getting Started

2.1 Required Hardware and Software Components

Hardware Components

- The 66AK2L06 EVM, rev. 3.0, with the following accessories:
  - A 12-V power supply
  - A mini-USB cable for a UART connection
  - An Ethernet cable
- The K2L-HSP FMC Adapter Rev.A with the following accesories:
  - A mini-USB cable to connect with a PC
- The DAC38J84, rev. D, with the following accessories:
  - A 5-V DC power supply
  - A mini-USB cable for connection with a PC
- The ADC12J4000 EVM with the following accessories:
  - A 5-V DC power supply
  - A mini-USB cable for GUI SPI program
  - An ADC-WB-BB EVM with short marching-length SMA (male) cables
- DC-264 MHz low-pass filter
- 4 SMA cables

Software Components (with links to downloadable GUI installers)

The demonstration package is a Windows® installer executable. Running this installer on the Windows host extracts the software components per the following directory structure:

- RFSDK2 <latest_version> Top level directory includes:
  - RFSDK2 <latest_version>-full-bin.tar.gz: Demo package to be installed on top of MCSDK 3.1.4.7 on 66AK2L06 EVM
  - RFSDK2 <latest_version>-66AK2Lx-Design-Demo-Win-GUI-Configs.zip: Board initialization and configurations files for ADC12J4000 and DAC38J84 EVM GUIs
  - mcsdk314_rfsdk.tar.gz: MCSDK patches for the demo
  - RFSDK2 <latest_version>-doc.tar.gz: Documentation and Release notes
- Configuration GUIs for data converter EVMs (Windows-based)
  - ADC12J4000 EVM GUI

– DAC38J84 EVM GUI

2.2 Hardware Setup

1. To connect the 66AK2L06, DAC38J84, and ADC12J4000 EVMs, do the following:
   (a) Plug the FMC male connector of the ADC12J4000 into J11 (FMC female) of the DLC.
   (b) Plug the FMC male connector of the DAC38J84 into J10 (FMC female) of the DLC.
   (c) Plug the J4 FMC male connector of the DLC into CN16 (FMC female) of the 66AK2L06 EVM.
   For a view of the setup with all the boards connected, see Figure 2.
2. To connect the clocks, do the following:
   (a) Connect an SMA cable from J15 of the DLC to the DEVCLK of the ADC12J4000.

NOTE: The LMK04828 on the DLC is a dual-PLL clock chip. The clock-in reference for PLL1 comes from the 66AK2L06 EVM (122.88 MHz). The onboard VCXO of 122.88 MHz on the deterministic latency adapter (DLA) is a reference for PLL2. The output of LMK04828 provides device clocks to both DAC38J84 and ADC12J4000.

3. To connect the DAC38J84 output to ADC12J4000 input (the loopback configuration), do the following:
   (a) Use length-matching SMA cables to connect J2 (VOUT+) and J3 (VOUT–) of the ADC-WB-BB EVM to VIN+ and VIN– of the ADC12J4000.
   (b) Connect DAC38J84 output at J2 (IOUTAP) to the DC-264 MHz low-pass filter.
   (c) Connect the other end of the DC-264 MHz low-pass filter to the input of ADC-WB-BB EVM J1 to complete the loop back.
   For a view of the setup with all the clock and loopback connections, see Figure 3.
4. To connect USB and Ethernet cables, do the following:
   (a) Using a mini-USB cable to connect the mini-USB port J6 on the 66AK2L06 EVM to the PC. (The J6 provides the board-management controller [BMC] and Linux® serial-terminal interfaces multiplexed onto the same port.)
   (b) Use mini-USB cables to connect the ADC12J4000, DAC38J84, and DLC to the Windows host.
   (c) Connect the 66AK2L06 EVM ETH-0 (lower port) to the same network as the Windows host over a 1-Gbps connection (either directly or through a gigabit switch).

NOTE: Follow the correct power-up sequence for proper initialization of the setup. The K2L EVM is powered up first, followed by the DAC and ADC EVMs. Finally, the K2L-HSP FMC Adapter is powered up.

5. For power considerations, do the following:
   (a) Using the 5-V DC power supplies to provide 5 V to both the ADC12J4000 and the DAC38J84.
   (b) Use the 12-V DC power supply to provide 12 V to the 66AK2L06 EVM.
6. For other considerations, do the following:
   (a) For initial test and debug purposes, check the output of the DAC38J84 on a spectrum analyzer before trying to loop back. Connect the DAC38J84 J2 (IOUTAP) to the spectrum analyzer input.
   (b) When the DAC38J84 J2 output is working, configure and connect the DAC38J84 and the ADC12J4000 to loop back.

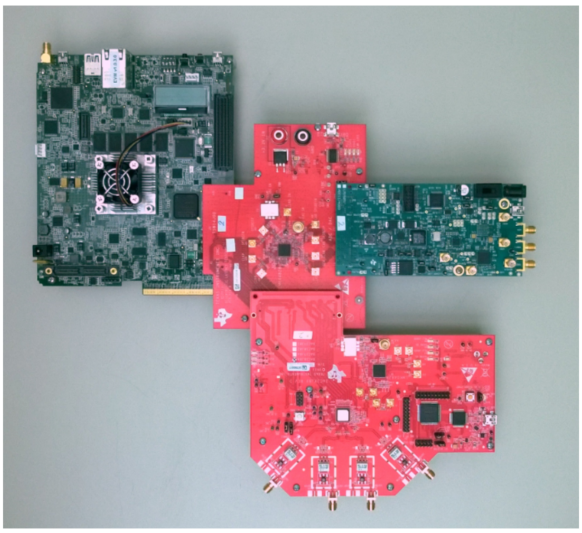

Figure 2. Boards Connected Together

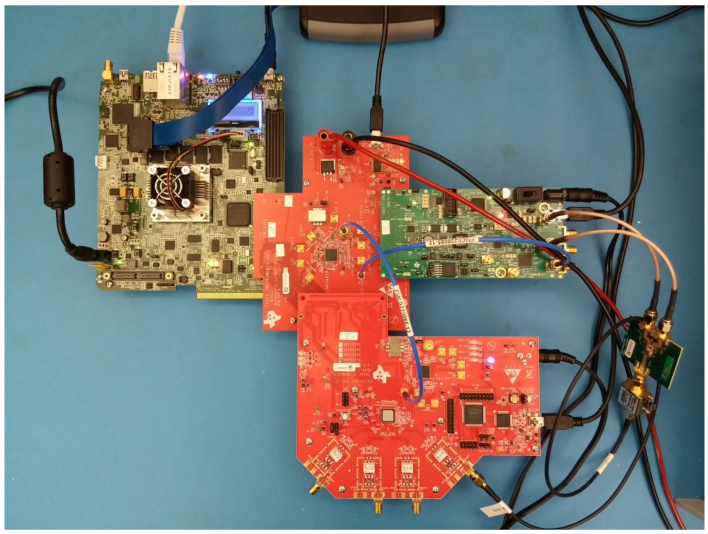

Figure 3. Complete Setup With Cables and Power Supplies Connected

2.3 Setup Software

2.3.1 Preparing the 66AK2L06 EVM for the Demonstration

To prepare the 66AK2L06 EVM for the demo, connect a terminal program (for example, Tera Term) to the 66AK2L06 EVM Linux COM port.

Use the following serial-port settings in the terminal program:

- **Baud Rate**: 115,200
- **Data**: 8 bit
- **Parity**: None
- **Stop**: 1 bit
- **Flow Control**: None

NOTE: The Silicon Labs™ CP210x VCP driver must be installed to enumerate the 66AK2L06 EVM virtual COM ports in Windows device manager.

Figure 4. 66AK2L06 EVM Virtual COM Ports

Though port numbers on your system may vary, the higher-numbered COM port (COM10) is for Linux.

To prepare the 66AK2L06 EVM for the demonstration, do the following:

1. **Update the UBIFS image on the 66AK2L06 EVM.**
   (a) Update the factory-installed MCSDK image on the 66AK2L06 to the image provided with MCSDK 3.01.04.07.
   (b) To update the UBIFS image on the 66AK2L06 EVM, tftp server is needed. Download the appropriate MCSDK installer (mcsdk_3_01_04_07_setupwin32.exe for Windows or mcsdk_3_01_04_07_setuplinux.bin for Linux) for your tftp host.
   (c) Run the installer and follow the prompts to install the new MCSDK on your tftp host machine.
   (d) When installed, the UBIFS image for the 66AK2L EVM is available in the images subdirectory under the MCSDK install directory. The image is named *k2l-evm-ubifs.ubi*.
   (e) Follow the instructions given in Using UBIFS File System to update the existing image on the EVM with the UBIFS image.
      - The image and directory names in this section may not match *k2l-evm-ubifs.ubi* but the procedure is the same. Use the appropriate *tftp_root* directory path, image name, and *serverip* according to your setup.
      - TI recommends using automated u-boot scripts *get_ubi_net* and *burn_ubi* to download and flash the UBIFS image, respectively.
2. **Install the device tree binary (dtb) patch.**
   (a) When the UBIFS image on the 66AK2L06 EVM is updated, update the dtb file on the EVM with the file in *mcsdk314_rfsdk.tar.gz* in the demonstration package.
   (b) Extract the dtb binary file from *mcsdk314_rfsdk.tar.gz* and follow the instructions in Updating Boot Volume Images From a Linux Kernel in the *Keystone-II MCSDK User Guide*.
      - The name of the patched dtb in the demo package may vary from the working dtb filename in the boot volume on the EVM. Ensure you copy the new dtb file to the boot volume with the original dtb filename. Failing to do this will cause the Linux boot to fail when restarting the board.

3. **Install the demonstration package** (user entries are *italicized*).
   (a) The Demo software is provided as a compressed archive named RFSDK2_<latest_version.tar.gz> in the Demo package. Copy this file to the tftp root directory of your tftp server.
   (b) With Linux booted, copy the above file to /home/root on the EVM (using tftp or scp).
   root@k2l-evm:~# *pwd*
   /home/root
   root@k2l-evm:~# *tftp -g -r* RFSDK2_<latest_version.tar.gz> <*tftp_server_ip_addr*>
   (c) Extract RFSDK2_<latest_version>-full-bin.tar.gz in the root directory
   root@k2l-evm:~# *cd /*
   root@k2l-evm:/# *tar xvf /home/root/* RFSDK2_<latest_version>-full-bin.tar.gz
   (d) Create a soft link to the default board configuration to finalize the installation
   root@k2l-evm:/# *cd /etc/radio/board*
   root@k2l-evm:/etc/radio/board# *ln -s lamarr-evm-demo1-mcsdk3147 default*
   root@k2l-evm:/etc/radio/board# *ls -l default*
   lrwxrwxrwx 1 root 42005 18 Dec 12 21:30 default → *lamarr-evm-demo1-mcsdk3147*
   (e) Reboot Linux on the EVM.

2.3.2 Installing PC-Side Software

Download GUI installers for the DAC38J84 and ADC12J4000 EVMs from the links in Section 2, Getting Started, and perform the following steps to install the corresponding GUIs:

1. Install the ADC12J4000 GUI.
   (a) After ADC12J4000 GUI is installed, go to the configuration files directory. Find this directory at C:\Program Files (x86)\Texas Instruments\ADC12J4000EVM GUIv<version_no>\Configuration Files.
   (b) Replace ADC12J4000_DB8_DDR.cfg with the corresponding file provided under RFSDK2_<latest_version>.66AK2Lx-Design-Demo-Win-GUI-Configs in the demo package.
2. Install the DAC34J84 GUI.

3 Running the Demo

3.1 Setting Up the DAC38J84 and ADC12J4000 EVMs

3.1.1 Power Up the Boards in the Following Sequence

1. 66AK2L06 EVM
2. ADC12J4000 EVM
3. DAC38J84 EVM

3.1.2 K2L-HSP FMC Adapter

1. Start the K2L-HSP FMC Adapter GUI. Ensure the USB Status indicator is green.

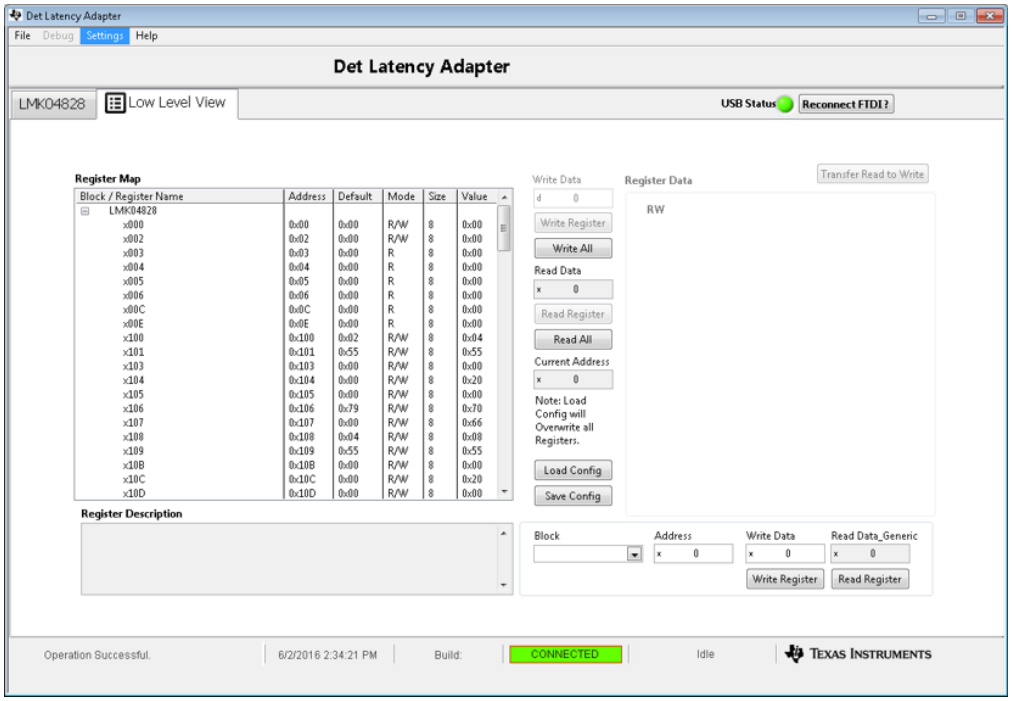

Figure 5. K2L-HSP FMC Adapter GUI

2. Click Load Config and select 66AK2L06_dac737p28.cfg under RFSDK_<latest_version>.66AK2Lx-Design-Demo-Win-GUI-Configs in the demo package. (This programs the required registers of the LMK04828.)

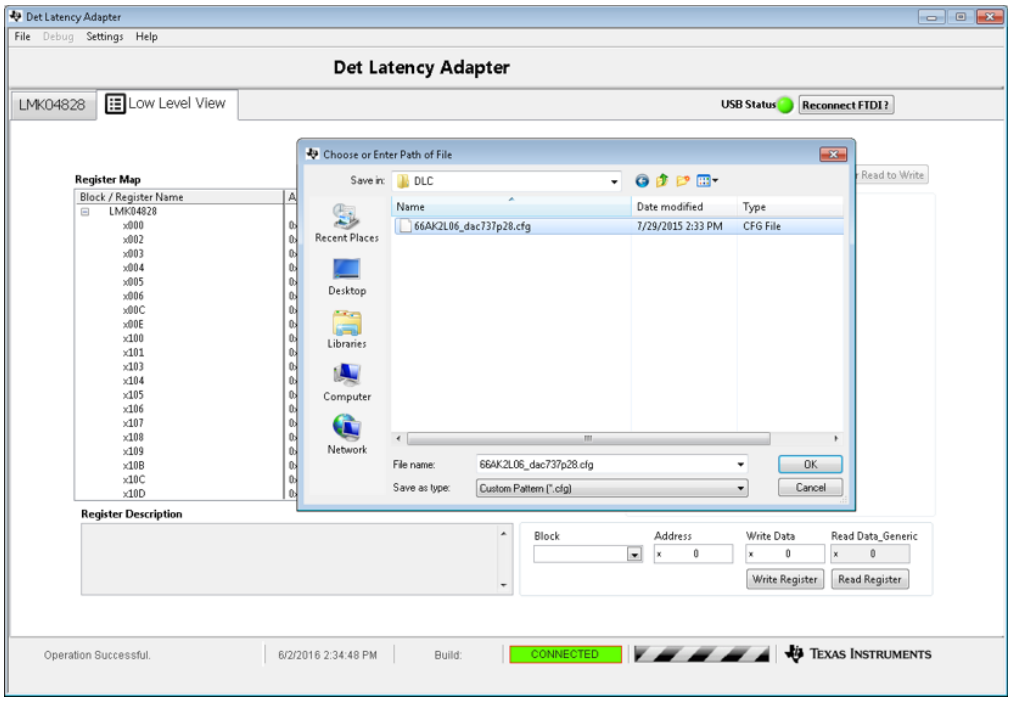

Figure 6. GUI-Load CFG

3. For the LMK04828 clock output settings, see Figure 7.

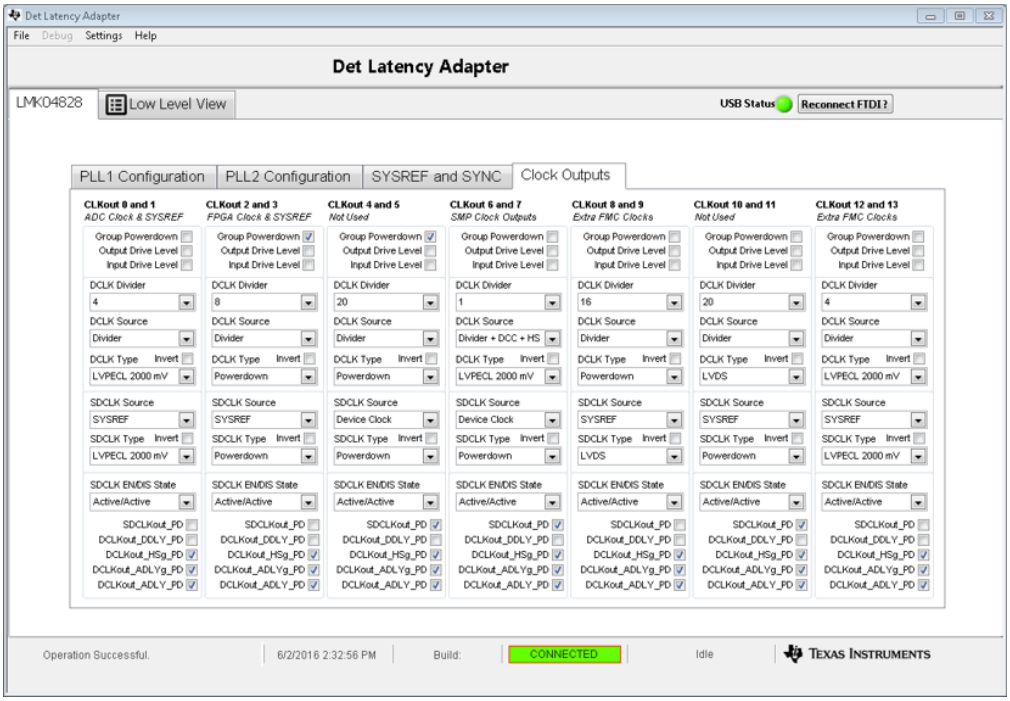

Figure 7. GUI Clock Outputs

The details of the clock configuration are the following:

- CLKOUT 6: ADC12J4000 device CLK is GTX CLKP (J15), div 1 for 2949.12 MHz, LVPECL. ADC12J4000 SysRef is unused.
- CLKOUT 12: DAC38J84 device CLK, div 4 for 737.28 MHz, LVPECL. DAC38J8x SysRef CLK is SDCLKOUT 13, LVPECL.
- When configured, the LMK PLL LOCK and VCXO LOCK LEDs on the DLC should be ON (see Figure 8). Ensure that the LMK LOCK LED is lit. If not, power-cycle the DLC and try to configure again.

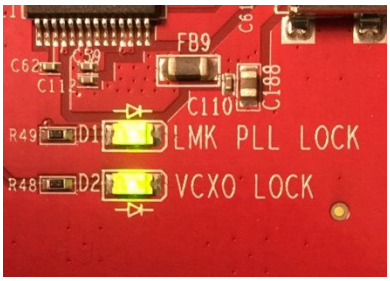

Figure 8. LED Status

3.1.3 DAC38J8x EVM GUI

1. Start the DAC34J84 GUI (Start → All Programs → Texas Instruments DACs → DAC3xJ8x GUI)
2. Ensure that the status of the USB is green.
3. Set the EVM Clocking Mode to Onboard.
4. Select DAC38J82 as the Device (this demonstration uses 2- of the 4-DAC channels on the DAC38J84).
5. Select DAC Data Input Rate to 368.64 Msps.
6. Select 2 as the Number of SerDes Lanes and as the Interpolation.
7. Click Program LLMK04828 and DAC3XJ8X.

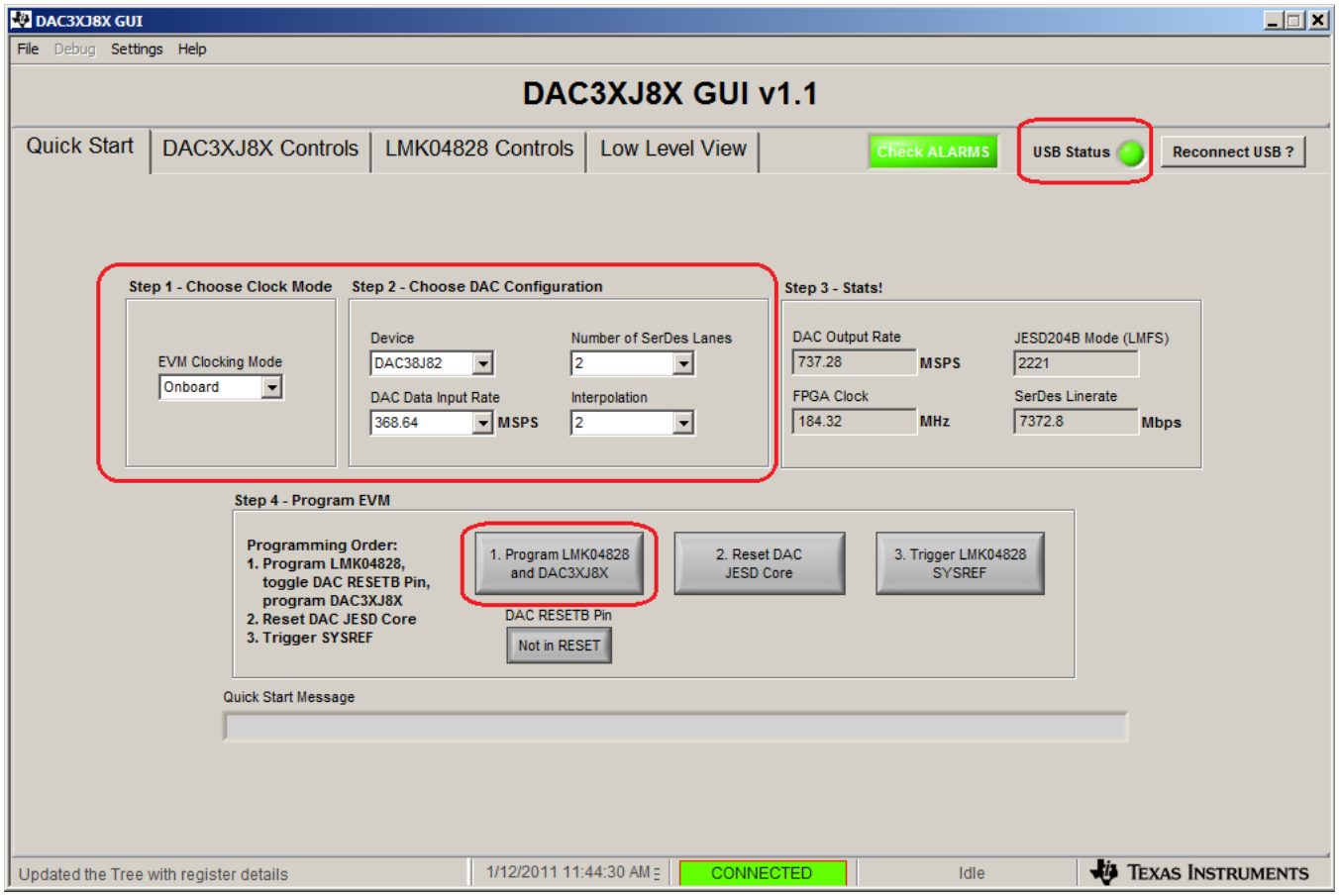

Figure 9. DAC38J8x GUI Start Page

8. When the programming is complete, click the Low-Level View tab and click Load Config.

9. Load the file K16_66AK2L06_rev3_737p28.cfg under RFSDK2_<latest_version>.66AK2Lx-Design-Demo-Win-GUI-Configs in the demonstration package.

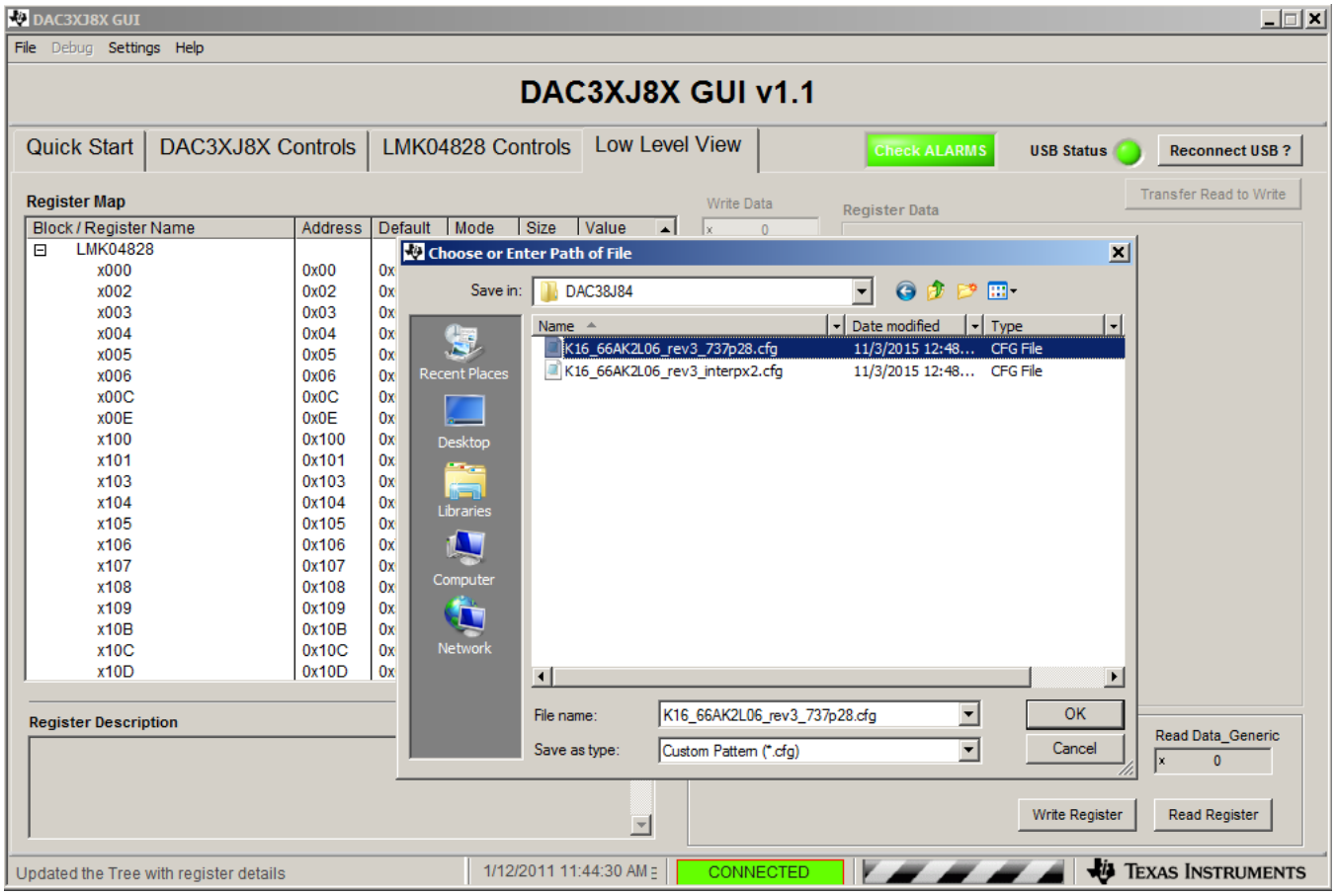

Figure 10. Low-Level View to Load Registers

For the SerDes configuration for the 66AK2L06, see Figure 11.

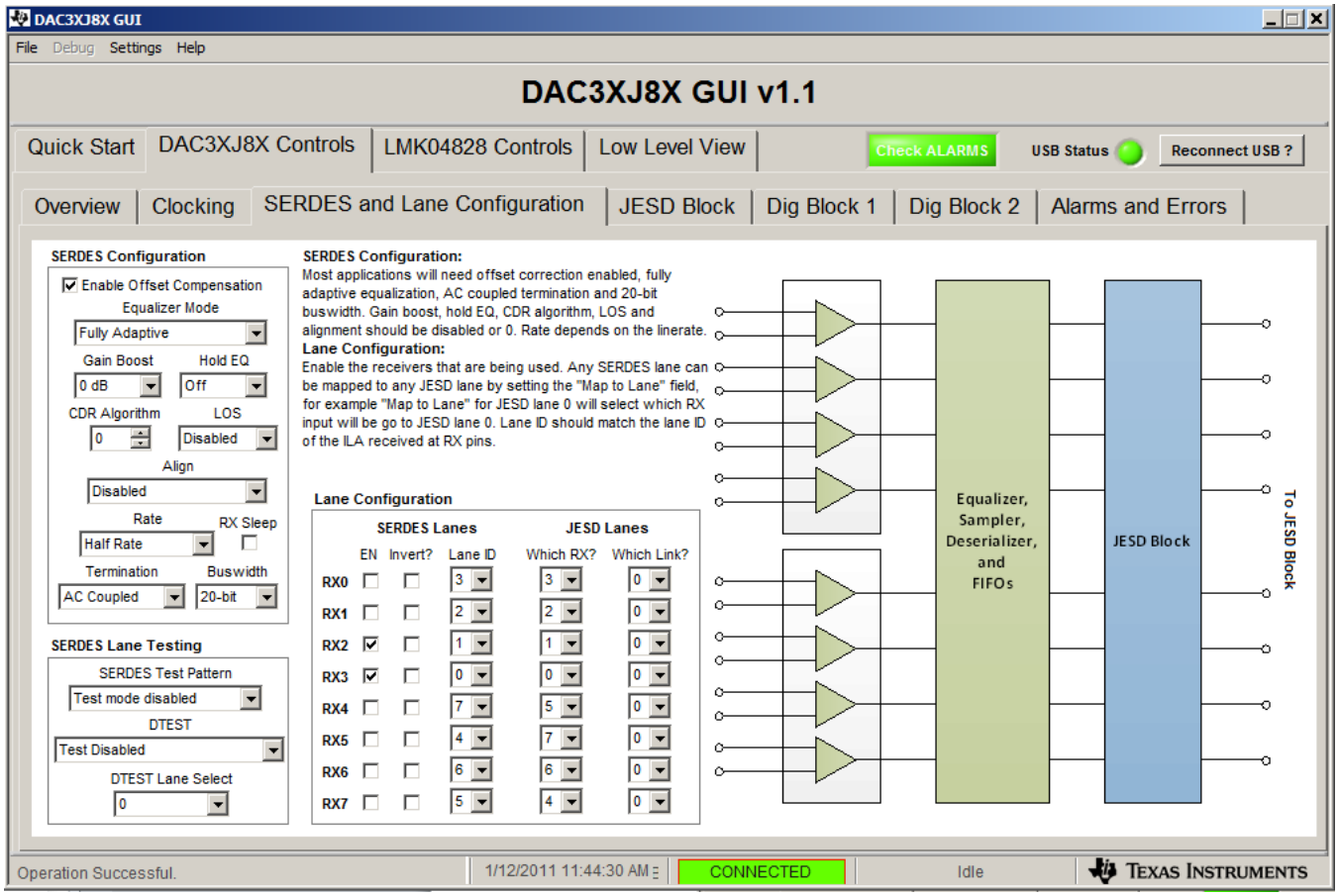

Figure 11. DAC38J8x GUI SERDES Lane Configuration

The course mixer of fs/4 is enabled, shifting the signal to 184.32 MHz. Refer to Figure 12.

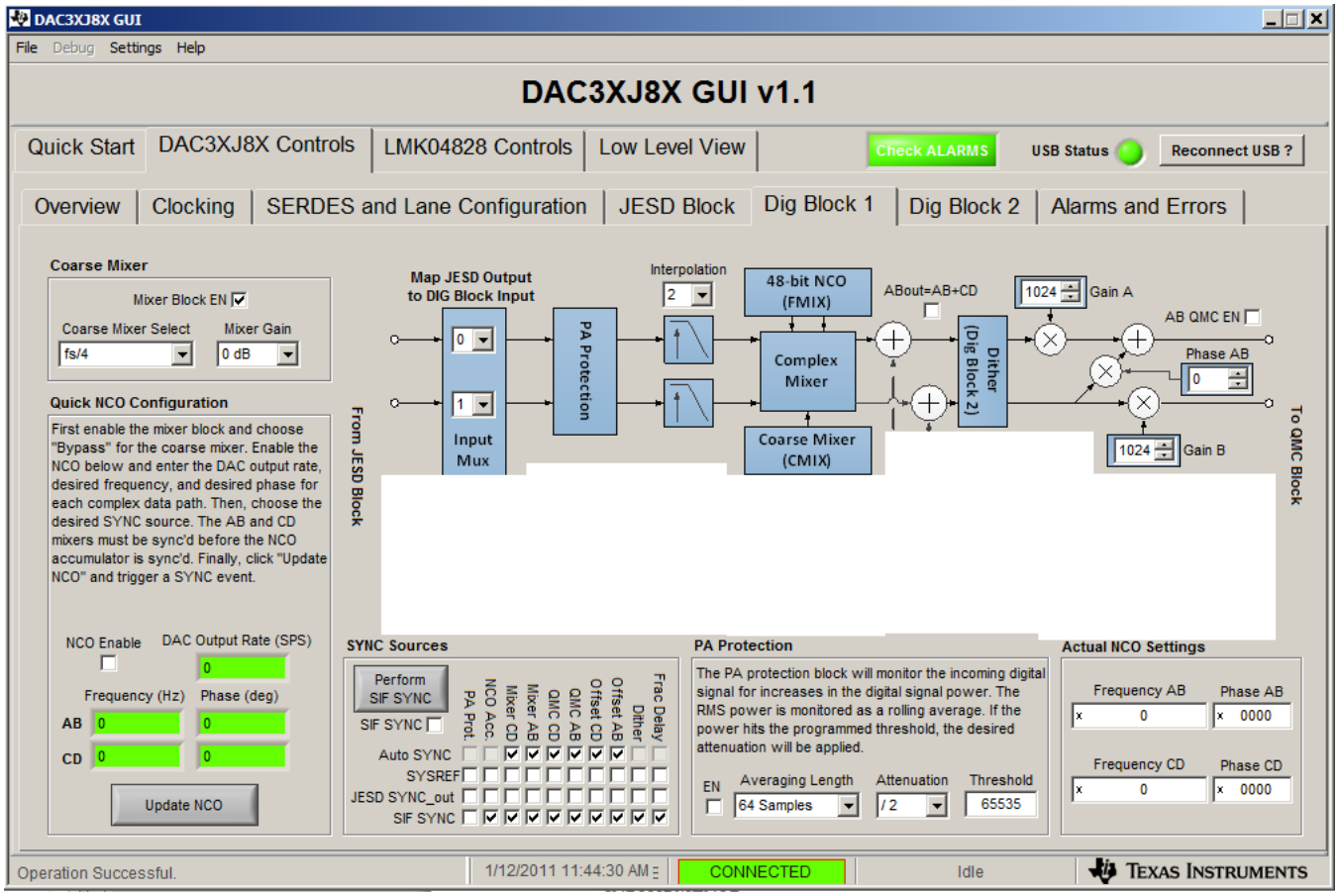

Figure 12. DAC38J8x GUI Course Mixer Setting

3.1.4 ADC12J4000 GUI

1. Start the ADC12J4000 GUI (Start → All Programs → Texas Instruments ADCs → ADC12J4000EVM GUI).
   (a) Ensure that the USB status is green. If the GUI does not connect to the board, click Reconnect FTDI until the green USB Status LED indicates a connection.
   (b) You may need to close the GUI for the DAC38J84 for the ADC12J4000 to work.
2. Set the clock source to External and set External Fs to 2949.12 MHz.
3. Set the mode to Decimate-by-8; DDR; P54
4. Click Program Clocks and ADC.
5. With the ADC12J4000_DB8_DDR_P54.cfg file replaced according to Section 2.3.2, the default configuration is best for this setup.

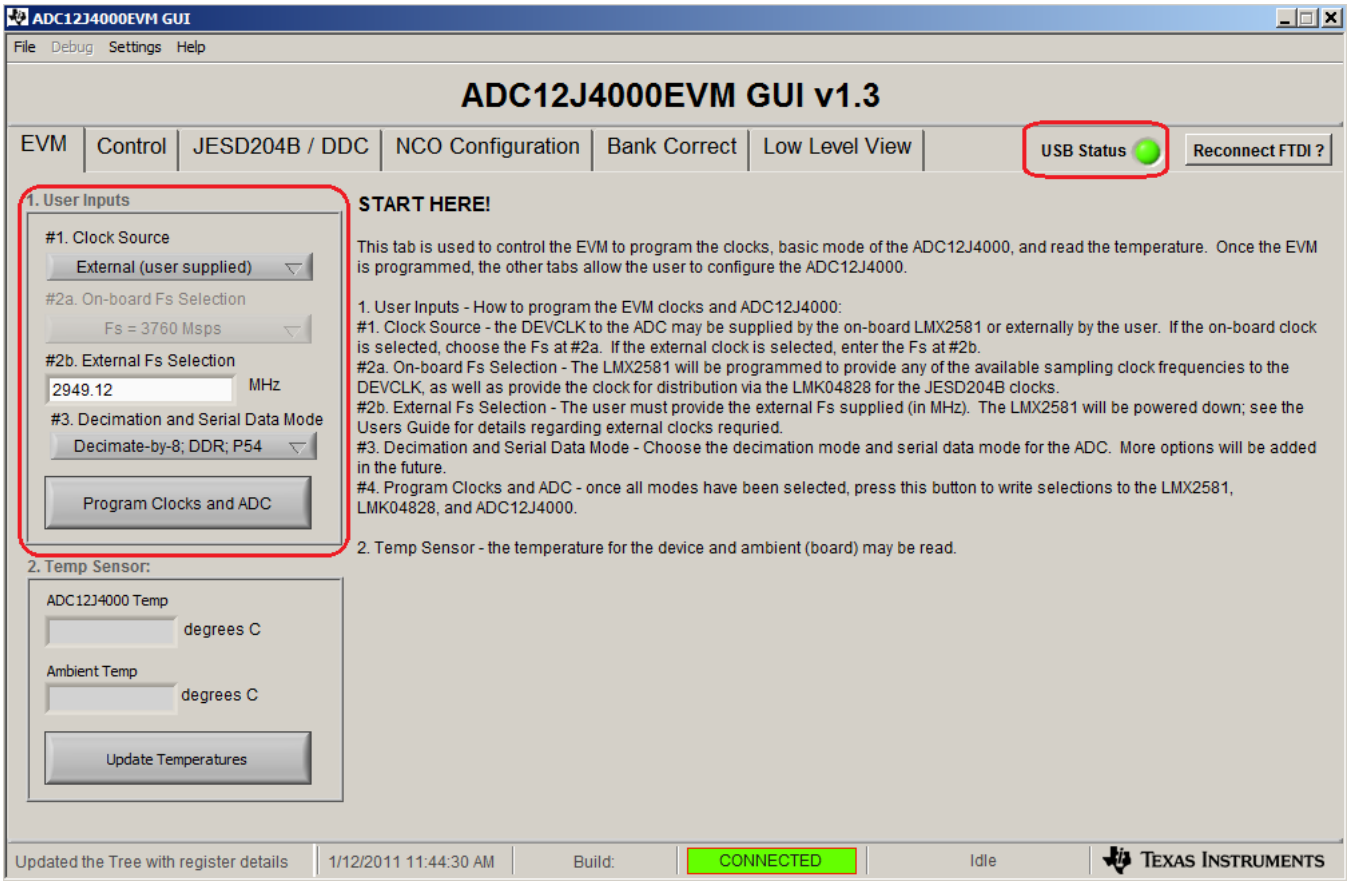

Figure 13. ADC12J4000EVM GUI Start Page

To view the JESD204B / DDC tab on the ADC12J4000 GUI, see Figure 14.

NOTE: While the data is in two's complement format and SYNC~ is differential, the corresponding status indicators on the GUI may reflect incorrect values.

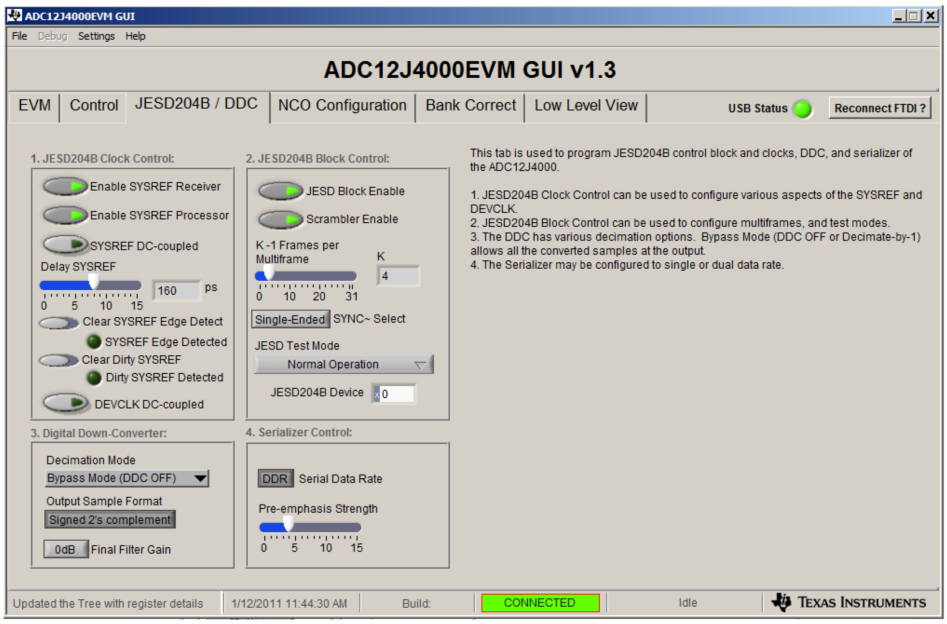

Figure 14. ADC12J4000EVM GUI -- JESD204B

3.2 Starting the Demonstration on 66AK2L06 EVM

1. Connect a terminal program (for example, Tera Term) to the 66AK2L06 EVM Linux COM port and login as the root user.
2. Determine the IP address assigned to the board using ifconfig. See Figure 15.

```
root@k2l-evm:~# ifconfig
eth0      Link encap:Ethernet  HWaddr 08:00:28:32:BA:5C
          inet addr:128.247.121.3  Bcast:0.0.0.0  Mask:255.255.254.0
          inet6 addr: fe80::800:2800:132:ba5c/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:11519 errors:0 dropped:0 overruns:0 frame:0
          TX packets:13 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:910369 (889.0 KiB)  TX bytes:1679 (1.6 KiB)
```

Figure 15. Querying the Board IP Address

3. Type "touch /tmp/rfsdk_stubbed_afe" in the 66AK2L06 Linux terminal. This requires running a loop back test with ADC and DAC, but not when JESDlpbk configuration is selected.
4. Open a browser and navigate to <EVM_IP_ADDRESS>:8080. To view the RFSDK Web GUI, see Figure 16.
5. Press "Wideband ADC12J4000 and DAC38J84 Demo".

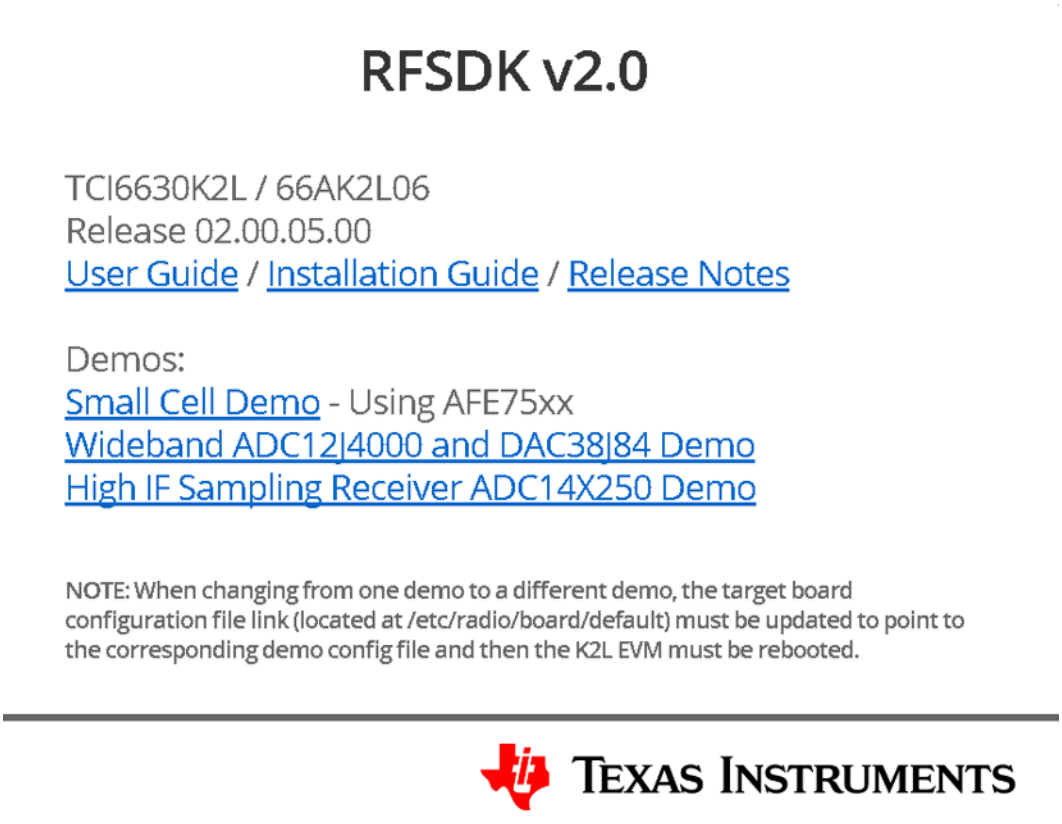

Figure 16. RFSDK Web GUI

6. The web GUI will navigate to the RFSDK v2.0 ADC12J4000 and DAC38J84 Demo Mode.

7. Press the Select button once the reset is completed to bring up the Radio Configuration Selection dialog as shown in Figure 17.
8. Select a configuration from 1×1-2xLTE75-HC-JESD121121x-DEMO1 or 1×1-2xLTE75-HC-JESD121121x-JESDlpbk. Press "Select".

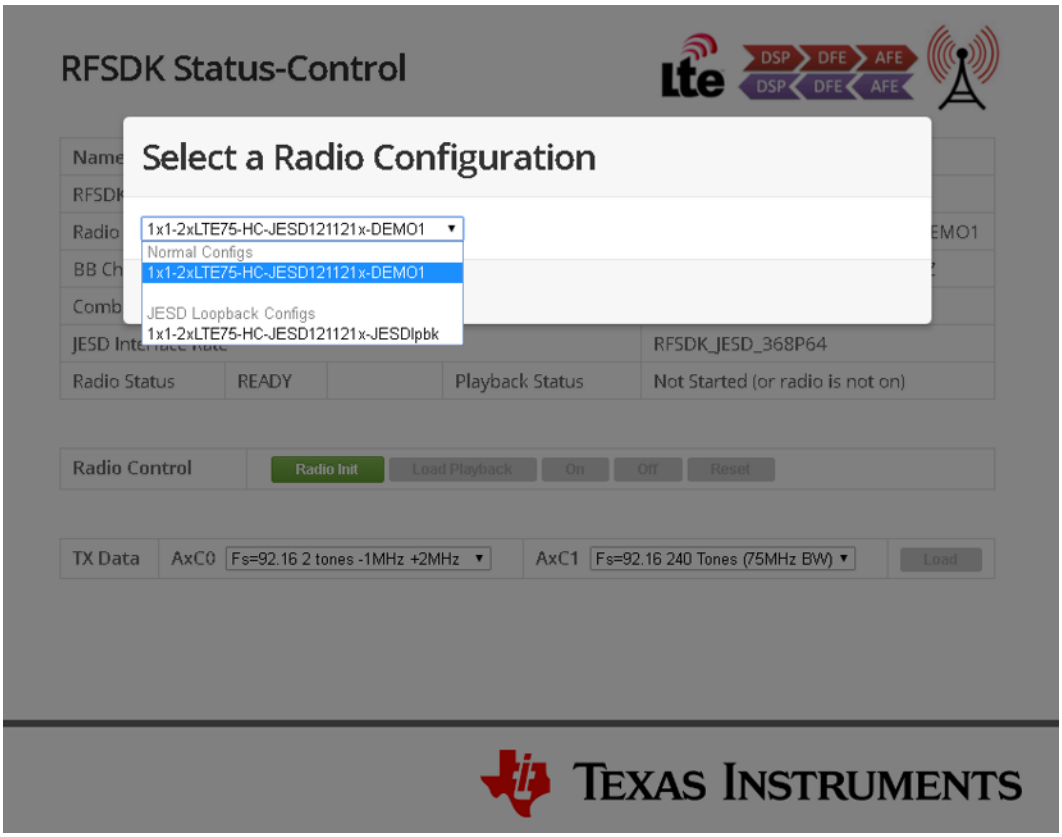

Figure 17. Radio Configuration Selection

9. In "Radio Control", press "Radio Init", "Load Playback", and "On" buttons in sequence to start the playback demonstration. (The status of playback should change to Started/Alive [this indicates the test is running]).

10. Click the AxC0 drop-down menu and select "Fs=92.16 2 tones, –1 MHz and +2 MHz", "Fs=92.16 2 tones, –2 MHz and +4 MHz" or "Fs=92.16 240 tones(75MHz BW)". This loads the selected signal patterns into the corresponding transmit buffers. Click the "load" button. The test patterns can be changed without having to stop the test.

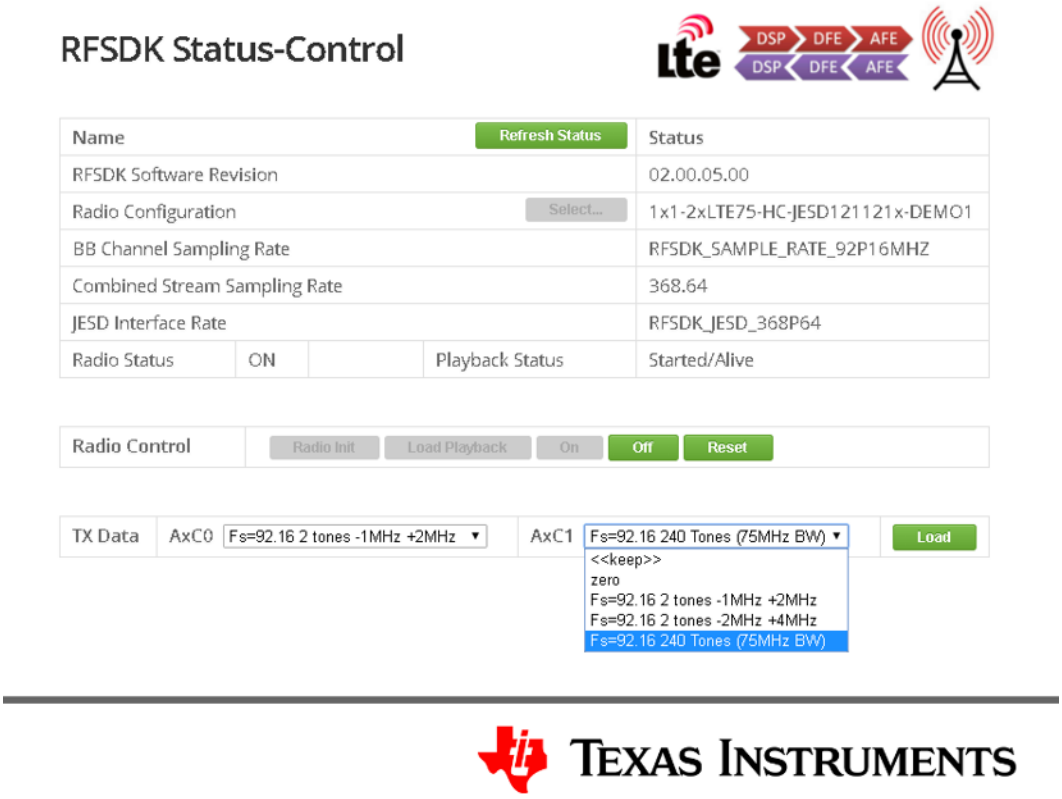

Figure 18. Loading Test Patterns

11. Navigate to the "TX Signal Capture @ DSP" page and press "Refresh Capture". This sends a request to the DSP to perform a signal capture of the Baseband data on the TX side (that is, before the signal data is sent to the digital front-end).

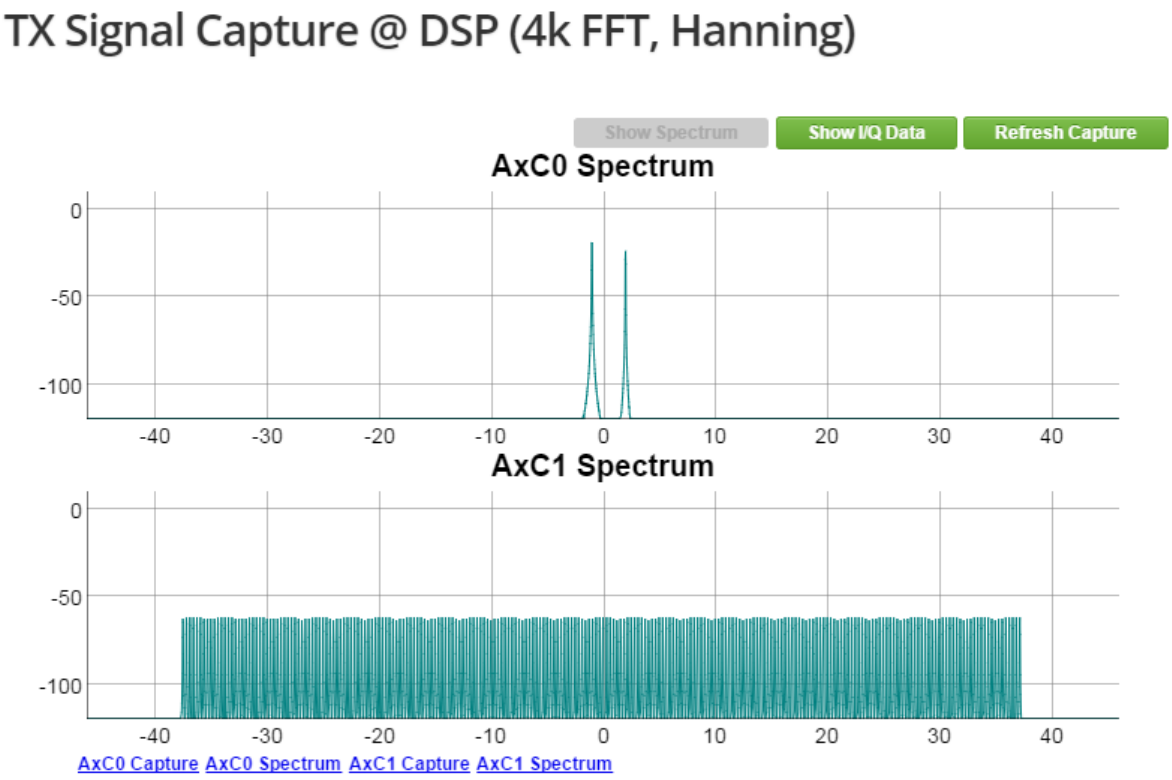

Figure 19. TX Signal Capture at DSP

Figure 19 shows that different test patterns are transmitted on both of the carriers. The first carrier is transmitting a 2-tone test pattern with the tones centered at –1 MHz and 2 MHz, respectively. The second carrier is set up to transmit 240 tones spread across a 75-MHz bandwidth.

12. Navigate to the "RX Signal Capture @ DSP" page and press "Refresh Capture". This sends a request to the DSP to perform a signal capture of the baseband data on the RX side (that is, after it has been looped back from the DAC38J84 to the ADC12J4000 and after being down-converted and filtered by the DFE). As shown in Figure 20, the test patterns transmitted on the respective carriers are recovered at the DSP after DAC to ADC loopback.

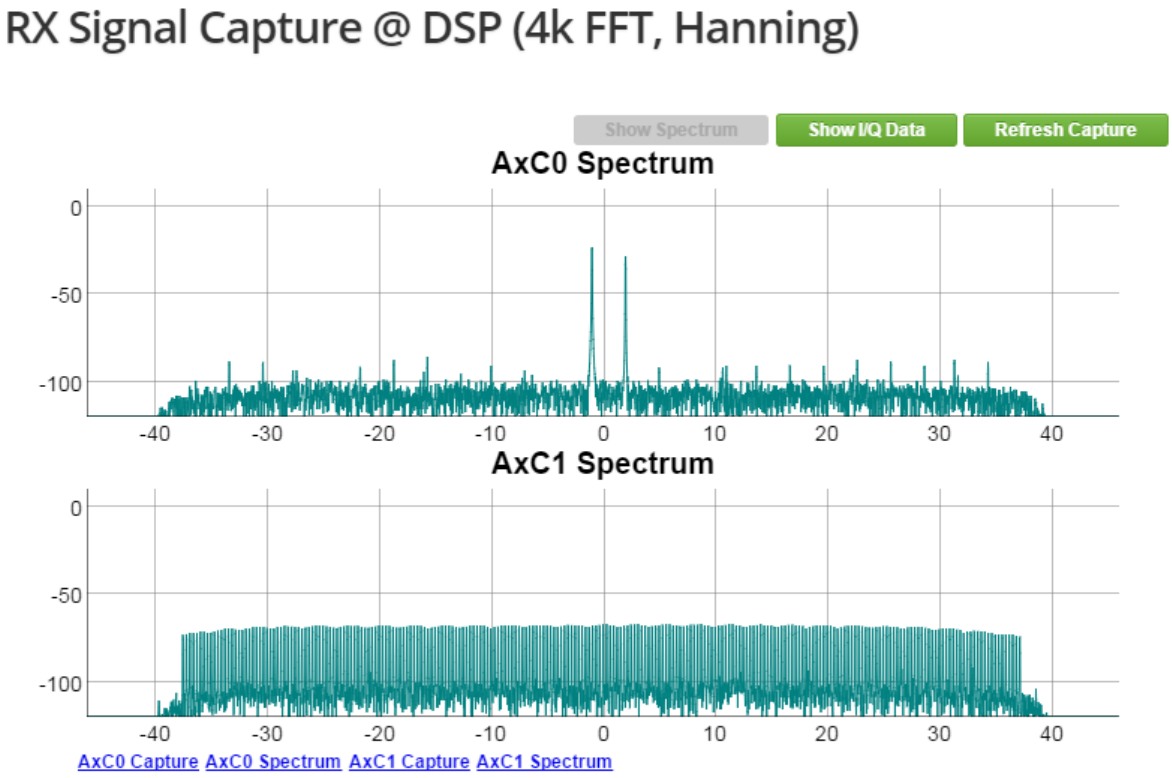

Figure 20. RX Signal Capture at DSP

For an alternative view of the combined RX spectrum from both carriers, go to the "Combined RX Signal Capture @ DSP" page as shown in Figure 21.

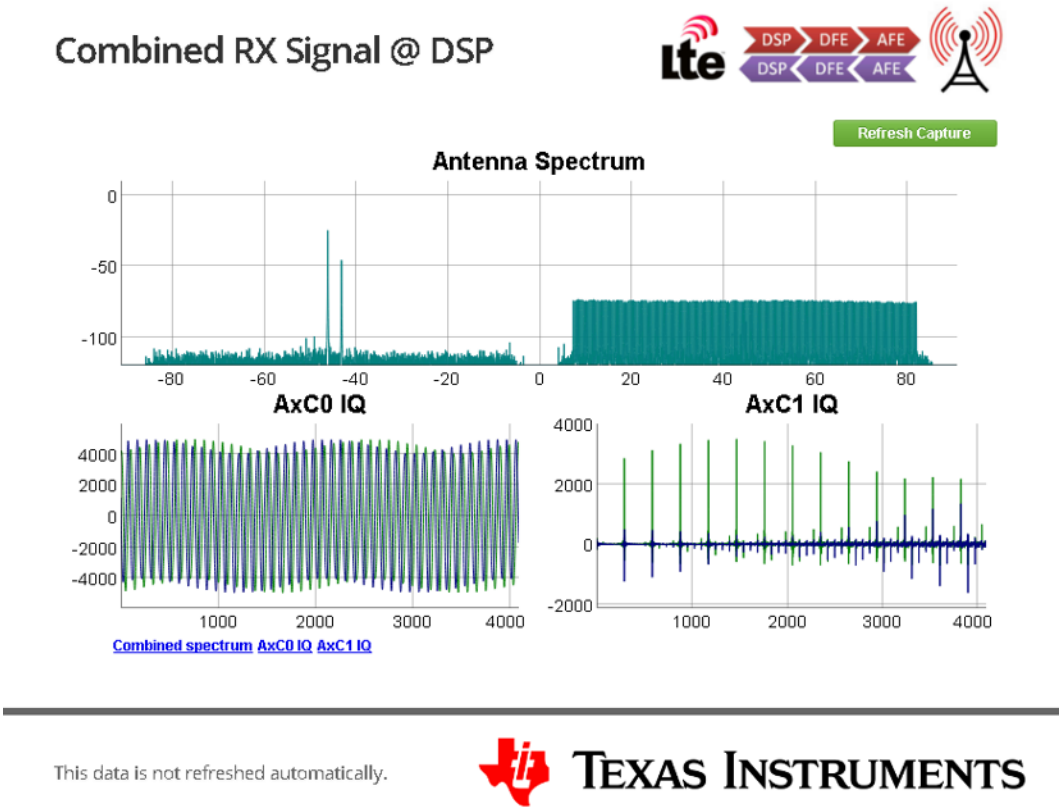

Figure 21. Combined RX Signal Capture at DSP

13. The RX captured data can be picked up by FFTC co-processor and display as shown in Figure 22.

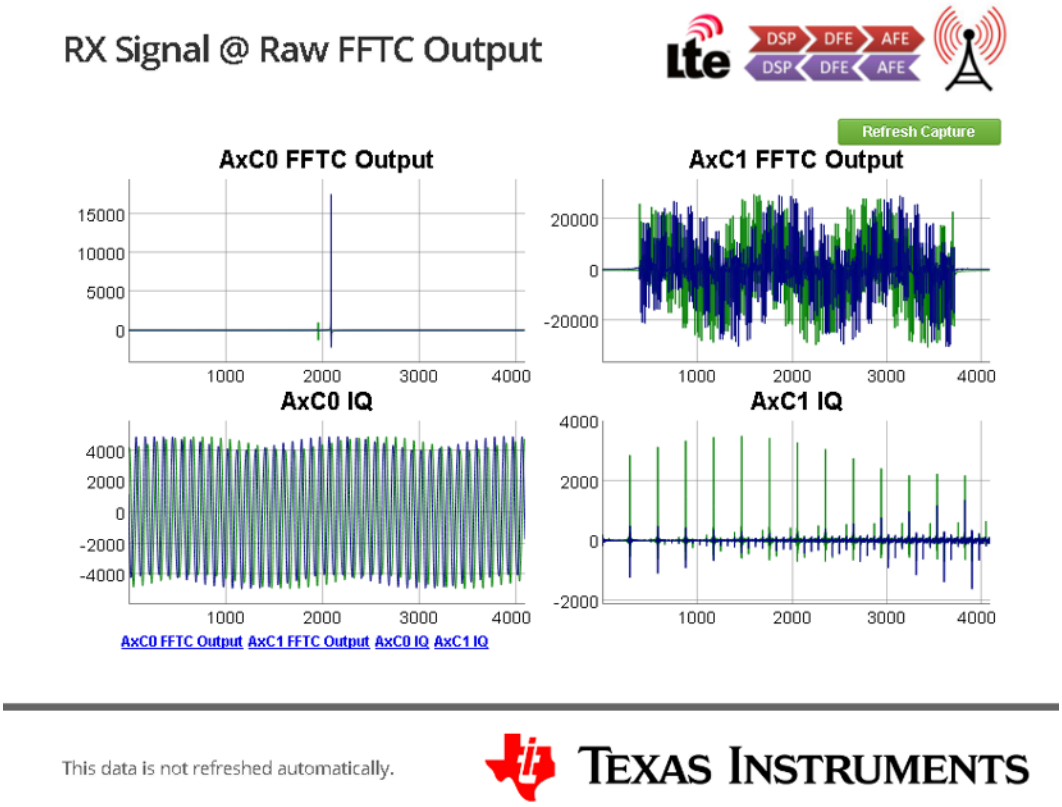

Figure 22. FFTC Output

14. Drag the mouse to zoom in on the graphs both vertically (to change the amplitude scale) and horizontally (to change the frequency scale) as shown in Figure 23 and Figure 24.

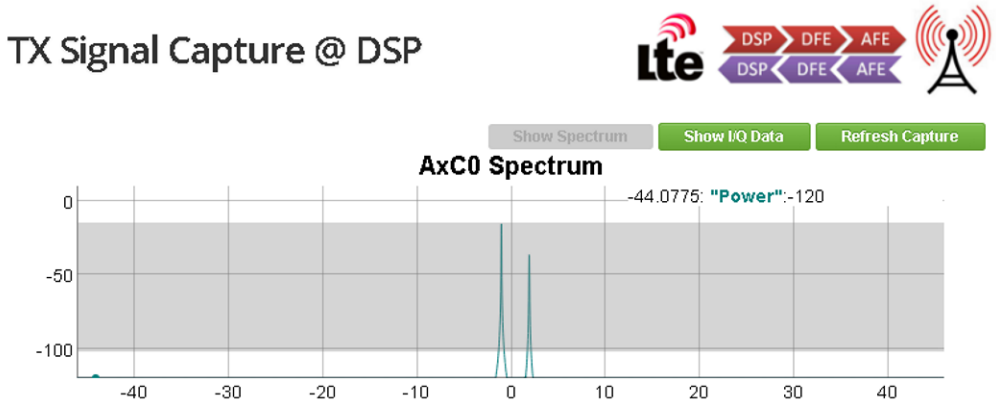

Figure 23. Changing Amplitude Scale on the GUI

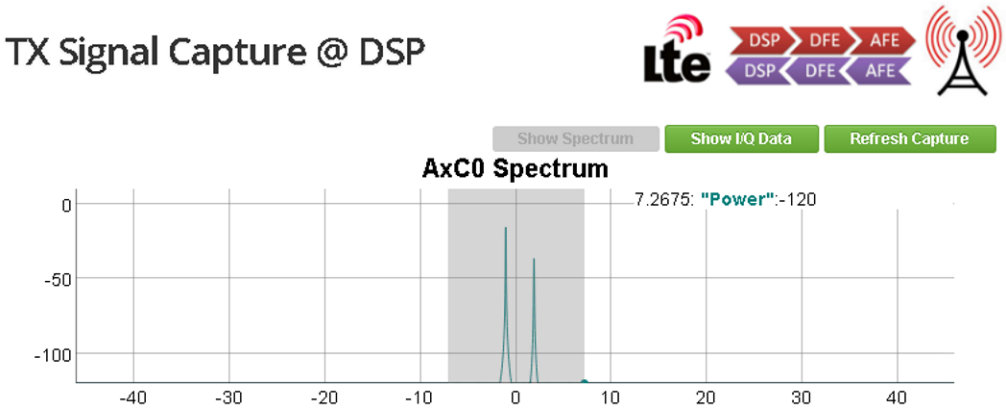

Figure 24. Changing Frequency Scale on the GUI

15. To stop the test, press the "Off" and "Reset" buttons on the Status-Control page.

4 Test and Debug

For a first-time setup, TI recommends using a spectrum analyzer to check the DAC38J8x output . For the 2-tone output and 75-MHz output, see Figure 25 and Figure 26.

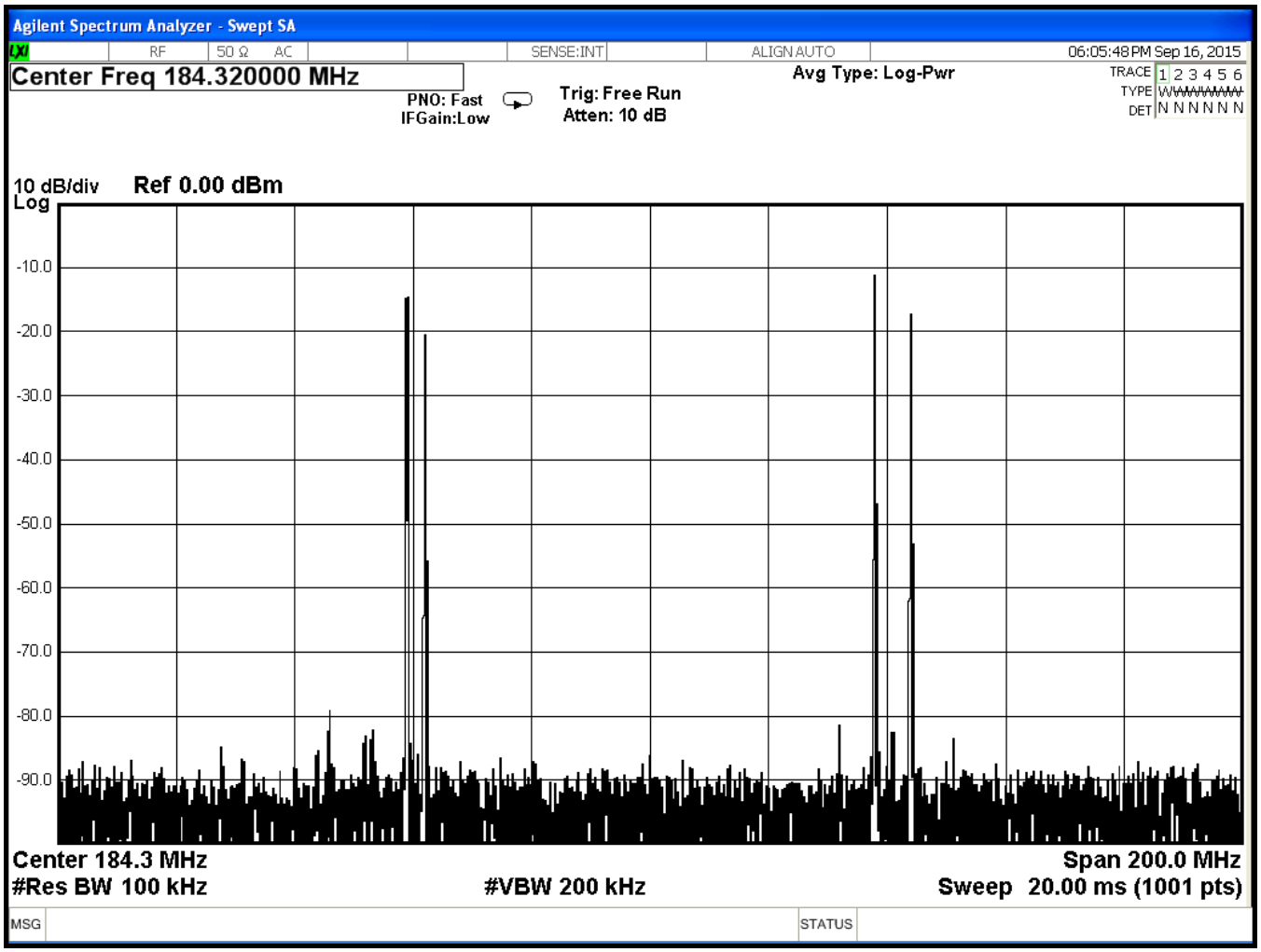

Figure 25. DAC Output – 2×75 MHz 2-Tone Data

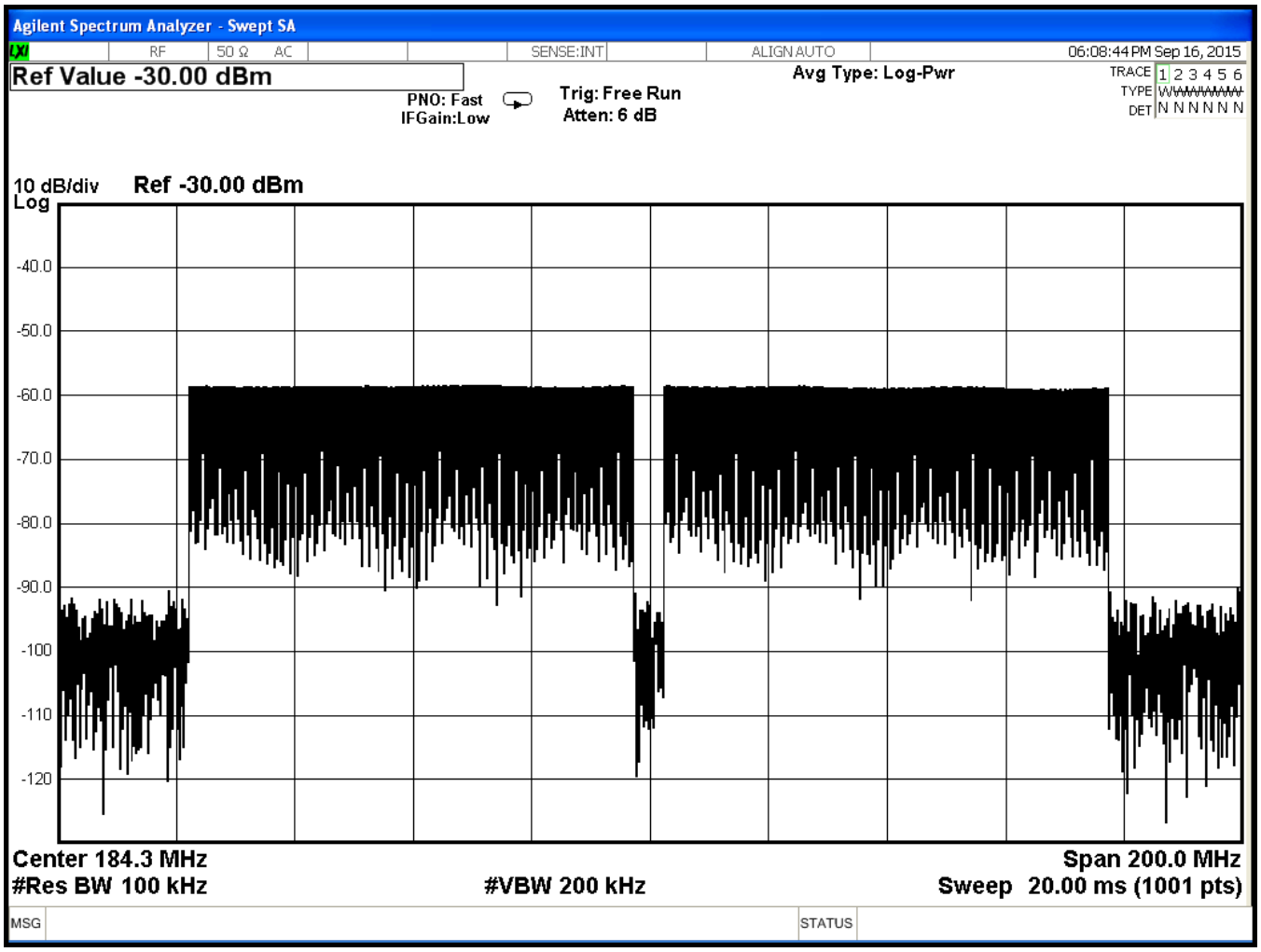

Figure 26. DAC Output -- 2×75 MHz Multi-Tone Data

The DAC38J8x EVM output is a real image and has the image in the second Nyquist zone. This image will be visible without the filter. To view the DAC output, see Figure 27.

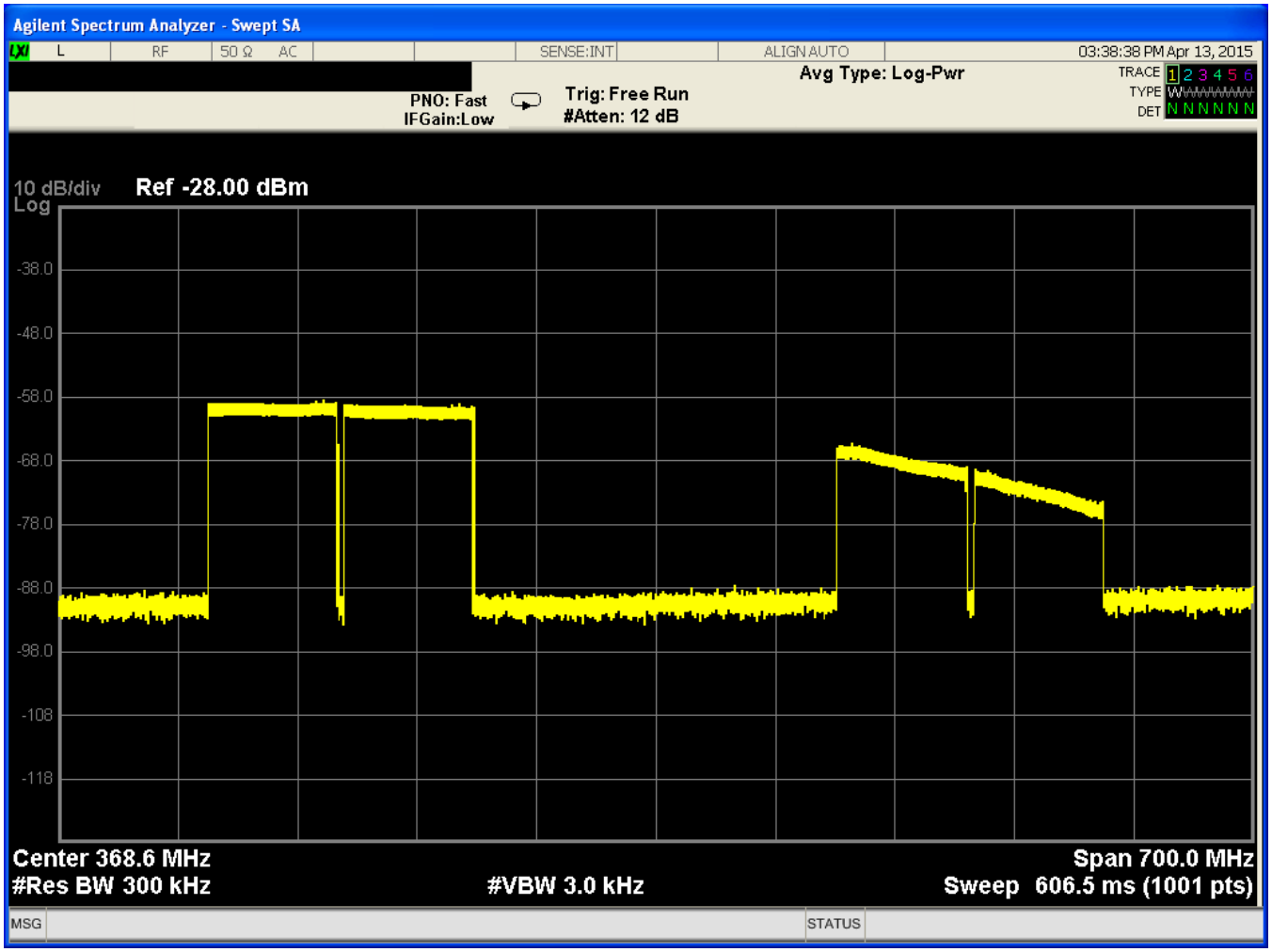

Figure 27. DAC Output -- 2×75 MHz Signal With its Image With no Filter Installed

When the DC-264 MHz low-pass filter is used, the image is filtered out. About 1-dB suppression exists at the high end of the band because the signal span is from 103.32 MHz to 265.32 MHz for 2×75 MHz. To view how the low-pass filter filters out the image, see Figure 28.

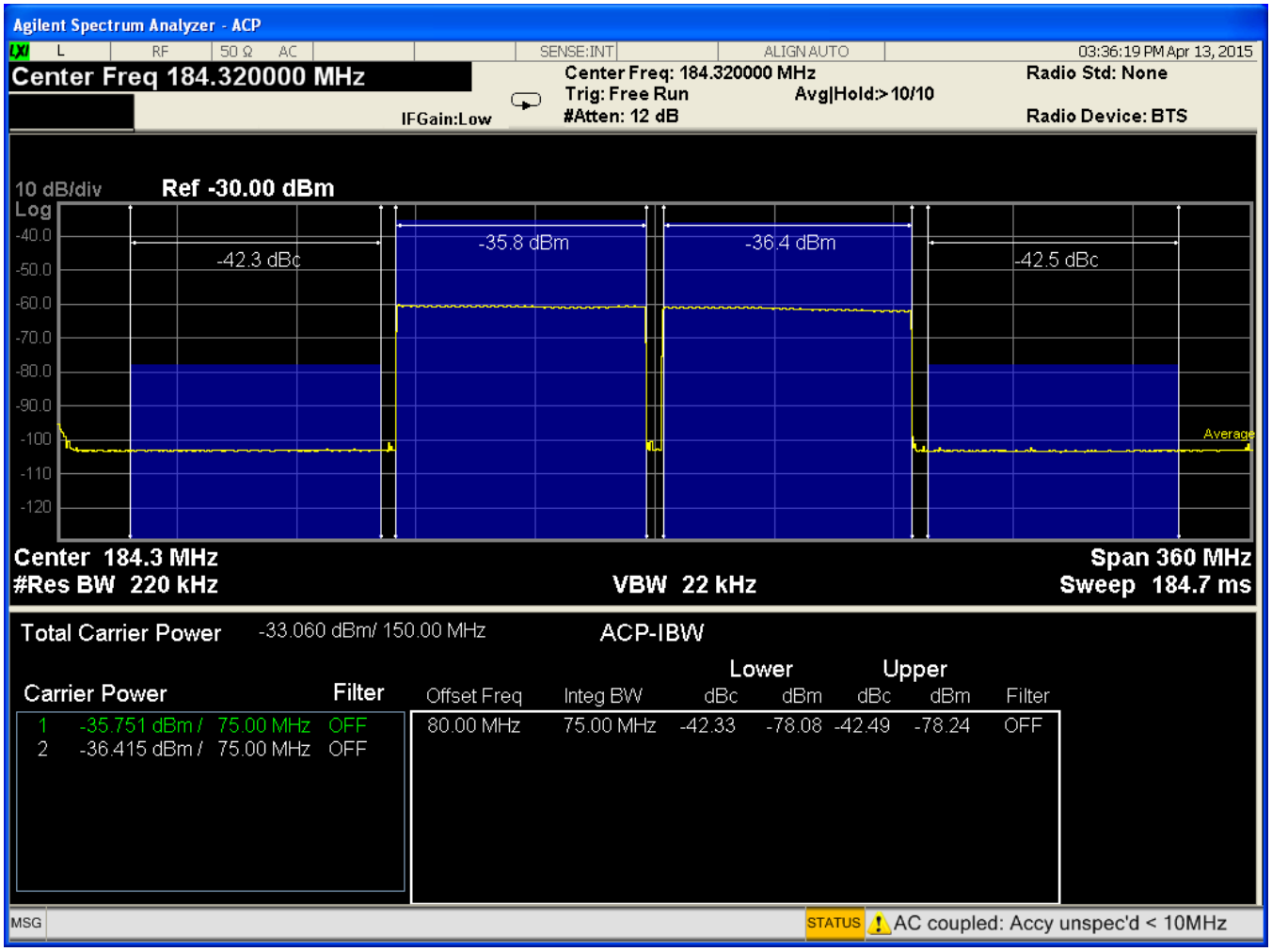

Figure 28. 2×75 MHz DAC Output with DC-264 Low Pass Filter

By default, the output power of the 2xLTE60 is –24 dBm. The adjacent channel power ratio is –58.7 dBc for the high side. The low side crosses DC and is unable to provide an accurate ACP measurement. To view the 2xLTE60 ACP test, see Figure 29.

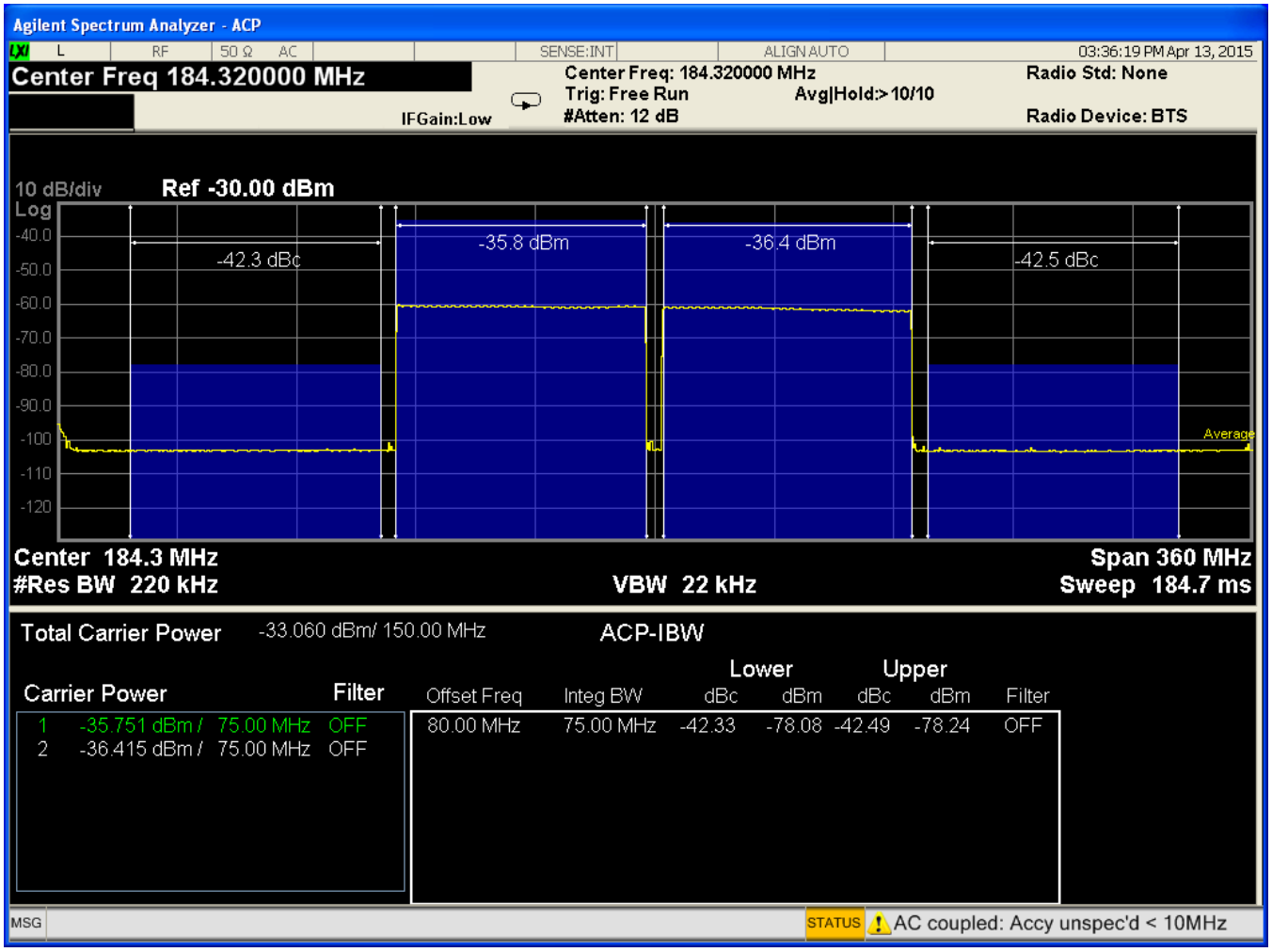

Figure 29. 2×75 MHz Data: Adjacent Channel Power Ratio Test

5 References

Refer to the following links for more information related to the hardware and software components in this demonstration:

66AK2L06 EVM

ADC12J4000 EVM

DAC38J84 EVM:

Keystone-II MCSDK User Guide

Keystone-II Architecture DFE User Guide

Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (November 2015) to B Revision **Page**

Revision A History

Changes from Original (April 2015) to A Revision **Page**

- Changed how "Sync In" and "Sync Out" appear in the system block diagram. 1
- Changed from K16_Lamarr_rev3_737p28.cfg to 66AK2L06_dac737p28.cfg 7
- Updated Image GUI-Load CFG 7
- Updated Image RFSDK Web GUI 15
- Updated Image Radio Configuration Selection 16
- Updated Image DEMO1 - Loading Test Patterns 17
- Updated Image TX Signal Capture at DSP 18
- Updated Image RX Signal Capture at DSP 19
- Updated Image Combined RX Signal Capture at DSP 20
- Updated Image Changing Amplitude Scale on the GUI 22
- Updated Image Changing Frequency Scale on the GUI 22
- Updated Image DAC Output – 2×75 MHz 2-Tone Data 23
- Updated Image DAC Output -- 2×75 MHz Multi-Tone Data 24
- Updated Image DAC Output -- 2×75 MHz Signal With its Image With no Filter Installed 25
- Updated Image 2×75 MHz DAC Output with DC-264 Low Pass Filter 26
- Updated Image 2×75 MHz Data: Adjacent Channel Power Ratio Test 27

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