TI Designs

Synchronization of JESD204B Giga-Sample ADCs using Xilinx® Platform for Phased-Array Radar Systems Design Guide

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- Radio Telescope
- Beamforming Antenna
- Test and Measurement: Oscilloscope
- Software-Defined Radios (SDRs)

Design Resources

TIDA-00432	Tool Folder Containing Design Files
ADC12J4000	Product Folder
LMK04828	Product Folder

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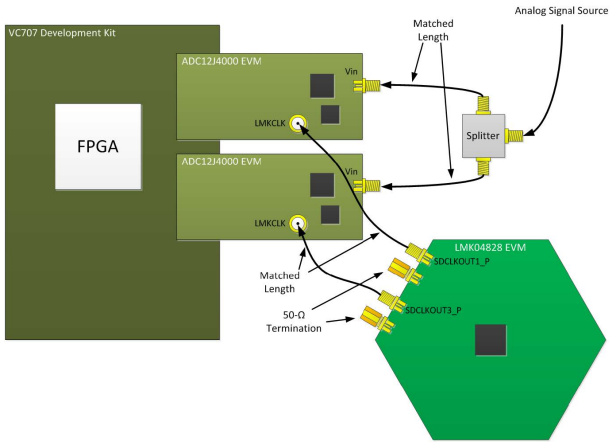

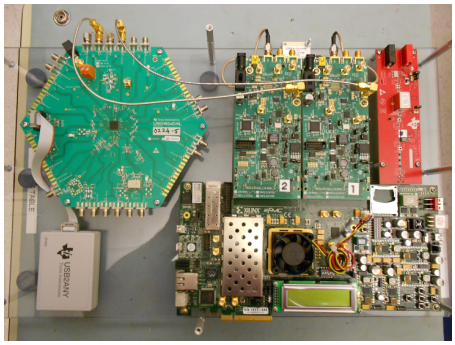

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General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is **intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments**. If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
   (a) Keep work area clean and orderly.
   (b) Qualified observer(s) must be present anytime circuits are energized.
   (c) Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   (d) All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   (e) Use stable and nonconductive work surface.
   (f) Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   (a) De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   (b) With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   (c) After EVM readiness is complete, energize the EVM as intended.

   WARNING: WHILE THE EVM IS ENERGIZED, NEVER TOUCH THE EVM OR ITS ELECTRICAL CIRCUITS AS THEY COULD BE AT HIGH VOLTAGES CAPABLE OF CAUSING ELECTRICAL SHOCK HAZARD.
3. Personal Safety
   (a) Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

1 Design Introduction

NOTE: The ADC12J4000 EVM for this design is labeled ADC12JXXXXEVM A or alternatively, ADC12J4000. Previous versions of the ADC12J4000 EVM are unable to be modified to work in this configuration.

The basic test setup includes the following (see Figure 1):

- A Xilinx VC707 development kit
- Two ADC12J4000 evaluation modules (EVMs)
- An LMK04828 EVM

The VC707 platform interfaces to both ADC12J4000 EVMs through two onboard FMC connectors. The FMC connectors are for the JESD204B data lines and SYNC signals. The FMC connectors also provide the clocks for the field-programmable gate array (FPGA) from the ADC12J4000 EVMs. Through a 0-degree power splitter and matched-length cables, a common phase-matched analog signal is provided to both ADC12J4000 EVMs.

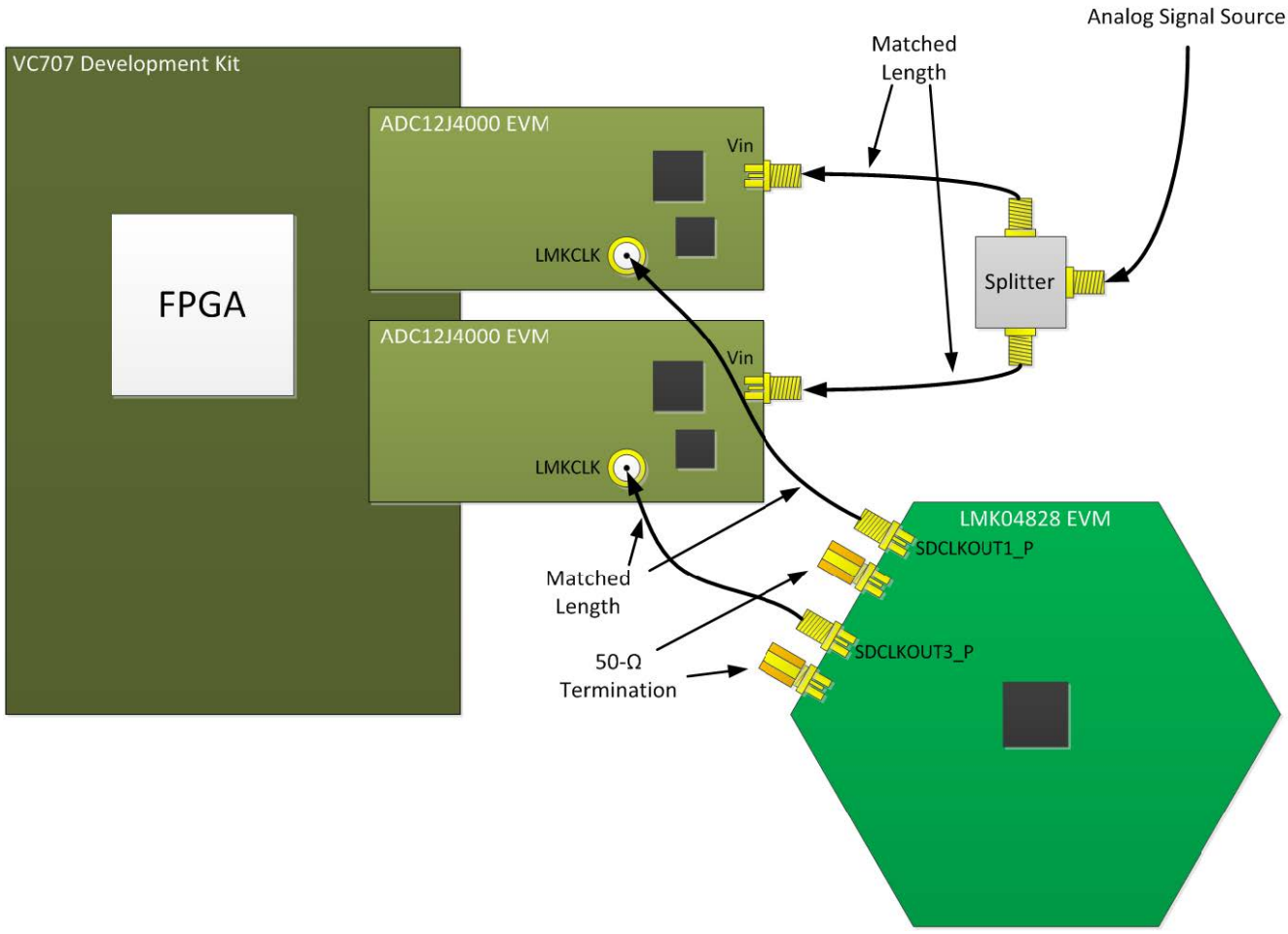

Figure 1. Hardware Block Diagram

Figure 2 shows the overall clocking scheme. The LMK04828 EVM creates two phase-aligned SYSREF signals that are sent to each ADC12J4000 EVM through matched-length cables to maintain phase alignment at the input of the LMK04828 on each ADC EVM. The LMK04828 clock chip onboard each analog-to-digital converter (ADC) EVM is set up in single-loop 0-delay mode to create a SYSREF signal for each ADC, which is phase-aligned to the SYSREF input (see Section 3.1 for details). This setting also generates phase-aligned device clocks for each ADC. The LMK04828 EVM acts as a frequency and phase reference for each ADC12J4000 EVM. Each ADC12J4000 EVM generates its own clocks from this reference.

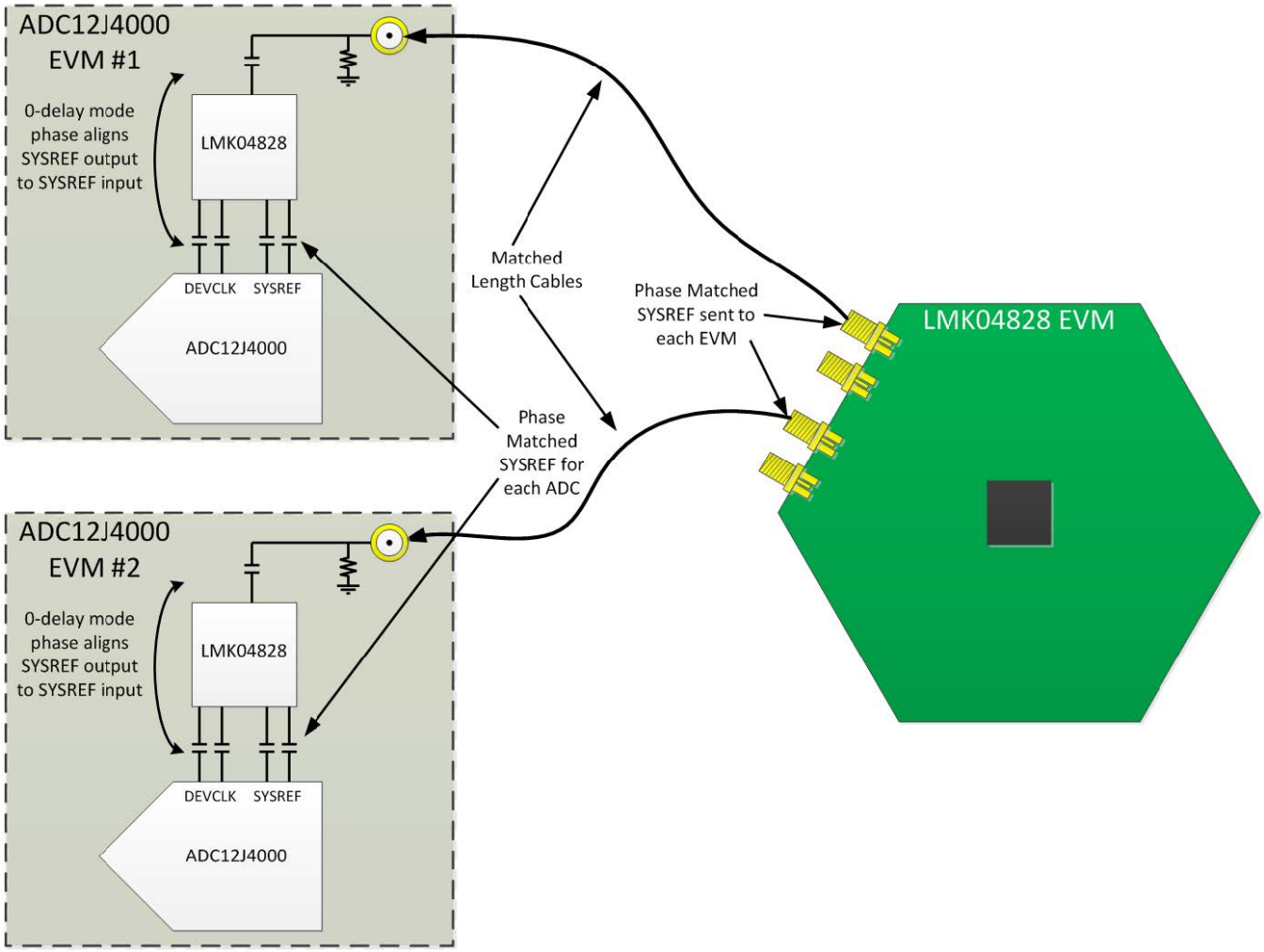

Figure 2. Block Diagram of Clocking Scheme

The following ADC12J4000 setup is for testing:

- JESD mode: Decimate-by-10, DDR = 1, P54 = 0, LMF = 2,2,2
- K = 16
- Fs = 2949.12 Msps

NOTE: The design can be modified for all of the other available ADC12J4000 modes or for other sampling rates.

2 Circuit Description

This system-level design shows how two ADC12J4000 EVMs can be synchronized together using a Xilinx VC707 platform. The design document describes the required hardware modifications and device configurations, including the clocking scheme. The design document also shows example configuration files for each EVM, describes FPGA firmware, and shows the relevant Xilinx IP block configuration parameters. Data on the actual hardware is displayed and analyzed. This data displays synchronization within 50 ps without characterized cables or calibrated propagation delays.

3 Hardware Configuration

The VC707 and LMK04828 EVMs must remain configured as defaults, but the ADC12J4000 EVM must be modified to accommodate the clocking solution.

3.1 ADC12J4000 EVM Setup

Figure 3 shows a block diagram for the setup of the ADC12J4000 EVM. The LMK04828 provides both the device clock and SYSREF signals to the ADC12J4000. The LMK04828 EVM is set up in single PLL 0-delay mode, which phase-locks the SYSREF signal of the the ADCs with the SYSREF reference signal provided to the SMA connector (labeled LMKCLK). This mode creates a phase-locked SYSREF and device clocks for each ADC on the separate ADC12J4000 EVMs.

For this clocking mode, modify the ADC12J4000 EVM so the onboard LMK04828 EVM can provide the device clock to the ADC12J4000. Modify the ADC12J4000 EVM by removing C32 and C33 and installing C262 and C263. For single-loop 0-delay mode, install C85 and C86 to apply the reference SYSREF signal to the OSCin+ pin of the LMK04828 EVM.

Due to the low-PFD frequency in this mode, modify the loop filter for PLL2 to stabilize the loop. Remove the installed components for LF1, LF2, and LF3. Install 12 nF, 0.22 nF, and 1 kΩ, respectively.

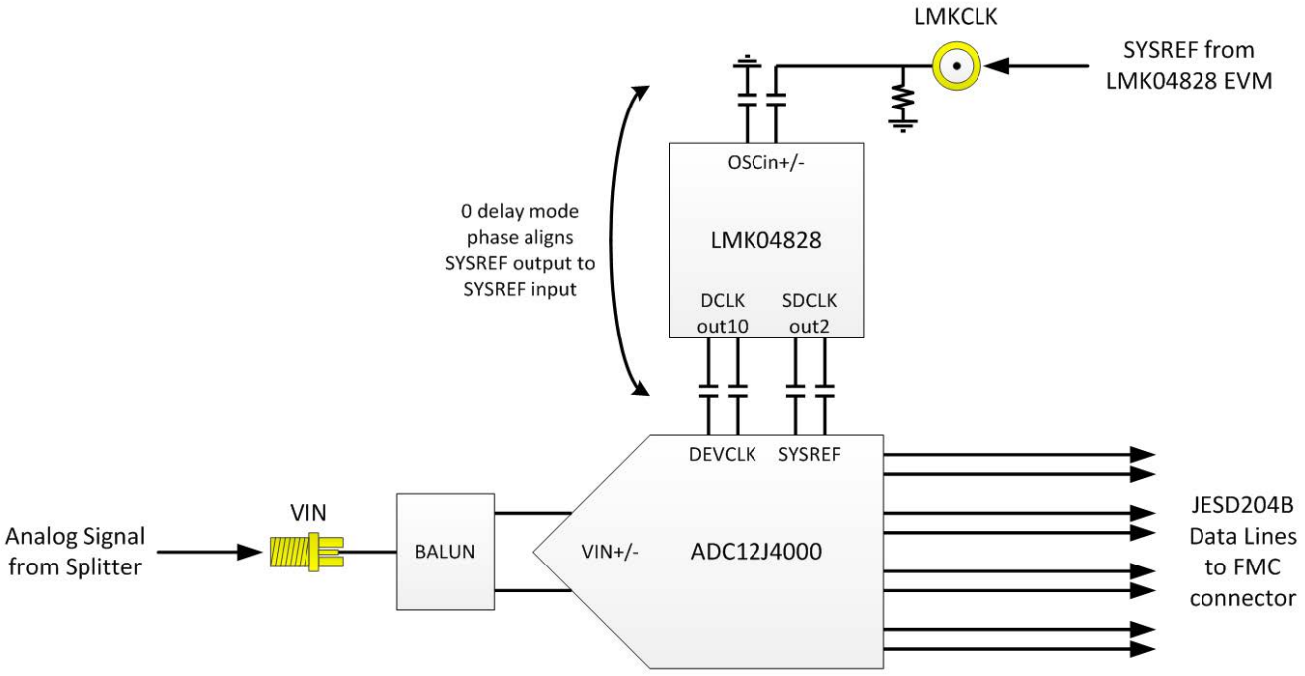

Figure 3. ADC12J4000 EVM Block Diagram

3.2 LMK04828 EVM Setup

The LMK04828 EVM must remain unmodified.

3.3 VC707 Development Kit

The VC707 Development Kit must remain unmodified.

4 Device Configurations

The specific device configurations for each board are presented in the following subsections.

4.1 ADC12J4000 EVM

The following devices must be configured on the ADC12J4000:

- The ADC
- The LMK04828

NOTE: The TRF3765 is unused in this clocking scheme and can be powered down.

For the test, the ADC12J4000 EVM was set up for decimate-by-10 using two SerDes lanes (Decimate-by-10, DDR = 1, P54 = 0, LMF = 2,2,2). For synchronization, the SYSREF receiver was enabled. The SYSREF timing was adjusted using the dirty SYSREF capture bit to detect timing errors and then using the programmable delays to meet setup and hold times. Both ADC12J4000s were loaded with the same configuration. An example configuration file for the ADC12J4000 GUI is in Section A.1.

The LMK04828 must be set up for single-loop 0-delay mode. Figure 4 shows a block diagram of the configuration. In this mode, only PLL2 is used (PLL1 can be disabled). The reference signal provided to the OSCin pin is the SYSREF signal from the LMK04828 EVM. Both R and N dividers are set to 1. By tracing the signal from the phase detector through the N divider, the VCO frequency is the reference frequency multiplied by the SYSREF divider. Because the output of the SYSREF divider is the feedback signal and both R and N dividers are set to 1, the phase detector forces the phase of the SYSREF divider output to match the phase of the reference signal.

The onboard LMK04828EVM also generates the device clock for the ADC12J4000. In this case, the device clock runs at 2949.12 MHz (the same frequency as the VCO). The LMK04828 from one of the boards also sends a device clock and SYSREF signal back to the FPGA through the FMC connector and each ADC board sends a reference clock to the related FPGA transceiver blocks (see Section 3.3). Figure 4 shows the output dividers.

Using the part in the nested 0-delay dual-loop mode with an external VCXO, improved phase-noise performance can be achieved. The higher-PFD frequency offered by the dual-loop mode improves the phase-noise performance but an external VCXO cannot be used based on the EVM hardware.

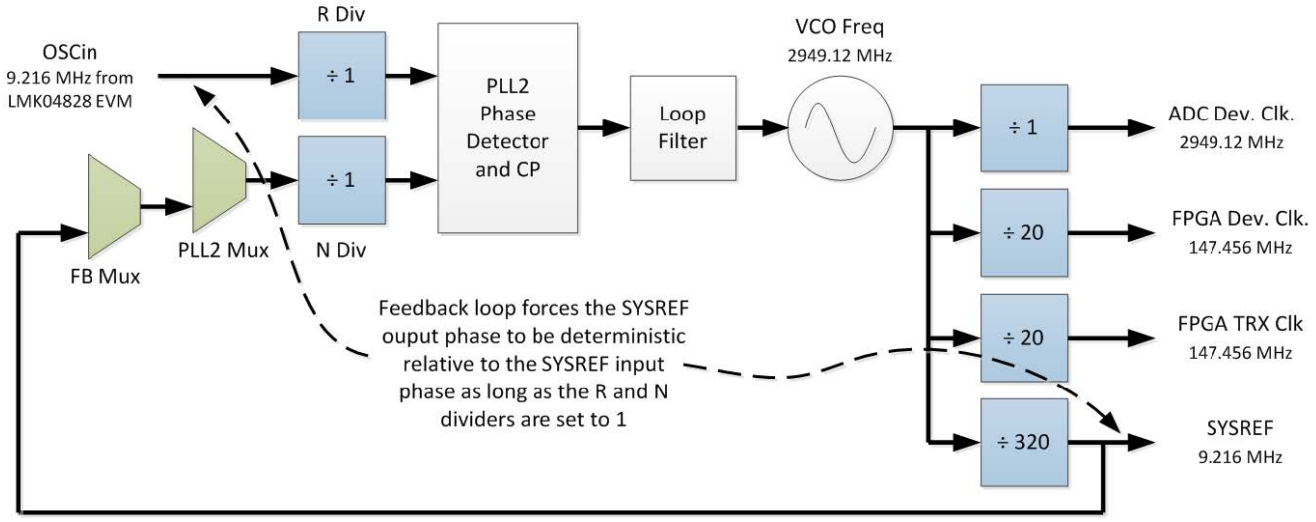

Figure 4. LMK04828 in Single-Loop 0-Delay Mode

The phases of the local multiframe clocks (LMFCs) between the ADCs and the FPGAs were not matched. Strict phase-matching of the LMFCs between the data converter and logic element is not required in many cases. When the digital downconverter (DDC) is used, the timing of the SYNC signal becomes critical because the start of the transmission of the initial lane-alignment sequence (ILAS) is for synchronization. In this case, all ADCs must transmit the ILAS on the same LMFC edge. This transmission is dependent on the SYNC signals meeting the required setup time with respect to the LMFC in the ADC. Because the SYNC signal is launched from the FPGA on an LMFC edge, the timing of the respective LMFCs is critical. The timing of the LMFCs is sufficient to synchronize the DDCs without adjusting the LMFC cycles.

4.2 LMK04828 EVM

The LMK04828 EVM is configured for dual-loop mode. The only clocks required for this setup are two phase-matched SYSREF clocks used as references for the ADC12J4000 EVMs. Alternatively, a signal generator could provide these clocks through a phase-matched power splitter. Any phase error between these clocks results in skewed-sampling instances in the ADCs. See an example configuration file for the LMK04828 EVM in Section A.2.

4.3 VC707

The firmware for the VC707 platform is a modified version of the design firmware of the hardware demonstration provided by Xilinx for the VC709 platform. Figure 5 shows a simplified block diagram of the firmware.

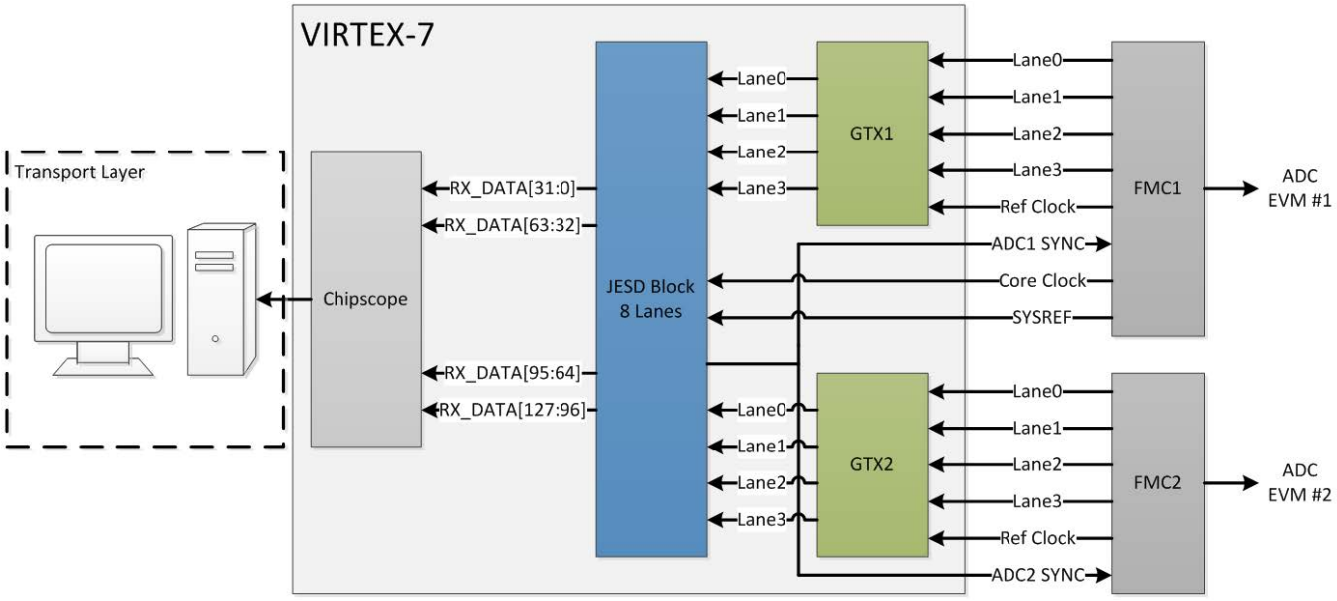

Figure 5. Block Diagram of the VC707 Firmware

4.3.1 Pin Assignments

Because this design uses of two FMC connectors, the appropriate signals for the second FMC connector require mapping. Each FMC connector has separate GT transceiver blocks. Each transceiver block receives its reference clock from the related FMC connector. The JESD-core clock and SYSREF signals come from the first FMC connector. See Table 1 and Table 2 for the signal mappings between the ADC EVM and the VC707 platform for FMC1 and FMC2, respectively. The serial lanes have inverted polarity that must be accounted for in the FPGA.

Table 1. FMC1 Signals for ADC EVM 1

Signal Name	ADC12J4000 Pins	LMK04828 Pins	FMC Pins	Virtex 7 Pins
Lane0+	DS0+		C7	D7
Lane0–	DS0–		C6	D8
Lane1+	DS1+		A3	C5
Lane1–	DS1–		A2	C6
SYNC	$\overline{\text{SYNC}}$		H31	L29
GT Ref Clk 1+		DCLKout4+	D4	A10
GT Ref Clk 1–		DCLKout4–	D5	A9
Core Clock+		DCLKout0+	G6	K39
Core Clock–		DCLKout0–	G7	K40
SYSREF+		SDCLKout3+	G9	M42
SYSREF–		SDCLKout3–	G10	L42

Table 2. FMC2 Signals for ADC EVM 2

Signal Name	ADC12J4000 Pins	LMK04828 Pins	FMC Pins	Virtex 7 Pins
Lane0+	DS0+		C7	P7
Lane0–	DS0–		C6	P8
Lane1+	DS1+		A3	N5
Lane1–	DS1–		A2	N6
SYNC	$\overline{\text{SYNC}}$		H31	V35
GT Ref Clk 2+		DCLKout4+	D4	K8
GT Ref Clk 2–		DCLKout4–	D5	K7

4.3.2 JESD Core Implementation

This design uses a single-JESD core implementation that must be modified for the appropriate LMFS configuration. The JESD core is set up for eight lanes (L = 8), although only two lanes from each ADC are used. In this case, the additional four lanes of the FPGA block output zeroes. Table 3 lists the JESD core parameters.

Table 3. Xilinx JESD Core Parameters

Parameter	Value
L	8 (extra 4 lanes ignored)
M	Unimportant, because transport layer is done in software
F	2
K	16
Scrambling	Enabled

Alternatively, the core can be set up for four lanes or as separate 2-lane cores. If using the DDC, the two SYNC signals from the separate JESD blocks must be ANDed together to create a single SYNC signal for distribution to both ADCs to synchronize the NCOs.

The transport layer is implemented in software, rather than firmware, to allow simple changes without recompiling. The data coming out of the JESD block is captured using an integrated logic analyzer (ILA) block and captured using the Xilinx ChipScope™software. The raw lane data was downloaded to the computer and remapped into samples using MATLAB. The example program is shown in Section A.3.

4.3.3 Transceiver Setup

The eight transceivers (only four used) are set up as two separate GT transceiver blocks, each with its own reference clock. The line rate is 5.89824 Gbps and the reference clock is 147.456 MHz. Each transceiver block is dedicated to an FMC connector with the reference clock for each block coming from its own FCM connector. Table 4 shows the transceiver properties for this setup.

Table 4. Transceiver Setup

PARAMETER	SETTING
Protocol File	JESD204
RX Line Rate (Gbps)	5.89824
RX Reference Clock (MHz)	147.456
Decoding	8B/10B
RX Internal Data Width	40
RX External Data Width	32
RXUSRCLK(MHz)	147.456
RXUSRCLK2(MHz)	147.456
RX Buffer Enabled	TRUE

5 Verification and Measured Performance

The performance of the system? sine waves? was/were measured by providing the same analog signal to each ADC using a phase-matched power splitter. Only sine waves were tested. The performance of the system was evaluated by calculating the phase difference between signals captured from each ADC. Because sine waves were used, the phase difference was measured by comparing the phases of the signals using an FFT and converting to a time value. The complex mixer was enabled at different frequencies to show that the NCOs were also synchronized. The data was captured by ChipScope and exported to a spreadsheet using the following TCL command:

write_hw_ila_data my_hw_ila_data_file.zip [upload_hw_ila_data hw_ila_1] –force

This command saves the data in a zip file which contains a file (waveform.csv). This CSV file was opened in MATLAB™ and the data streams representing the I data from each ADC was extracted. The data from this CSV file represents the output directly from the JESD block. Figure 5 shows these frames of data as RX_DATA streams. A MATLAB script, which acted as the transport layer, reassembled the data into samples. By taking a FFT of each signal, finding the largest bin, and comparing the phase, the phase shift was analyzed. An example of the MATLAB script is included in the appendices.

Table 5 reports the measured skews between the two ADCs and Figure 6, Figure 7, and Figure 8 show the time domain view of the captured samples. Skews can come from phase differences between either the sampling clock or the analog input. The cables in the setup were neither characterized or phase matched. The phase matching of the splitters remains unverified. Sampling clock skews can come from the cables between the LMK04828EVM and the ADC12J4000EVMs or from mismatches in the onboard LMK04828-clock chips. Analog-input skews can be from the short cables between the splitter and the analog inputs, from the splitter itself, or from phase mismatches between the onboard baluns. A different splitter measured at 2140 MHz. Because all skews are significantly smaller than a sampling clock period, the deterministic latency was achieved and the ADCs synchronized.

Table 5. Uncalibrated Skew Results

Input Frequency (MHz)	NCO Frequency (MHz)	Phase Skew (Degrees)	Time Skew (PS)
70	0	0.506	20.09
500	430	7.709	42.8
2140	2070	9.406	12.2

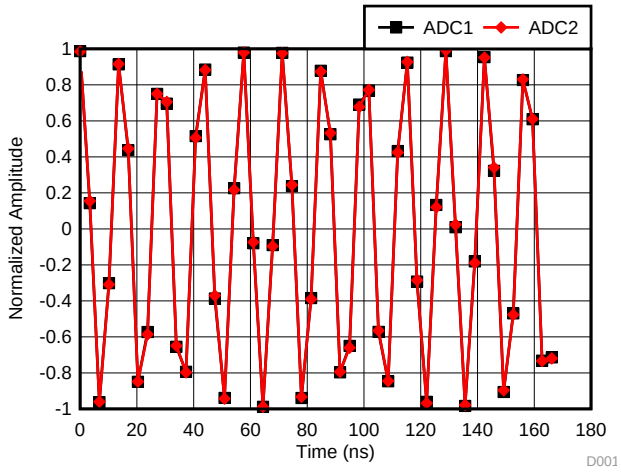

Figure 6. Sampled Signals at 70 MHz With Complex Mixer Disabled (NCO Frequency = 0)

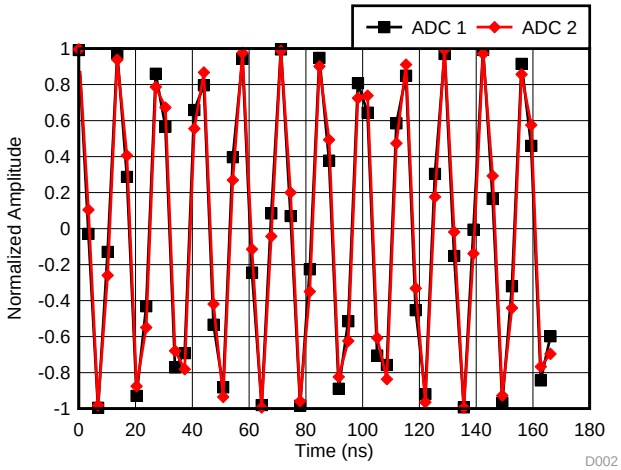

Figure 7. Sampled Signals at 500 MHz With Complex Mixer Enabled (NCO Frequency = 430 MHz)

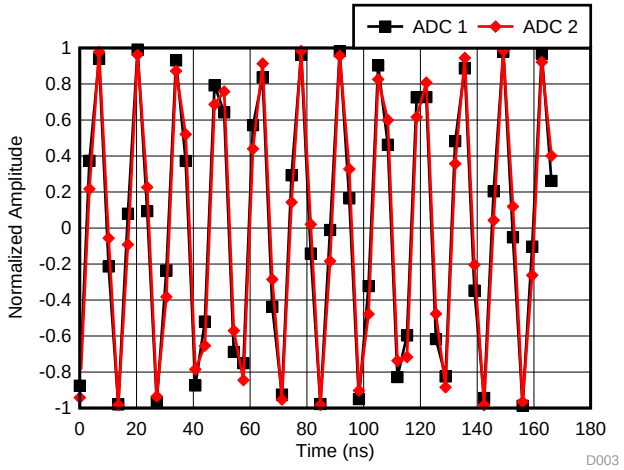

Figure 8. Sampled Signals at 2140 MHz With Complex Mixer Enabled (NCO Frequency = 2070 MHz)

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-00432.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00432.

6.3 Layer Plots

To download the layer plots, see the design files at TIDA-00432.

6.4 Altium Project

To download the Altium project files, see the design files at TIDA-00432.

6.5 Layout Guidelines

To download the Layout Guidelines, see the design files at TIDA-00432.

6.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00432.

6.7 Software Files

To download the software files, see the design files at TIDA-00432.

Appendix A Example Files

A.1 Example ADC12J4000EVM Configuration File

LMK04828
0x000 0x80
0x000 0x00
0x002 0x00
0x100 0x14
0x101 0x55
0x103 0x00
0x104 0x02
0x105 0x01
0x106 0x70
0x107 0x01
0x108 0x0A
0x109 0x55
0x10B 0x02
0x10C 0x22
0x10D 0x00
0x10E 0xF0
0x10F 0x10
0x110 0x14
0x111 0x55
0x113 0x00
0x114 0x02
0x115 0x01
0x116 0xF1
0x117 0x01
0x118 0x08
0x119 0x55
0x11B 0x00
0x11C 0x02
0x11D 0x00
0x11E 0xF9
0x11F 0x00
0x120 0x08
0x121 0x55
0x123 0x00
0x124 0x22
0x125 0x00
0x126 0xF8
0x127 0x00
0x128 0x01
0x129 0x55
0x12B 0x01
0x12C 0x22
0x12D 0x00
0x12E 0xF0
0x12F 0x11
0x130 0x18
0x131 0x55
0x133 0x01
0x134 0x22
0x135 0x00
0x136 0xF9
0x137 0x00
0x138 0x20
0x139 0x03

```
0x13A 0x01
0x13B 0x40
0x13C 0x00
0x13D 0x08
0x13E 0x03
0x13F 0x15
0x140 0x00
0x141 0x00
0x142 0x08
0x143 0x11
0x144 0xFF
0x145 0x00
0x146 0x00
0x147 0x00
0x148 0x02
0x149 0x02
0x14A 0x02
0x14B 0x02
0x14C 0x00
0x14D 0x00
0x14E 0x00
0x14F 0x7F
0x150 0x01
0x151 0x02
0x152 0x00
0x153 0x00
0x154 0x78
0x155 0x00
0x156 0x78
0x157 0x00
0x158 0x78
0x159 0x00
0x15A 0x78
0x15B 0xF4
0x15C 0x20
0x15D 0x00
0x15E 0x00
0x15F 0x0B
0x160 0x00
0x161 0x01
0x162 0x80
0x163 0x00
0x164 0x00
0x165 0x50
0x17C 0x15
0x17D 0x33
0x166 0x00
0x167 0x00
0x168 0x01
0x169 0x58
0x16A 0x20
0x16B 0x00
0x16C 0x00
0x16D 0x00
0x16E 0x13
0x139 0x00 // Set SYSREF_Mux to "Normal"
0x143 0x11 // Set SYNC_MUX to "Pin"
0x140 0x00 // Turn on all the SYSREF blocks
0x144 0x74 // Enable syncing of all clock outputs
0x143 0x11 // Trigger SYNC event using "Pin" mode
```

0x143 0x31
0x143 0x11
0x144 0xFF // Disable syncing of all clock outputs
0x139 0x03 // Set SYSREF_MUX to "Continuous"
ADC12J4000
0x0021 0x00 // Initiate reset of all registers
0x0021 0x01 // De-assert reset
0x0030 0x00 // SYSREF receiver and processor off
0x0040 0x04 // Set serializer pre-emphasis for high speed PCB
0x0066 0x03 // Foreground calibration mode with timing optimization enabled
0x002B 0x13 // Change reserved register to proper setting
0x0208 0x07 // Change over-range processing to longest interval
0x0051 0x84 // Calibration optimized for large signals
0x0201 0xBE // Scrambler on, KM1 = 15, DDR, JESD disabled
0x0200 0x14 // 6.02dB gain, decimate-by-10
0x0202 0x40 // P54 PLL off, Differential SYNC, Normal data mode
0x0030 0xC0 // SYSREF receiver and processor on
0x0210 0x00 // Set NCO Preset 0 to 0
0x0211 0x00
0x0212 0x00
0x0213 0x00
0x0201 0xBF // Scrambler on, KM1 = 15, DDR, JESD enabled
0x0050 0x0E // Initiate a foreground calibration

A.2 Example LMK04828EVM Configuration File

[SETUP]
ADDRESS=888
CLOCK=8
DATA=4
LE=2
PART=LMK04828B
PINPOSITION00=1
PINPOSITION01=10
PINPOSITION02=5
PINPOSITION03=6
PINPOSITION04=7
[MODES]
NAME00=R0 (INIT)
VALUE00=144
NAME01=R0
VALUE01=16
NAME02=R2
VALUE02=512
NAME03=R256
VALUE03=65539
NAME04=R257
VALUE04=65877
NAME05=R259
VALUE05=66305
NAME06=R260
VALUE06=66594
NAME07=R261
VALUE07=66816
NAME08=R262
VALUE08=67312
NAME09=R263
VALUE09=67408
NAME10=R264
VALUE10=67587

```
NAME11=R265
VALUE11=67925
NAME12=R267
VALUE12=68353
NAME13=R268
VALUE13=68642
NAME14=R269
VALUE14=68864
NAME15=R270
VALUE15=69360
NAME16=R271
VALUE16=69456
NAME17=R272
VALUE17=69640
NAME18=R273
VALUE18=69973
NAME19=R275
VALUE19=70400
NAME20=R276
VALUE20=70658
NAME21=R277
VALUE21=70912
NAME22=R278
VALUE22=71417
NAME23=R279
VALUE23=71424
NAME24=R280
VALUE24=71704
NAME25=R281
VALUE25=72021
NAME26=R283
VALUE26=72448
NAME27=R284
VALUE27=72706
NAME28=R285
VALUE28=72960
NAME29=R286
VALUE29=73465
NAME30=R287
VALUE30=73472
NAME31=R288
VALUE31=73736
NAME32=R289
VALUE32=74069
NAME33=R291
VALUE33=74496
NAME34=R292
VALUE34=74754
NAME35=R293
VALUE35=75008
NAME36=R294
VALUE36=75513
NAME37=R295
VALUE37=75520
NAME38=R296
VALUE38=75784
NAME39=R297
VALUE39=76117
NAME40=R299
VALUE40=76544
```

```
NAME41=R300
VALUE41=76834
NAME42=R301
VALUE42=77056
NAME43=R302
VALUE43=77553
NAME44=R303
VALUE44=77584
NAME45=R304
VALUE45=77830
NAME46=R305
VALUE46=78165
NAME47=R307
VALUE47=78592
NAME48=R308
VALUE48=78850
NAME49=R309
VALUE49=79104
NAME50=R310
VALUE50=79609
NAME51=R311
VALUE51=79616
NAME52=R312
VALUE52=79909
NAME53=R313
VALUE53=80131
NAME54=R314
VALUE54=80385
NAME55=R315
VALUE55=80704
NAME56=R316
VALUE56=80896
NAME57=R317
VALUE57=81160
NAME58=R318
VALUE58=81411
NAME59=R319
VALUE59=81664
NAME60=R320
VALUE60=81922
NAME61=R321
VALUE61=82176
NAME62=R322
VALUE62=82432
NAME63=R323
VALUE63=82705
NAME64=R324
VALUE64=83199
NAME65=R325
VALUE65=83327
NAME66=R326
VALUE66=83480
NAME67=R327
VALUE67=83738
NAME68=R328
VALUE68=83970
NAME69=R329
VALUE69=84290
NAME70=R330
VALUE70=84482
```

NAME71=R331
VALUE71=84758
NAME72=R332
VALUE72=84992
NAME73=R333
VALUE73=85248
NAME74=R334
VALUE74=85696
NAME75=R335
VALUE75=85887
NAME76=R336
VALUE76=86019
NAME77=R337
VALUE77=86274
NAME78=R338
VALUE78=86528
NAME79=R339
VALUE79=86784
NAME80=R340
VALUE80=87160
NAME81=R341
VALUE81=87296
NAME82=R342
VALUE82=87672
NAME83=R343
VALUE83=87808
NAME84=R344
VALUE84=88214
NAME85=R345
VALUE85=88320
NAME86=R346
VALUE86=88696
NAME87=R347
VALUE87=89076
NAME88=R348
VALUE88=89120
NAME89=R349
VALUE89=89344
NAME90=R350
VALUE90=89600
NAME91=R351
VALUE91=89867
NAME92=R352
VALUE92=90112
NAME93=R353
VALUE93=90369
NAME94=R354
VALUE94=90692
NAME95=R355
VALUE95=90880
NAME96=R356
VALUE96=91136
NAME97=R357
VALUE97=91404
NAME98=R380
VALUE98=97301
NAME99=R381
VALUE99=97587
NAME100=R358
VALUE100=91648

NAME101=R359
VALUE101=91904
NAME102=R360
VALUE102=92172
NAME103=R361
VALUE103=92505
NAME104=R362
VALUE104=92704
NAME105=R363
VALUE105=92928
NAME106=R364
VALUE106=93184
NAME107=R365
VALUE107=93440
NAME108=R366
VALUE108=93715
NAME109=R371
VALUE109=94976
NAME110=R8189
VALUE110=2096384
NAME111=R8190
VALUE111=2096640
NAME112=R8191
VALUE112=2096979
OSCIN00=122.88
EXTRA_PLL_N_DIV_1_00=1
OSCIN01=122.88
EXTRA_PLL_N_DIV_1_01=1
PINS=0
[BURST]
COUNT=0

A.3 Example Matlab Program for Analyzing Skew

```
%-------------------------------------------------------%
% Import Data Saved from Chipscope                      %
%-------------------------------------------------------%

% Import the data from the Xilinx Chipscope capture. Import as a string
% rather than as a number for the routine below. Only import the columns
% that contain the I data for each board

%   data1 = RX_DATA[31:0]   % Board 1 - I data
%   data2 = RX_DATA[95:64]  % Board 2 - I data

% Declare variables for imported data

Fs = 294.912e6;
Fin = 99.93e6;
N = length(data1)*2;
num_bits = 15;

%-------------------------------------------------------%
% Transport Layer Implementation                        %
%-------------------------------------------------------%

data = char(data1);
samples_board_1 = zeros(length(data1)*2,1);
for i=1:length(data1)
    samples_board_1((i-1)*2+1) = bin2dec([data(i,25:32),data(i,17:24)]);
    samples_board_1(i*2) = bin2dec([data(i,9:16),data(i,1:8)]);
end

% Convert data to 2's complement number in Matlab and remove offset
samples_board_1 = typecast(uint16(samples_board_1),'int16');
samples_board_1 = double(samples_board_1);
samples_board_1 = samples_board_1 - mean(samples_board_1);

data = char(data2);
samples_board_2 = zeros(length(data2)*2,1);
for i=1:length(data1)
    samples_board_2((i-1)*2+1) = bin2dec([data(i,25:32),data(i,17:24)]);
    samples_board_2(i*2) = bin2dec([data(i,9:16),data(i,1:8)]);
end

% Convert data to 2's complement number in Matlab and remove offset
samples_board_2 = typecast(uint16(samples_board_2),'int16');
samples_board_2 = double(samples_board_2);
samples_board_2 = samples_board_2 - mean(samples_board_2);

%-------------------------------------------------------%
% Analyze Skew                                          %
%-------------------------------------------------------%

% Plot time domain data for each board.
figure(1)
plot(1:length(samples_board_2),samples_board_2,...
1:length(samples_board_1),samples_board_1)

% Get FFT of for each board.
```

```
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
A = 2^(num_bits-1);

figure(2)
plot(20*log10(abs(X*2/N/A)));
figure(3)
plot(20*log10(abs(Y*2/N/A)));

% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));

% Get the phase of each signal at the appropriate bin.
phase_x = angle(X(index_x));
phase_y = angle(Y(index_y));

% Calculate the phase difference and time skew.
phase_diff = phase_y - phase_x;
phase_diff_deg = phase_diff / pi * 180;
skew_ps = phase_diff / (2*pi*Fin) / 1e-12;

if(skew_ps >= 0)
    fprintf('Board2 lags Board1 by %f degrees or %f ps\n',...
    phase_diff_deg, skew_ps);
else
    fprintf('Board1 lags Board2 by %f degrees or %f ps\n',...
    -phase_diff_deg, -skew_ps);
end
```

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