Kang Hsia

TI Designs High Speed: CerTIfied Design
TSW308x Wideband Digital to RF Transmit Solution

TI Designs High Speed

TI Designs High Speed designs are analog solutions created by TI's analog experts. CerTIfied Designs offer the theory, component selection, simulation, complete PCB schematic & layout, bill of materials, measured performance, and certification testing results of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

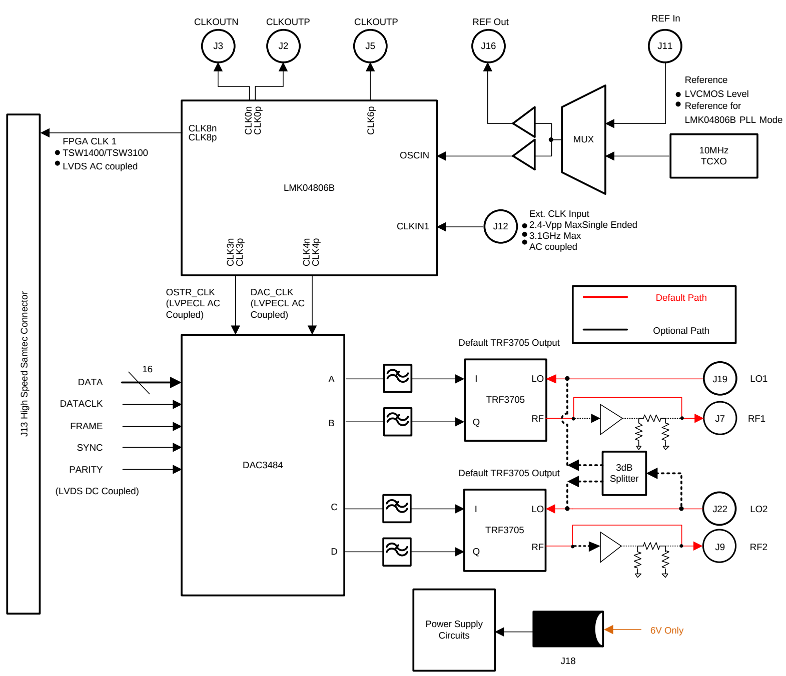
Design Zip File	Schematics and Layout Files
TSW3085EVM	Tools Folder
TSW3085 Design Package	Schematic, PCB Layout, BOM
TSW3084EVM	Tools Folder
TSW3084 Design Package	Schematic, PCB Layout, BOM
TSW30H84	Tools Folder
TSW30SH84	Tools Folder
TSW30H84, TSW30SH84 Design Package	Schematic, PCB Layout, BOM

Design Description

The TSW308X Evalutaion Module is a circuit board that allows system designers to evaluate the performance of Texas Instruments' transmit signal chain solution. This EVM includes the LMK04806B for clocking the DAC348X digital-to-analog converter (DAC), as well as a TRF3705 for up-converting the I/Q output from the DACs to an RF carrier.

TI E2E™ Community

ASK Our Analog Experts
WebBench Calculator Tools
TI Designs Precision Library



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 Introduction

1.1 Overview

The Texas Instruments TSW308x evaluation module (EVM) provides a basic platform to evaluate the DAC348x in a complete RF transmit signal chain. The TSW308x evaluation module (EVM) is a family of circuit boards that allow designers to evaluate the performance of the Texas Instruments DAC348x digital-to-analog converters (DAC). The DAC348x family consists of DAC3482, DAC3484, and DAC34H84. The 16-bit, 1.25 GSPS, DAC348x has integrated 2x/4x/8x/16x interpolation filters, 32-bit NCO, on-chip PLL, and exceptional linearity at high IFs. The EVM provides a flexible environment to test the DAC348x under a variety of clock, data input, and RF output conditions. For ease of use as a complete RF transmit solution, the TSW308xEVM includes the LMK04806B low-noise, clock generator/jitter cleaner for clocking the DAC348x and provides FPGA reference clocks to the TSW1400EVM (or TSW3100EVM). It also includes on-board TRF3705 I/Q modulators, which provide IF-to-RF upconversion for basic transmitter evaluation. This EVM is ideally suited for mating with the Texas Instruments TSW1400 pattern generation board for evaluating WCDMA, LTE, or other high performance modulation schemes.

The TSW3085 (populated with DAC3482) has one pair of I/Q channel and is designed as a single RF channel transmit solution, while the TSW3084 (populated with DAC3484) and TSW30H84 (populated with DAC34H84) have two pairs of I/Q channel and are designed for dual RF channels transmit solution. Both the TSW3085 and TSW30H84 can accept up to 625MSPS of input data rate for each I or Q channel. The TSW3084 can be considered as a lower bus width alternative for the dual RF channel while accepting up to 312.5MSPS of input data rate.

Each transmit channel of the TSW308x has the TRF3705 quadrature modulator, which follows immediately after the DAC348x as part of the signal chain. Its output ranging from 300 MHz to 4 GHz, to up-convert the I/Q outputs from the DAC to RF. The default RF signal paths is the direct TRF3705 I/Q modulator output. To add flexibility to the RF evaluation, the modulator outputs can also connect to the optional RF amplifier and programmable attenuator path to meet additional test conditions and requirements.

The EVM can be used along with TSW1400 or TSW3100 to perform a wide varieties of test and measurement. This board is also compatible with Altera® and Xilinx® FPGA development platforms for rapid evaluation and prototyping. The on-board HSMC connector input allows direct connection to the HSMC compatible Altera development platforms, and the externally attached FMC-DAC-Adapter board available from TI enables the connection of the EVM to the Xilinx development platforms with FMC headers.

Other DAC348x families can be evaluated on different EVM platforms. For details of the DAC348x family and the corresponding EVM part number, see Table 1.

Table 1. DAC348x Family

DAC Part No.	DAC3484	DAC3482	DAC34H84	DAC34SH84
EVM Part No.	TSW3084EVM	TSW3085EVM	TSW30H84EVM	TSW30SH84EVM
Output Channels	4	2	4	4
Maximum DAC Rate	1.25 GSPS	1.25 GSPS	1.25 GSPS	1.5 GSPS
Digital Interface	16-Bit LVDS Interface	16-Bit LVDS Interface	32-Bit LVDS Interface	32-Bit LVDS Interface
Maximum Data Rate per Channel	312.5 MSPS	625 MSPS	625 MSPS	750 MSPS
Maximum LVDS Bus Toggle Rate	1.25 GSPS	1.25 GSPS	1.25 GSPS	1.5 GSPS
Pattern Generator Support	TSW1400/TSW3100	TSW1400/TSW3100	TSW1400/TSW3100	TSW1400/TSW3100 with limited data rate support

See the DAC348x EVM web folders at:

- http://www.ti.com/tool/dac3482evm
- http://www.ti.com/tool/dac3484evm
- http://www.ti.com/tool/dac34h84evm
- http://www.ti.com/tool/dac34sh84evm

For evaluation of the DAC348x family with transformer coupled IF output, see the DAC348xEVM user's guide (SLAU432).

For evaluation of the TSW30SH84 with the on-board DAC34SH84, see the TSW30SH84EVM user's guide (SLAU433).

1.2 EVM Block Diagram

Figure 1 shows the TSW3084EVM block diagram, Figure 2 shows the TSW3085EVM block diagram, and Figure 3 shows the TSW30H84EVM block diagram.

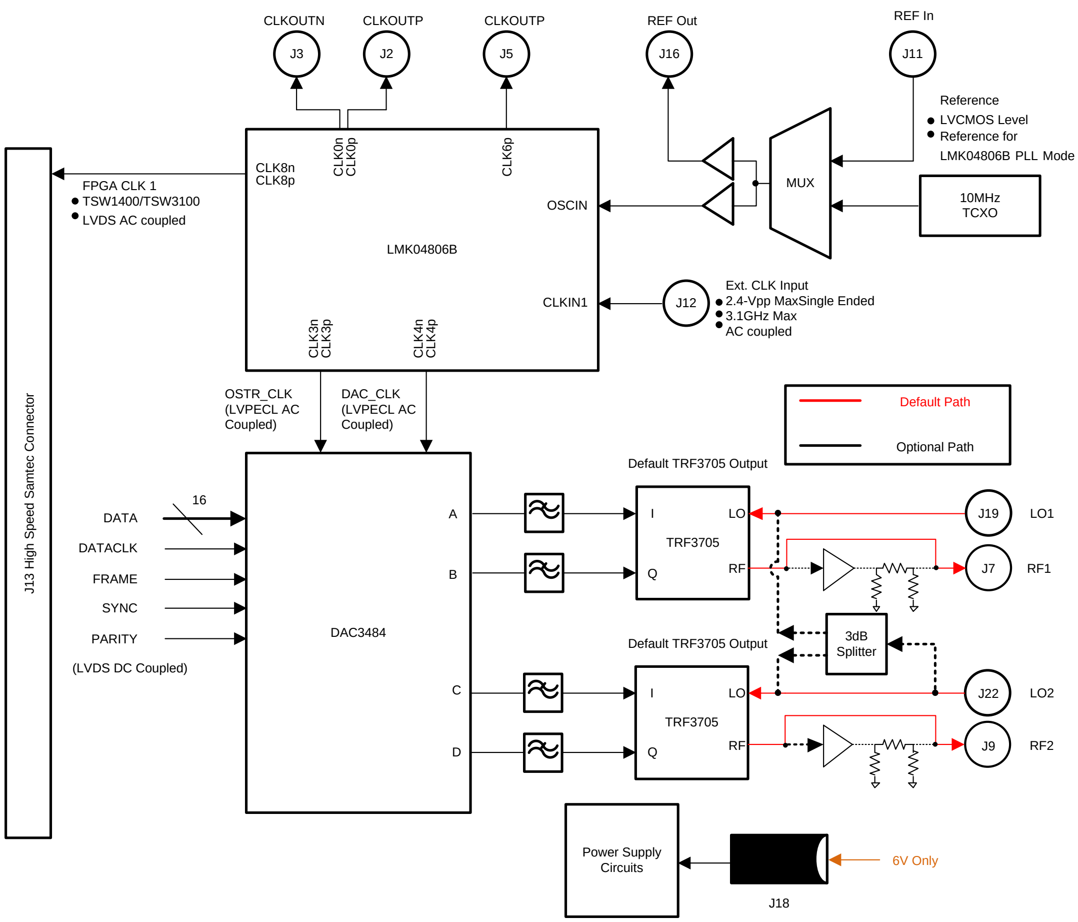


Figure 1. TSW3084EVM Block Diagram

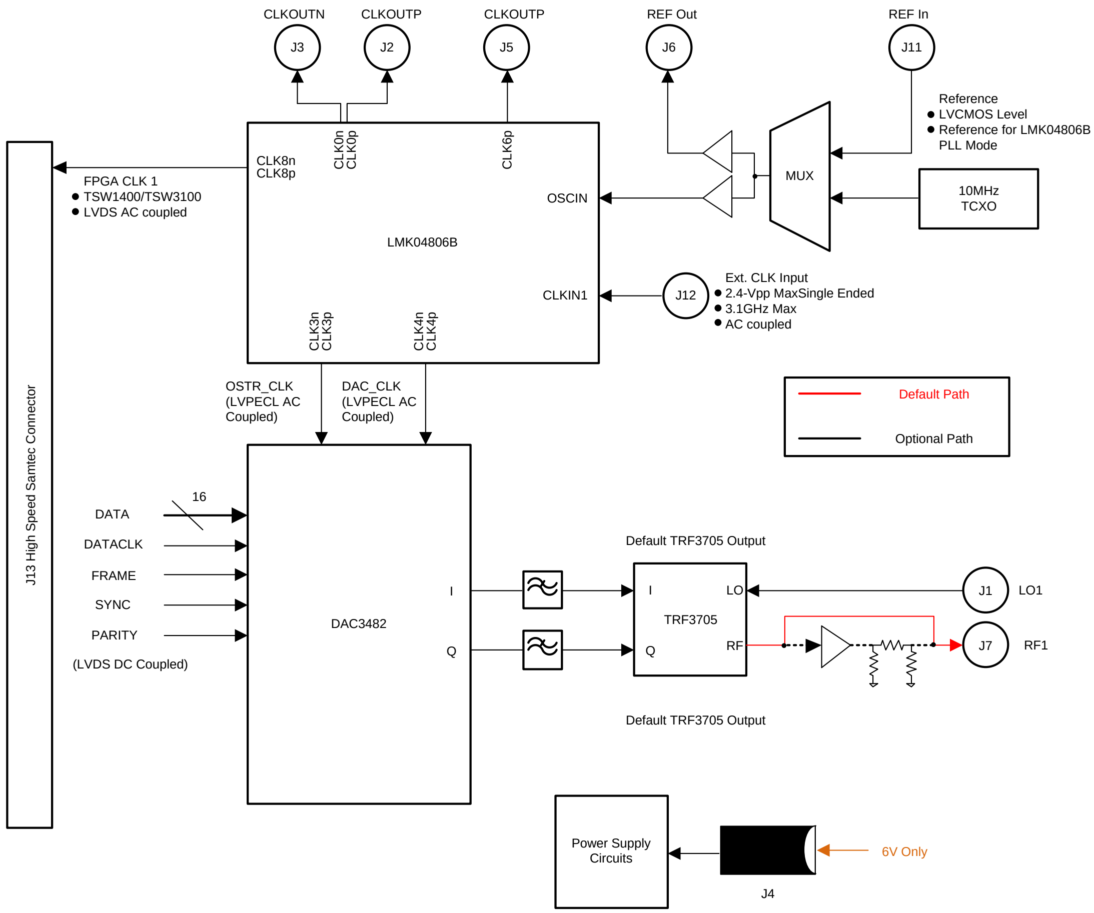


Figure 2. TSW3085EVM Block Diagram

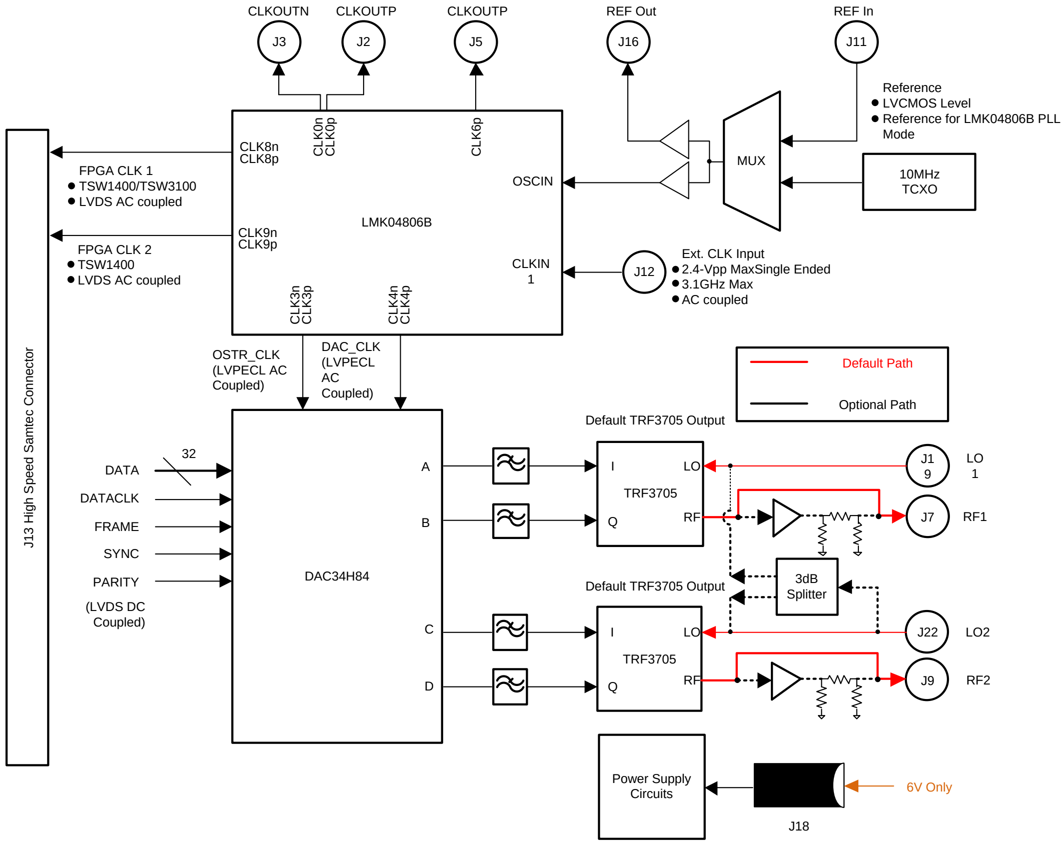


Figure 3. TSW30H84EVM Block Diagram

2 Software Control

2.1 Installation Instructions

Perform the following steps to install the software.

1. Open the folder named TSW308x_Installer_vxpx (xpx represents the latest version).
2. Run Setup.exe.
3. Follow the onscreen instructions.
4. Once installed, launch the program by clicking on the TSW308x program in Start>Programs>Texas Instruments DACs>TSW308x. For Windows XP system, the installation directory is located at C:\Program Files\Texas Instruments\TSW308x. For Windows 7 system, it is located at C:\Program Files (x86)\Texas Instruments\TSW308x
5. When plugging in the USB cable for the first time, you are prompted to install the USB drivers.
   (a) When a pop-up screen opens, select *Continue Downloading*.
   (b) Follow the onscreen instructions to install the USB drivers.
   (c) If needed, the drivers can be accessed directly in the install directory.

2.2 Software Operation

The software allows programming control of the DAC, the LMK, and the attenuator devices. The front panel provides a tab for full programming of each device. The GUI tabs provide a more convenient and simplified interface to the most used registers of each device.

Each device has its own custom control interface. At the top level of the GUI are five control tabs. The first four are used to configure the DAC348x and the last for the LMK04800. The attenuator control window on the right side of the GUI is used to program the attenuator.

2.2.1 Input Tab Control Options

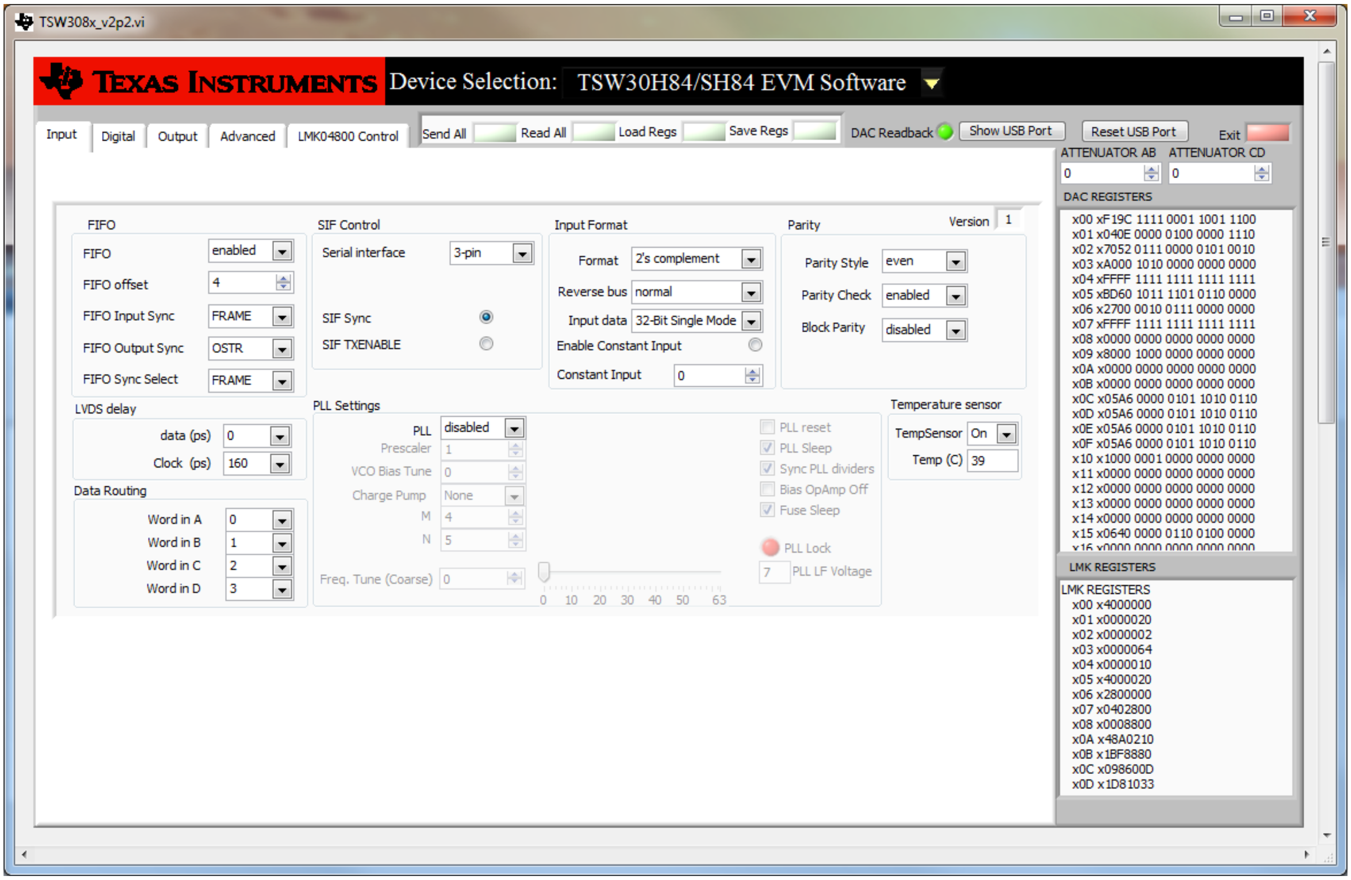


Figure 4. Input Tab Control Options – DAC348x

- FIFO: allows the configuration of the FIFO and FIFO synchronization (sync) sources.
- LVDS delay: provides internal delay of either the LVDS DATA or LVDS DATACLK to help meet the input setup/hold time.
- Data Routing: provides flexible routing of the A, B, C, and D sample input data to the appropriate digital path. **Note:** the DAC3482 does not support this mode.
- SIF Control: provides control of the Serial Interface (3-wire or 4-wire) and Serial Interface Sync (*SIF Sync*).
- Input Format: provides control of the input data format (that is, 2's complement or offset binary).
- Parity: provides configuration of the parity input.
- PLL Settings: provides configuration of the on-chip PLL circuitry.
- Temperature Sensor: provides temperature monitoring of DAC348x die temperature.

2.2.1.1 FIFO Settings

The DAC348x has 8-samples deep FIFO to relax the timing requirement of a typical transmitter system. The FIFO has an input pointer and an output pointer, and both pointers can accept various input sources as reset triggers of input and output pointer position. One important application for input and output pointer control is the ability to synchronize multiple DACs in the system. For additional information, see the relevant DAC348x data sheet.

- FIFO Offset: The default position of FIFO output pointer after reset by the synchronization source. This setting can be used to change the latency of the DAC348x.
- Data Formatter Sync (DAC3482 and DAC3484): Synchronization source for FIFO data formatter. Select between LVDS FRAME or LVDS SYNC signals.

- FIFO Sync Select (DAC34H84 and DAC34SH84): Select the internal digital routing of LVDS ISTR or LVDS SYNC to the FIFO ISTR path
- FIFO Input Sync: Synchronization source for FIFO input pointer. Select among the LVDS FRAME (ISTR), LVDS SYNC, and/or SPI register SIF-SYNC to reset the FIFO input pointer position.
- FIFO Output Sync: Synchronization source for FIFO output pointer. Select among the LVDS FRAME (ISTR), LVDS SYNC, SPI register SIF-SYNC, and/or OSTR signal to reset the FIFO output pointer position.
  - For single device application without the need for precise latency control, Single Sync Source Mode may be used. The FIFO output pointer position can be reset with LVDS FRAME (ISTR), LVDS SYNC, and/or SPI register SIF-SYNC. See the Single Sync Source Mode in the relevant DAC348x data sheet for details.
  - For multiple device synchronization, select the OSTR signal as the FIFO output synchronization source. If the DAC is configured to accept external DAC Clock input, then the OSTR signal is the external LVPECL signal to the OSTRP/N pins. If the DAC is configured to accept the internal on-chip PLL clock, then the OSTR signal is the internally generated PFD frequency. See the Dual Sync Sources Mode in the relevant DAC348x data sheet for details.

2.2.1.2 LVDS Delay Settings

Depending on the signal source implementation (that is, TSW1400, TSW3100, or FGPA system), the following options can be implemented to meet the minimum setup and hold time of DAC348x data latching:

- Set the on-chip LVDS DATACLK delay: The DAC348x includes on-chip LVDS DATA or DATACLK delay. The delay ranges from 0 ps to 280 ps with an approximate 40-ps step. This LVDS DATACLK delay does not account for additional PCB trace-to-trace delay variation, only the internal DATACLK delay. The TSW1400 and TSW3100 pattern generators send out LVDS DATA and DATACLK as edge-aligned signal. Typical setting of 160 ps or more help meet the timing requirement for most of the pattern generator and DAC348x EVM setup.
- Modify the external LVDS DATACLK PCB trace delay: Additional trace length can be added to the DATACLK P&N PCB trace length.
  - At the top side of the TSW3084, set SJP9, SJP10, SJP11, and SJP12 to the 2-3 position for approximately 2 inches (320 ps) of trace delay.
  - At the top side of the TSW3085, set SJP1, SJP6, SJP7, and SJP8 to the 2-3 position for approximately 2 inches (320 ps) of trace delay.
  - At the top side of the TSW30H84, set SJP9, SJP10, SJP11, and SJP12 to the 2-3 position for approximately 1 inches (160 ps) of trace delay.

2.2.1.3 PLL Settings

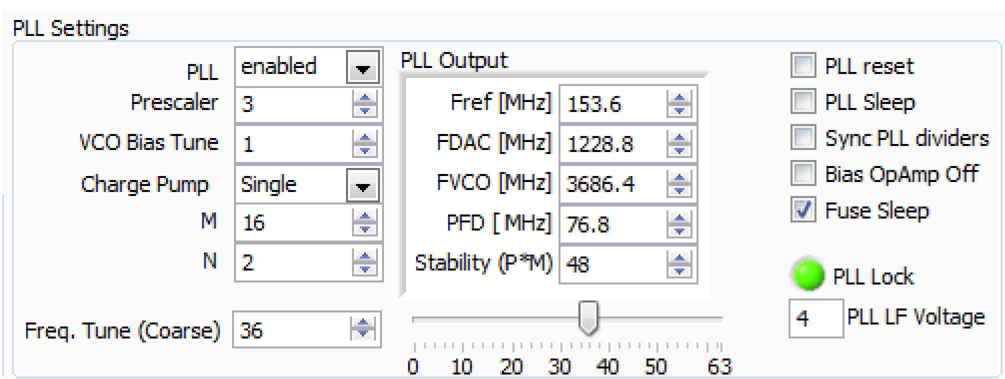


Figure 5. PLL Configuration

Perform the following steps to configure the PLL.

1. Enable PLL.
2. Uncheck *PLL reset* and *PLL sleep*.
3. Set *M* and *N* ratio such that F_{DAC} = (M)/(N) × Fref.
4. For the DAC3482, DAC3484, and DAC34H84, set the *prescaler* such that the F_{DAC} × prescaler is within 3.3 GHz and 4 GHz.
5. For the DAC34SH84, set the *prescaler* such that the F_{DAC} × prescaler is within 2.7 GHz and 3.3 GHz.
6. Set *VCO Bias Tune* to 1.
7. *Charge Pump* setting
   (a) If stability (P × M) is less than 120, then set to *Single*.
   (b) If stability (P × M) is greater than 120, then set to *Double* or install external loop filter.
8. Adjust the *Freq. Tune (Coarse)* accordingly. For additional information, see the relevant DAC348x data sheet.

2.2.2 Digital Tab Control Options

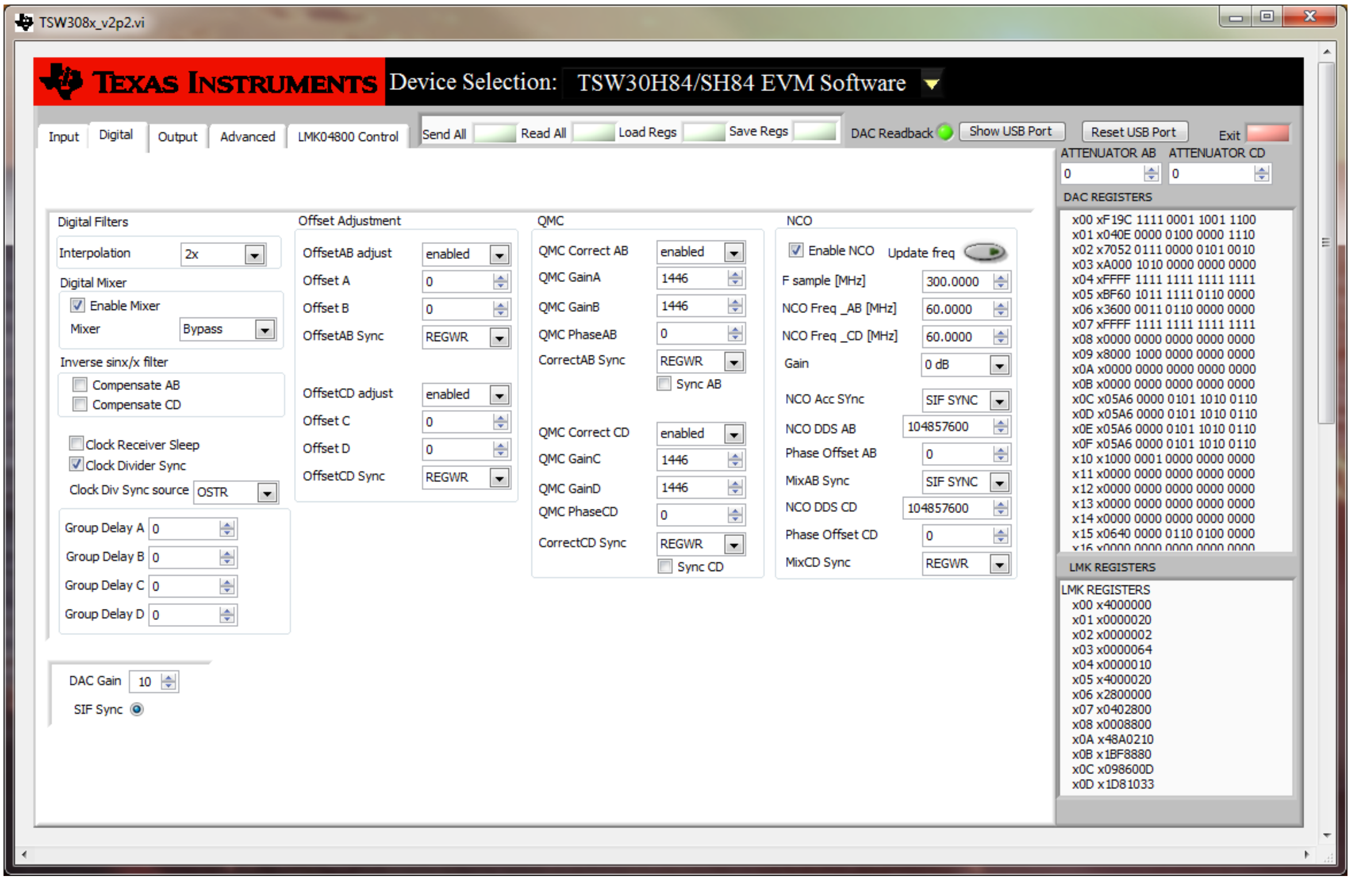


Figure 6. Digital Tab Control Options – DAC348x

- Interpolation: allows control of the data rate versus DAC sampling rate ratio (that is, data rate × interpolation = DAC sampling rate).
- Digital Mixer: allows control of the coarse mixer function.
  Note: If fine mixer (NCO) is used, the Enable Mixer button must be checked, and the coarse mixer must be bypassed. See the following NCO bullet for detail.

- Inverse sinx/x filter: allows compensation of the sinx/x attenuation of the DAC output.
  Note: If inverse sinx/x filter is used, the input data digital full-scale must be backed off accordingly to avoid digital saturation.
- Clock Receiver Sleep: allows the DAC clock receiver to be in sleep mode. The DAC has minimum power consumption in this mode.
- Clock Divider Sync: allows the synchronization of the internal divided-down clocks using either Frame, Sync, or OSTR signal. Enables the divider sync as part of the initialization procedure or resynchronization procedure.
- Group Delay: allows adjustment of group delay for each I/Q channel. This is useful for wideband sideband suppression. **Note:** This feature is not available for the DAC34SH84.
- Offset Adjustment: allows adjustment of dc offset to minimize the LO feedthrough of the modulator output. This section requires synchronization for proper operation. The synchronization options follow:
  - **REGWR: auto-sync from SIF register write. If this option is chosen, the GUI automatically synchronizes the offset adjustment with each value update by writing to 0x08 (Offset A) or 0x0A (Offset C) registers last.**
  - *OSTR*: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source.
  - *SYNC*: sync from the external LVDS SYNC signal.
  - **SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**
- QMC Adjustment: allows adjustment of the gain and phase of the I/Q channel to minimize sideband power of the modulator output.
  - **REGWR: auto-sync from SIF register write. If this option is chosen, the GUI automatically synchronizes the offset adjustment with each value update by writing to 0x10 (QMC PhaseAB) or 0x11 (QMC PhaseCD) registers last.**
  - *OSTR*: sync from the external LVPECL OSTR signal. Clock Divider Sync must be enabled with OSTR set as sync source.
  - *SYNC*: sync from the external LVDS SYNC signal.
  - **SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**
- NCO: allows fine mixing of the I/Q signal. The procedure to adjust the NCO mixing frequency follows.
  1. Enter the DAC sampling frequency in Fsample.
  2. Enter the desired mixing frequency in both NCO freq_AB and NCO freq_CD.
  3. Press Update freq.
  4. Synchronize the NCO block from the following options.
  - **REGWR: auto-sync from SIF register write. Writing to either Phase OffsetAB or Phase OffsetCD can create a sync event.**
  - *OSTR*: sync from the external LVPECL OSTR signal. Clock Divider Sync must be enabled with OSTR set as sync source. See the data sheet for OSTR period requirement.
  - *SYNC*: sync from the external SYNC signal.
  - **SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**

2.2.3 Output Tab Control Options

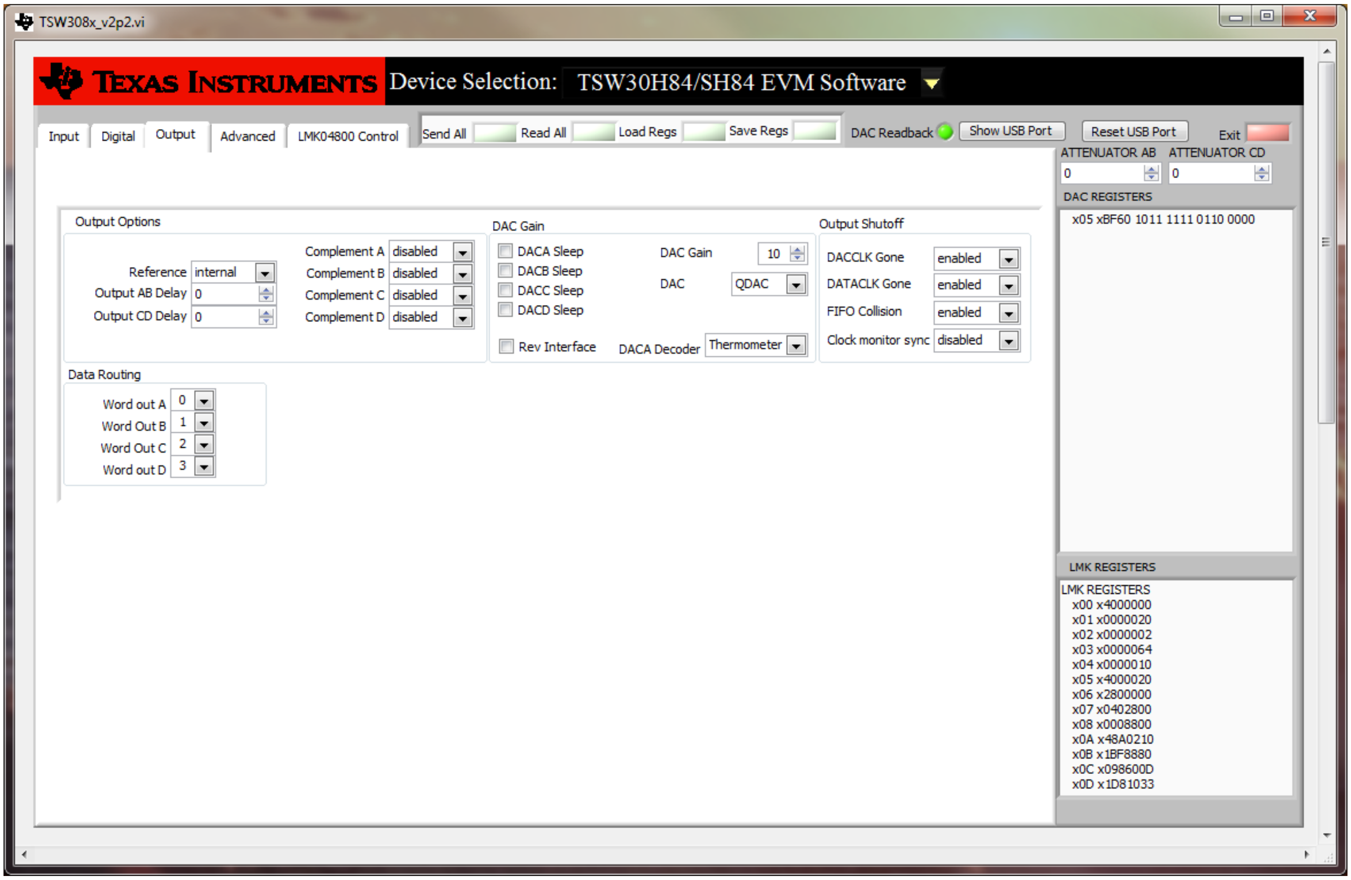


Figure 7. Output Tab Control Options – DAC348x

- Output Options: allows the configuration of reference, output polarity, and output delay
- Data Routing: provides flexible routing of the A, B, C, and D digital path to the desired output channels. **Note:** The DAC3482 does not support this mode.
- DAC Gain: configures the full-scale DAC current and DAC3484/DAC3482 mode. With Rbiasj resistor set at 1.28 kΩ:
  - DAC Gain = 15 for 30-mA, full-scale current.
  - DAC Gain = 10 for 20-mA, full-scale current (default).
- Output Shutoff On: allows outputs to shut off when DACCLK GONE, DATACLK GONE, or FIFO COLLISION alarm event occurs.

2.2.4 LMK04800

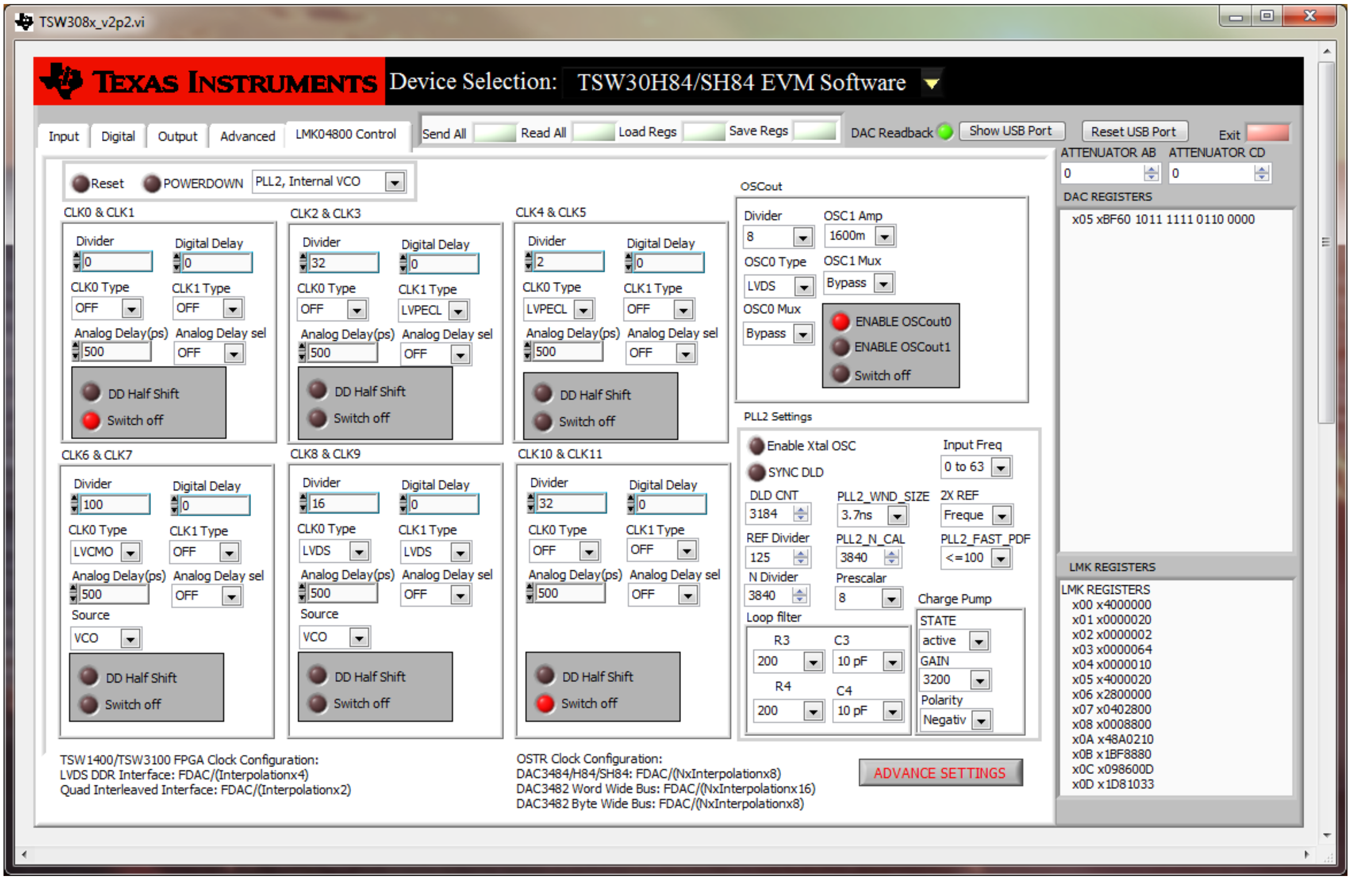


Figure 8. LMK04800 Tab Control Options

Clock control is determined by register values in the LMK04800 Control tab. The LMK04800 has 12 available output clocks. See the LMK04800 family data sheet for detailed explanations of the register configurations.

The following LMK04806 outputs are used by the TSW3084EVM:

- CLK3: DAC3484 DAC sampling clock. This clock type is AC coupled LVPECL. If the DAC3484 is configured for internal PLL mode, this becomes the reference clock input for the PLL block.
- CLK8: TSW1400/TSW3100 FPGA input clock. This clock type is AC coupled LVDS. The clock rate must be set to F_{DAC}/interpolation/2.
- CLK4: DAC3484 FIFO OSTR Clock. This clock type is AC coupled LVPECL.
  - The OSTR signal can be a slower periodic signal or a pulse depending on the application.
  - The OSTR clock rate must be at most F_{DAC}/interpolation/8. See the DAC348x data sheet for more detail.
  - The FIFO OSTR clock must be disabled when the DAC348x is using the on-chip PLL for DACCLK generation.
- CLK6: Spare output clock at SMA J5.
- CLK0: Spare output clock at SMA J2 and J3.

The following LMK04806 outputs are used by the TSW3085EVM:

- CLK3: DAC3482 DAC sampling clock. This clock type is AC coupled LVPECL. If the DAC3482 is configured for internal PLL mode, this becomes the reference clock input for the PLL block.
- CLK8: TSW1400/TSW3100 FPGA input clock. This clock type is AC coupled LVDS. The clock rate

must be set to F_{DAC}/interpolation/4.

- CLK4: DAC3482 FIFO OSTR Clock. This clock type is AC coupled LVPECL.
  - The OSTR signal can be a slower periodic signal or a pulse depending on the application.
  - The OSTR clock rate must be at most F_{DAC}/interpolation/16 for word-wide interface and F_{DAC}/interpolation/8 for byte-wide interface. See the DAC348x data sheet for more detail.
  - The FIFO OSTR clock must be disabled when the DAC348x is using the on-chip PLL for DACCLK generation.
- CLK6: Spare output clock at SMA J5.
- CLK0: Spare output clock at SMA J2 and J3.

The following LMK04806 outputs are used by the TSW30H84EVM:

- CLK4: DAC34H84 DAC sampling clock. This clock type is AC coupled LVPECL. If the DAC34H84 is configured for internal PLL mode, this becomes the reference clock input for the PLL block.
- CLK8: TSW1400/TSW3100 FPGA input clock (#1). This clock type is AC coupled LVDS. The clock rate must be set to F_{DAC}/interpolation/4.
- CLK9: TSW1400 FPGA input clock (#2). This clock type is AC coupled LVDS. It is required to evaluate the TSW30H84 and TSW30SH84 with the TSW1400. The clock rate must be set to F_{DAC}/interpolation/4.
- CLK3: DAC34H84 FIFO OSTR Clock. This clock type is AC coupled LVPECL.
  - The OSTR signal can be a slower periodic signal or a pulse depending on the application.
  - The OSTR clock rate must be at most F_{DAC}/interpolation/8. See the DAC34H84 data sheet (SLAS751) for more detail.
  - The FIFO OSTR clock must be disabled when the DAC348x is using the on-chip PLL for DACCLK generation.
- CLK6: Spare output clock at SMA J5.
- CLK0: Spare output clock at SMA J2 and J3.

The clock settings are divided into subcontrol sections. These sections allow the user to set the divide ratio, digital delay, type, analog delay, and ON/OFF control. Note that clock pairs share several settings.

The OSCout control section allows the user to configure the settings for the OSCIN input. The TSW308xEVM uses this input as the reference input for Single Loop mode of operation (default configuration). This mode uses PLL2 of the device. This reference can be provided by either the onboard 10-MHz oscillator (default) or from an external source brought in through SMA J11. For details, see Section 5.

The PLL2 Settings control section allows the user to configure the settings for the internal PLL2. The LMK04800 family contains four devices that cover internal VCO frequencies from 1840 MHz to 3072 MHz. The VCO range of the LMK04806B is 2370 MHz to 2600 MHz . The TSW308xEVM default test case uses settings to set the internal VCO to 2457.6 MHz and is locked to the 10-MHz input source on OSCIN.

The default Single Loop PLL settings provided by the example file provide a 1228.8 MHz of DAC sampling clock, the divided-down FPGA clock(s) for the TSW1400/TSW3100 pattern generator FPGA input clock, and the divided-down OSTR clock for DAC348x's OSTR input. The CLK6 (J5) is configured as a divided-by-100 CMOS clock. This can be used as part of EVM functionality verification. For details, see Section 4.5.

After the default settings are loaded, the output clocks are synchronized with the onboard 10-MHz reference oscillator as indicated by *LMK LOCK* LED(D7) being illuminated.

Clicking on the Advance Settings tab at the bottom of the GUI opens a new window allowing the user to set other internal registers for different modes of operation as shown in Figure 9.

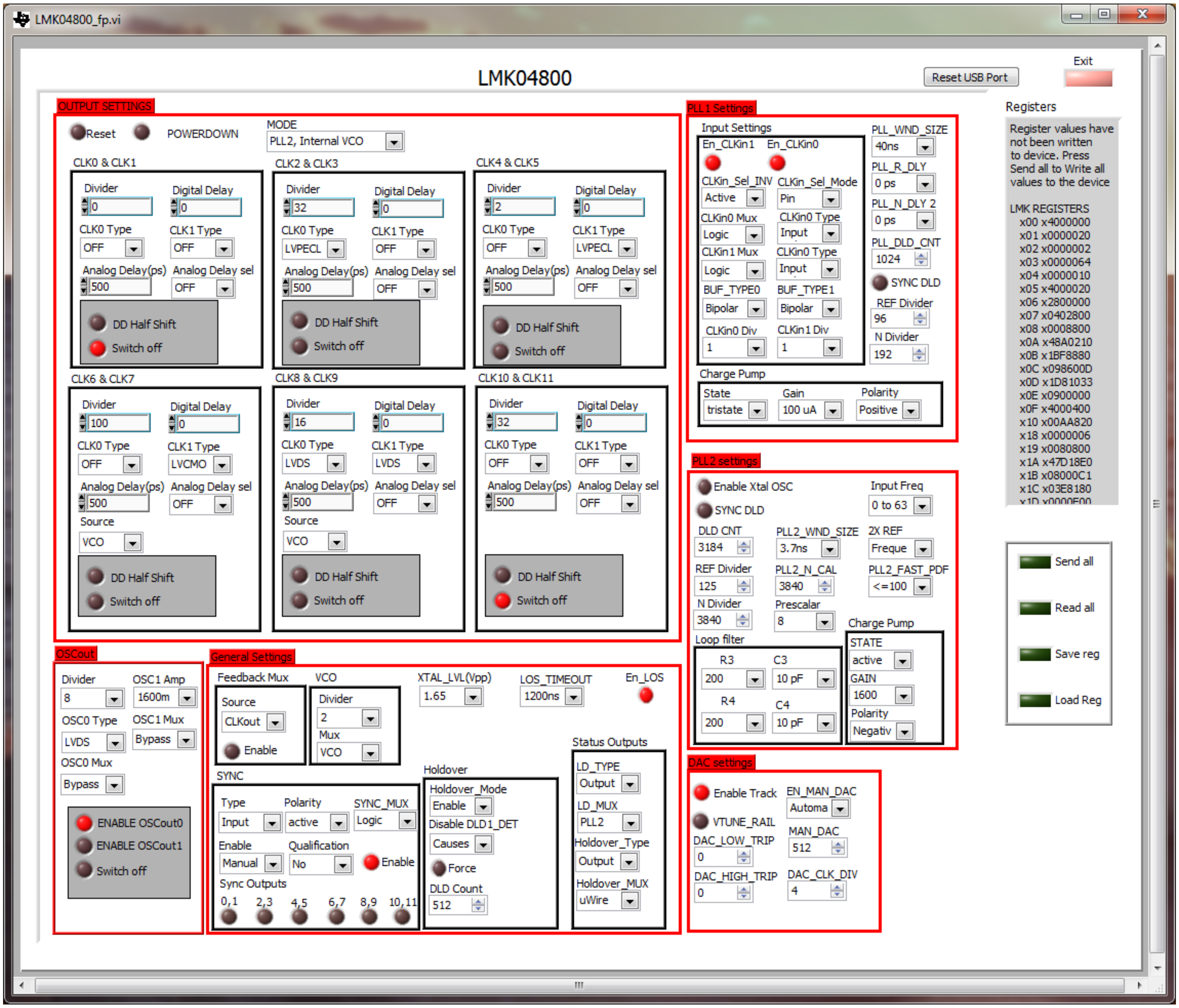


Figure 9. LMK04800 Advanced Settings Control Panel

2.2.5 Register Control

- Send All: sends the register configuration to all devices.
- Read All: reads register configuration from DAC348x and LMK04800 devices.
- Load Regs: loads a register file for all devices. For Windows XP system, example configuration files for the common frequency plan are located in the install directory: C:\Program Files\Texas Instruments\TSW308x\Configuration Files. For Windows 7 system, the files are located in the install directory: C:\Program Files (x86)\Texas Instruments\TSW308x\Configuration Files
  - Select *Load Regs* button.
  - Double-click on the *Configuration Files* folder and respective sub-folders for the EVM.
  - Double-click on the desired register file.
  - Click on *Send All* to ensure all the values are loaded properly.
- Save Regs: saves the register configuration for all devices.

2.2.6 Attenuator Control

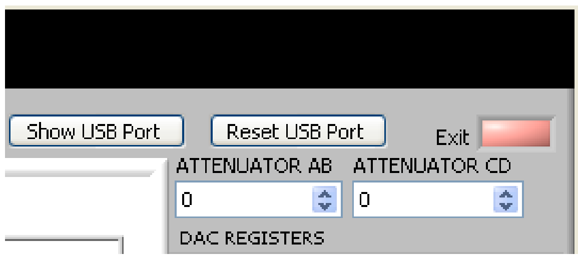


Figure 10. RF Attenuator Control

Each of the RF path on the TSW308xEVM contains a 50-Ω, RF digitally controlled attenuator that operates from DC to 4 GHz. This highly versatile digital step attenuator (DSA) covers a 0-dB to 31.75-dB attenuation range in 0.25-dB steps. It maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss (1.9 dB, typical) and low-power consumption. The user can enter a value from 0 (minimum attenuation) to 31.75 (maximum attenuation) in 0.25 increments inside the Attenuator window (Figure 10) or by clicking on the drop-up/-down arrows.

2.2.7 Miscellaneous Settings

- Reset USB: toggle this button if the USB port is not responding. This generates a new USB handle address.
  - Note: It is recommended that the board be reset after every power cycle, and the reset USB button on the GUI be clicked.

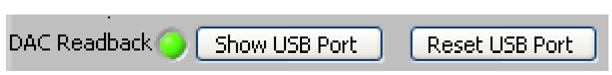


Figure 11. USB Port Reset

- Exit: stops the program

3 Basic Test Procedure with TSW1400

This section outlines the basic test procedure for testing the EVM with the TSW1400.

3.1 TSW1400 Overview

The TSW1400 is a high speed data capture and pattern generator board. When functioning as a pattern generator, it has a maximum LVDS bus rate of 1.5 GSPS, and this allows evaluation of the DAC348x and also DAC34SH84 with maximum 750 MSPS of input data rate per channel.

See the TSW1400 user's guide (SLWU079) for more detailed explanation of the TSW1400 setup and operation. This document assumes that the High Speed Data Converter Pro software (www.ti.com/tool/tsw1400evmC107) is installed and functioning properly.

3.2 Test Block Diagram for TSW1400

The test set-up for general testing of the TSW3084 and TSW30H84EVM with the TSW1400 pattern generator card is shown in Figure 12.

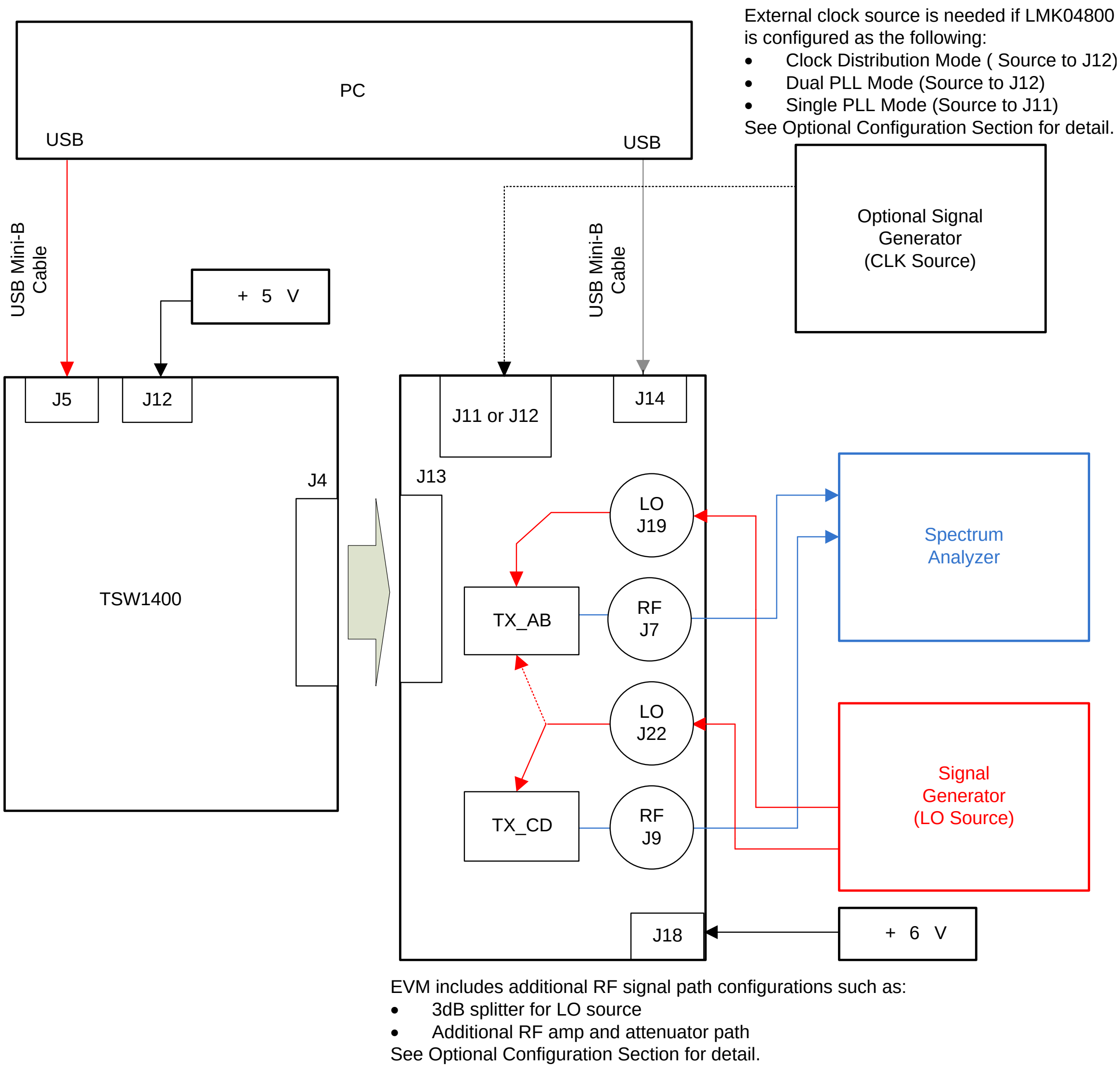


Figure 12. TSW1400 and TSW3084/TSW30H84 Test Setup Block Diagram

The test setup for general testing of the TSW3085 with the TSW1400 pattern generator is shown in Figure 13

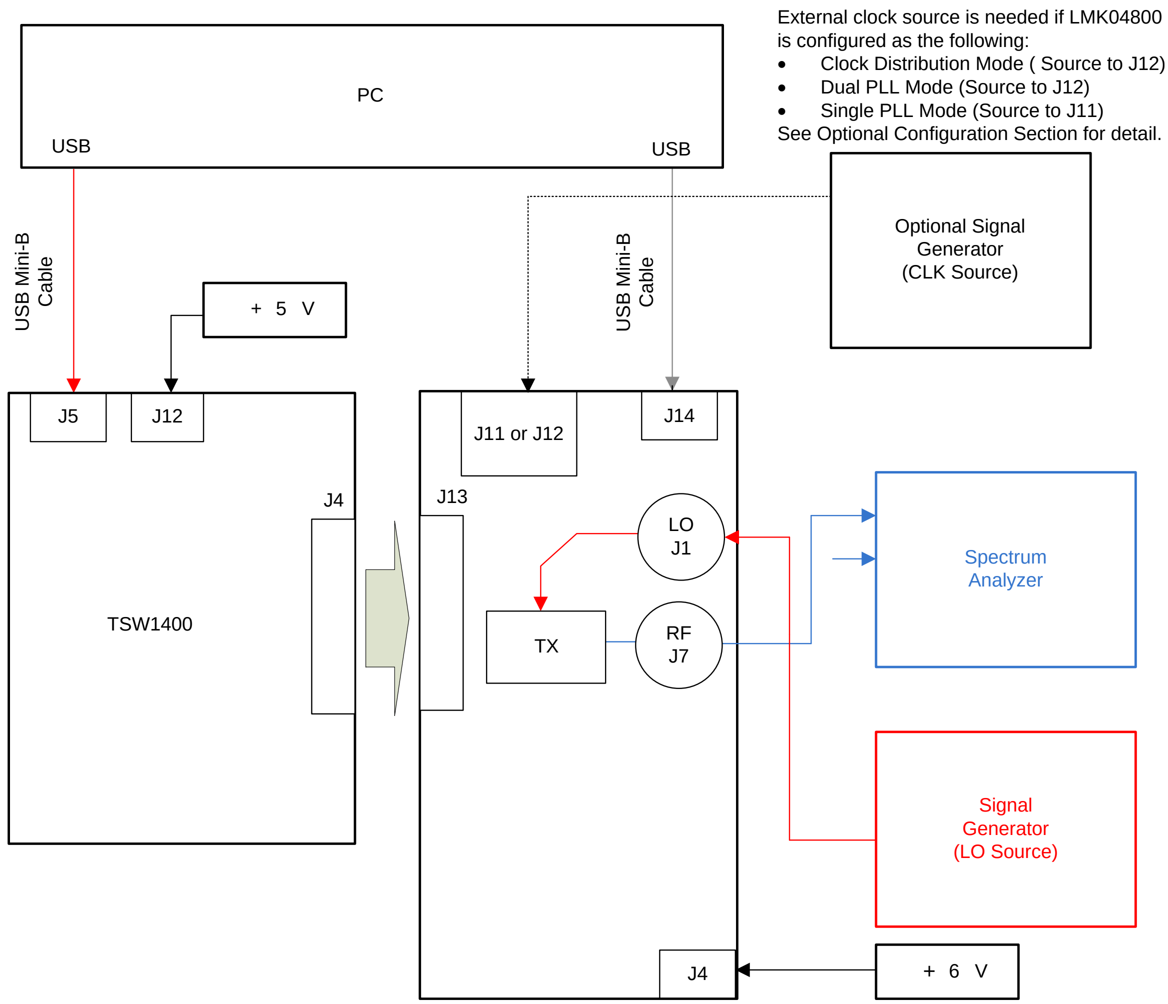


Figure 13. TSW1400 and TSW3085 Test Setup Block Diagram

3.3 Test Setup Connection

TSW1400 Pattern Generator.

1. Connect 5-V power supply to J12, *5V_IN* jack of the TSW1400 EVM.
2. Connect PC's USB port to J5 USB port of the TSW1400 EVM. The cable should be a standard A to mini-B connector cable.

TSW3084/TSW30H84 EVM

1. Connect J13 connector of TSW3084/TSW30H84 EVM to J4 connector of TSW1400 EVM.
2. Connect 6 V to the J18, *Power In* jack of the TSW3084/TSW30H84 EVM.
3. Connect PC's USB port to J14 USB port of the TSW3084/TSW30H84 EVM. The cable should be a standard A to mini-B connector cable.
4. Provide 10-dBm maximum, 300-MHz to 4-GHz LO source to connectors J19 and/or J22. The J19 or the J22 connector routes the LO source to the respective TRF3705 modulator TX path. Optionally, the EVM can be configured to share the LO source between the two TX paths through an on-board 3 dB splitter. The source should be connected to J22 in this case. See the *TX Path Optional Configuration* section for details.
5. Connect the RF output port of J7 and/or J9 to the spectrum analyzer.

6. If an external reference is to be used with LMK04806B in single PLL mode, provide a 3.3-Vpp maximum, 140-MHz maximum clock to J11. Change SJP5 solder jumper to position 2-3 to route the external reference source to the LMK04806B OSCIN input.
7. If the LMK04806B is configured in clock distribution mode, provide a 2.4-Vpp maximum, 3.1-GHz maximum clock to J12. The external clock source will route to the LMK04806B CLKIN1 input.

Table 2. TSW3084/TSW30H84 EVM Jumpers: (make sure the following jumpers are at their default setting)

Reference Designator	Setting	Function
JP2	1-2	DAC3484/DAC34H84 TXENABLE
JP3	2-3	DAC3484/DAC34H84 SLEEP
JP4	1-2	10-MHz TCXO Enable
JP12, JP13	2-3	TRF3705 Power Down
JP14, JP15	2-3	TRF3705 Gain Control
SJP2	2-3	CPLD EEPROM W/P
SJP3	1-2	USB Bus Power
SJP4	1-2	CPLD Clock Select
SJP5	1-2	Internal/External Reference Select for LMK04806B OSCIN
SJP9, SJP10, SJP11, SJP12	2-3	DAC3484/DAC34H84 DATACLK delay. Default is zero trace delay.

TSW3085 EVM

1. Connect J13 connector of TSW3085 EVM to J4 connector of TSW1400 EVM.
2. Connect 6 V to the J4, *Power In* jack of the TSW3085 EVM.
3. Connect PC’s USB port to J14 USB port of the TSW3085 EVM. The cable should be a standard A to mini-B connector cable.
4. Provide 10 dBm maximum, 300-MHz to 4-GHz LO source to connectors J1. The J1 connector routes the LO source to the respective TRF3705 modulator TX path.
5. Connect the RF output port of J7 to the spectrum analyzer.
6. If an external reference is to be used with LMK04806B in single PLL mode, provide a 3.3-Vpp maximum, 140 MHz maximum clock to J11. Change SJP5 solder jumper to position 2-3 to route the external reference source to the LMK04806B OSCIN input.
7. If the LMK04806B is configured in clock distribution mode, provide a 2.4-Vpp maximum, 3.1-GHz maximum clock to J12. The external clock source will route to the LMK04806B CLKIN1 input.

Table 3. TSW3085 EVM Jumpers: (make sure the following jumpers are at their default setting)

Reference Designator	Setting	Function
JP2	1-2	DAC3482 TXENABLE
JP3	2-3	DAC3482 SLEEP
JP4	1-2	10-MHz TCXO Enable
JP5	2-3	TRF3705 Power Down
JP1	2-3	TRF3705 Gain Control
SJP2	2-3	CPLD EEPROM W/P
SJP3	1-2	USB Bus Power
SJP4	1-2	CPLD Clock Select
SJP5	2-3	Internal/External Reference Select for LMK04806B OSCIN
SJP1, SJP6, SJP7, SJP8	2-3	DAC3482 DATACLK delay. Default is zero trace delay.

3.4 TSW308x Example Setup Procedure

1. Turn on power to both boards, and press the reset button SW1 on the TSW308xEVM.
2. Start the TSW308x EVM GUI program. When the program starts, press the *RESET USB Port* button in the GUI, and verify USB communication.
3. Select the appropriate EVM platform on the software menu.

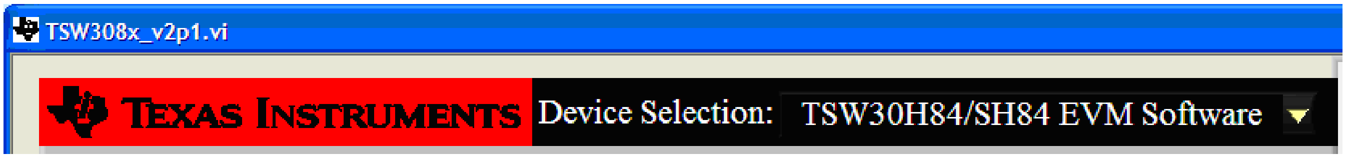


Figure 14. EVM Platform Selection

4. Click on *LOAD REGS*, browse to the installation folder, and load example files. The example files are located at *C:\Program Files\Texas Instruments\TSW308x\Configuration Files*. To configure the LMK04806B in single PLL mode, select the file in the LMK04806 PLL Mode 10-MHz reference folder. To configure the LMK04806B in clock distribution mode, select the file in the *LMK04806 Clock Distribution Mode* folder.

   For the TSW3084, the files contain settings for 4x interpolation with the DAC3484 running at 1228.8 MSPS. The data rate for each DAC is at 307.2 MSPS. The NCO is enabled at 30 MHz.

   For the TSW30H84, the files contain settings for 2x interpolation with the DAC34H84 running at 1228.8 MSPS. The data rate for each DAC is at 614.4 MSPS. The NCO is enabled at 30 MHz.

   For the TSW3085, the files contain settings for 2x interpolation with the DAC3482 running at 1228.8 MSPS. The data rate for each DAC is at 614.4 MSPS. The NCO is enabled at 30 MHz.
5. Click on *Send All* to write all of the values to the devices. If the LMK04806B is programmed properly in single PLL mode, the *LMK LOCK* LED (D7) near the device illuminates. The updated register configuration for the LMK04806B now appears as shown in Figure 8.
6. Note: J5 (CLK6) is configured as a divide-by-100 CMOS clock. This is used to verify EVM functionality.

3.5 TSW1400 Example Setup Procedure

1. Start the High Speed Converter Pro GUI program. When the program starts, select the DAC tab and then select appropriate device in the *Select DAC* menu.

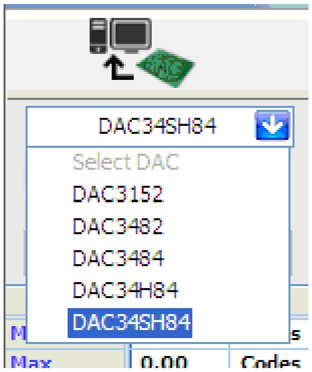


Figure 15. Select DAC348x Family in the High Speed Converter Pro GUI Program

2. When prompted *Do you want to update the firmware for DAC?*, select *YES*.

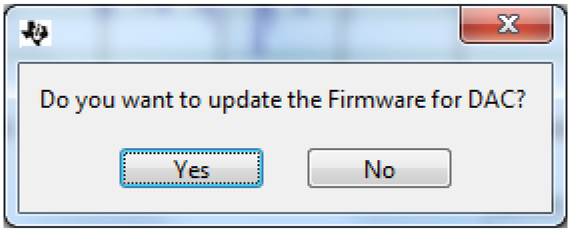


Figure 16. Load DAC Firmware Prompt

3. Click on the button labeled *Load File to transfer into TSW1400*, located near the top left of the GUI.

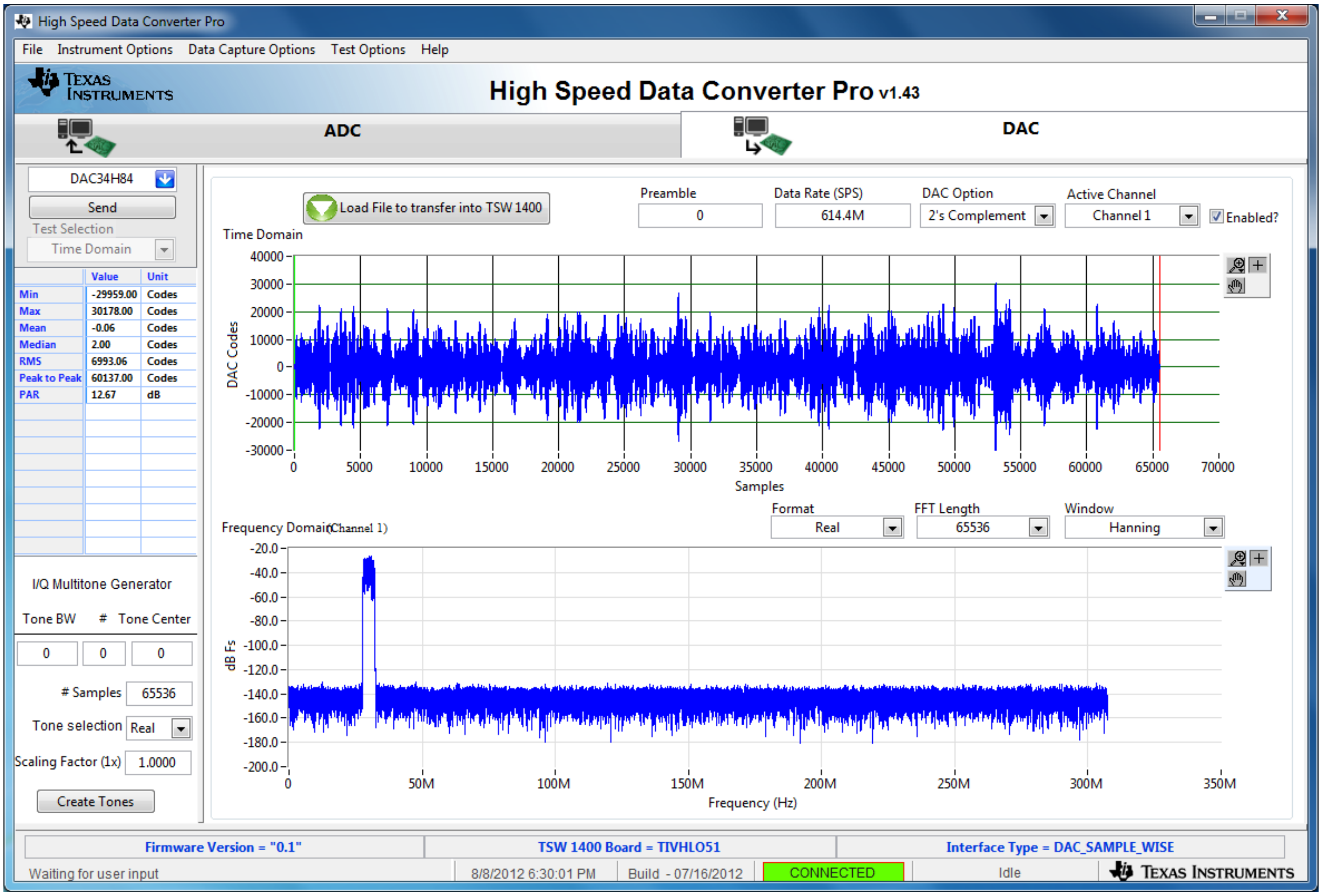
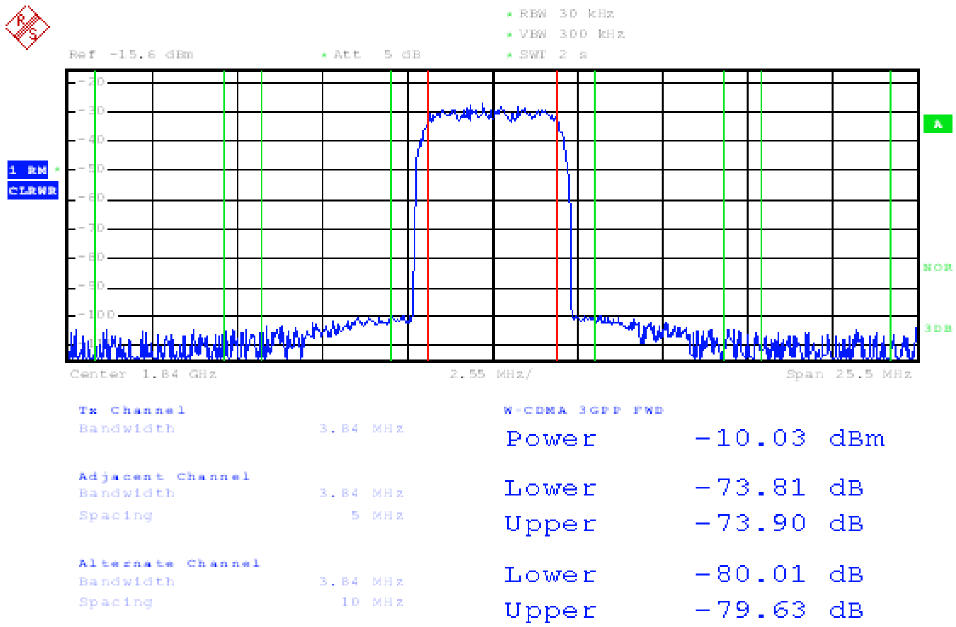


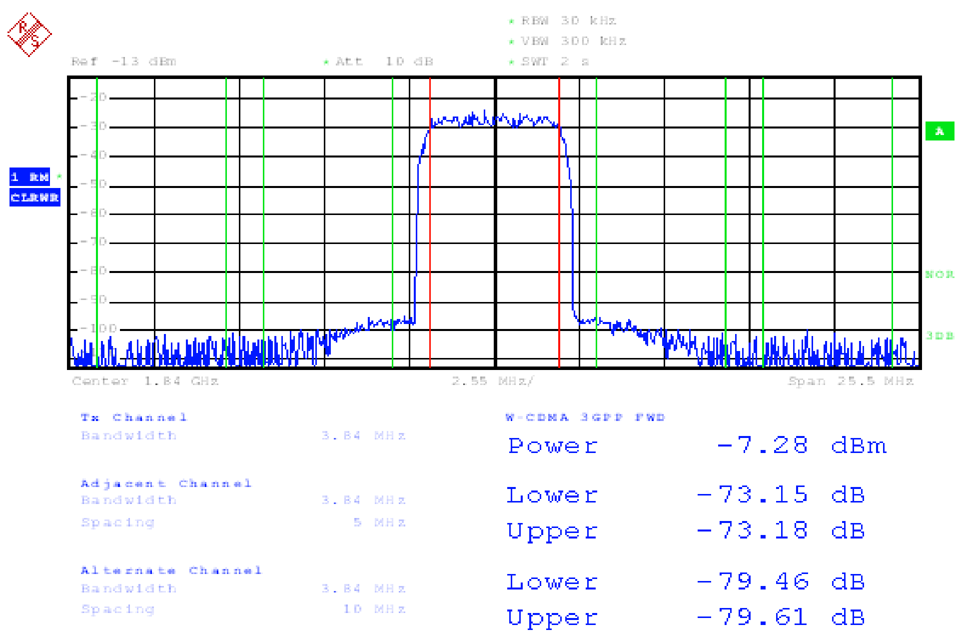
Figure 17. Load File to Transfer into TSW1400

4. For the TSW3084, select the file WCDMA_TM1_complexIF30MHz_Fdata307.2MHz_1000.tsw under C:\Program Files\Texas Instruments\High Speed Data Converter Pro\1400 Details\Testfiles
5. For the TSW30H84 and TSW3085, select the file WCDMA_TM1_complexIF30MHz_Fdata614.4MHz_1000.tsw under C:\Program Files\Texas Instruments\High Speed Data Converter Pro\1400 Details\Testfiles
6. Enter 307.2M or 614.4M for the *Data Rate* and 2's complement for the *DAC Option*.
7. Select Hanning for *Window*.
8. In the *DAC Selection* panel on the left side of the GUI, click on *Send* to load the data into memory.
9. **Toggle the SIF SYNC button of the TSW308x EVM GUI to synchronize the appropriate digital blocks, if the example file with NCO setting is used.**
10. Verify the spectrum using the spectrum analyzer at the RF output ports, J7 or J9.
11. With 1780 MHz of LO, the expect results are shown in Figure 18 (TRF3705 Low-Gain Mode) and Figure 19 (TRF3705 High-Gain Mode).



NOTE: Baseband = 30 MHz, NCO = 30 MHz with NCO Gain disabled, QMC Gain = 1446, LO = 1780 MHz

Figure 18. TSW308x WCDMA Output (TRF3705 Low-Gain Mode)



NOTE: Baseband = 30 MHz, NCO = 30 MHz with NCO Gain disabled, QMC Gain = 1446, LO = 1780 MHz

Figure 19. TSW308x WCDMA Output (TRF3705 High-Gain Mode)

4 Basic Test Procedure with TSW3100

This section outlines the basic test procedure for testing the EVM with the TSW3100.

4.1 TSW3100 Overview

The TSW3100 is a high speed pattern generator board. See the TSW3100 user's guide (SLLU101) for more detailed explanations of the TSW3100 setup and operation. This document assumes that the TSW3100 software is installed and functioning properly. The TSW308x needs TSW3100 operating software version 2.5 or higher with TSW3100 board Rev D (or higher).

The TSW308xEVM sends the FPGA reference clock to the FPGA of the TSW3100EVM in LVDS format. Therefore, a 100-Ω LVDS termination resistor is needed at the TSW3100 FPGA clock input. All the latest TSW3100EVMs from TI have the 100-Ω termination installed at the bottom side of the board on pins T31 and T32 of the FPGA. Contact TI Application Support if the 100-Ω termination is missing and assistance is needed for the 100-Ω installation.

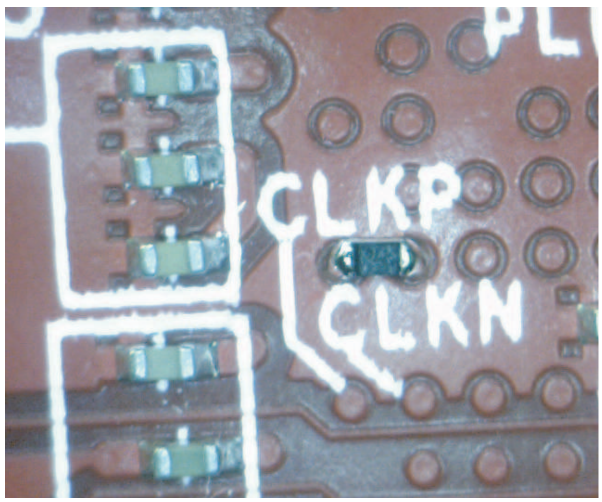


Figure 20. TSW3100 FPGA Clock 100-Ω LVDS Termination at Pins T31 and T32 of the FPGA

4.2 Test Block Diagram for TSW3100

The test setup for general testing of the TSW3084 and TSW30H84EVM with the TSW3100 pattern generation board is shown in Figure 21.

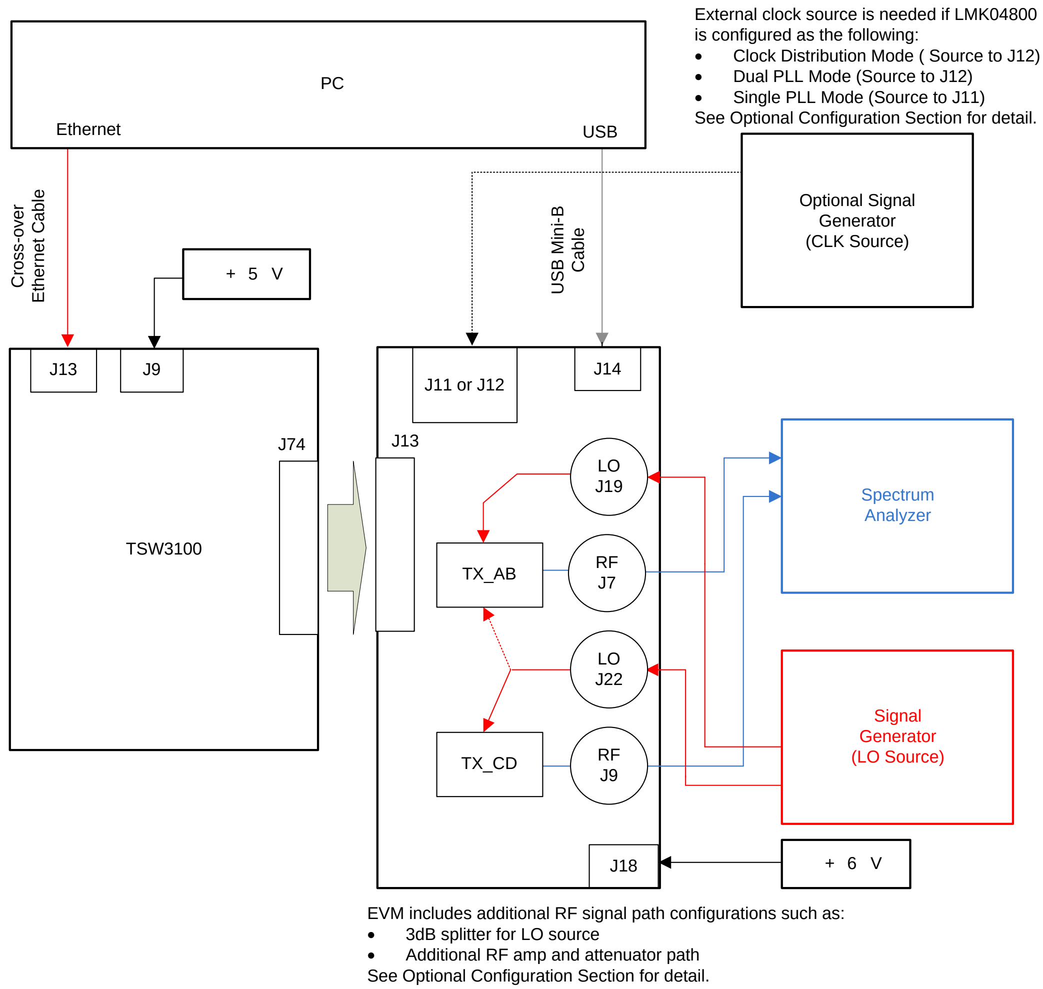


Figure 21. TSW3100 and TSW3084/TSW30H84 Test Setup Block Diagram

The test setup for general testing of the TSW3085EVM with the TSW3100 pattern generation board is shown in Figure 22.

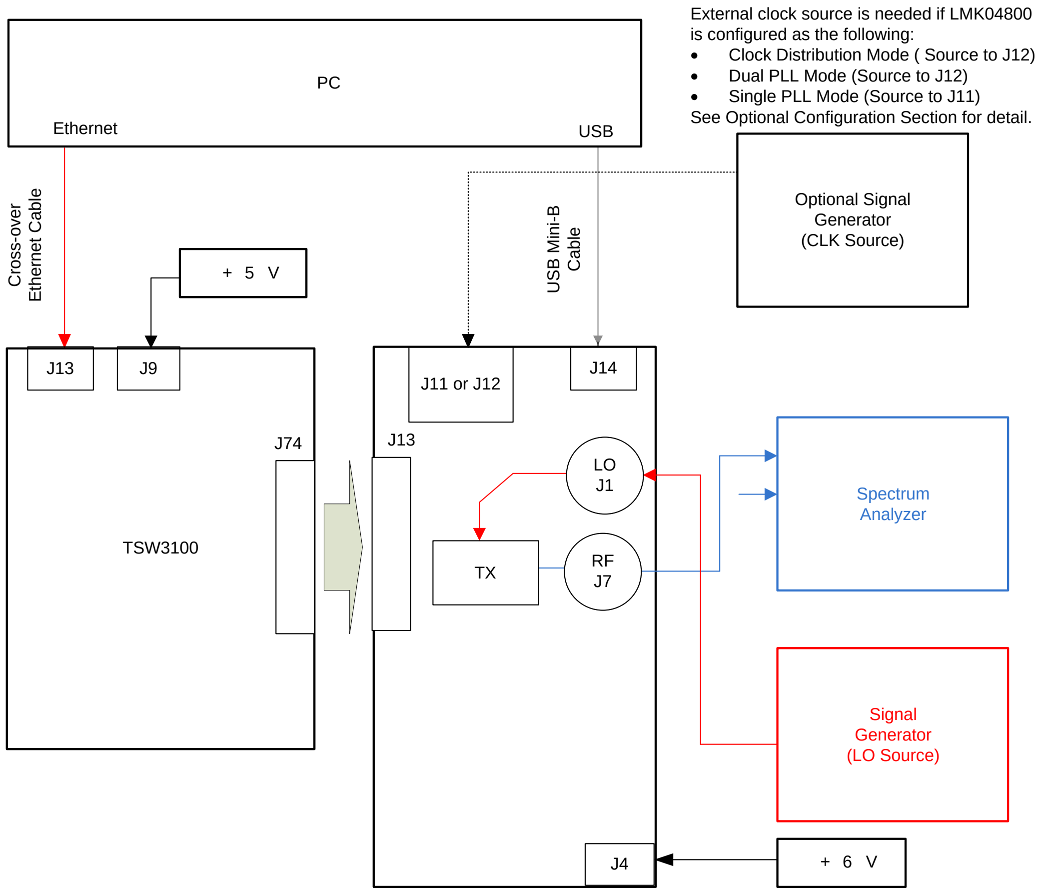


Figure 22. TSW3100 and TSW3085 Test Setup Block Diagram

4.3 Test Setup Connection

TSW3100 Pattern Generator

1. Connect 5-V power supply to J9, *5V_IN* jack of the TSW3100EVM.
2. Connect the PC's Ethernet port to J13, *Ethernet* port of the TSW3100. The cable must be a standard crossover Cat5e Ethernet cable.

TSW3084/TSW30H84/TSW3085 EVM

1. Connect J13 connector of TSW3084, TSW30H84, and TSW3085 EVM to J74 connector of TSW3100
2. See *Section 3.3 Test Setup Connection* for signal connections and jumper settings.

4.4 TSW308x Example Setup Procedure

See *Section 3.4 TSW308x Example Setup Procedure* for TSW308x Example setup for the GUI.

4.5 TSW3100 Example Setup Procedure

TSW3100 Single-Carrier WCDMA Output Example Setup

1. TSW3100 Single-Carrier WCDMA Output Example Setup
   - Start the TSW3100_CommsSignalPattern Software
   - For TSW3085 and TSW30H84, configure the TSW3100 to output a 614.4 MSPS, LVDS DDR format, 30-MHz IF Single-Carrier WCDMA output. See Figure 23 for details.
     – Change Interpolation value to DAC Clock Rate / Interpolation / 3.84 (that is, **1228.8** / **2**/ **3.84** = **160**)
     – Enter desired Offset Frequency (that is, 30 MHz) for each desired carrier
     – Select the **LVDS** output button
     – Check the *LOAD and Run* box
     – Press the green *Create* button

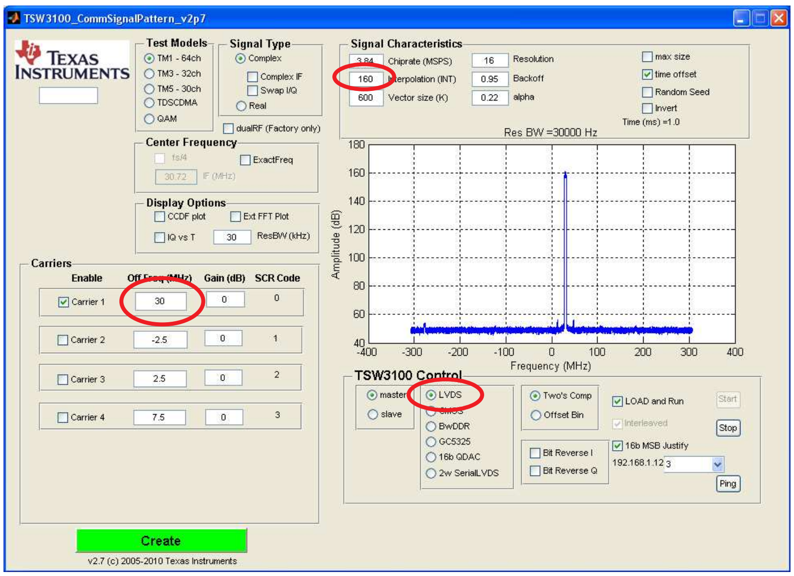


Figure 23. TSW3100 GUI for LVDS DDR Format

   - For TSW3084, configure the TSW3100 to output a 307.2 MSPS, LVDS Quad Interleave format, 30-MHz IF Single-Carrier WCDMA output.
     – Change Interpolation value to DAC Clock Rate / Interpolation / 3.84 (that is, **1228.8** / **4** / **3.84** = **80**)
     – Enter desired Offset Frequency (that is, 30 MHz) for each desired carrier
     – Select the **16b QDAC** output button
     – Check the *LOAD and Run* box
     – Press the green *Create* button

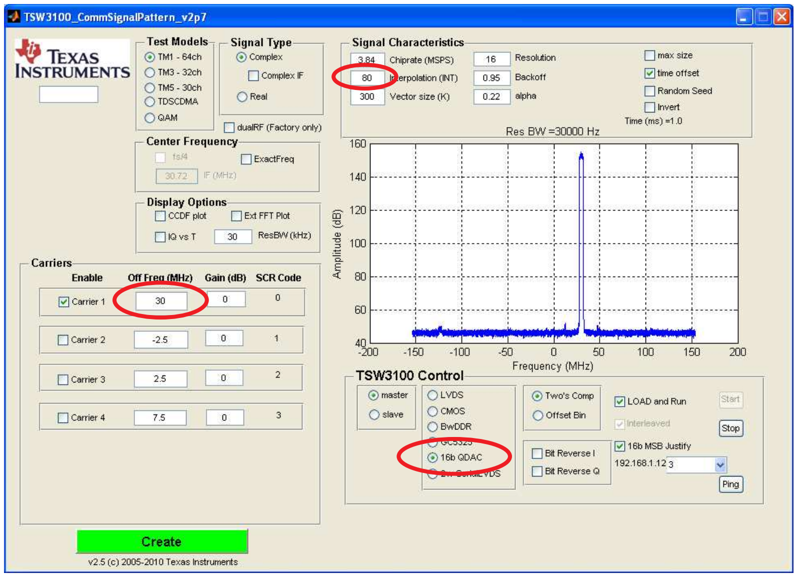


Figure 24. TSW3100 GUI for LVDS Quad Interleaved Format

2. **(Toggle the SIF SYNC button to synchronize the appropriate digital blocks, if example file with NCO setting is used.)**
3. Verify the spectrum using the Spectrum Analyzer at the two RF outputs of the TSW308xEVM (J7 for TSW3085. J7 and J9 for TSW3084 and TSW30H84).
4. With 1780 MHz of LO, the expect results are shown in Figure 18 (TRF3705 Low-Gain Mode) and Figure 19 (TRF3705 High-Gain Mode).

5 Optional Configuration

The onboard LMK048000 has the following configuration options for the flexible clocking of the DAC348x.

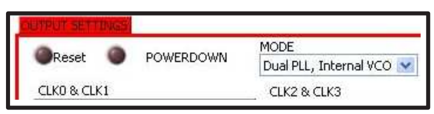


Figure 25. LMK04800 Mode Selection

5.1 Configuring the LMK04800 for Clock Distribution Mode

To use this mode:

- Provide a 2.4-Vpp maximum, 3.1-GHz maximum external clock at SMA J12.
- Select the *Clock Distribution* option in the LMK04800 Control tab.

5.2 Configuring the LMK04800 for Single PLL (PLL2 Only) Mode

To use this mode:

- The default reference is a 10-MHz crystal oscillator for the Single PLL mode. For the TSW3084 adn TSW30H84, set SJP5 to the 1-2 position. For the TSW3085, set SJP5 to the 2-3 position.
- Optionally, a 3.3-Vpp maximum, 140-MHz maximum external reference can be applied at SMA J11. For the TSW3084 and TSW30H84, set SJP5 to the 2-3 position. For the TSW3085, set SJP5 to the 1-2 position.
- Select the *PLL2* options in the LMK04800 Control tab.

5.3 Configuring the LMK04800 for Dual PLL (PLL1 + PLL2) Mode.

To use this mode, the following steps must be made to the EVM:

- Replace oscillator Y1 with a VCXO, such as a FVXO-HC73 series 3.3-V VCXO from Fox.
- Install R273, R274, R90, C177, and C300.
- Provide an external reference at SMA J12.
- Select the Dual PLL options in the LMK04800 Control tab.

Consult the LMK04800 data sheet (SNAS489) for proper device configuration for this mode of operation.

6 Transmit Path Optional Configuration

6.1 Shared LO Path (TSW3084 and TSW30H84 only)

To share the LO source between the two transmit paths, the following configuration can be done:

- Install 0 Ω to R192
- Install 17.4 Ω to R190, R189, and R191
- Remove R188

6.2 Additional RF amp and attenuator path

To add additional gain and attenuation adjustment to the transmit path, the following configuration can be done:

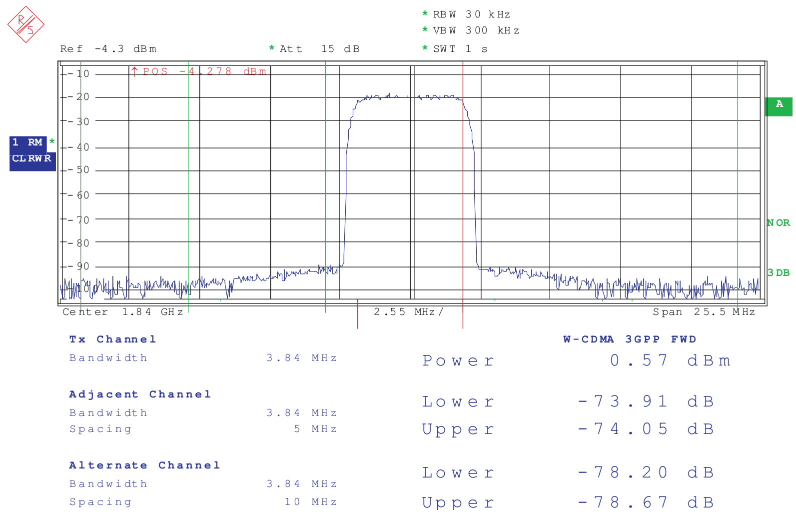
For TX Path #1 (TSW3084, TSW3085, and TSW30H84)

- Remove C258 and R165
- Install 0 Ω to R161, R163, and R293
- Install 0 Ω or ferrite bead to FB23

For TX Path #2 (TSW3084 and TSW30H84)

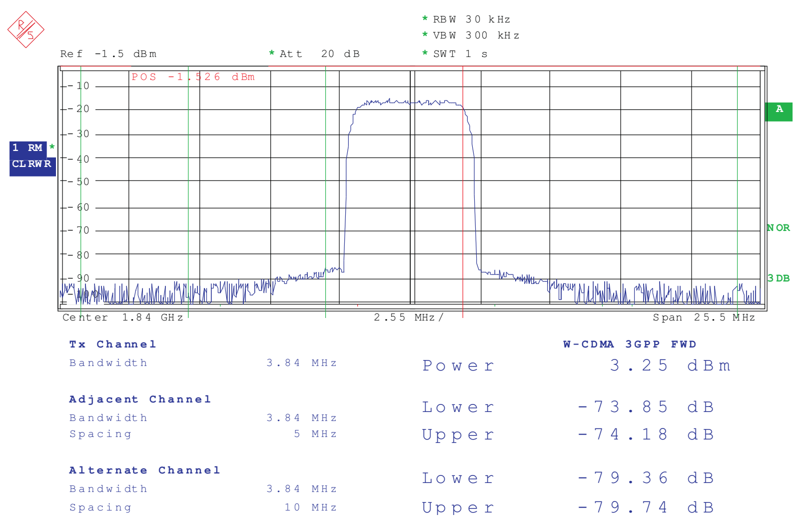
- Remove C268 and R166
- Install 0 Ω to R162, R164, and R294
- Install 0 Ω or ferrite bead to FB21

With the default example pattern and LO of 1780 MHz, the RF signal chain output can be measured at J7 and J9 connectors. The expected results are shown in Figure 26 and Figure 27.



NOTE: Baseband = 30 MHz, NCO = 30 MHz with NCO Gain disabled, QMC Gain = 1446, LO = 1780 MHz

Figure 26. TSW308x RF Amp / Attenuator Output (TRF3705 Low-Gain Mode)



NOTE: Baseband = 30 MHz, NCO = 30 MHz with NCO Gain disabled, QMC Gain = 1446, LO = 1780 MHz

Figure 27. TSW308x RF Amp / Attenuator Output (TRF3705 High-Gain Mode)

Matching components can be changed depending on the RF frequency range. See the schematic in the TSW308x design package (listed in Section 7), TRF3705 data sheet (SLWS223), and the Avago MGA-30689 data sheet for details.

7 References

7.1 Related Products From Texas Instruments

Quad-Channel, 16-Bit, 1.25 GSPS Digital-to-Analog Converter (DAC) , DAC3484 (SLAS749)

Dual-Channel, 16-Bit, 1.25 GSPS Digital-to-Analog Converter (DAC) , DAC3482 (SLAS748)

Quad-Channel, 16-Bit, 1.25 GSPS Digital-to-Analog Converter (DAC) , DAC34H84 (SLAS751)

Quad-Channel, 16-Bit, 1.5 GSPS Digital-to-Analog Converter (DAC) , DAC34SH84 (SLAS808)

300-MHz to 4-GHz Quadrature Modulator, TRF3705 (SLWS223)

LMK04800 Family Low-Noise Clock Jitter Cleaner with Dual Loop PLLs (SNAS489)

7.2 Related Tools From Texas Instruments

TSW1400 High Speed Data Capture/Pattern Generator Card (SLWU079)

TSW3100 High Speed Digital Pattern Generator (SLUU101)

FMC-DAC-ADAPTER Physical Design Database Rev D Board (SLOR102)

TSW3084EVM Design Package (SLAC515)

TSW30H84EVM Design Package (SLAC517)

TSW308x EVM Software (SLAC507)

High Speed Data Converter Pro software (SLWC107)