bq24650EVM Synchronous, Switch-Mode, Battery Charge Controller for Solar Power

This user's guide describes the features and operation of the bq24650EVM Evaluation Module (EVM). The EVM assists users in evaluating the bq24650 synchronous battery charger. The EVM is also called the HPA639 A. The manual includes the bq24650EVM bill of materials, board layout, and schematic.

Contents

1 Introduction 2
1.1 Features 2
1.2 General Description 2
1.3 I/O Description 2
1.4 Control and Key Parameters Settings 3
1.5 Recommended Operating Conditions 3
2 Test Summary 5
2.1 Definitions 5
2.2 Safety 5
2.3 Quality 5
2.4 Apparel 5
2.5 Equipment 5
2.6 Equipment Setup 6
2.7 Procedure 7
3 PCB Layout Guideline 9
4 Bill of Materials, Board Layout, and Schematic 10
4.1 Bill of Materials 10
4.2 Board Layout 11
4.3 Schematic 17

List of Figures

1 Original Test Setup for HPA639 A Evaluation Board 6
2 Top Layer 11
3 Second Layer 12
4 Third Layer 13
5 Bottom Layer 14
6 Top Assembly 15
7 Bottom Assembly 16
8 bq24650EVM Schematic 17

List of Tables

1 I/O Description 2
2 Control and Key Parameters Settings 3
3 Recommended Operating Conditions 3
4 Bill of Materials 10

1 Introduction

1.1 Features

- Synchronous switch-mode battery charge controller for solar power
- Resistor-programmable up to 26-V battery voltage
- Input operating range: 5 V–28 V
- LED indication for charge status
- Test points for key signals available for testing purposes; easy probe hook-up.
- Jumpers available; easy-to-change setting

1.2 General Description

The bq24650 is a highly integrated switch-mode battery charge controller. It provides input voltage regulation, which reduces charge current when input voltage falls below a programmed level. When the input is powered by a solar panel, the input regulation loop maintains the panel at maximum power output.

The bq24650 offers a constant-frequency, synchronous PWM controller with high-accuracy current and voltage regulation, charge preconditioning, charge termination, and charge status monitoring.

The bq24650 changes the battery in three phases: preconditioning, constant current, and constant voltage. Charge is terminated when the current reaches one-tenth of the fast charge rate. A programmable fast-charge timer provides a safety backup. The precharge timer is fixed at 30 minutes. The bq24650 automatically restarts the charge cycle if the battery voltage falls below an internal threshold and enters a low, quiescent-current sleep mode when the input voltage falls below the battery voltage.

The bq24650 supports the battery from 2.1 V to 26 V with VFB set to a 2.1-V feedback reference. The charge current is programmed by selecting an appropriate sense resistor. The bq24650 is available in a 16-pin, 3.5x3.5 mm^2, thin QFN package.

For details, see the bq24650 data sheet (SLUSA75).

1.3 I/O Description

Table 1. I/O Description

Jack	Description
J1–VIN	Positive input
J1–PGND	Negative input
J2–VSYS	Connected to system
J2–VOUT	Connected to charger output
J2–PGND	Ground
J2–TS	Temperature qualification voltage Input

1.4 Control and Key Parameters Settings

Table 2. Control and Key Parameters Settings

Jack	Description	Factory Setting
JP1	Select external TS input or internal valid TS setting 1-2 : External TS input 2-3 : Internal valid TS setting	Jumper ON 1-2 (external TS)
JP2	The pullup power source supplies the LEDs when JP2 ON. LED has no power source when JP2 is OFF.	Jumper ON (LED power available)
JP3	TERM_EN setting 2-3 : Connect TERM_EN to VREF to enable termination 1-2 : Connect TERM_EN to GND to disable termination	Jumper ON 2-3 (enable termination)
JP4	Charger enable/disable setting. MPPSET is pulled to GND and the charger is disabled when JP4 OFF; charger is enabled when JP4 is ON.	Jumper OFF (disable charger)

1.5 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit	Notes
Supply voltage, V_{IN}	Input voltage	5	20	28	V	
Battery voltage, V_{OUT}	Voltage applied at VOUT terminal of J2	2.1	12.6	26	V	
Supply current	Maximum input current	0		8	A	
Charge current, I_{chrg}	Battery charge current	0	2	8	A	For charge current above 2 A, replace R6 and L1 with high-current rating components
Operating junction temperature range, T_J		0		125	°C	

The bq24650EVM board requires a regulated supply approximately 1 V minimum above the regulated voltage of the battery pack to a maximum input voltage of 28 Vdc. The charge voltage is programmed via a resistor divider from the battery to ground, with the midpoint tied to the VFB pin.

R13 and R15 can be changed to regulate output between approximately 2.1 V to 26 V.

$$V_{OUT} = 2.1\ V \times \left(1 + \frac{R13}{R15}\right) \quad (1)$$

It is set at 12.6 Vdc from the factory.

A solar panel has a unique point on the V-I or V-P curve, called the maximum power point (MPP), at which the entire photovoltaic (PV) system operates with maximum efficiency and produces its maximum output power. The constant voltage algorithm is the simplest maximum power point tracking (MPPT) method. The bq24650 automatically reduces charge current, so the maximum power point is maintained for maximum efficiency.

If the solar panel or other input source cannot provide the total power of the system and bq24650 charger, the input voltage drops. Once the voltage sensed on the MPPSET pin drops below 1.2 V, the charger maintains the input voltage by reducing the charge current.

$$V_{MPPSET} = 1.2\ V \times \left(1 + \frac{R17}{R19}\right) \quad (2)$$

It is set at 17.8 Vdc from the factory.

Battery current is sensed by resistor RSR connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is fixed at 40 mV.

$$I_{CHARGE} = \frac{40\ mV}{R_6} \quad (3)$$

It is set at 2 Adc from the factory.

2 Test Summary

2.1 Definitions

This procedure details how to configure the HPA639 A evaluation board. The following naming conventions are followed on the test procedure.

VXXX :	External voltage supply name (VADP, VBT, VSBT)
LOADW:	External load name (LOADR, LOADI)
V(TPyyy):	Voltage at internal test point TPyyy. For example, V(TP1) means the voltage at TP1.
V(Jxx):	Voltage at jack terminal Jxx.
V(TP(XXX)):	Voltage at test point XXX. For example, V(MPPSET) means the voltage at the test point which is marked as MPPSET.
V(XXX, YYY):	Voltage across point XXX and YYY.
I(JXX(YYY)):	Current going out from the YYY terminal of jack XX.
Jxx(BBB):	Terminal or pin BBB of jack xx
Jxx ON :	Internal jumper Jxx terminals are shorted
Jxx OFF:	Internal jumper Jxx terminals are open
Jxx (-YY-) ON:	Internal jumper Jxx adjacent terminals marked as YY are shorted
Measure:→A,B	Check specified parameters A, B. If measured values are not within specified limits the unit under test has failed.
Observe: →A,B	Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points and individual components.

2.2 Safety

1. Safety Glasses are to be worn.
2. This test must be performed by qualified personnel who are trained in electronics theory and understand the risks and hazards of the assembly to be tested.
3. ESD precautions must be followed while handling electronic assemblies and performing this test.
4. Precautions must be observed to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.

2.3 Quality

1. Test data can be made available on request from Texas Instruments.

2.4 Apparel

1. Electrostatic smock
2. Electrostatic gloves or finger cots
3. Safety glasses
4. Ground ESD wrist strap.

2.5 Equipment

2.5.1 Power Supplies

Power Supply #1 (PS#1): a power supply capable of supplying 30 V at 3 A is required.

2.5.2 Loads

LOAD#1 A 30-V (or greater), 5-A (or greater) electronic load that can operate at constant current and constant voltage mode.

LOAD#2: An HP 6060B 3-V to 60-V/0A to 60-A, 300-W system dc electronic load or equivalent.

2.5.3 Meters

Seven Fluke 75 multimeters (equivalent or better) or four equivalent voltage meters and three equivalent current meters.

The current meters must be capable of measuring 5-A+ current.

2.6 Equipment Setup

1. Set the power supply #1 (PS#1) for 21-V ±500-mVdc, 2.5-A ±0.1-A current limit, and then turn off supply.
2. Connect the output of PS#1 in series with a current meter (multimeter) to J1 (VIN, PGND).
3. Connect a voltage meter across J1 (VIN, PGND).
4. Connect Load#1 in series with a current meter to J2 (VOUT, PGND). Turn off Load#1.
5. Connect Load#2 in series with a current meter to J2 (VSYS, PGND). Turn off Load#2.
6. Connect a voltage meter across J2 (VOUT, PGND).
7. Connect a voltage meter across J2 (VSYS, PGND).
8. Check all jumper shunts. JP1: connect 1-2 (External TS); JP2: ON; JP3: connect 2-3 (Enable TERM_EN); JP4: OFF.

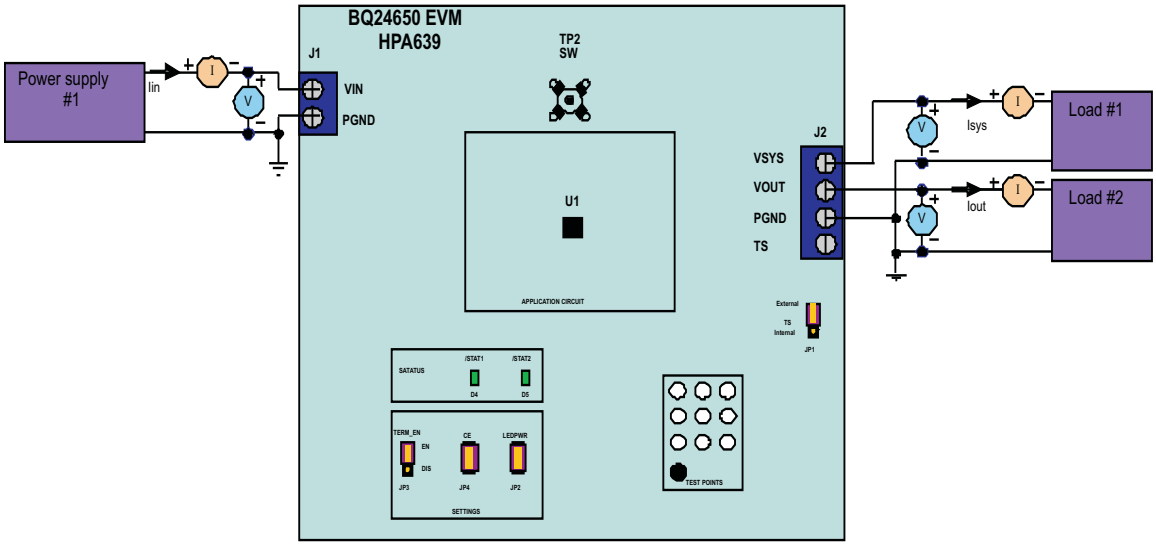

Figure 1. Original Test Setup for HPA639 A Evaluation Board

2.7 Procedure

2.7.1 Power Supply and VREF

Ensure that Section 2.6 steps are followed.

Disconnect LOAD#1#2. Turn on PS#1.
Measure → V(J2(VSYS)) = 21 V ±500 mV
Measure → V(J2(VOUT)) = 0 V ±500 mV
Measure → V(TP(VREF)) = 3.3 V ±200 mV
Measure → V(TP(REGN)) = 0 V ±200 mV

2.7.2 Charger Enable and Battery Detection

Connect 2-3 of JP1 (Internal TS); Short JP4 (Charger Enable)
Measure → V(TP(VREF)) = 3.3 V ±200 mV
Measure → V(TP(REGN)) = 6 V ±200 mV
Observe → V(J2(VOUT))=12.6 V ±500 mV
Observe → D4 (/STAT1) OFF, D5 (/STAT2) OFF

2.7.3 Charge Current/Voltage Regulation and Battery Temperature Qualification

Reconnect LOAD#2, and turn on. Use the constant voltage mode. Set the output voltage to 8 V.
Measure → I(J2(VOUT)) = 0.2 A ±100 mA
Observe → D4 (/STAT1) ON, D5 (/STAT2) OFF

Increase the voltage of LOAD#2 to be 10.5 V.
Measure → I(J2(VOUT)) = 2 A ±200 mA
Observe → D4 (/STAT1) ON, D5 (/STAT2) OFF

Open 2-3 of JP1
Measure → I(J2(VOUT)) = 0 A ±100 mA
Observe → D4 (/STAT1) OFF, D5 (/STAT2) OFF

Connect 2-3 of JP1 (Internal TS)
Measure → I(J2(VOUT)) = 2 A ±200 mA
Observe → D4 (/STAT1) ON, D5 (/STAT2) OFF

2.7.4 Charger Termination

Increase the voltage of LOAD#2 slowly to approximately 12.6 V.
Observe → I(J2(VOUT)) decreases from 2 A while V(J2(VOUT)) becomes constant.
Observe → I(J2(VOUT)) drops to zero when it is less than 0.2 A.

2.7.5 Maximum Power Point, Input Voltage Regulation

Connect the output of the Load#1 in series with a current meter (multimeter) to J2 (SYS, PGND). Ensure that a voltage meter is connected across J2 (SYS, PGND). Resume other status as in Section 2.7.3. (Short JP1, JP4, set LOAD#2 to 10.5 V.)

2.7.6 Final Step

Turn on the power of Load#1. Set the load current to 1 A. Increase the load current slowly and observe the following.

Observe → V(J1(VIN)) = 17.8 V ±500 mV.
Keep increasing I(J2(VSYS)),
Observe → I(J2(VOUT)) decreases from 2 A toward 0 A while V(J1(VIN)) become constant 17.8 V ±500 mV. Ensure that I(J2(VOUT))= 0 A ±100 mA and → (J2(VSYS)) = 2.4 A ±200 mA.

2.7.7 Test Complete

Turn off the power supply, and remove all connections from the unit under test.

3 PCB Layout Guideline

1. It is critical that the exposed thermal pad on the backside of the bq24650 package be soldered to the PCB ground. Ensure that sufficient thermal vias are right underneath the IC, connecting to the ground plane on the other layers.
2. The control stage and the power stage must be routed separately. At each layer, the signal ground and the power ground are connected only at the thermal pad.
3. Charge current sense resistor must be connected to SRP, SRN with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins must be placed as close to the IC as possible.
4. Decoupling capacitors for VREF, VCC, REGN must make the interconnections to the IC as short as possible.
5. Decoupling capacitors for BAT must be placed close to the corresponding IC pins, and make the interconnections to the IC as short as possible.
6. Decoupling capacitor(s) for the charger input must be placed close to the Q1A drain and Q1B source.
7. Take the EVM layout for design reference.

4 Bill of Materials, Board Layout, and Schematic

4.1 Bill of Materials

Table 4. Bill of Materials

001	RefDes	Value	Description	SIZE	PART NUMBER	MFR
3	C1, C2, C7	10 µF	Capacitor, Ceramic, 35V, X7R, 10%	1210	STD	STD
3	C3, C5, C8	1.0 µF	Capacitor, Ceramic, 35V, X7R, 10%	805	STD	STD
1	C4	2.2 µF	Capacitor, Ceramic, 35V, X7R, 20%	1210	STD	STD
3	C6, C11, C12	0.1 µF	Capacitor, Ceramic, 50V, X7R, 10%	603	STD	STD
0	C9, C13	Open	Capacitor, Ceramic, 50V, X7R, 10%	603	STD	STD
2	C10, C16	1.0 µF	Capacitor, Ceramic, 16V, X7R, 10%	805	STD	STD
1	C14	0.1 µF	Capacitor, Ceramic, 16V, X7R, 10%	603	STD	STD
2	C15, C17	22 pF	Capacitor, Ceramic, 50V, X7R, 10%	603	STD	STD
2	D1, D3	PDS1040-13	Diode, 10A 40V Schottky Barrier Rectifier	PowerDI 5	PDS1040-13	Diodes
1	D2	ZLLS350-7	Diode, Schottky, 1.16A, 40-V	SOD-523	ZLLS350-7	Zetex
2	D4, D5	LTST-C190GKT	Diode, LED, Green, 2.1V, 20mA, 6mcd	603	LTST-C190GKT	Lite On
1	J1	ED120/2DS	Terminal Block, 2 pin, 15A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
1	J2	ED120/4DS	Terminal Block, 4 pin, 15A, 5.1mm	0.80 x 0.35 inch	ED120/4DS	OST
2	JP2, JP4	PEC02SAAN	Header, 2 pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
2	JP1, JP3	PEC03SAAN	Header, 3 pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	L1	10 µH	Inductor, SMT, 102mΩ, 7.0A, 20%	0.255 x 0.270 inch	IHLP2525CZER100M01 IHLP2525CZEB100M01	Vishay
1	Q1	Si7288-T1	FET, Dual N Chan, 40V, 20A, 19 mΩ	SO8-PowerPak	SI7288DP-T1	Vishay/ Siliconix
1	Q2	2N7002-7-F	MOSFET, N-ch, 60V, 115mA, 1.2Ω	SOT23	2N7002-7-F	Diodes
2	R1, R2	3.9	Resistor, Chip, 1/4W, 5%	1206	STD	STD
1	R3	10	Resistor, Chip, 1/8W, 5%	805	STD	STD
0	R4, R8	Open	Resistor, Chip, 1/8W, 5%	805	STD	STD
1	R5	2.2	Resistor, Chip, 1/10W, 5%	603	STD	STD
1	R6	0.02	Resistor, Metal Film, 1/4 watt, 0.1%, Axial	1206	WSLP1206R0200FEA	Vishay
2	R7, R10	0	Resistor, Chip, 1/10W, 5%	603	STD	STD
1	R9	5.23K	Resistor, Chip, 1/10W, 1%	603	STD	STD
1	R11	100	Resistor, Chip, 1/10W, 5%	603	STD	STD
1	R12	30.1k	Resistor, Chip, 1/10W, 1%	603	STD	STD
2	R13, R17	499k	Resistor, Chip, 1/10W, 1%	603	STD	STD
1	R14	10k	Resistor, Chip, 1/10W, 5%	603	STD	STD
2	R15, R18	100k	Resistor, Chip, 1/10W, 1%	603	STD	STD
0	R16	Open	Resistor, Chip, 1/10W, 5%	603	STD	STD
2	R20, R21	10k	Resistor, Chip, 1/8W, 5%	805	STD	STD
1	R19	36k	Resistor, Chip, 1/8W, 5%	805	STD	STD
0	TP1, TP3–TP7	Open	Test Point, 0.020 Hole	0.020"	STD	STD
0	TP2	Open	Adaptor, 3.5-mm probe clip (or 131-4244-00)	0.200 inch	131-5031-00	Tektronix
1	U1	BQ24650RVA	IC, High Efficiency Synchronous Switch-Mode Fast Charge Controller for Solar Power	QFN16[RVA]	BQ24650RVA	TI
10	CE, GND, MPPSET, REGN, STAT1, STAT2, TS, TERM_EN, VCC, VREF	TP-5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	–		PCB, 3 In x 3 In x 0.062 In		HPA639	Any
4			Bumper foot (install after final wash)	0.440 x 0.2	SJ-5303	3M
4			Shunt, 100-mil, Black	0.100	929950-00	3M

4.2 Board Layout

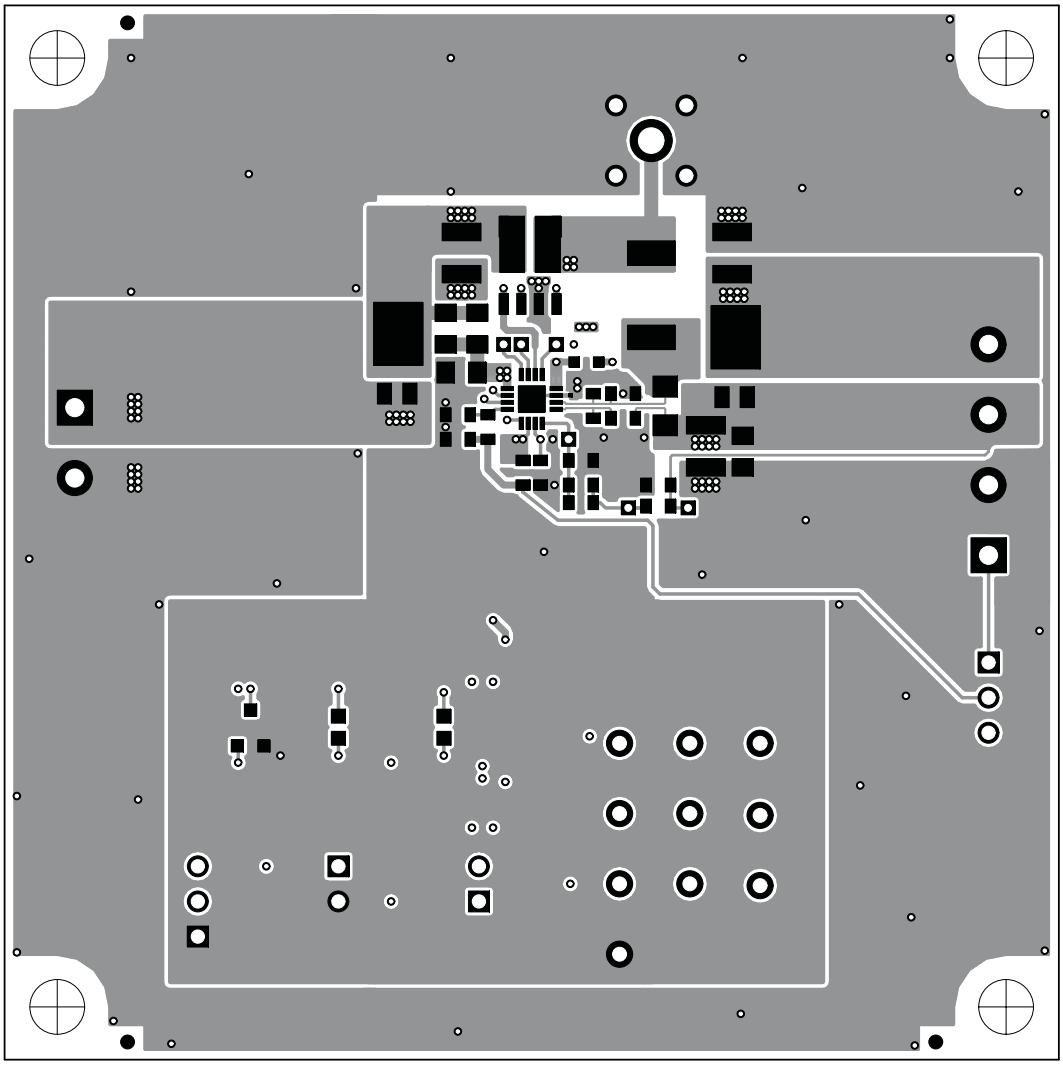

Figure 2. Top Layer

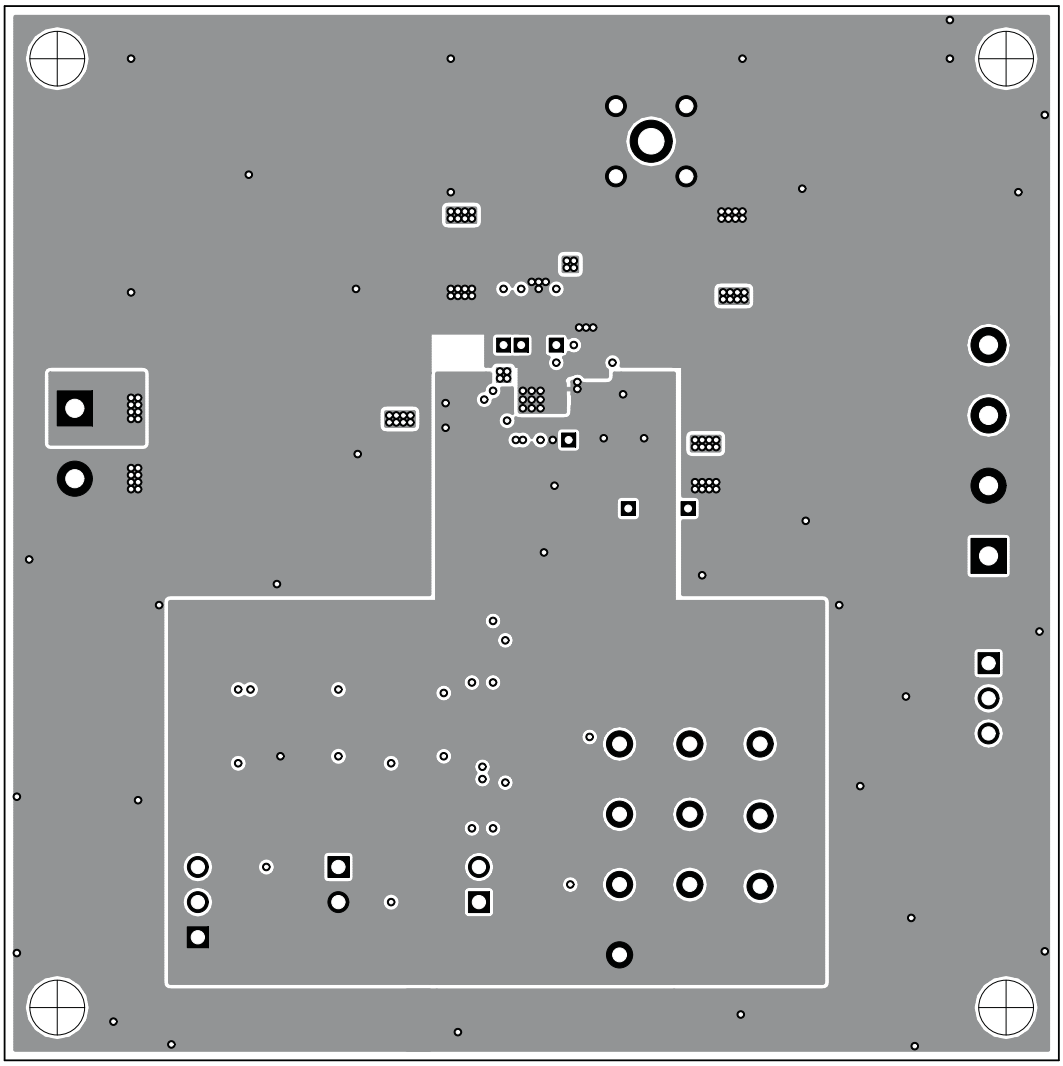

Figure 3. Second Layer

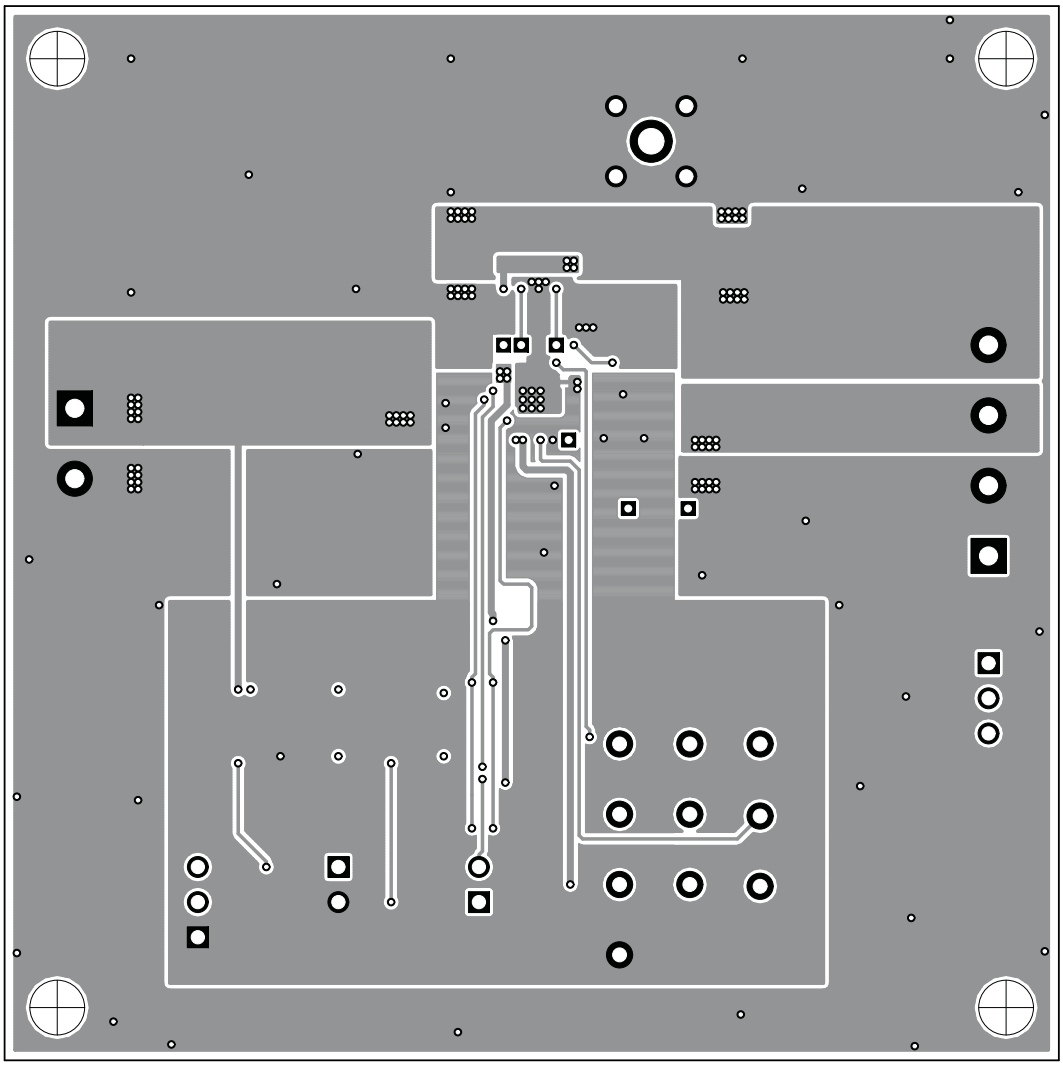

Figure 4. Third Layer

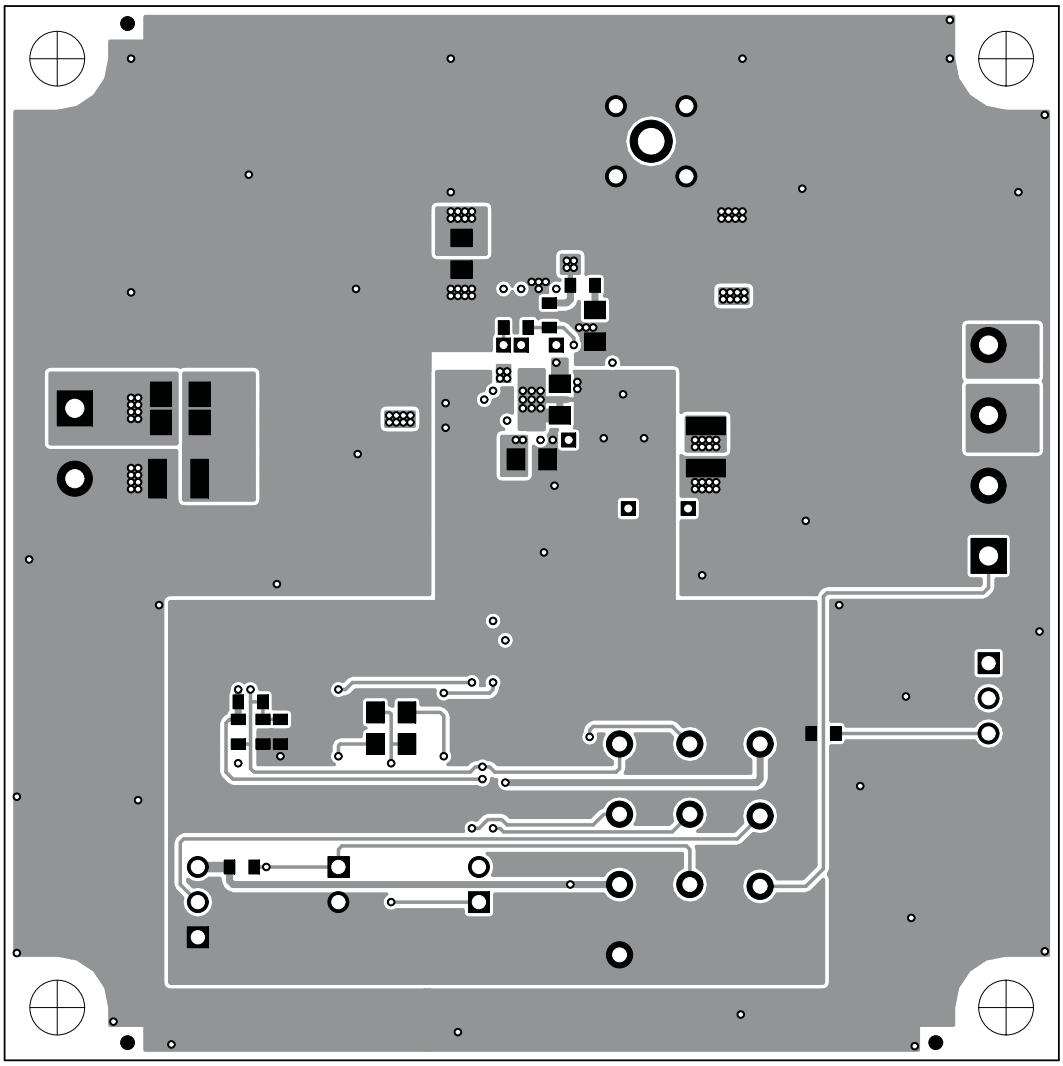

Figure 5. Bottom Layer

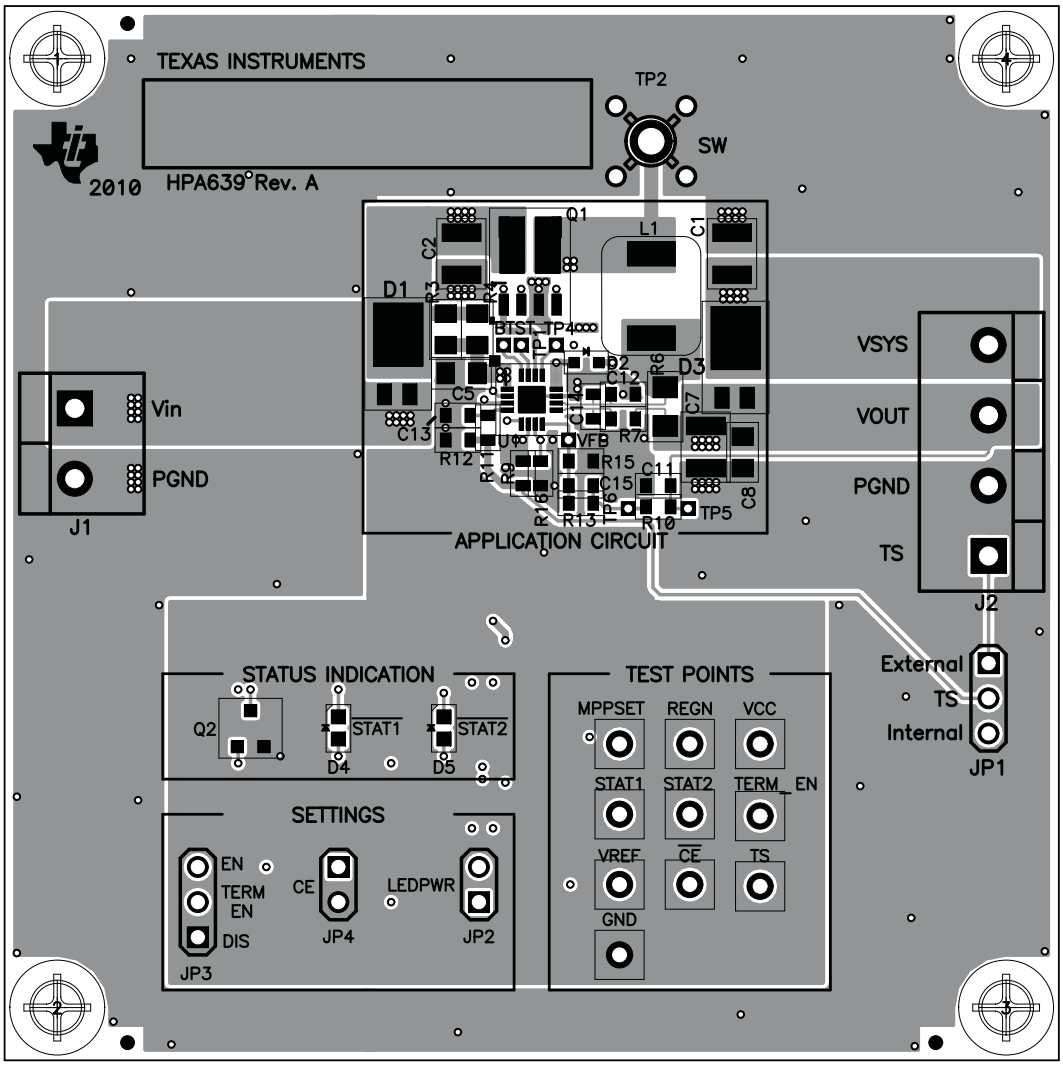

Figure 6. Top Assembly

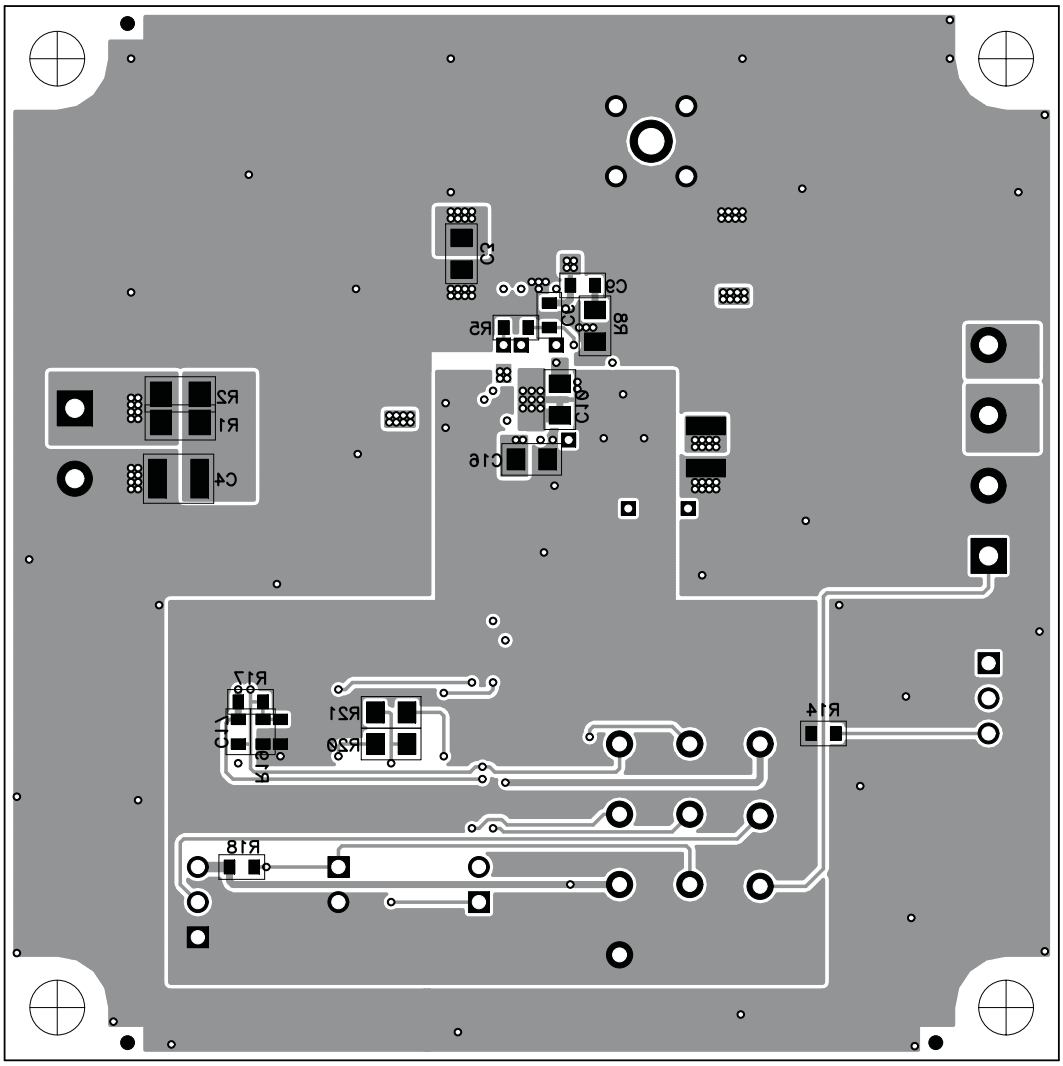

Figure 7. Bottom Assembly

4.3 Schematic

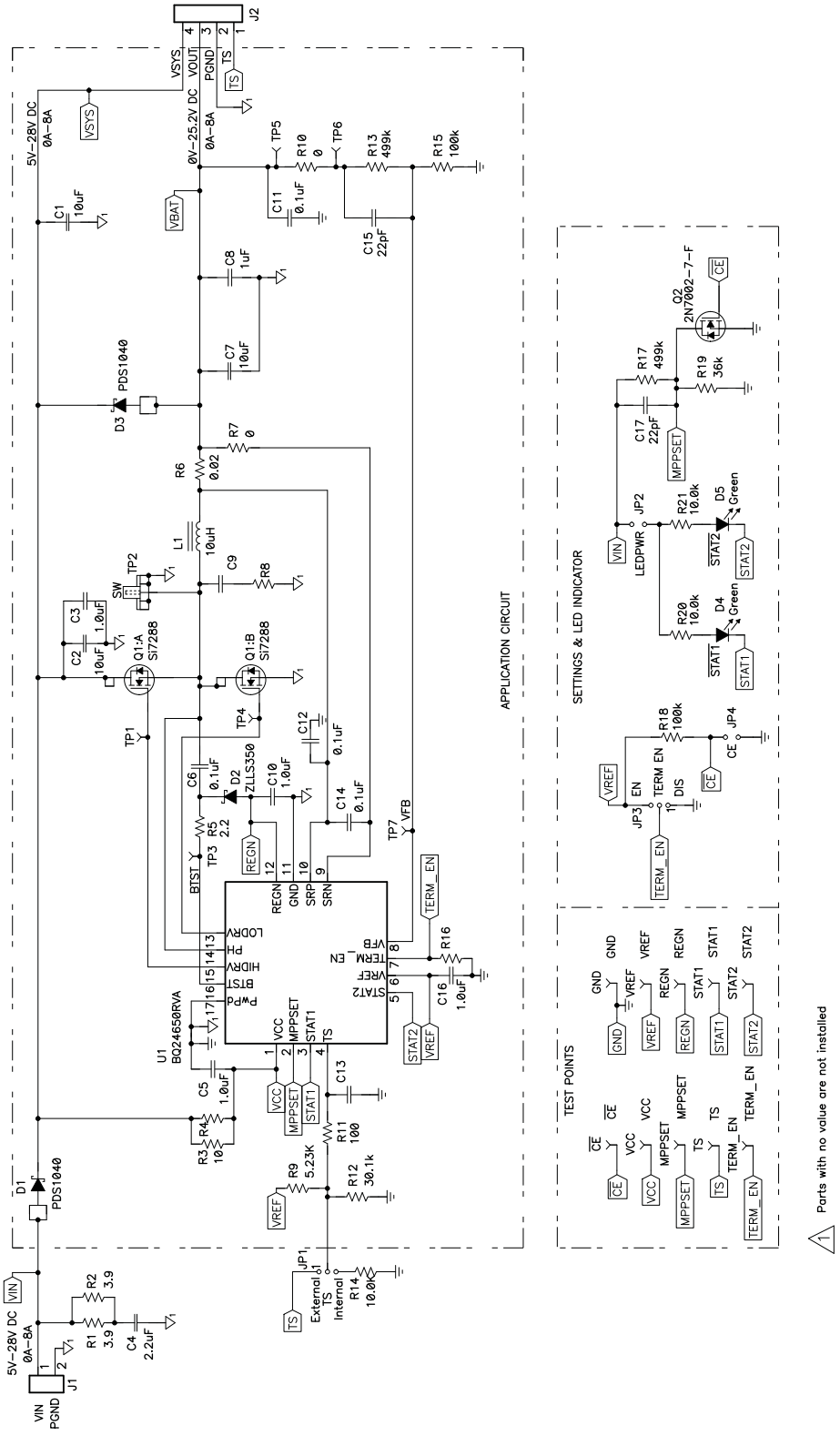

Figure 8. bq24650EVM Schematic

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 18 V to 22 V and the output voltage range of 0 V to 18 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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