Test Report: PMP22992

Dual 15-V, 120-mA Isolated Bias Power Supply Reference Design Using Buck and Push-Pull Converters

1 Description

This isolated power supply provides dual +15-V outputs at 120 mA each. This power supply is designed for biasing a MOSFET-based power stage that generates excitation for a separately excited synchronous motor (SSM). This design uses a combination of the LMR50410-Q1 buck pre-regulator and the SN6505-Q1 open-loop transformer driver with spread-spectrum modulation. The wide input voltage range and flexibility make this design a versatile solution for wide range of applications where isolated power is necessary. This internal reference design is an alternative to the PMP22760 which uses a single-chip solution based on the LM5180-Q1.

Figure 1-1. PCB Top View

Figure 1-2. PCB Bottom View

Figure 1-3. PCB Aerial View

Figure 1-4. PCB Side View

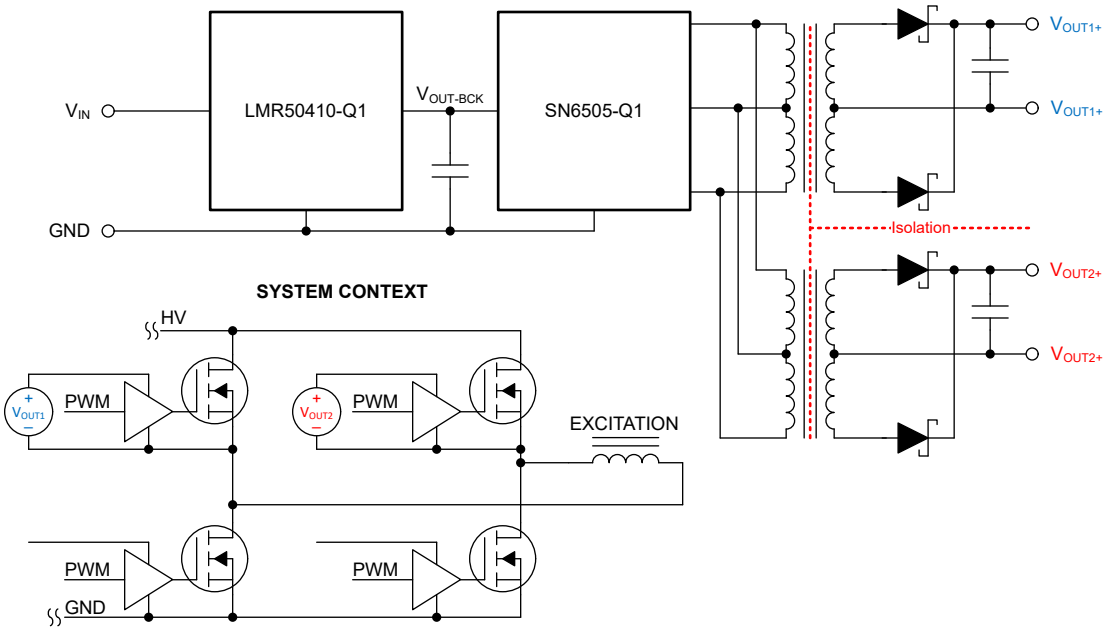


Figure 1-5. Functional Block Diagram

2 Test Prerequisites

2.1 Voltage and Current Requirements

Table 2-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage range	12 V to 15 V (fully tested) 6 V to 36 V (operational)
Output voltage and current	Two isolated outputs, each +15 V, 120 mA
Switching frequency	2.1 MHz (buck), 450 kHz (push-pull)
Topology	Buck pre-regulator + open-loop push-pull
Transformer dielectric strength (WE 750316853)	3125 VAC at 2 seconds, 2500 VAC at 1 minute
Secondary-to-primary capacitance(1)	11.5 pF at 100 kHz
Secondary-to-secondary capacitance(1)	Approximately 7.5 pF at 100 kHz

(1) Terminals V_{OUT1}, V_{OUT2}, $V_{OUT-BCK}$ are shorted with a jumper for the measurement. The value is taken with an accurate RCL meter. Naturally, the system is disabled.

2.2 Required Equipment

The following test equipment was used during the design development and testing:

- Oscilloscopes Rohde & Schwarz RTB2004, RTH1004
- Bench multimeters Keysight 34410A, Keithley 2700, Keithley 2100, Keithley 2110
- Hand-held multimeters Agilent U1272A, Brymen BM869s
- Regulated laboratory power supply E3648A
- Electronic load Keithley 2380-120-60

2.3 Considerations

The functional block diagram shows the system context of the isolated bias power supply. The isolated output rails see fast dv/dt transients during switching. For this reason, the primary-to-secondary and secondary-to-secondary capacitance must be as low as possible. Low parasitic capacitances mitigate unwanted current and help to maintain signal integrity and low EMI of the whole system.

2.4 Dimensions

The design uses a 1.6-mm thick two-layer PCB with 35-µm copper plating. Dimensions are 34 mm × 13.5 mm × 10 mm (L × W × H).

2.5 Signal Descriptions

Signal	Description
V_{IN}	Input voltage (V_{IN} to GND)
$V_{OUT-BCK}$	Output voltage of the LMR50410-Q1 buck converter (V_{OUT} to GND)
V_{OUT1}	Isolated output 1 voltage (V_{OUT1}+ to V_{OUT1}–)
I_{OUT1}	Isolated output 1 current (from V_{OUT1}+ to V_{OUT1}–)
V_{OUT2}	Isolated output 2 voltage (V_{OUT2}+ to V_{OUT2}–)
I_{OUT2}	Isolated output 2 current (from V_{OUT2}+ to V_{OUT2}–)
P_{OUT}	Total output power (both outputs)
Efficiency	Total system efficiency

3 Testing and Results

3.1 Efficiency Graphs

The following figure shows the overall efficiency of the system. Both outputs are connected in series and loaded with the electronic load. This ensures identical loading of both isolated outputs.

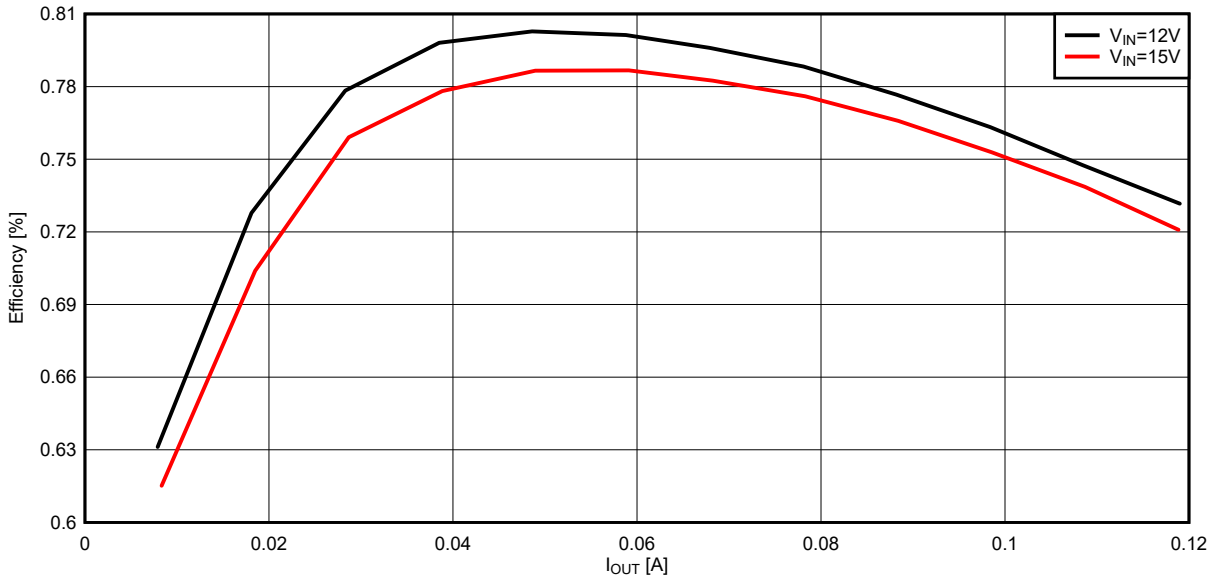


Figure 3-1. LMR50410-Q1+SN6505-Q1 Efficiency

3.2 Efficiency Data

Table 3-1. Equal Loading for V_{IN} = 12 V

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	$V_{OUT-BCK}$ (V)	V_{OUT1} (V)	V_{OUT2} (V)	I_{OUT} (W)	P_{OUT} (W)	Efficiency (%)
12.002	0.0077	0.092	4.1165	16.920	17.051	0.0000	0.000	n/a
12.003	0.0080	0.096	4.1165	16.309	16.328	0.0001	0.004	3.84%
12.001	0.0333	0.400	4.1016	15.961	15.967	0.0079	0.252	63.12%
11.999	0.0652	0.782	4.0821	15.733	15.726	0.0181	0.569	72.78%
12.007	0.0944	1.133	4.0820	15.592	15.581	0.0283	0.882	77.83%
12.004	0.1242	1.491	4.0818	15.453	15.453	0.0385	1.190	79.81%
12.001	0.1544	1.853	4.0817	15.314	15.294	0.0486	1.488	80.28%
12.008	0.1853	2.225	4.0815	15.174	15.148	0.0588	1.783	80.13%
12.005	0.2136	2.564	4.0814	15.047	15.014	0.0679	2.041	79.60%
12.003	0.2457	2.949	4.0813	14.903	14.864	0.0781	2.325	78.83%
12.001	0.2788	3.346	4.0811	14.754	14.709	0.0882	2.599	77.67%
12.007	0.3129	3.757	4.0807	14.597	14.545	0.0984	2.868	76.33%
12.004	0.3484	4.182	4.0803	14.434	14.378	0.1085	3.126	74.75%
12.001	0.3856	4.628	4.0799	14.253	14.199	0.1190	3.386	73.17%

Table 3-2. Equal Loading for V_{IN} = 15 V

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	$V_{OUT-BCK}$ (V)	V_{OUT1} (V)	V_{OUT2} (V)	I_{OUT} (W)	P_{OUT} (W)	Efficiency (%)
15.000	0.0065	0.098	4.1168	16.920	17.052	0.0000	0.000	n/a
15.005	0.0067	0.101	4.1166	16.309	16.329	0.0001	0.004	3.67%
15.003	0.0288	0.432	4.1016	15.957	15.952	0.0083	0.266	61.52%
15.001	0.0551	0.827	4.0824	15.730	15.722	0.0185	0.582	70.40%
15.009	0.0787	1.181	4.0822	15.588	15.676	0.0287	0.897	75.91%
15.008	0.1027	1.541	4.0819	15.448	15.432	0.0388	1.199	77.81%
15.006	0.1269	1.904	4.0818	15.310	15.289	0.0490	1.498	78.66%
15.003	0.1518	2.277	4.0815	15.166	15.139	0.0591	1.792	78.67%
15.002	0.1746	2.619	4.0814	15.033	15.001	0.0682	2.050	78.25%
15.010	0.1999	3.000	4.0811	14.889	14.851	0.0783	2.328	77.60%
15.007	0.2264	3.398	4.0808	14.742	14.697	0.0884	2.602	76.59%
15.005	0.2540	3.811	4.0804	14.582	14.531	0.0986	2.869	75.29%
15.002	0.2824	4.237	4.0801	14.421	14.366	0.1087	3.129	73.86%
15.010	0.3123	4.688	4.0793	14.245	14.185	0.1189	3.379	72.09%

3.3 Voltage Regulation Graphs

The following figure shows the load regulation plot of the converter. Both outputs are connected in series and loaded with the electronic load. This ensures identical loading of both isolated outputs. Note that for the no-load condition, the forward voltage of the secondary diodes is practically zero and the output exceeds 17 V. Pre-loading the output with approximately 500 µA brings the voltage significantly lower.

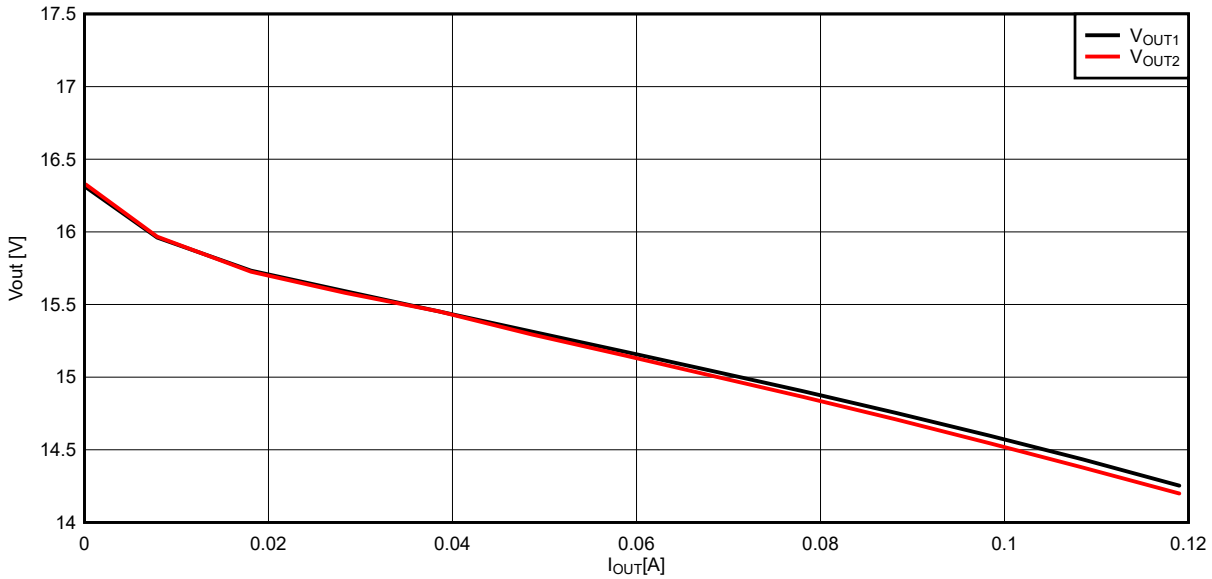


Figure 3-2. LM50410-Q1 + SN6505-Q1 Load Regulation for V_{OUT} = 15 V, V_{IN} = 12 V

3.4 Cross-Loading Performance

The following figure shows the load regulation and cross-regulation. This test sweeps load current I_{OUT1} = 10 mA to 120 mA while maintaining constant I_{OUT2} = 100 mA. Both outputs are floating and maintain the isolation barrier.

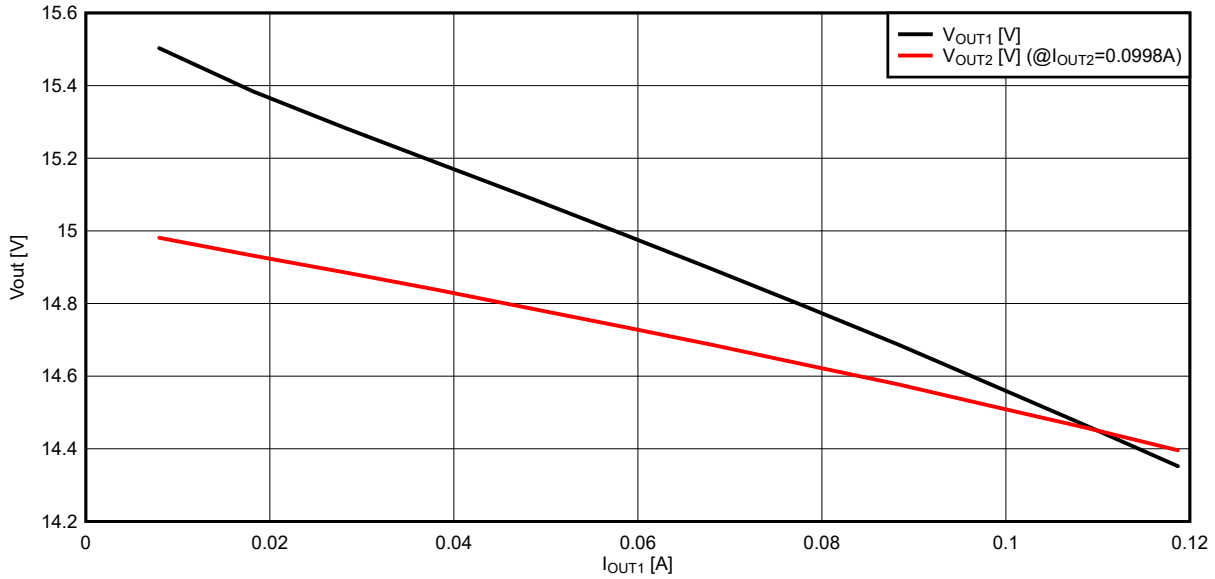


Figure 3-3. LM50410-Q1 + SN6505-Q1 Load Regulation for V_{OUT} = 15 V

3.5 Cross-Loading Performance Data

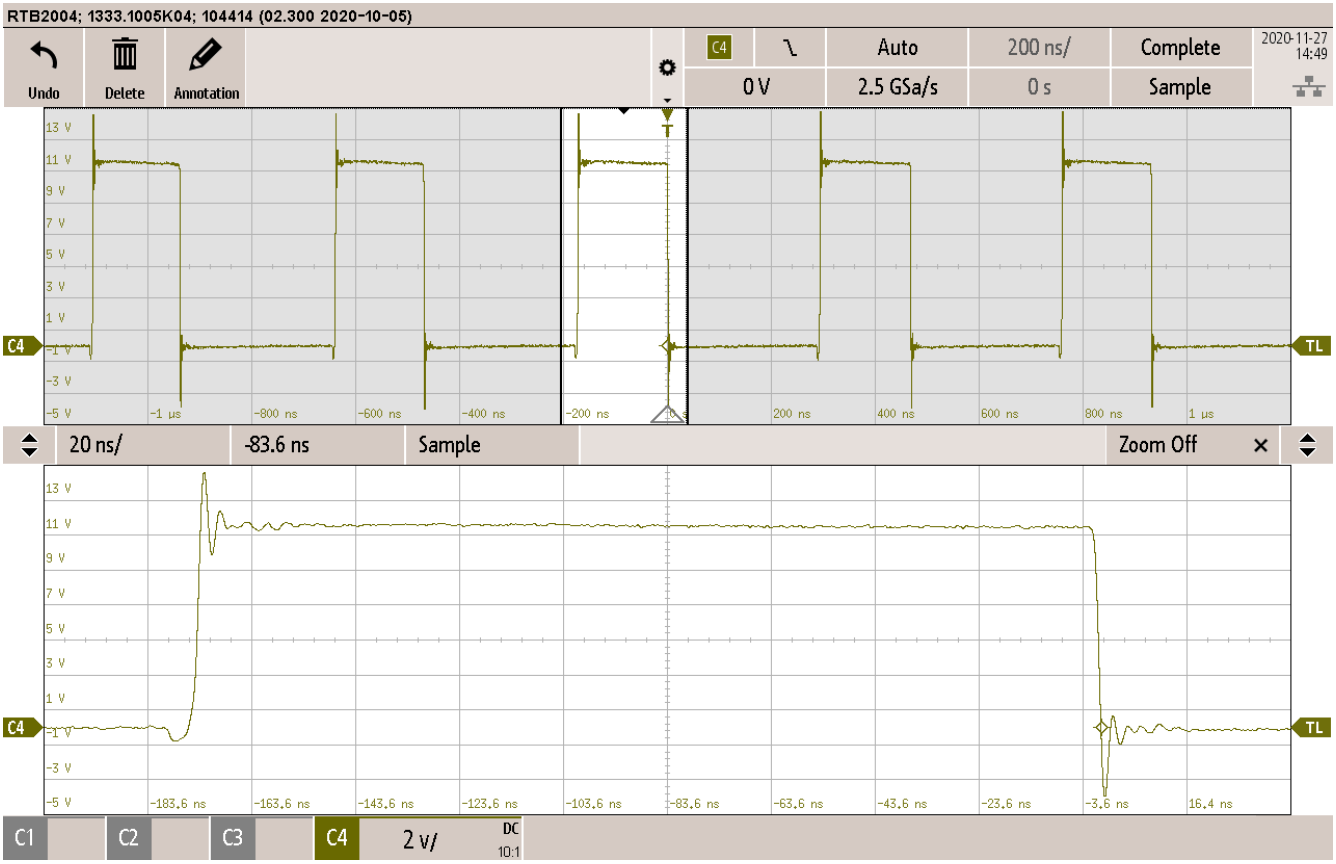
Table 3-3. Cross-Loading for V_{IN} = 12 V

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	$V_{OUT-BCK}$ (V)	V_{OUT1} (V)	V_{OUT2} (V)	I_{OUT1} (A)	I_{OUT2} (A)	P_{OUT} (W)	Efficiency (%)
12.001	0.1696	2.035	4.0817	15.503	14.981	0.0080	0.0996	0.243	11.95%
11.999	0.1854	2.225	4.0815	15.384	14.932	0.0182	0.0996	0.551	24.75%
12.008	0.2009	2.412	4.0815	15.282	14.885	0.0283	0.0996	0.854	35.41%
12.006	0.2169	2.604	4.0814	15.184	14.836	0.0385	0.0996	1.156	44.39%
12.005	0.2331	2.798	4.0813	15.087	14.785	0.0486	0.0997	1.452	51.90%
12.003	0.2495	2.995	4.0812	14.987	14.734	0.0588	0.0998	1.747	58.35%
12.002	0.2646	3.176	4.0811	14.896	14.687	0.0680	0.0998	2.010	63.30%
12.000	0.2814	3.377	4.0810	14.793	14.632	0.0781	0.0997	2.298	68.05%
11.999	0.2986	3.583	4.0809	14.688	14.578	0.0882	0.0999	2.582	72.05%
12.008	0.3159	3.793	4.0807	14.577	14.518	0.0984	0.0998	2.862	75.46%
12.007	0.3337	4.007	4.0805	14.466	14.459	0.1085	0.0998	3.139	78.35%
12.005	0.3520	4.226	4.0802	14.352	14.396	0.1187	0.0998	3.412	80.75%

4 Waveforms

4.1 Switching

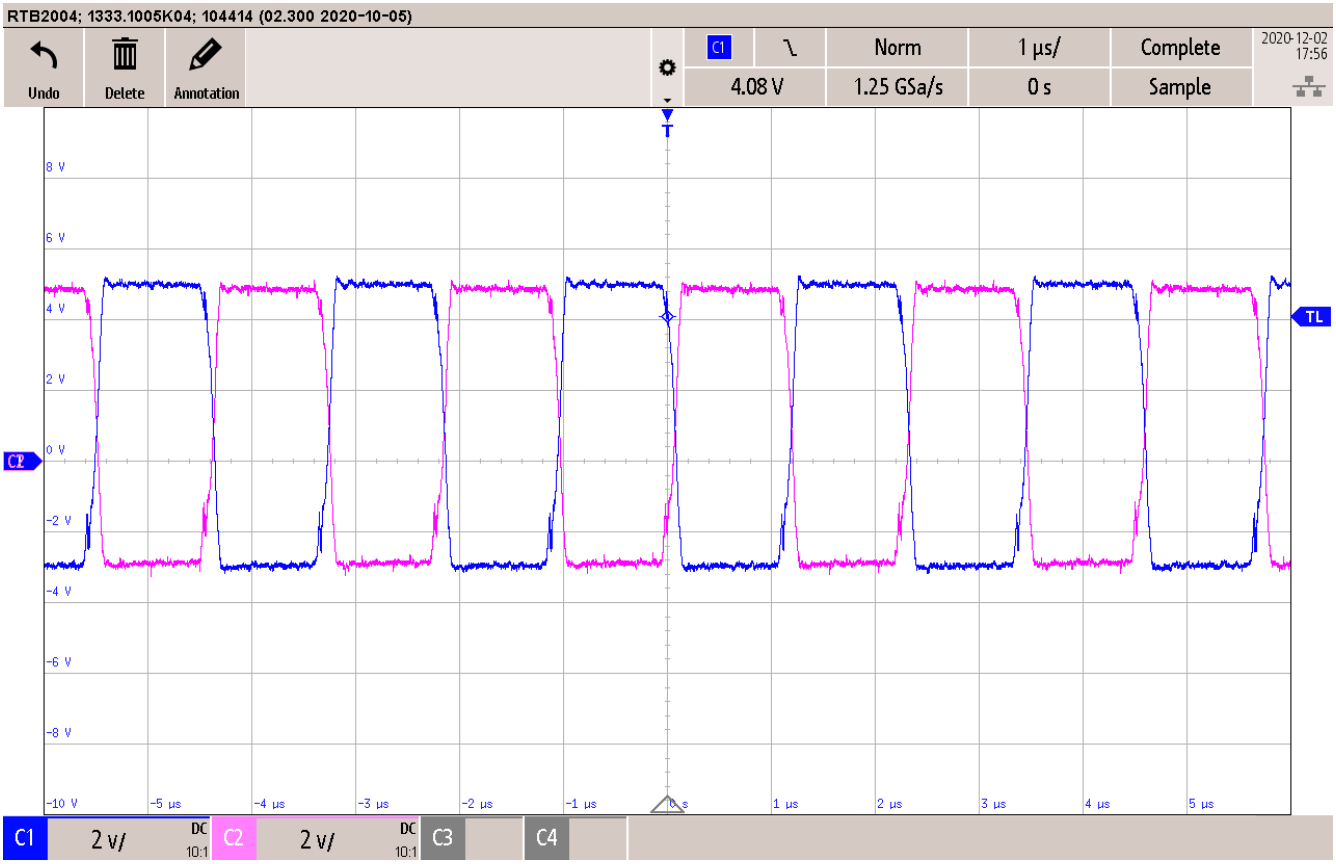
Figure 4-1 shows the LMR501410-Q1 switch node at 50% of nominal load.



CH1 - pin 3

Figure 4-1. LMR50410-Q1 Switch Node

Figure 4-2 shows the output ripple V_{OUT1} with 330-Ω resistive load.



CH1 - pin 1, CH2 - pin 3

Figure 4-2. SN6505-Q1 Switch Node

4.2 Output Voltage Ripple

Output voltage ripple measurements use the proper ripple-measurement technique that minimizes the voltage probe grounding loop. The oscilloscope uses the 20-MHz bandwidth limit.

In Figure 4-3, the SN6505-Q1 is not assembled. Figure 4-4 shows the output ripple V_{OUT1} with 165-Ω resistive load. Figure 4-5 shows the output ripple V_{OUT1} with 330-Ω resistive load.

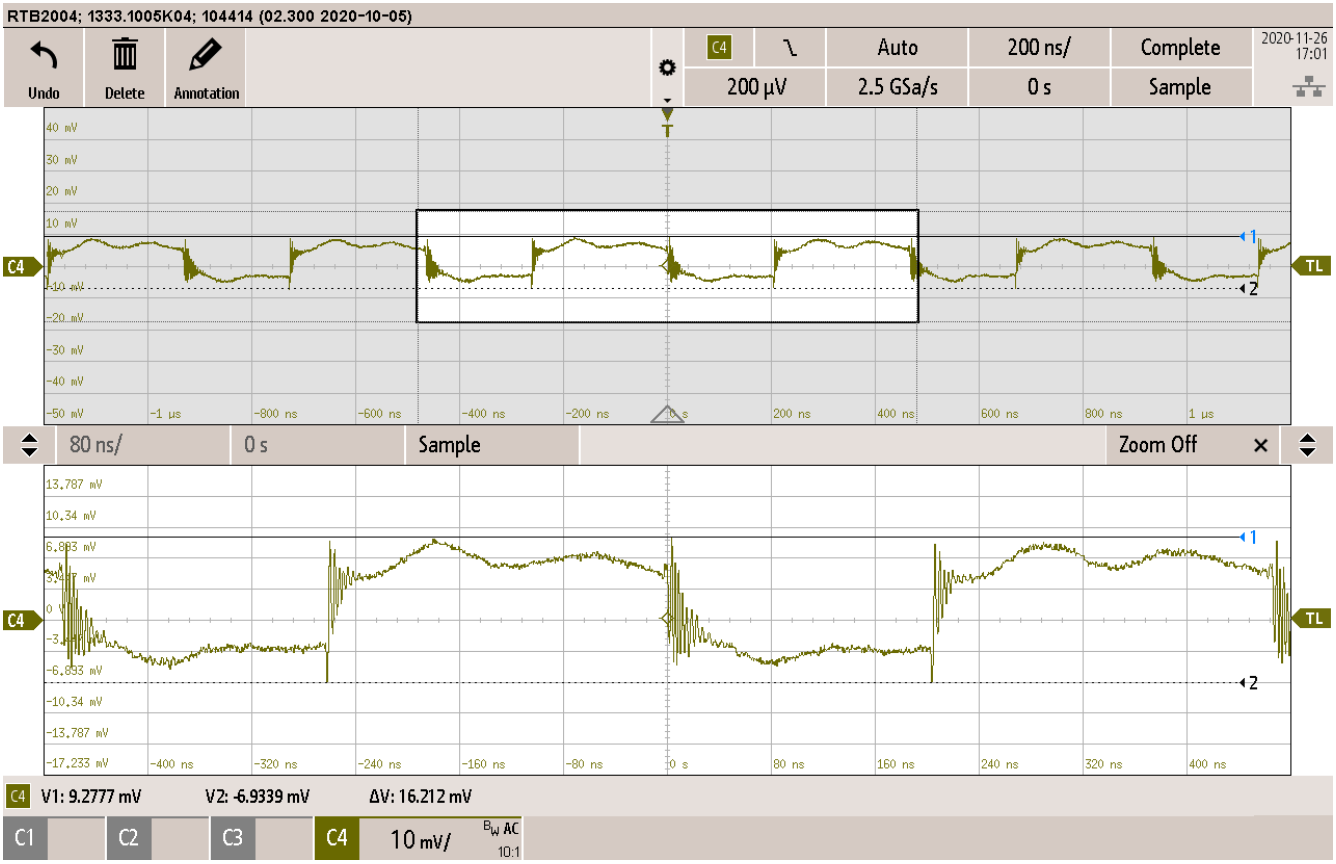


Figure 4-3. LMR50410-Q1 Output Voltage Ripple in CCM Mode

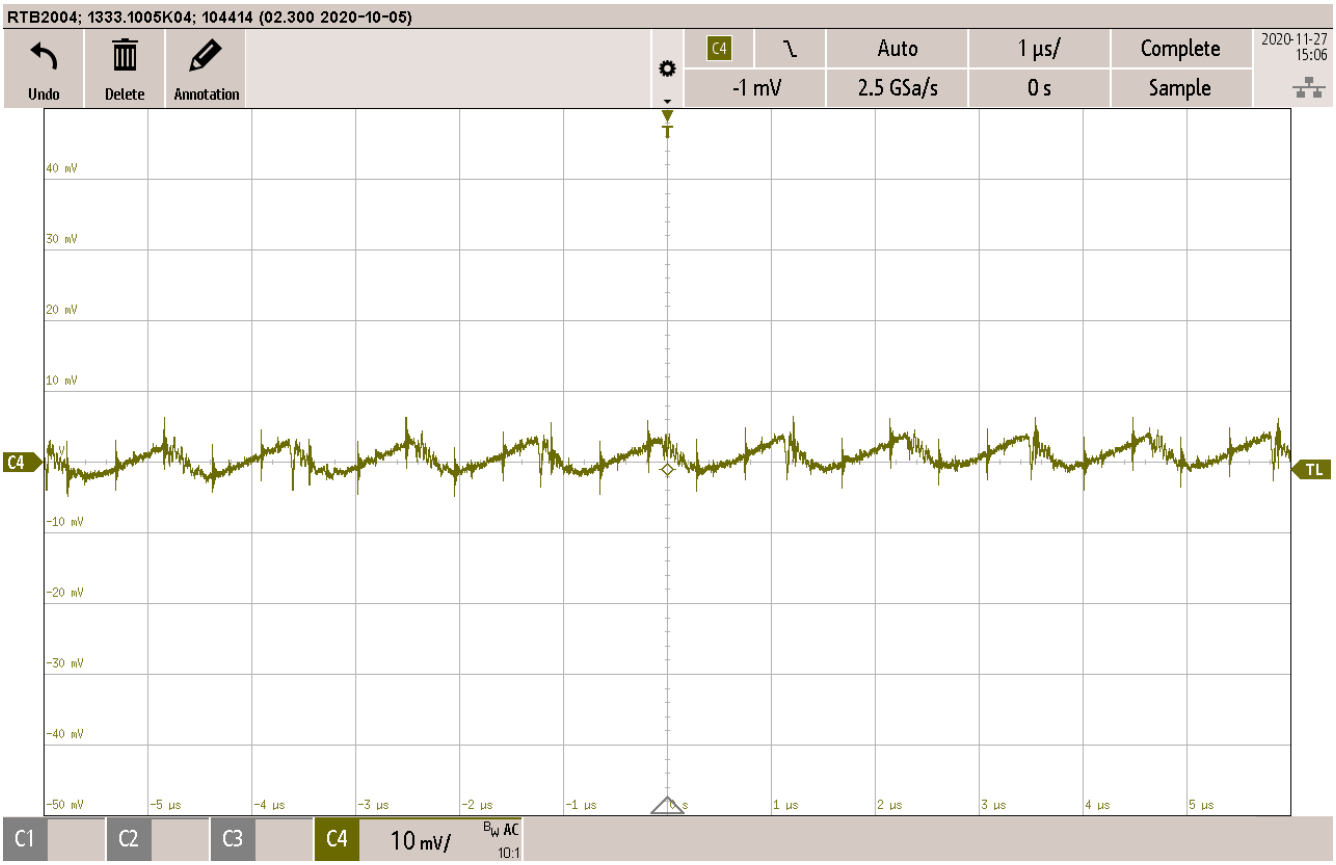


Figure 4-4. SN6505-Q1 Output Voltage Ripple

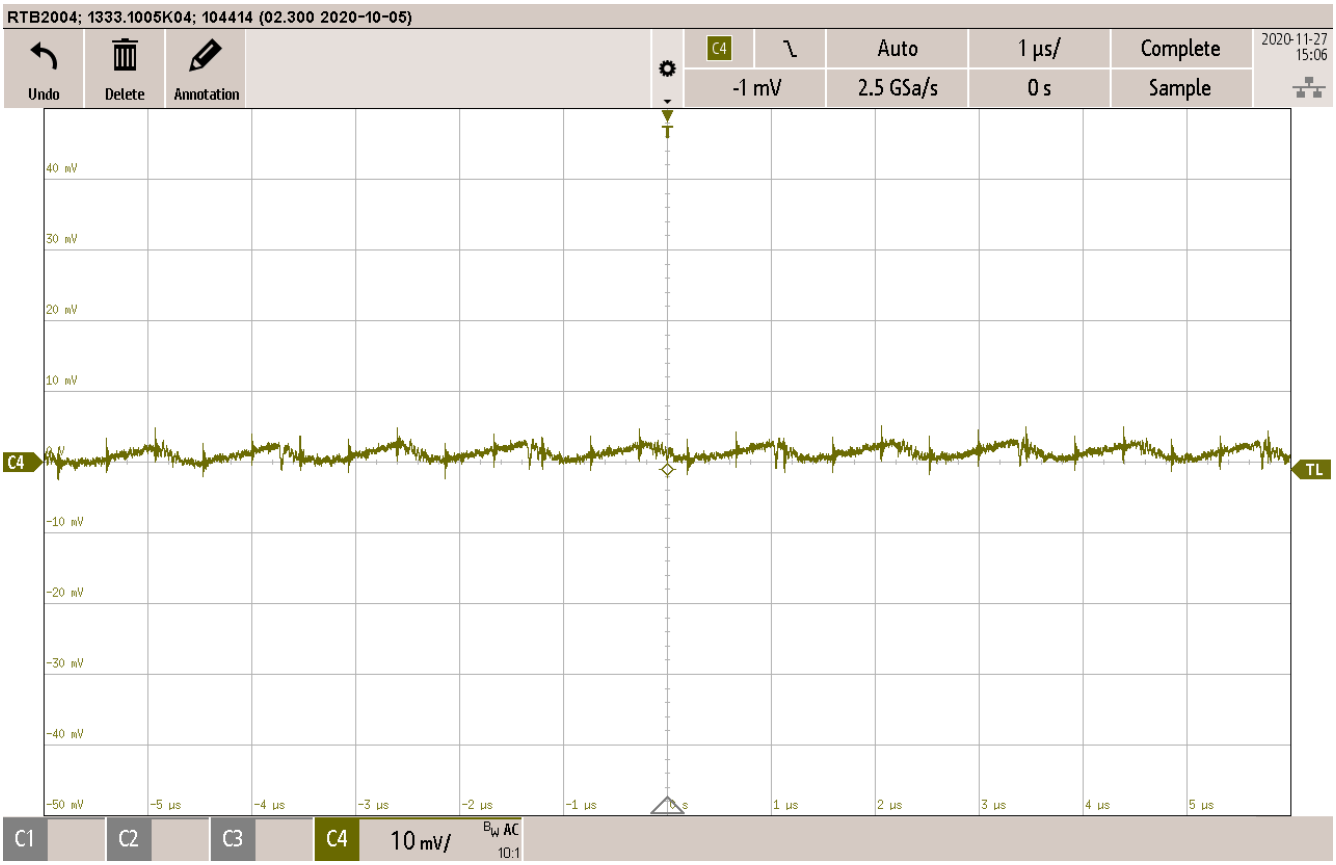
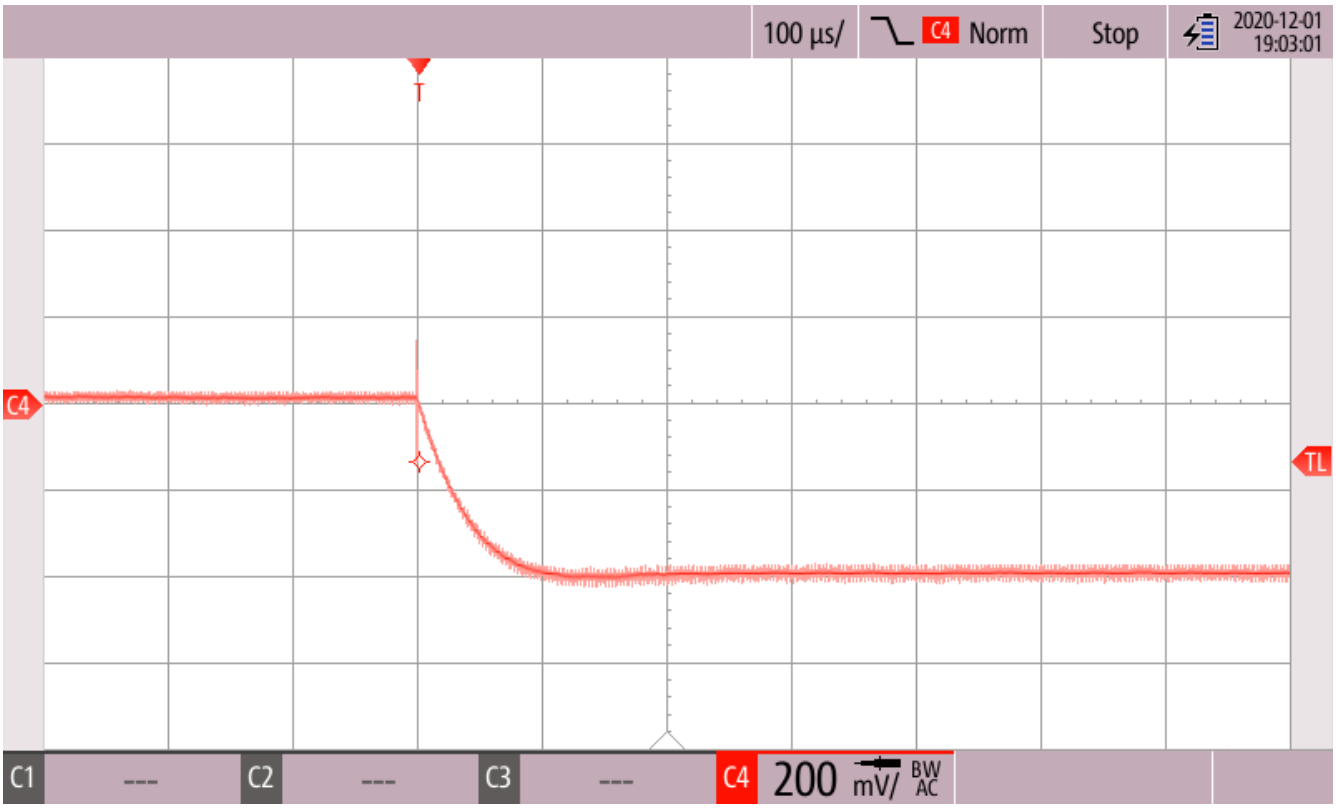


Figure 4-5. SN6505-Q1 Output Voltage Ripple

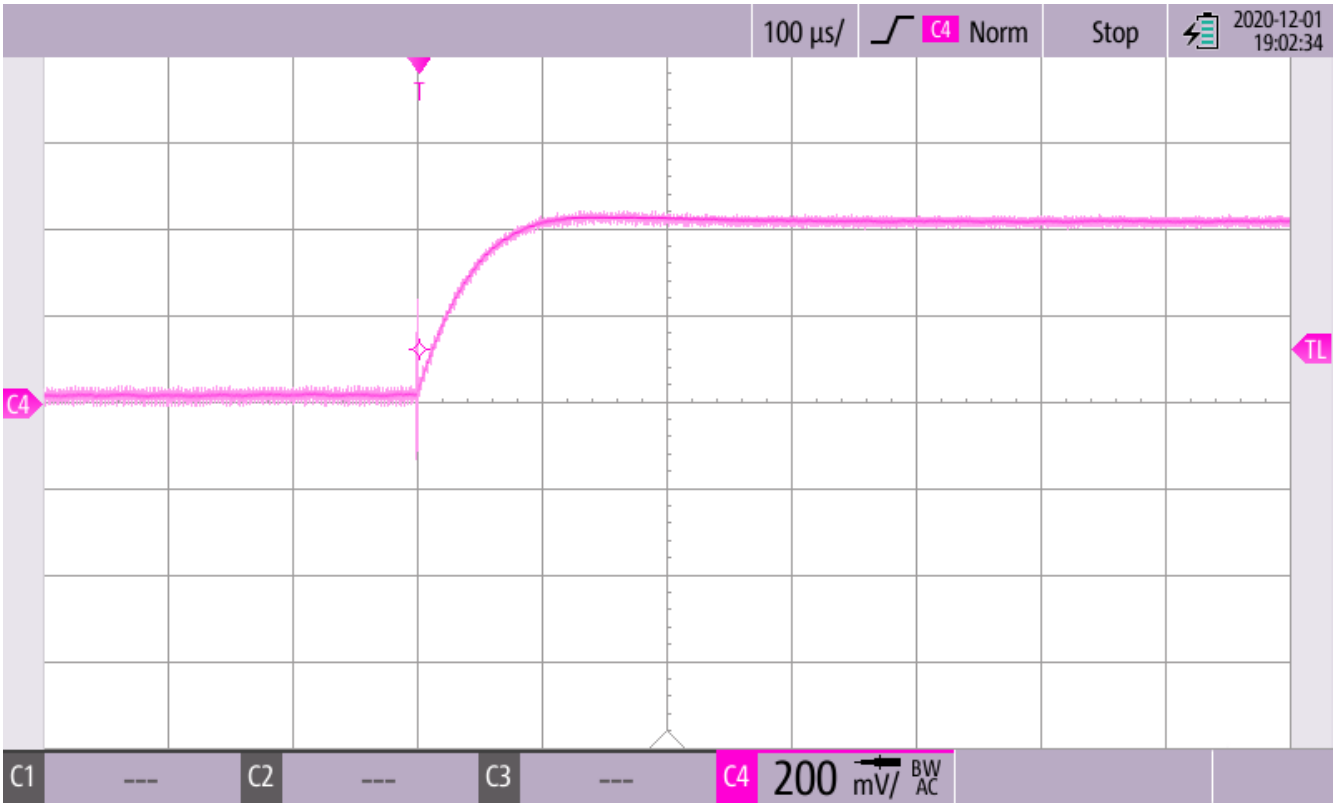
4.3 Load Transients

The following waveforms show the load transients.



Scope Rider handheld oscilloscope with isolated channels

Figure 4-6. V_{OUT1} During the Transient From 330- to 165-Ω Resistive Load

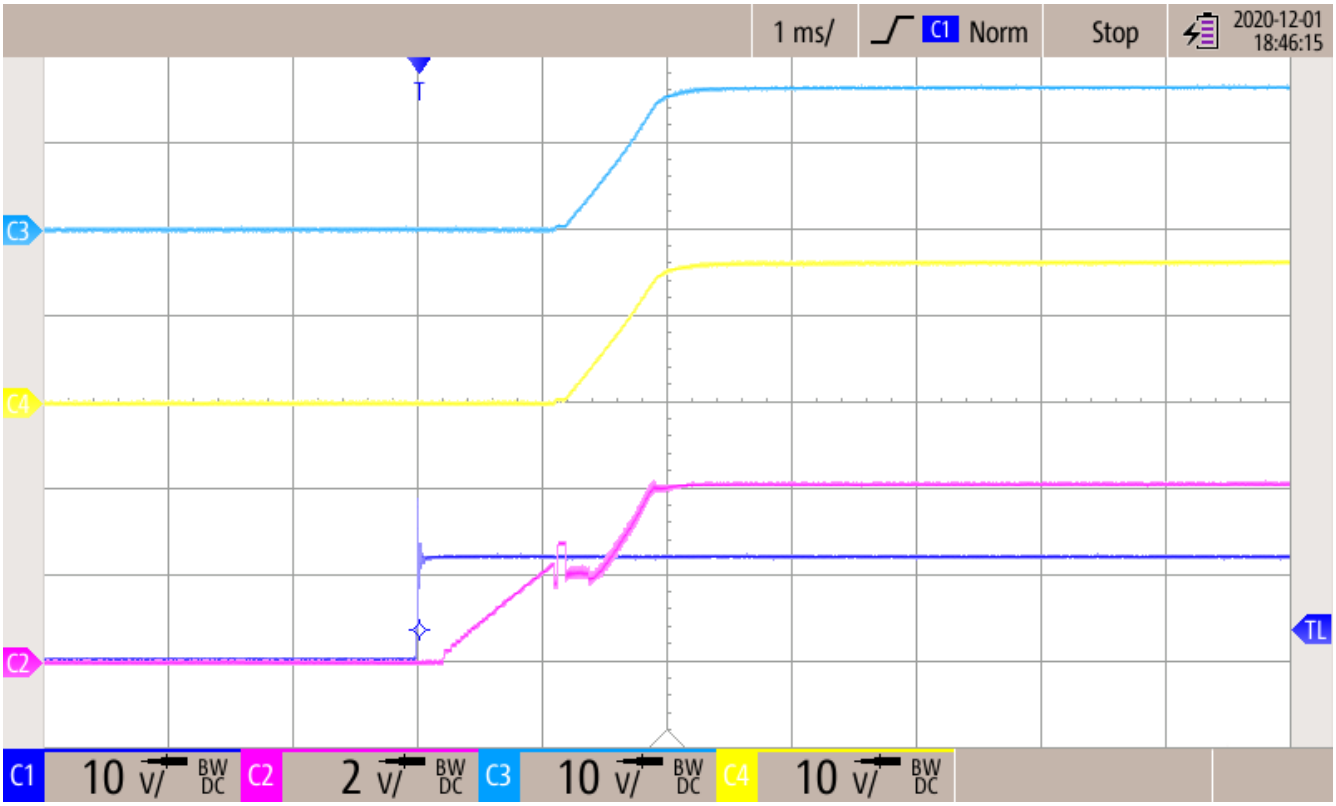


Scope Rider handheld oscilloscope with isolated channels

Figure 4-7. V_{OUT1} During the Transient From 165- to 330-Ω Resistive Load

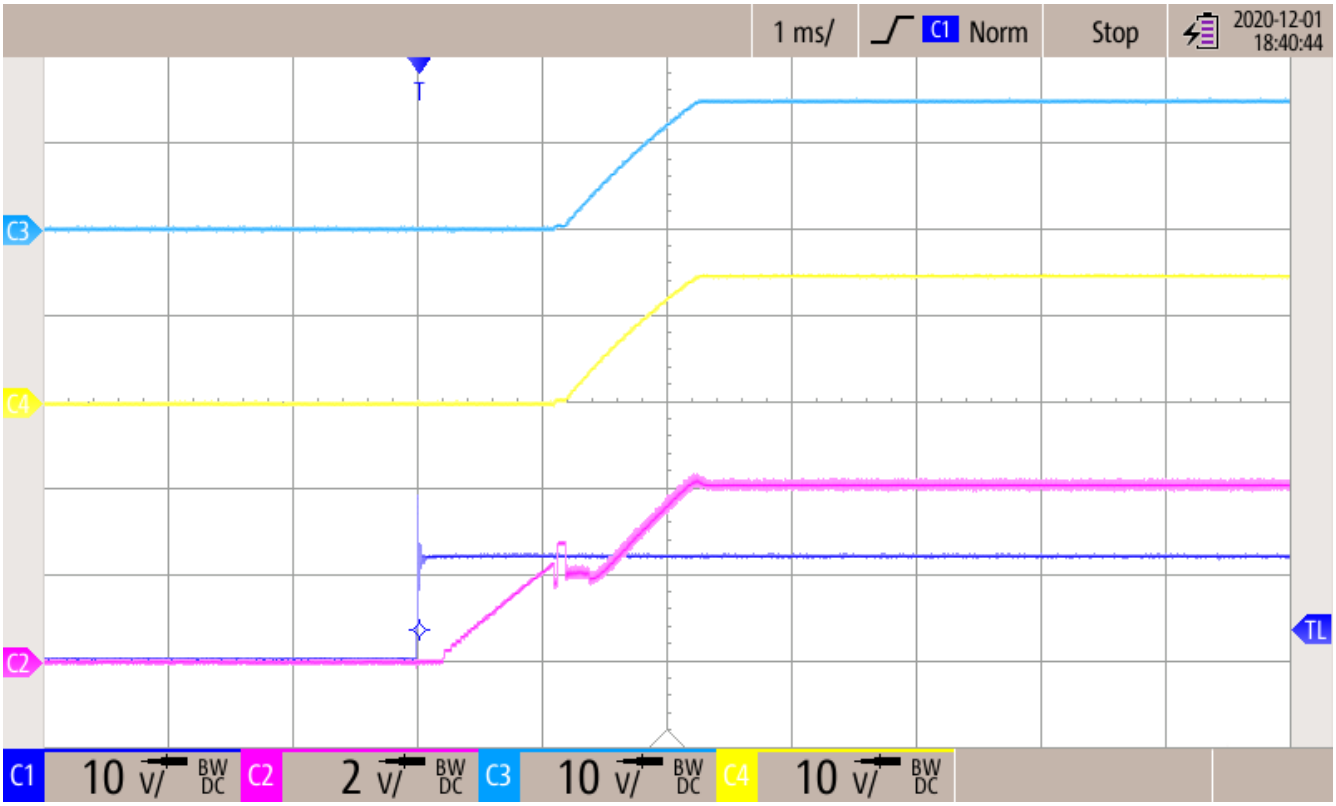
4.4 Start-up Sequence

The oscilloscope screenshot in Figure 4-8 shows start-up to the no-load condition. Note that the glitch at the output of the buck converter happens when the SN6505-Q1 starts switching. Figure 4-9 illustrates how soft-start (SN6505B-Q1) improves this behavior. Both of the waveforms are taken using a Scope Rider handheld oscilloscope with isolated channels.



CH1 - V_{IN}, CH2 - $V_{out-bck}$, CH3 - V_{OUT1}, CH4 - V_{OUT2}

Figure 4-8. Start-up to No-Load Condition



CH1 - V_{IN}, CH2 - $V_{out-bck}$, CH3 - V_{OUT1}, CH4 - V_{OUT2}

Figure 4-9. Start-up to 2 × 150-Ω Load

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265