Test Report: PMP22771

Four Output Flyback Bias Converter Reference Design for Inverter and Motor Drive Applications

1 Description

This isolated primary regulated flyback converter provides a total of eight output voltages. These outputs consist of four isolated pairs of +18-V and –5.1-V outputs, with three pairs capable of 25 mA maximum for and one capable of 75 mA maximum. These outputs are designed to be used as an IGBT driver bias supply for a total of six IGBTs (25 mA for three high-side drivers and 75 mA for three low-side drivers). It operates over an input voltage range of 7 V–32 V in a compact form factor with a single transformer.

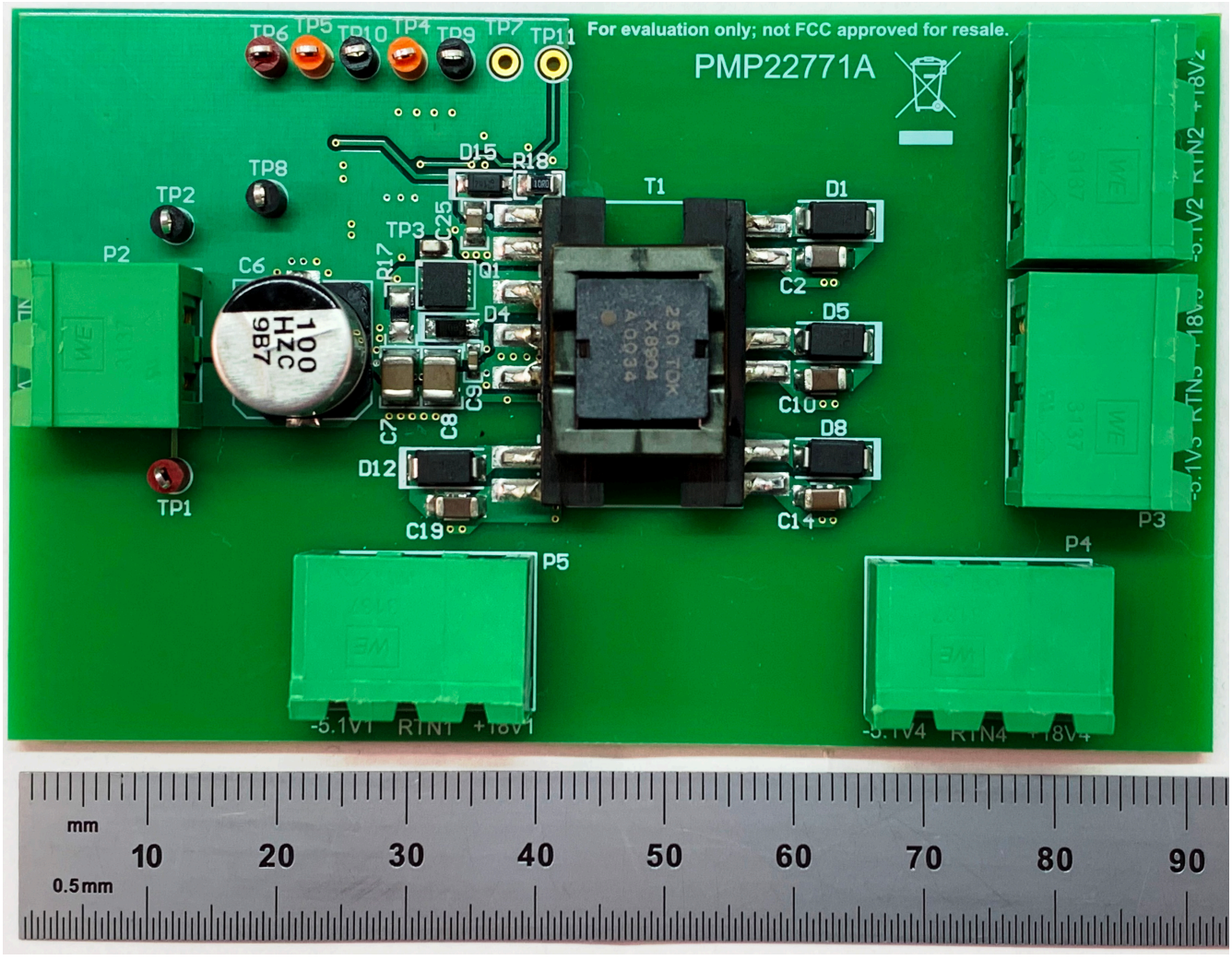


Figure 1-1. Top of PCB

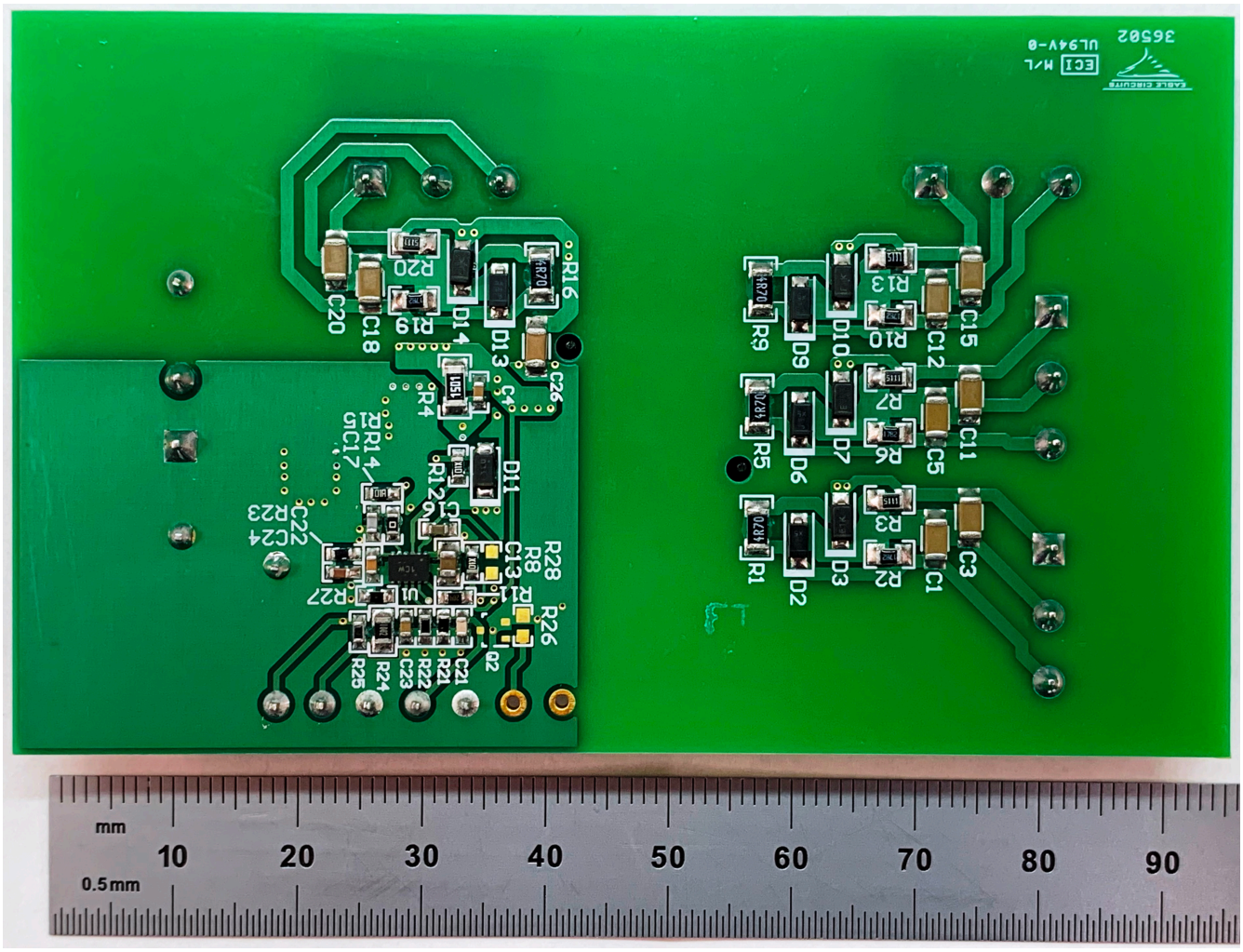


Figure 1-2. Bottom of PCB

2 Test Prerequisites

2.1 Voltage and Current Requirements

Table 2-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage range	7 V–32 V
Output voltage and current	+18 V and –5.1 V, 75 mA (3X) +18 V and –5.1 V, 25 mA
Switching frequency	400 kHz
Isolation	2600 VAC (NP, NF-NS), 1300 VAC (coil-coil)

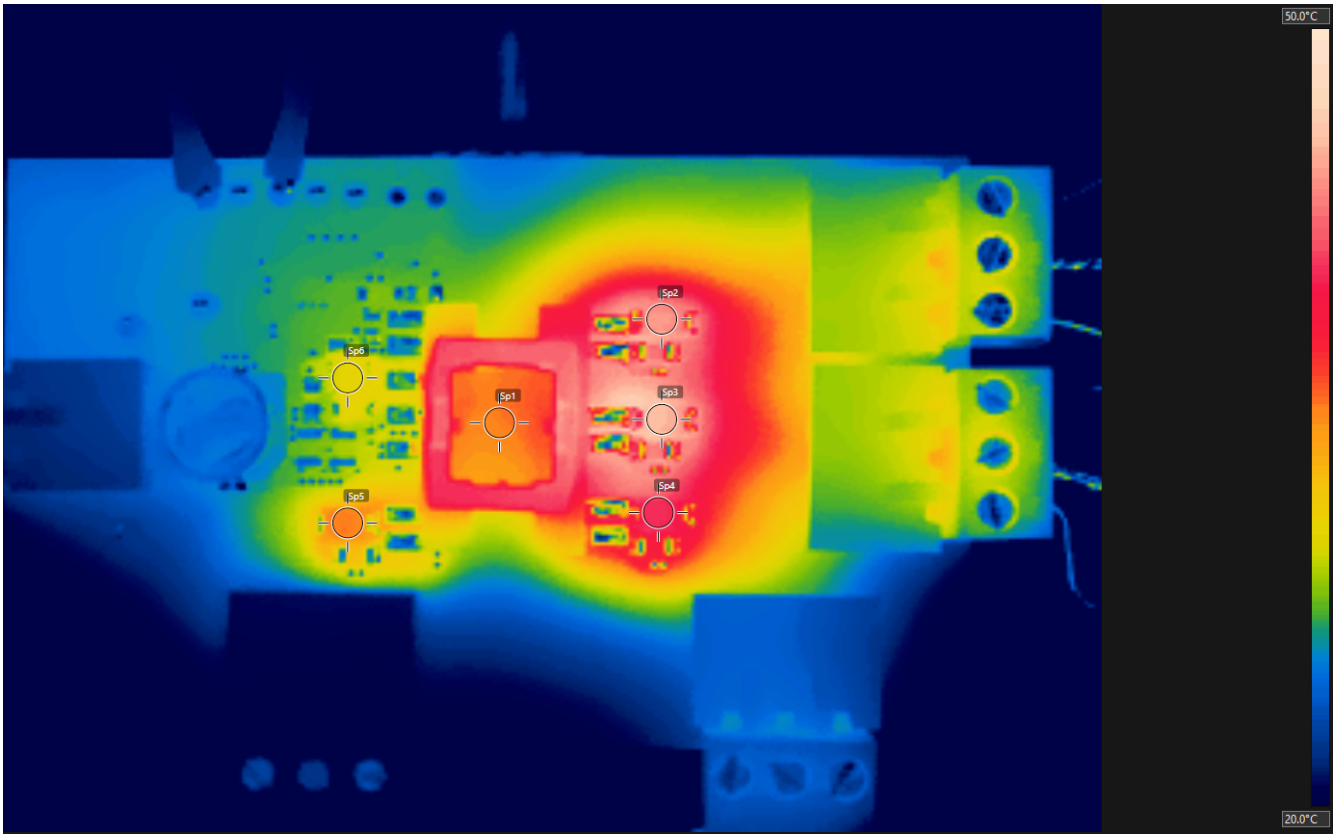
2.2 Required Equipment

- Four loads (2 W each)
- Power supply capable of 50 V and 1 A
- Oscilloscope and probes
- Digital multimeters
- Stability measurement device (Venable or Bode100)

3 Testing and Results

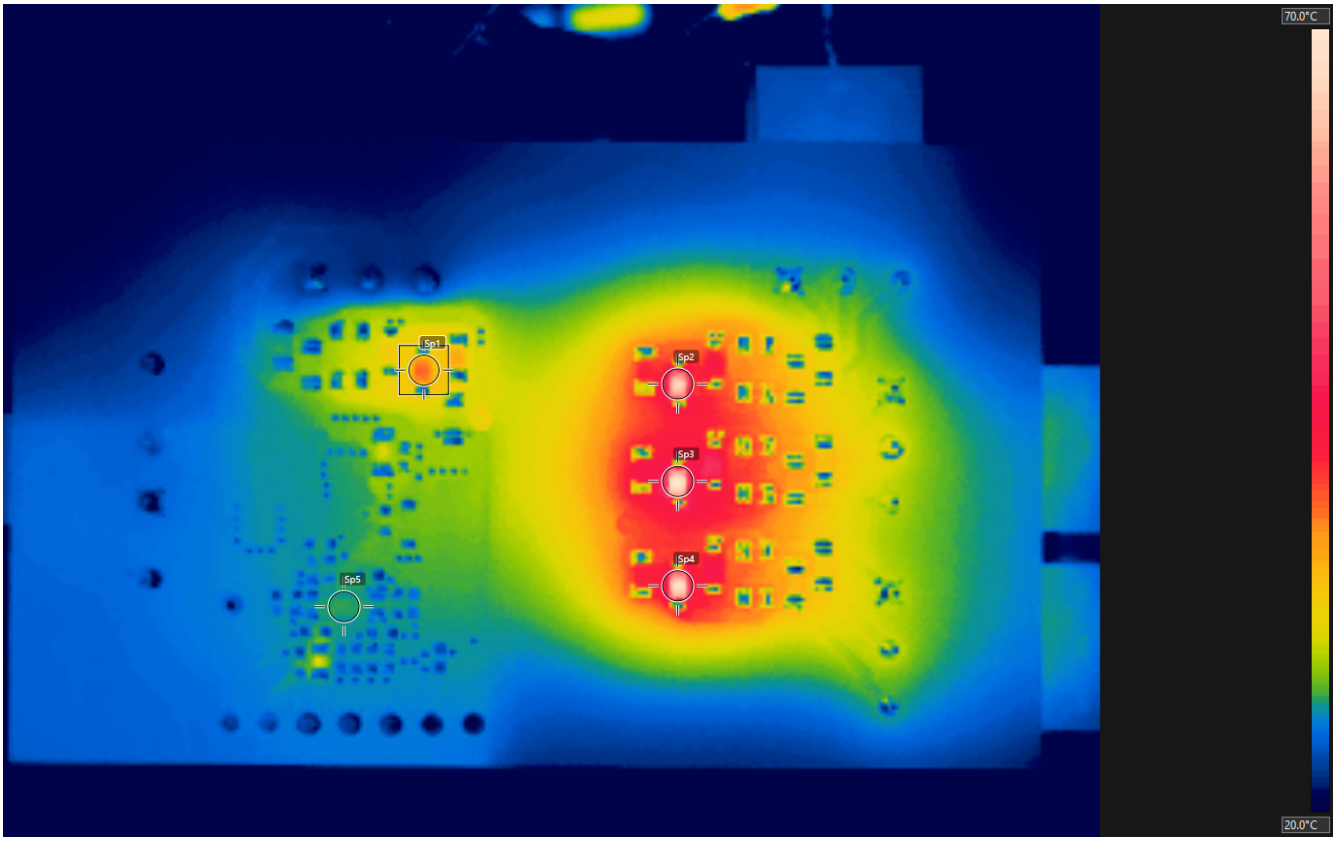
3.1 Thermal Images

These thermal images show the operating temperature of the top and bottom of the board with 12-V input and all outputs at full load. The images were captured at room temperature after operating for 30 minutes.



Measurement Location	Temperature (C)
Sp1	36.3
Sp2	44.8
Sp3	45.9
Sp4	41.4
Sp5	36.3
Sp6	31.8

Figure 3-1. Top Side Thermal Image



Measurement Location	Temperature (C)
Sp1	42.0
Sp2	67.6
Sp3	70.6
Sp4	69.2
Sp5	28.8

Figure 3-2. Bottom Side Thermal Image

3.2 Efficiency and Power Dissipation Graphs

This data displays the efficiency and power dissipation of the converter at 50% and 100% of maximum output power at four different input voltages (7 V, 12 V, 16 V, and 24 V).

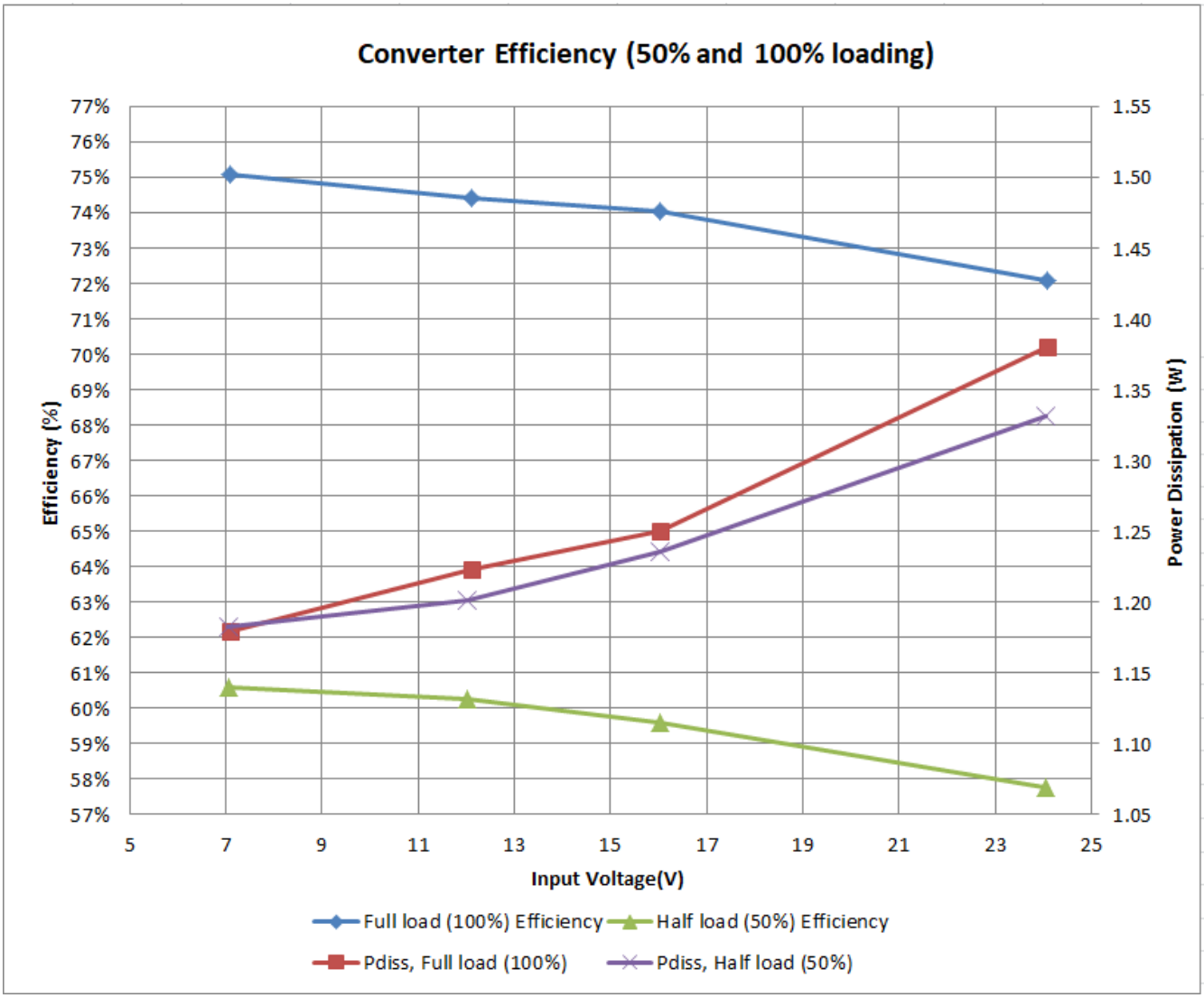


Figure 3-3. Efficiency and Power Dissipation Graph

Resistive loads were used as shown in the following table.

	Resistance (ohms)							
	18V/75mA	5.1V/75mA	18V/25mA	5.1V/25mA	18V/25mA	5.1V/25mA	18V/25mA	5.1V/25mA
50% load	480	136	1430	400	1430	400	1430	400
100% load	240	68	720	200	720	200	720	200

Figure 3-4. Converter Load Resistance

3.3 Efficiency and Power Dissipation Data

The following image shows the efficiency data for the converter

Vin	Iin	Vout1	Vout1	Vout2	Vout2	Vout3	Vout3	Vout4	Vout4	Po	Pin	Efficiency, Full load (100%)	Pdiss, Full load (100%)
7.0790	0.6696	18.128	-5.008	18.569	-5.081	18.562	-5.094	18.549	-5.055	3.560	4.740	75.1%	1.180
12.1046	0.3954	18.136	-5.008	18.575	-5.094	18.579	-5.079	18.570	-5.053	3.563	4.786	74.4%	1.223
16.0233	0.3006	18.143	-5.009	18.585	-5.095	18.587	-5.079	18.583	-5.052	3.566	4.817	74.0%	1.251
24.0924	0.2055	18.152	-5.010	18.602	-5.096	18.603	-5.078	18.607	-5.051	3.570	4.951	72.1%	1.381
Vin	**Iin**	**Vout1**	**Vout1**	**Vout2**	**Vout2**	**Vout3**	**Vout3**	**Vout4**	**Vout4**	**Po**	**Pin**	**Efficiency, Half load (50%)**	**Pdiss, Half load (50%)**
7.0436	0.4263	18.413	-5.020	18.713	-5.098	18.715	-5.086	18.711	-5.059	1.820	3.003	60.6%	1.183
12.0147	0.2516	18.421	-5.021	18.728	-5.100	18.726	-5.086	18.730	-5.059	1.822	3.023	60.3%	1.201
16.0300	0.1908	18.426	-5.022	18.735	-5.101	18.734	-5.085	18.744	-5.058	1.823	3.059	59.6%	1.236
24.0491	0.1311	18.411	-5.021	18.717	-5.100	18.724	-5.081	18.745	-5.054	1.821	3.153	57.8%	1.332

Figure 3-5. Efficiency and Power Dissipation Data

3.4 Cross Regulation

This image shows the output voltage regulation with various 100% and 50% loading combinations with the input voltage set to 12 V.

Voltage regulation is optimally balanced between the +18 V and –5.1V when loaded equally. TI recommends keeping the load imbalance between the +18 V and the –5.1 V to less than 25% to minimize power dissipation in the output Zener diodes.

Load	**100%**	**100%**	**50%**	**50%**	**50%**	**50%**	**50%**	**50%**
Vout	18.128	-5.008	18.714	-5.100	18.721	-5.086	18.695	-5.059
Load	**50%**	**50%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**
Vout	18.406	-5.019	18.585	-5.092	18.583	-5.078	18.595	-5.054
Load	**50%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**
Vout	19.608	-3.727	18.583	-5.093	18.581	-5.080	18.585	-5.054
Load	**100%**	**50%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**
Vout	18.062	-5.112	18.574	-5.094	18.579	-5.079	18.573	-5.052
Load	**100%**	**100%**	**50%**	**100%**	**100%**	**100%**	**100%**	**100%**
Vout	18.141	-5.009	19.074	-4.683	18.591	-5.077	18.582	-5.050
Load	**100%**	**100%**	**100%**	**50%**	**100%**	**100%**	**100%**	**100%**
Vout	18.135	-5.008	18.545	-5.128	18.582	-5.076	18.576	-5.050

Figure 3-6. Output Voltage Regulation

3.5 Loop Gain

Bode plots data are shown in the following tables and figures.

Table 3-1. Voltage and Current Requirements

Vin (V)	Bandwidth (kHz)	Phase Margin (°)	Gain Margin (dB)
7	8.17	88.2	27
12	12.1	71.3	23
32	11.3	71.3	21

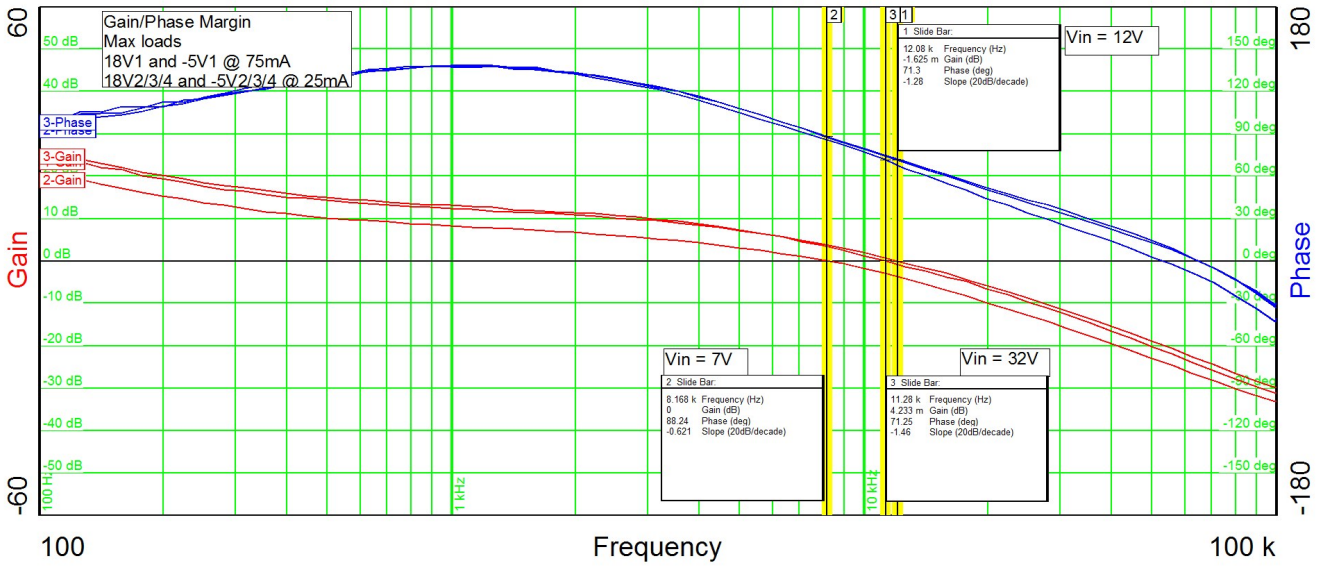


Figure 3-7. 100% Loading; +18 V and –5.1 V at 75 mA and (3X) +18 V and –5 V at 25 mA

Table 3-2. Voltage and Current Requirements

Vin (V)	Bandwidth (kHz)	Phase Margin (°)	Gain Margin (dB)
7	11.5	79.0	24
12	12.1	78.9	26
32	12.0	79.3	23

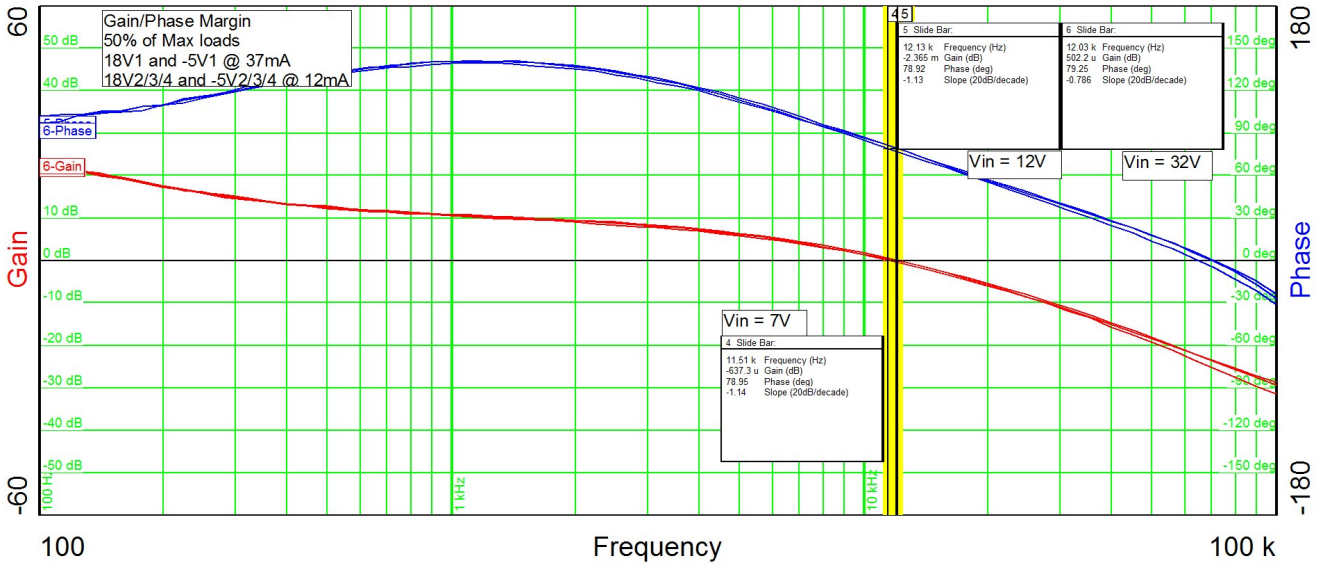
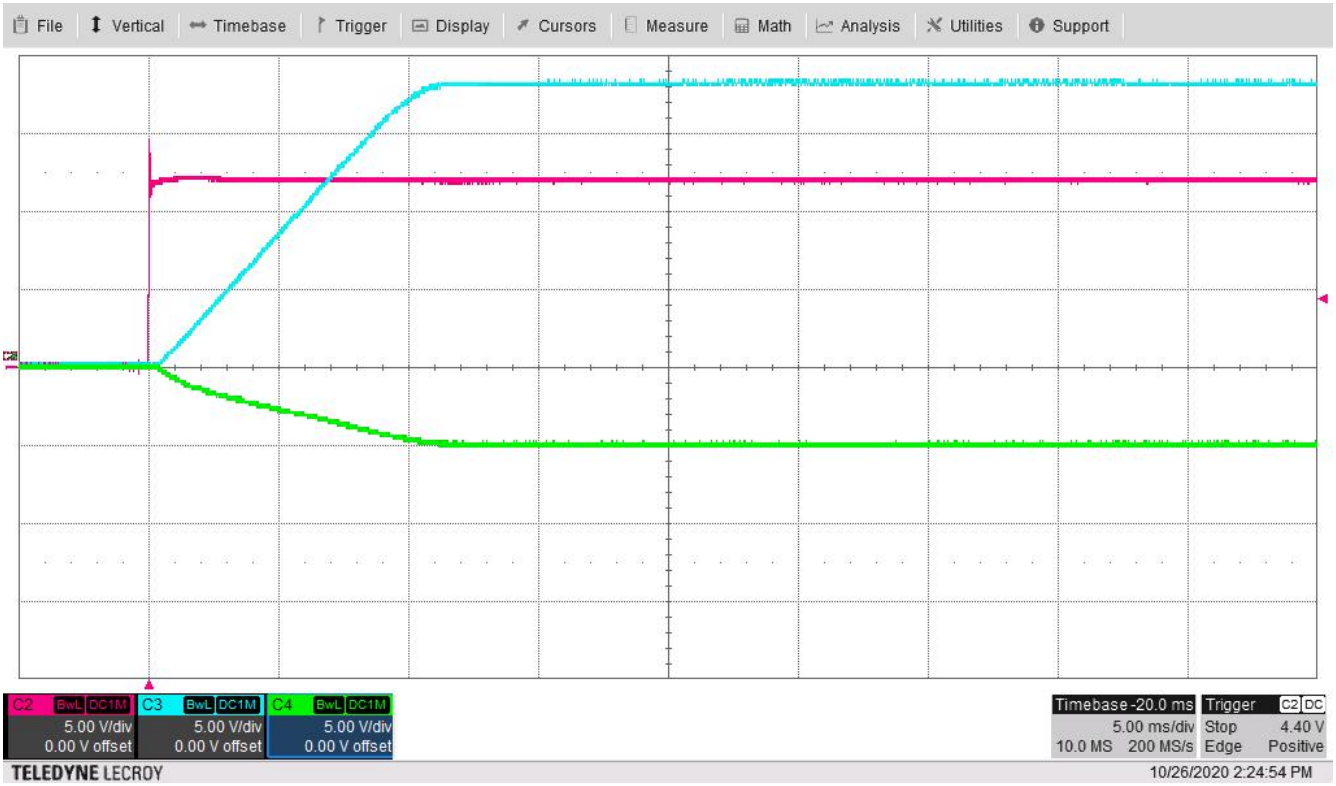


Figure 3-8. 50% Loading; +18 V and –5.1 V at 37 mA and (3X) +18 V and –5 V at 12 mA

4 Waveforms

4.1 Start-up

Start-up behavior is shown in the following figures.

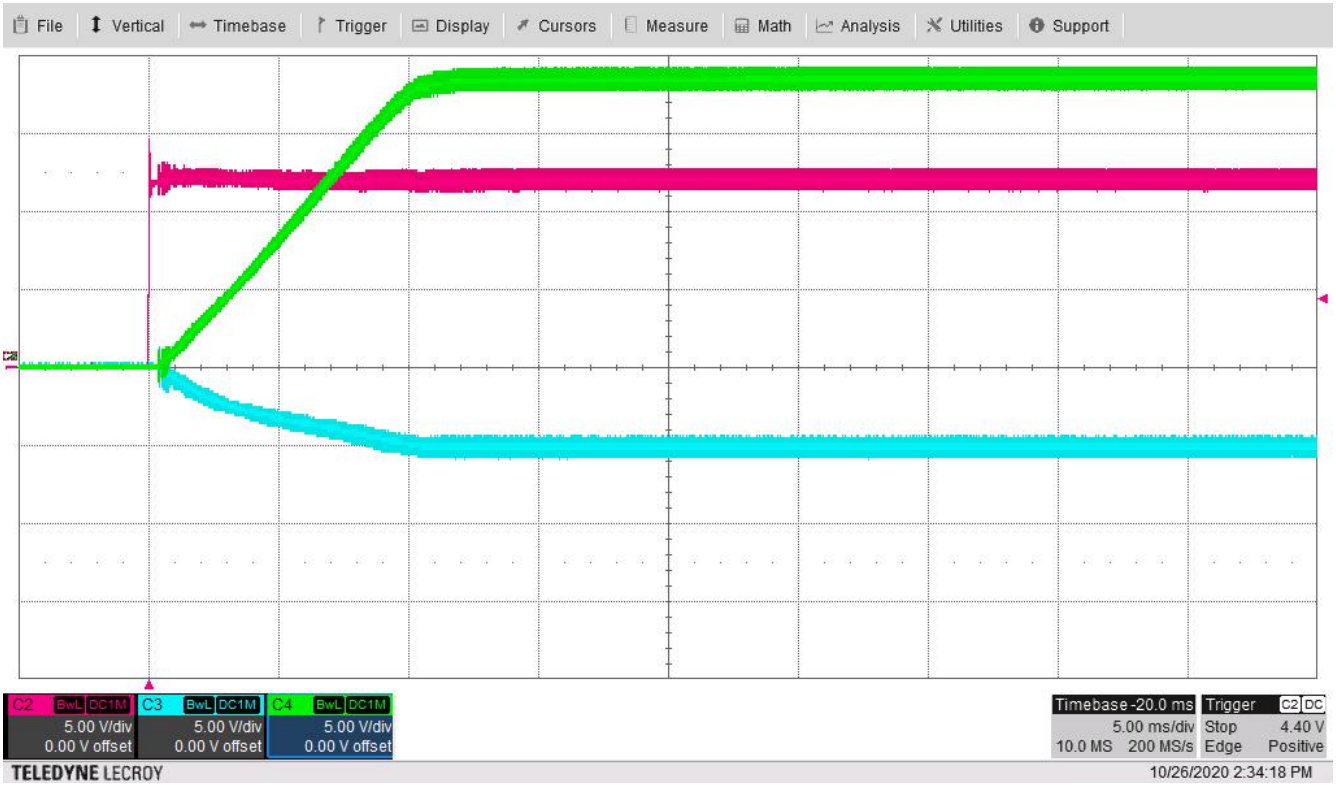


All outputs are at max loads

Figure 4-1. Start-up Sequence for +18V1 (Blue) and –5.1V1 (Green) With Vin = 12 V (Red)

All outputs are unloaded

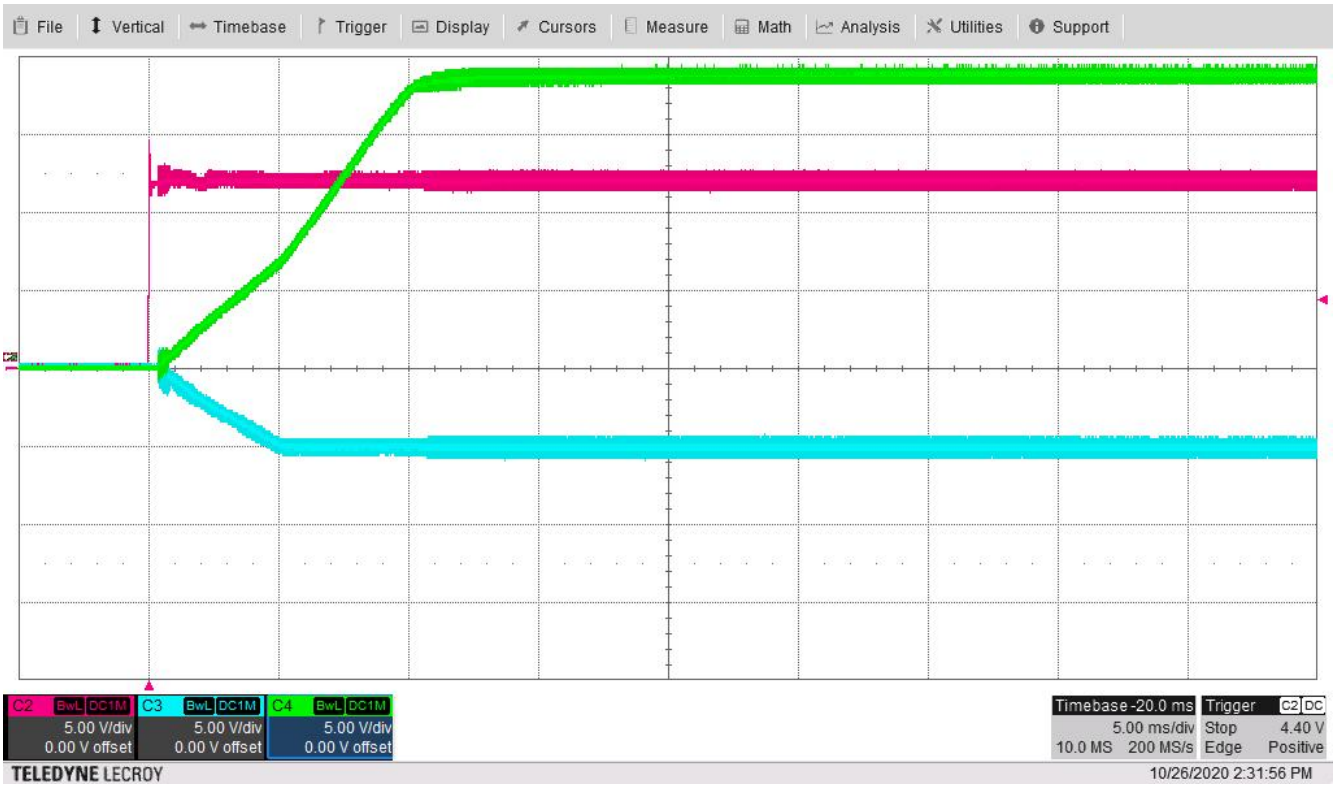
Figure 4-2. Start-up Sequence for +18V1 (Blue) and –5.1V1 (Green) With Vin = 12 V (Red)



All outputs are at max loads

Noise on isolated outputs V2, V3, or V4 can be reduced by adding a common-mode capacitor, similar to C26, on each output

Figure 4-3. Start-up Sequence for +18V4 (Blue) and –5.1V4 (Green) With Vin = 12 V (Red)



All outputs are unloaded

Figure 4-4. Start-up Sequence for +18V4 (Blue) and –5.1V4 (Green) With Vin = 12 V (Red)

4.2 Switching Waveforms

Switching behavior is shown in the following figures.

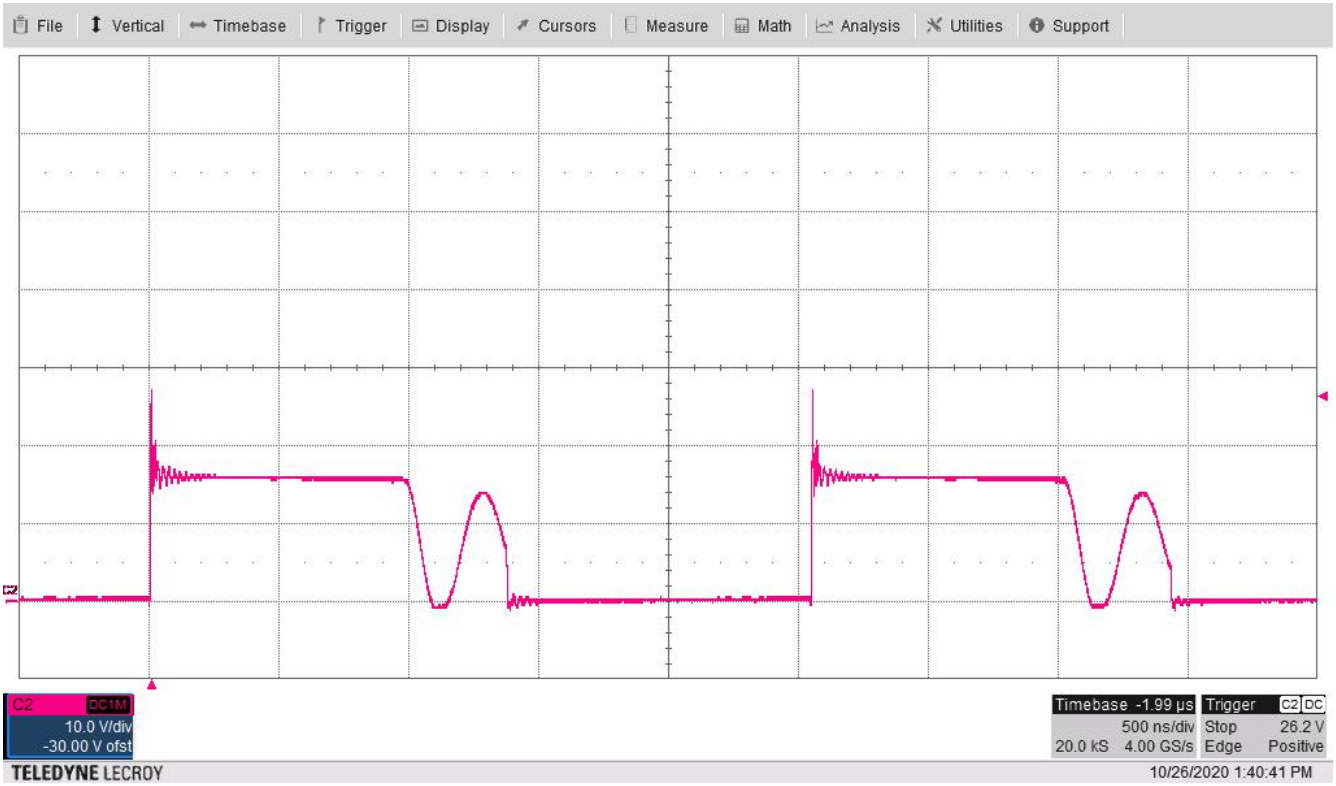


Figure 4-5. FET Switch Node Voltage at TP3 With Vin = 7 V and Maximum Loads

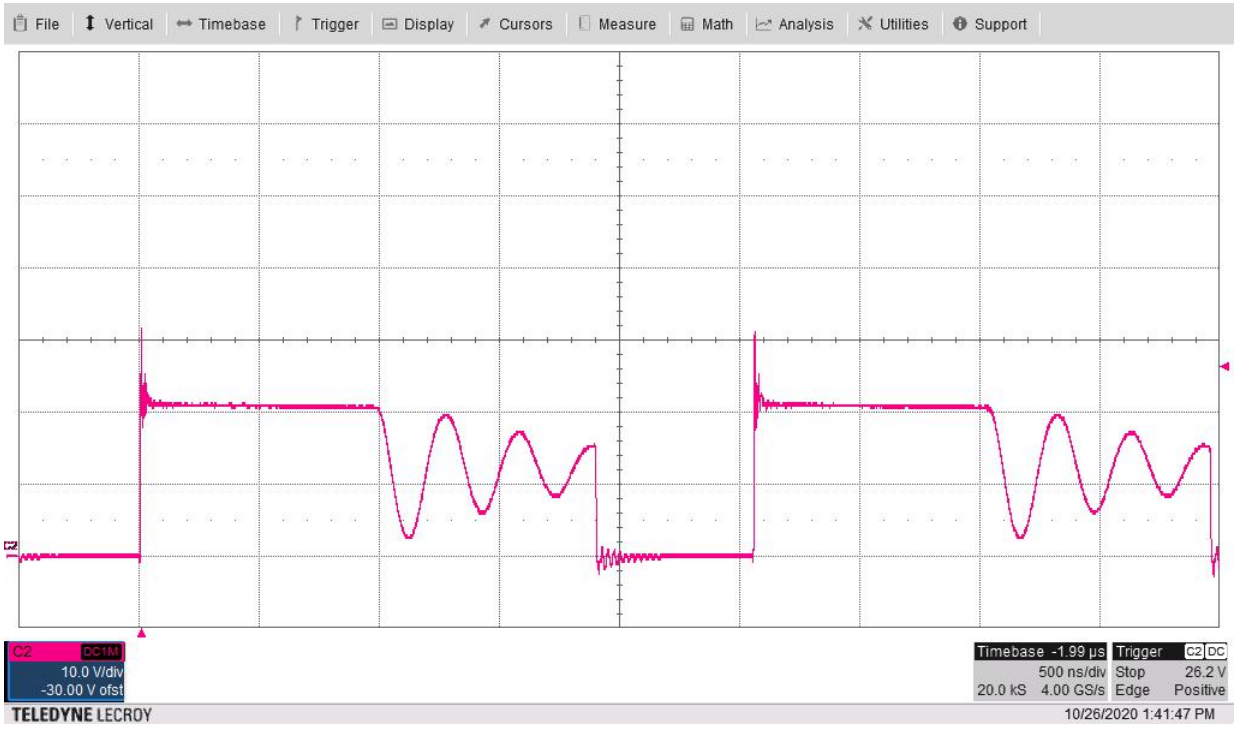


Figure 4-6. FET Switch Node Voltage at TP3 With Vin = 12 V and Maximum Loads

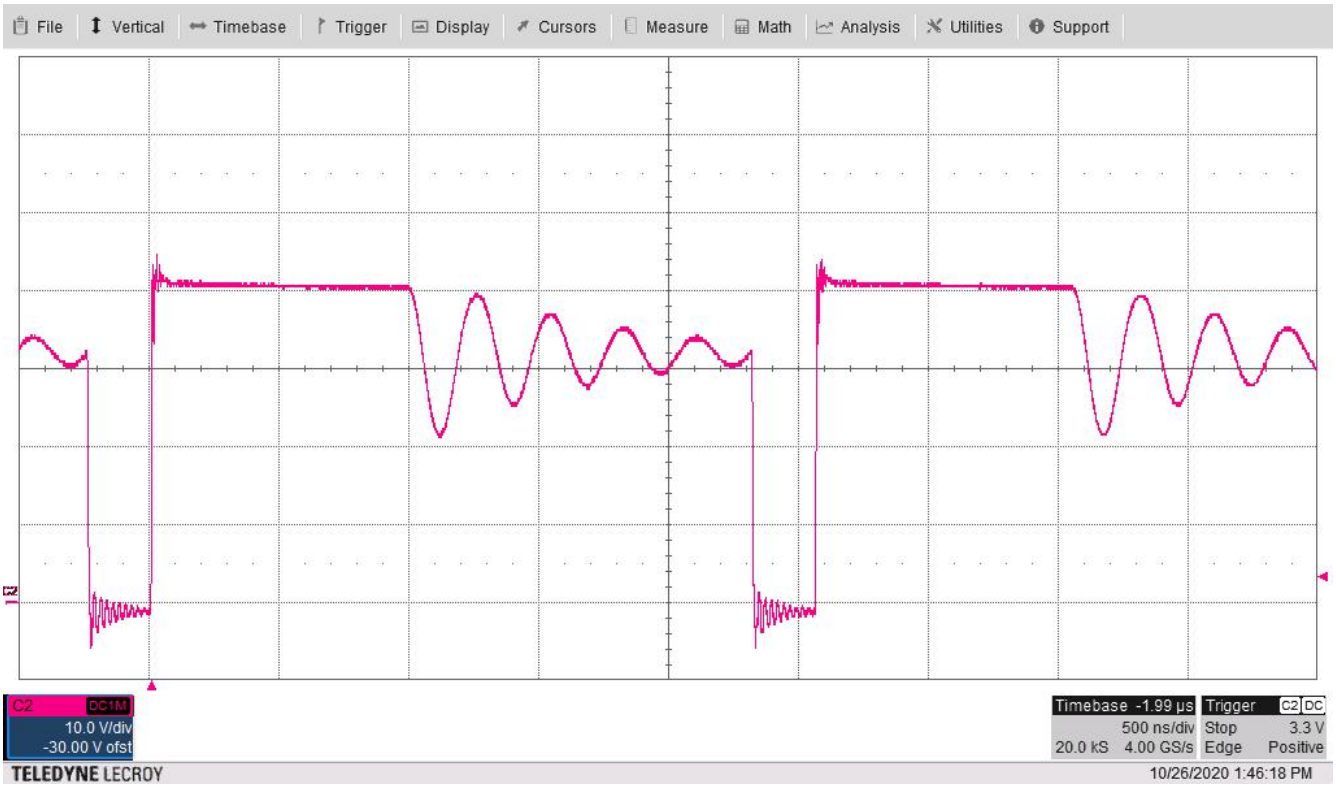


Figure 4-7. FET Switch Node Voltage at TP3 With Vin = 32 V and Maximum Loads

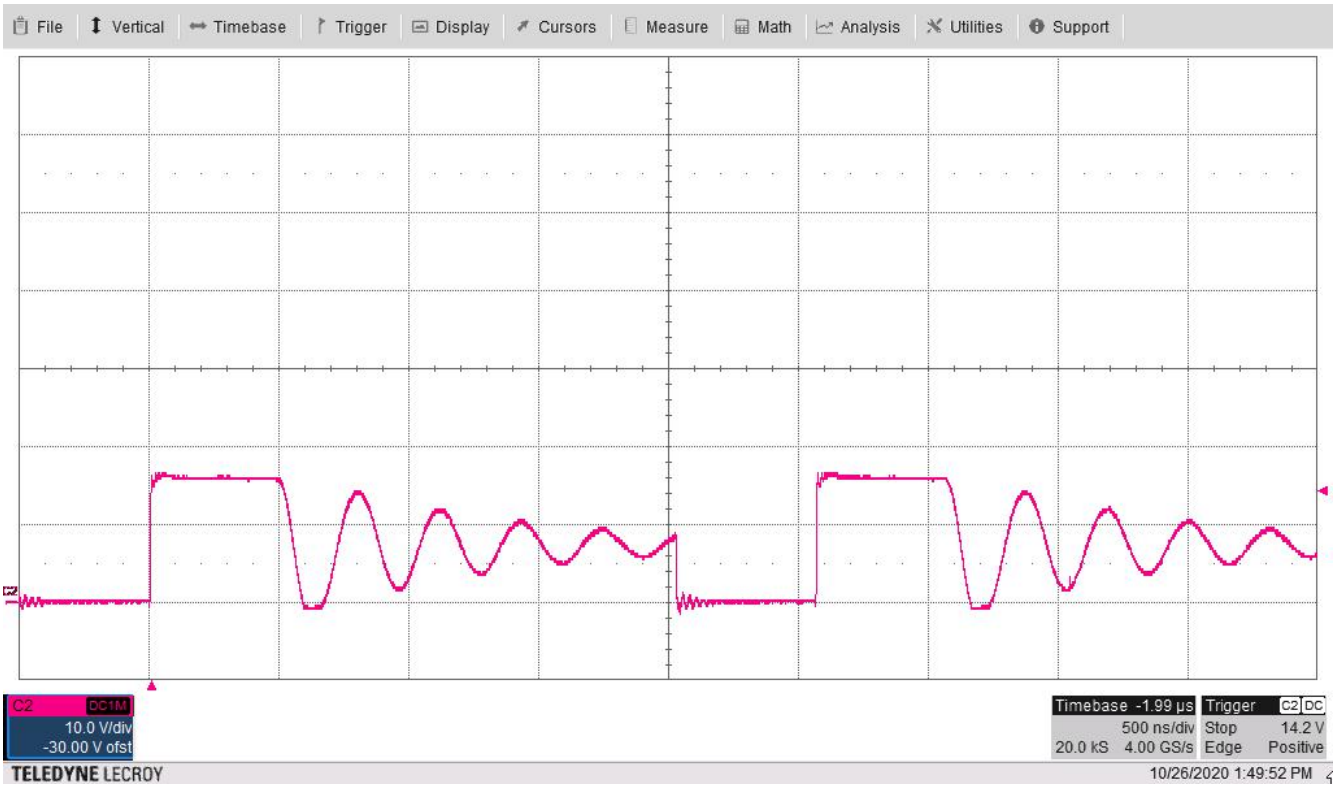


Figure 4-8. FET Switch Node Voltage at TP3 With Vin = 7 V and no Loads

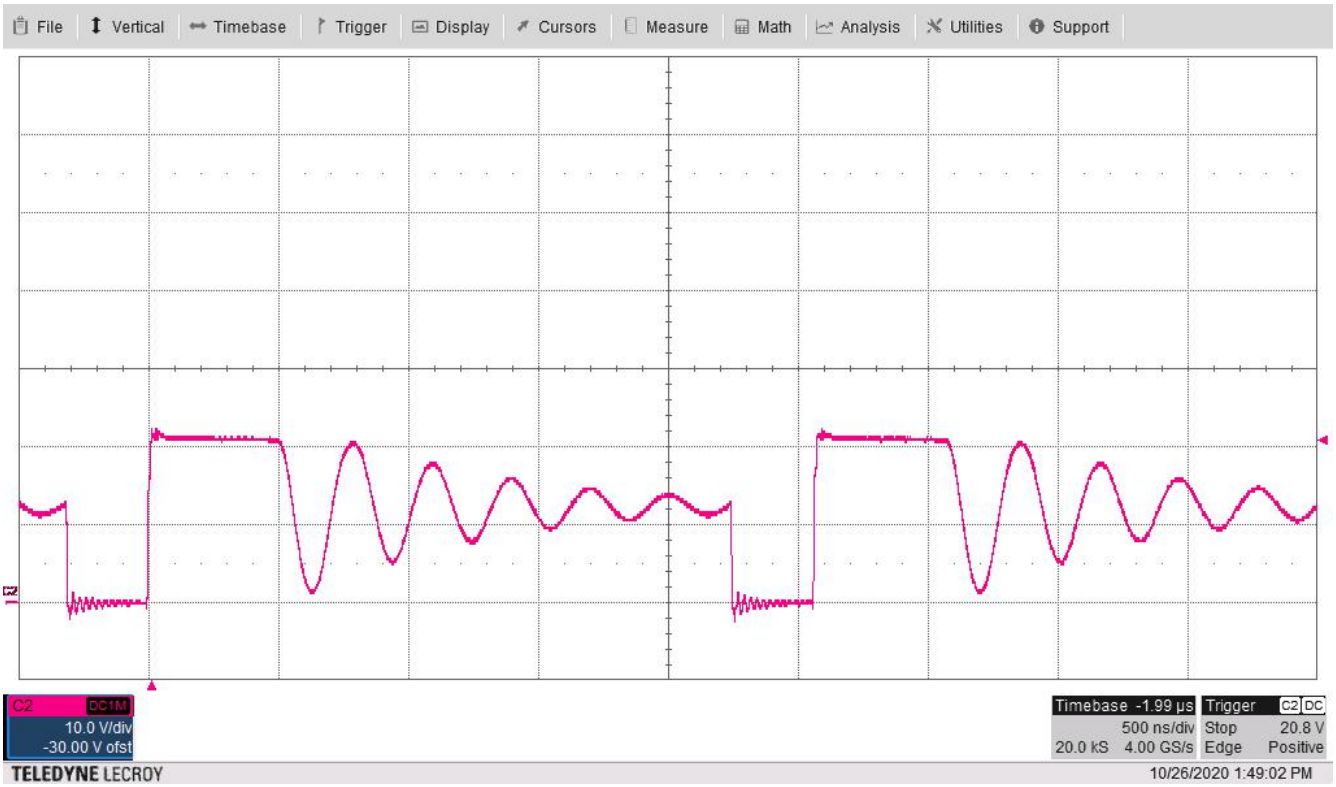


Figure 4-9. FET Switch Node Voltage at TP3 With Vin = 12 V and no Loads

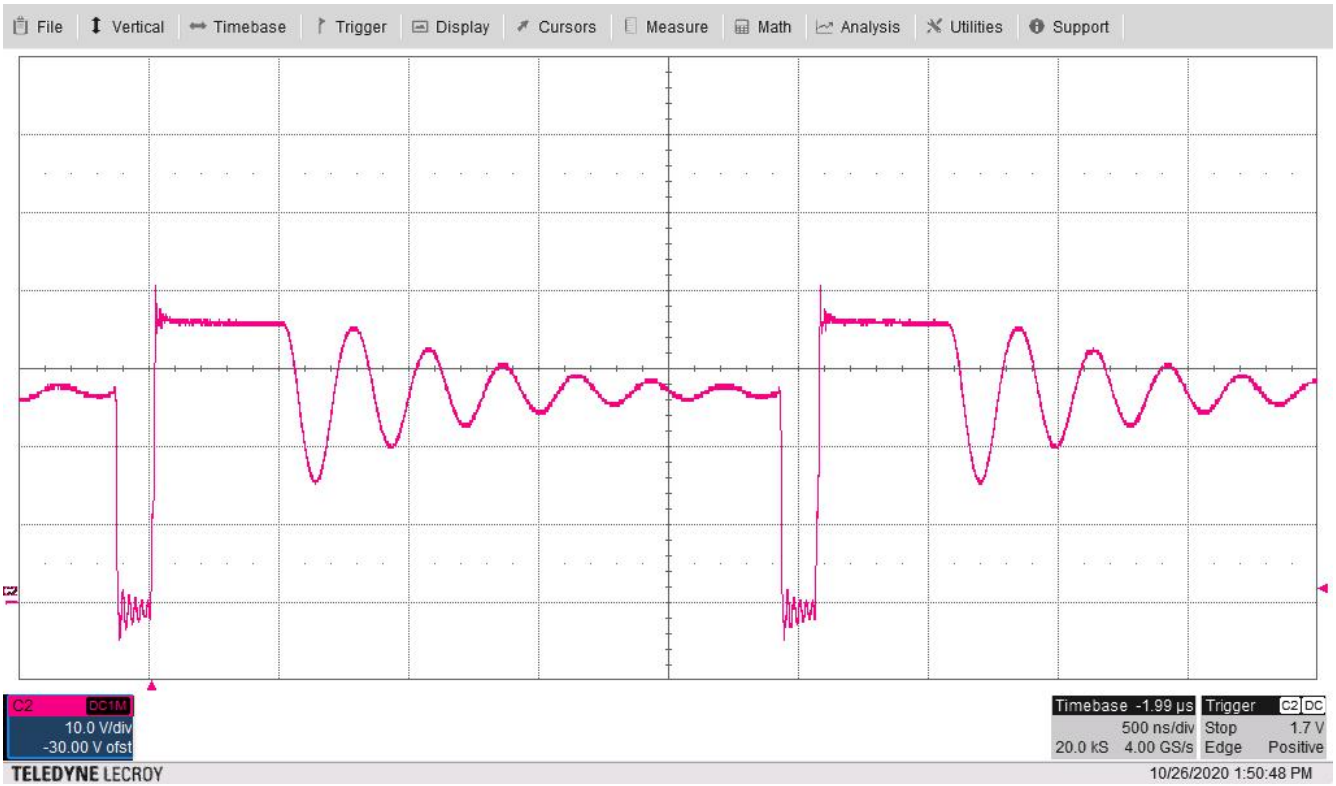


Figure 4-10. FET Switch Node Voltage at TP3 With Vin = 27 V and no Loads

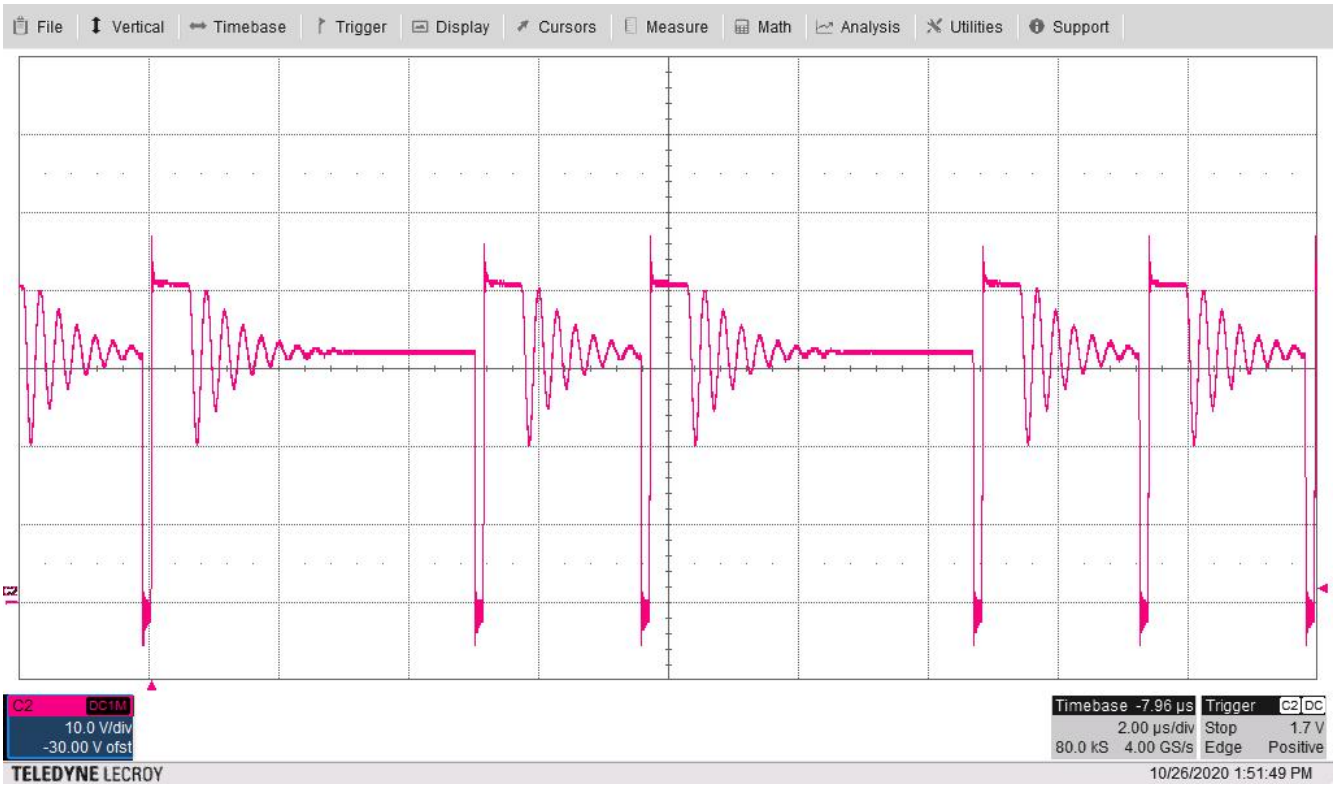


Figure 4-11. FET Switch Node Voltage at TP3 With Vin = 32 V and no Loads (Note Pulse Skipping)

4.3 Output Voltage Ripple

Output voltage ripple is shown in the following figures.

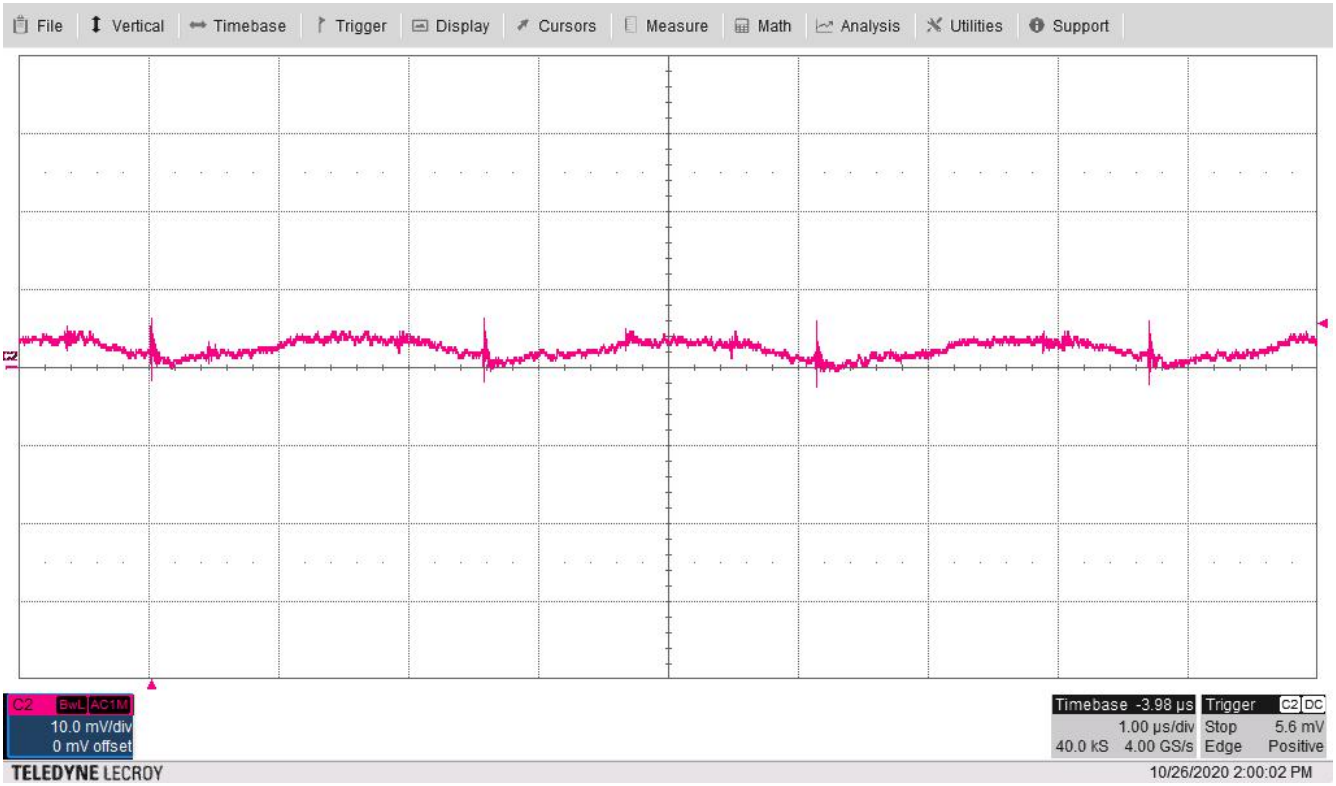


Figure 4-12. 18V1 Ripple Voltage With Vin = 12 V and all Maximum Loads, Bandwidth = 20 MHz

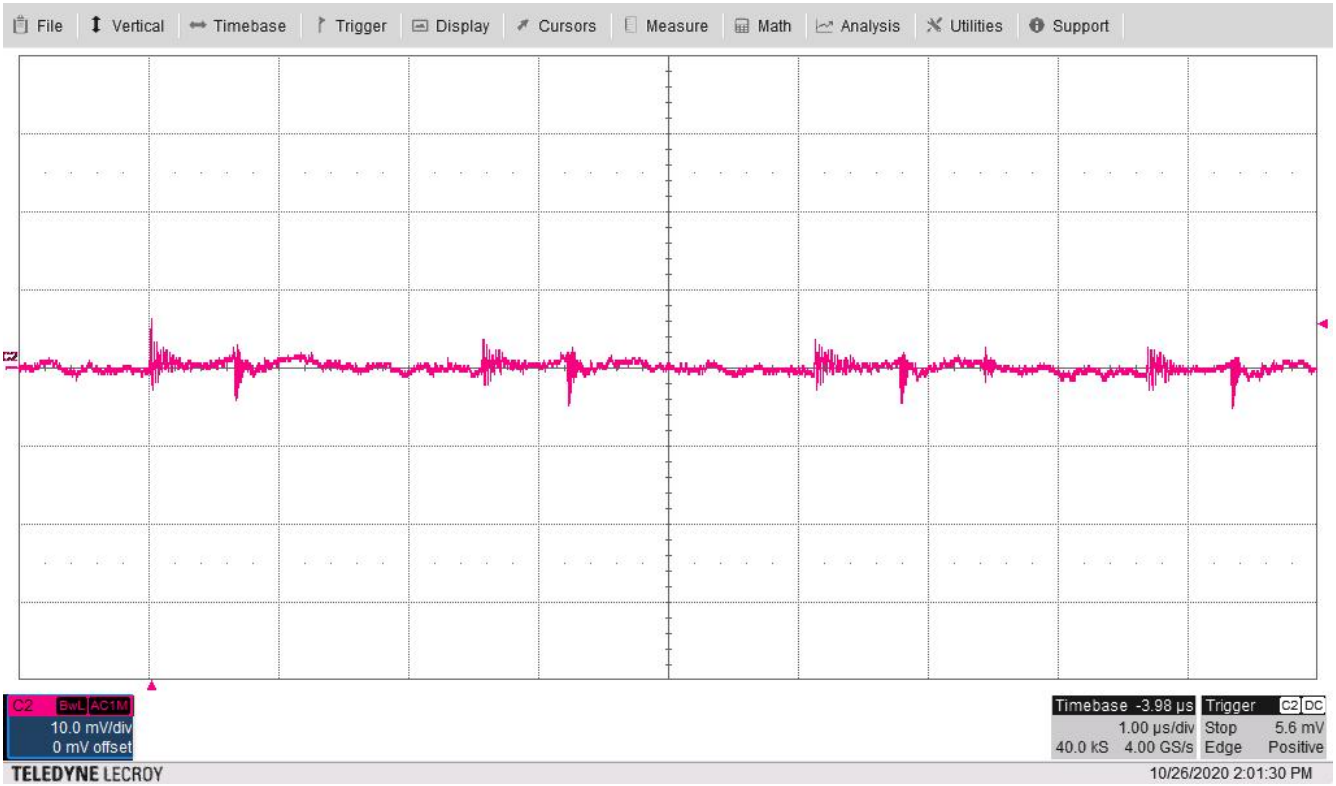


Figure 4-13. –5.1V1 Ripple Voltage With Vin = 12 V and all Maximum Loads, Bandwidth = 20 MHz

Figure 4-14. 18V2 Ripple Voltage With Vin = 12 V and all Maximum Loads, Bandwidth = 20 MHz

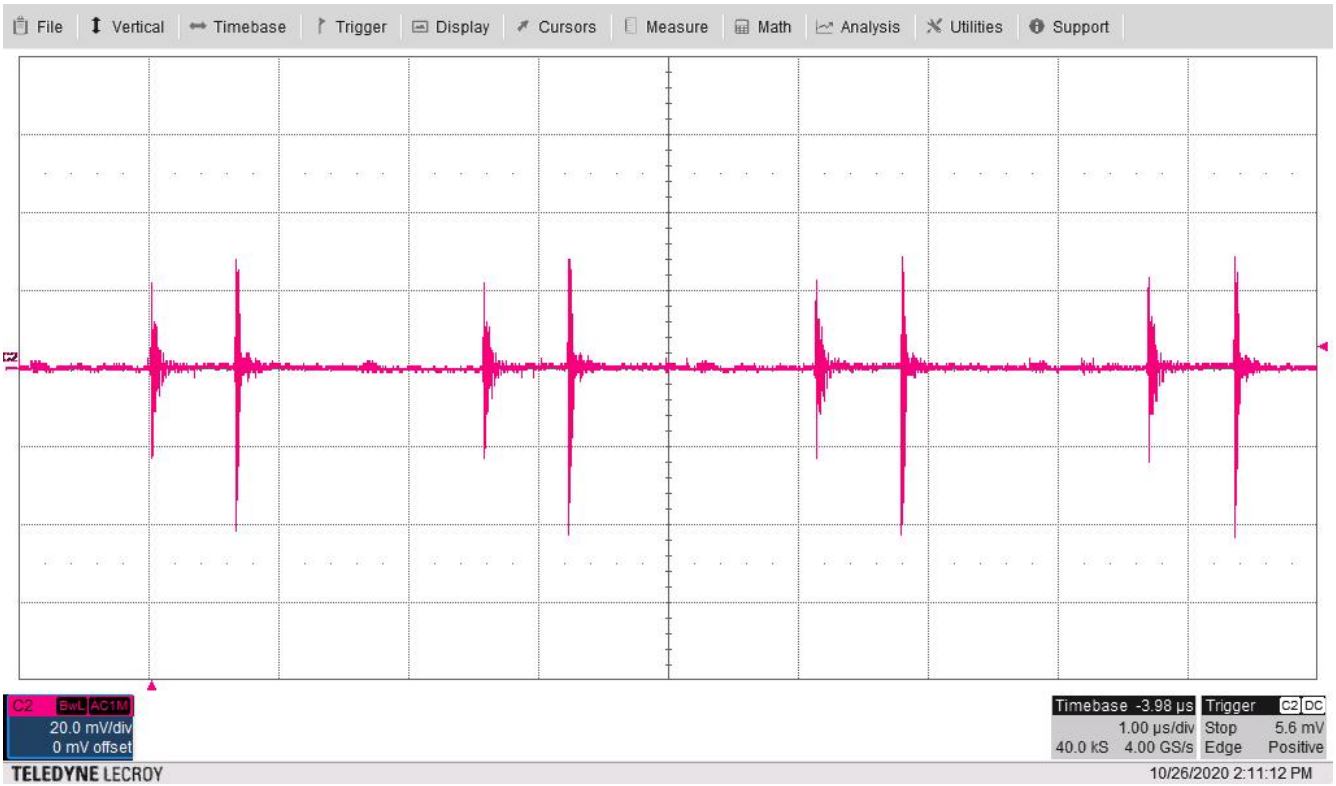


Figure 4-15. –5.1V2 Ripple Voltage With Vin = 12 V and all Maximum Loads, Bandwidth = 20 MHz

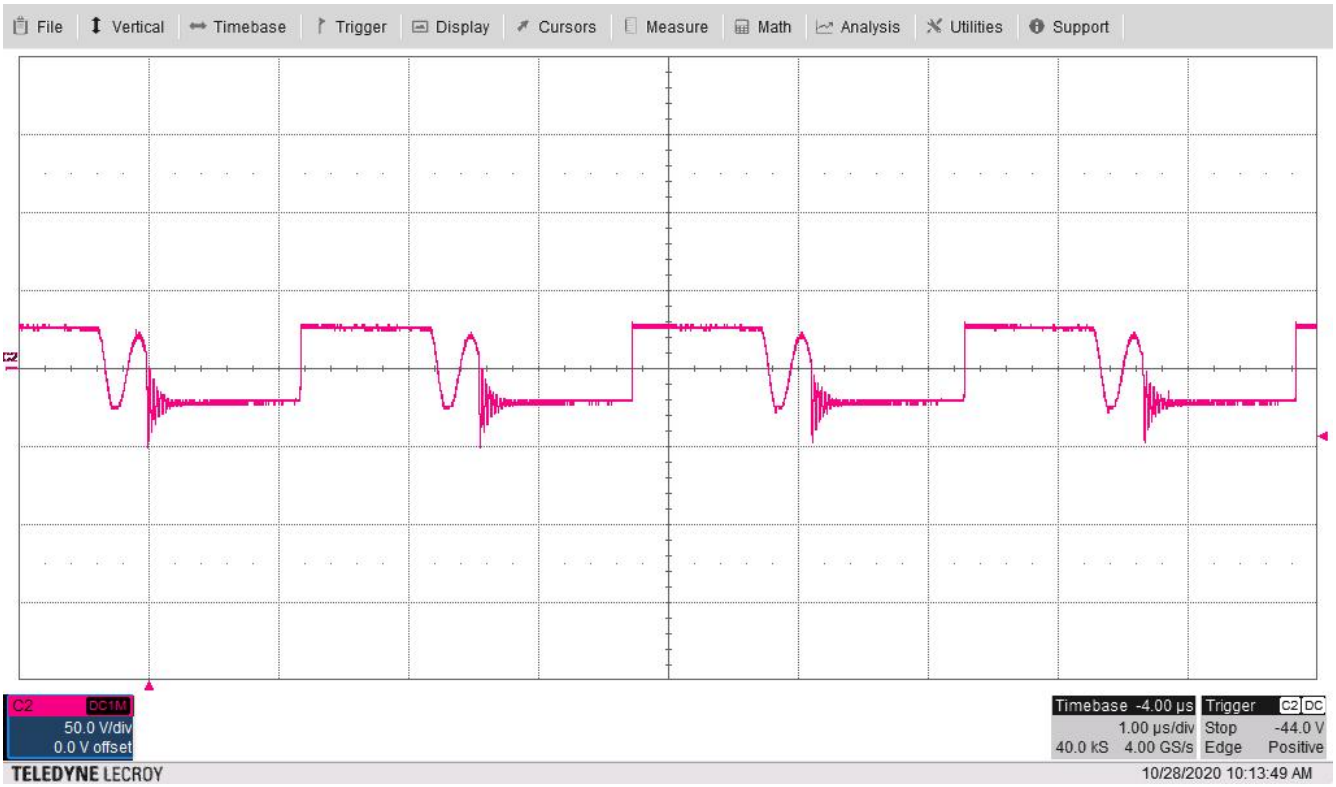


Figure 4-16. Transformer Secondary Switch Node Voltage (T1 – pin 6 and pin 7) With Vin = 7 V and Maximum Loads

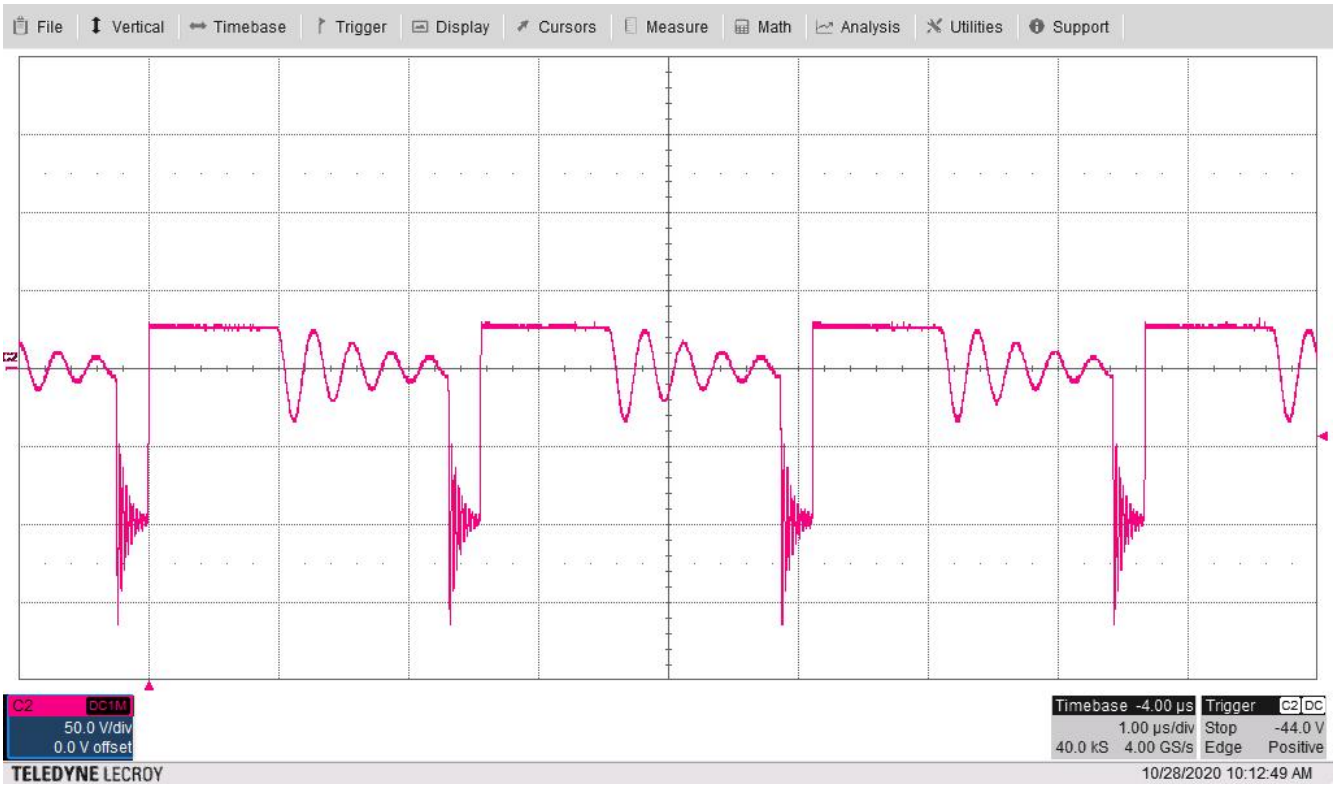
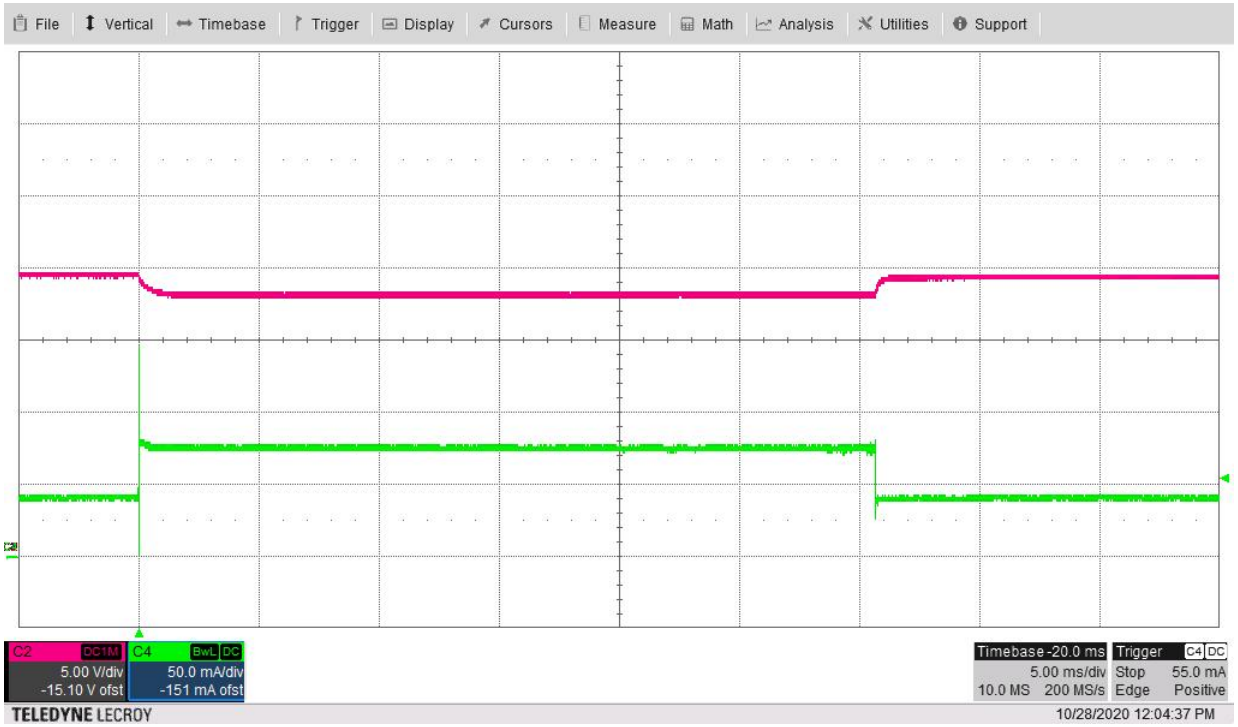


Figure 4-17. Transformer Secondary Switch Node Voltage (T1 – pin 6 and pin 7) With Vin = 32 V and Maximum Loads

4.4 Load Transients

Load transient response is shown in the following figures.



All other outputs are at maximum load

Figure 4-18. 50% Load Transient (38 mA to 75 mA, Green) on 18V1 (Red) for Vin = 12 V

All other outputs are at maximum load

Figure 4-19. 50% Load Transient (38 mA to 75 mA, Green) on –5.1V1 (Red) for Vin = 12V

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