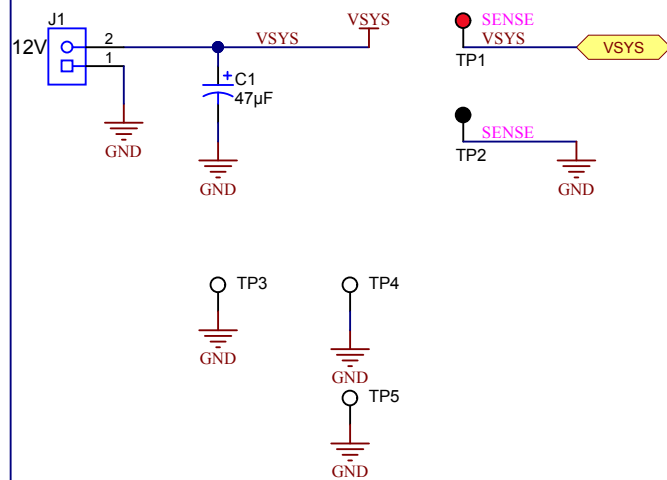
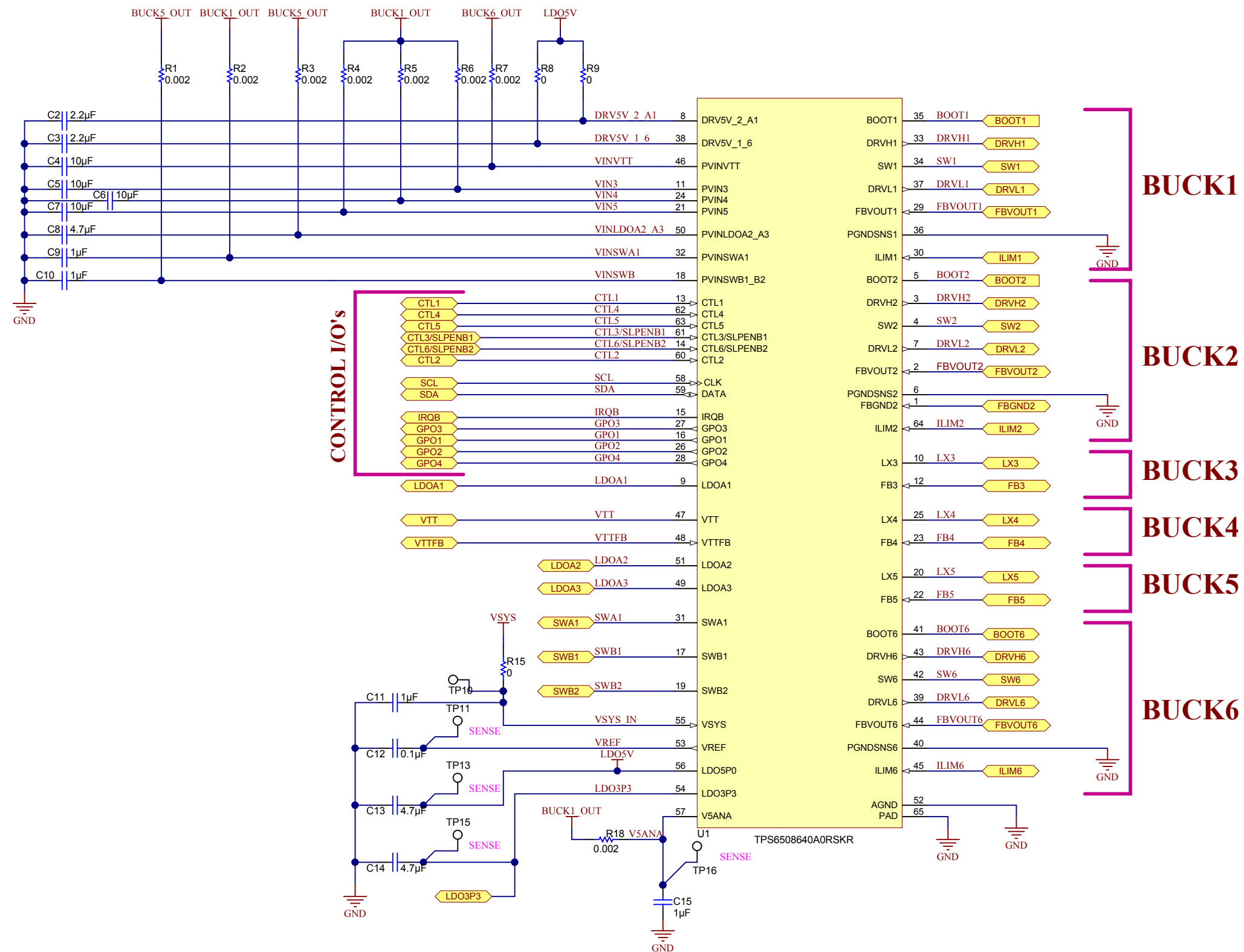
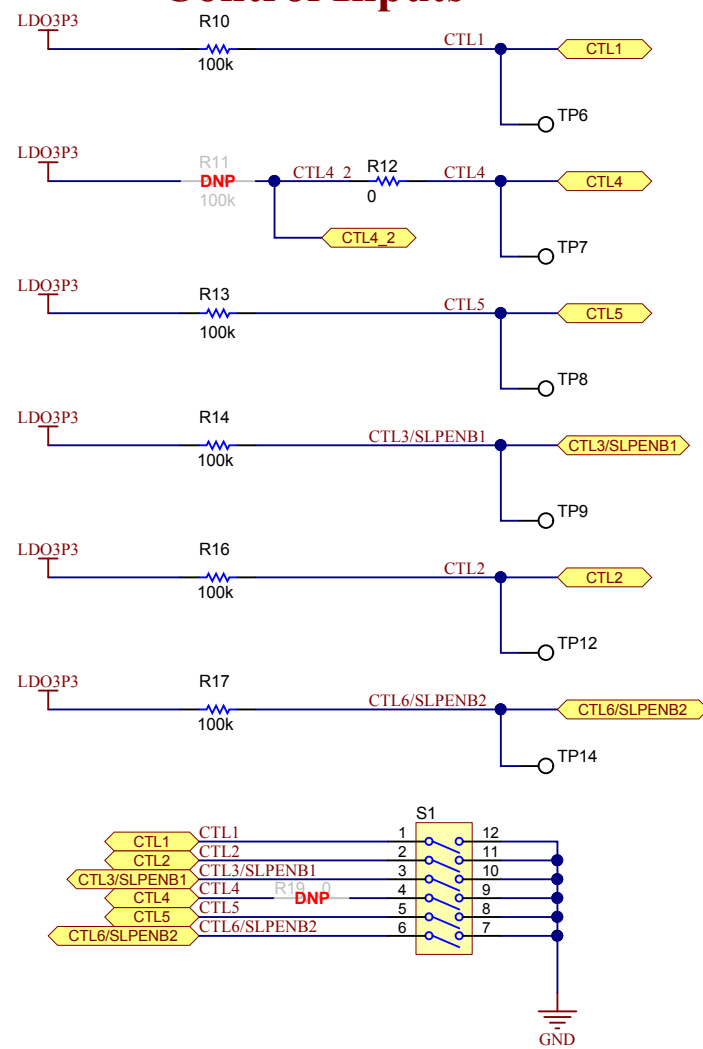


VSYS Input (12V)



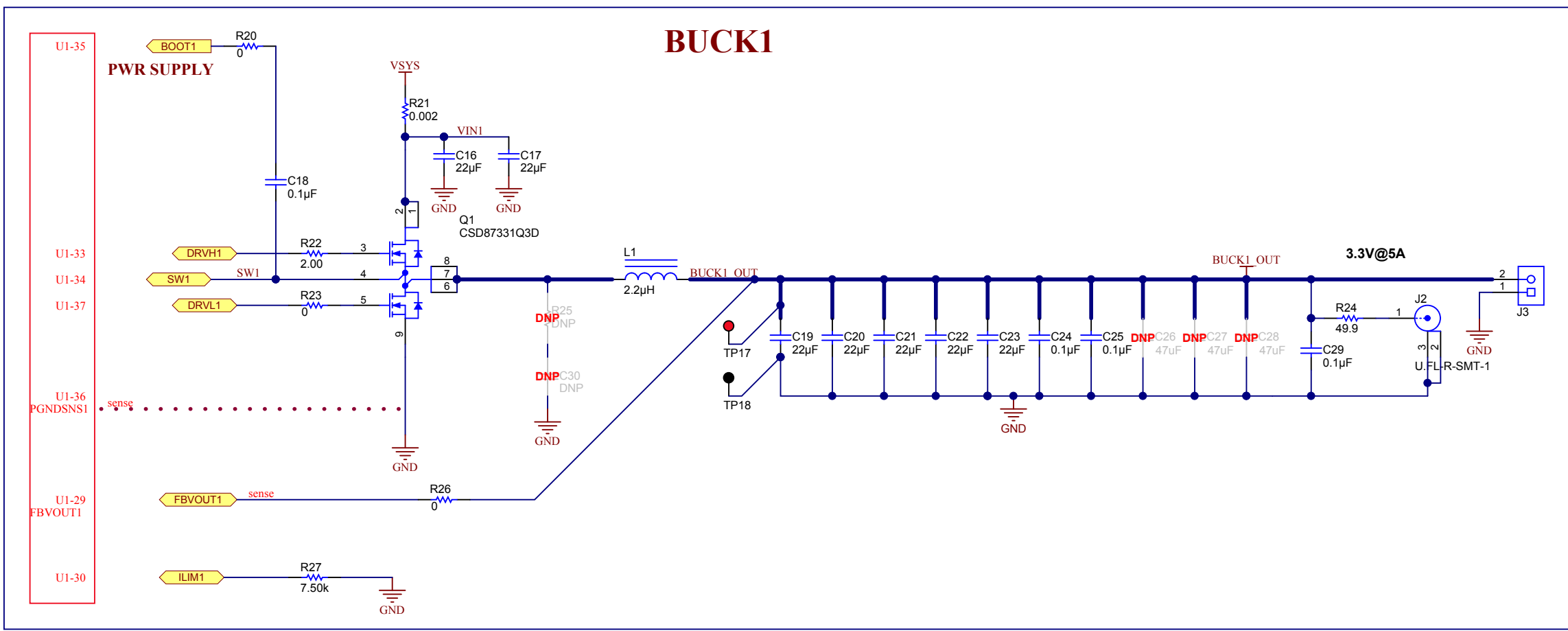
Control Inputs



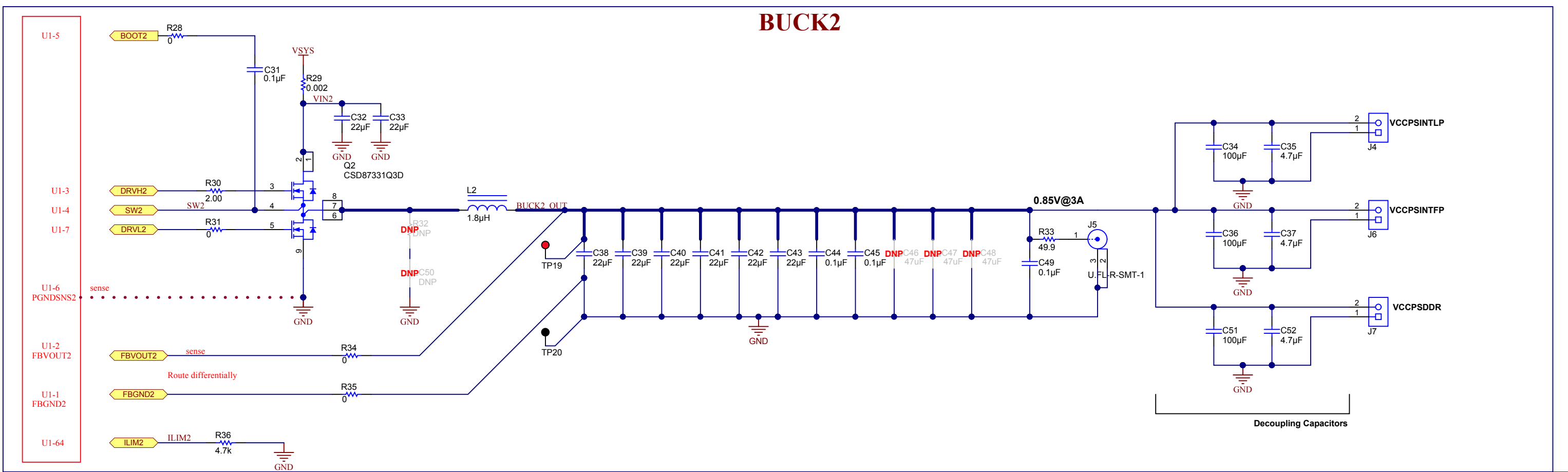
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TID #: PMP12004-HE	Project Title: XILINX RRRH & WIRELESS BH	
Number: PMP12004-HE Rev: B	Sheet Title: PMIC Overview	
SVN Rev: Version control disabled	Assembly Variant: 003	Sheet: 1 of 7
Drawn By:	File: PMP12004-HE_sh1.SchDoc	Size: B
Engineer: R Sheikh/M Battan	Contact: http://www.ti.com/support	

BUCK1



BUCK2

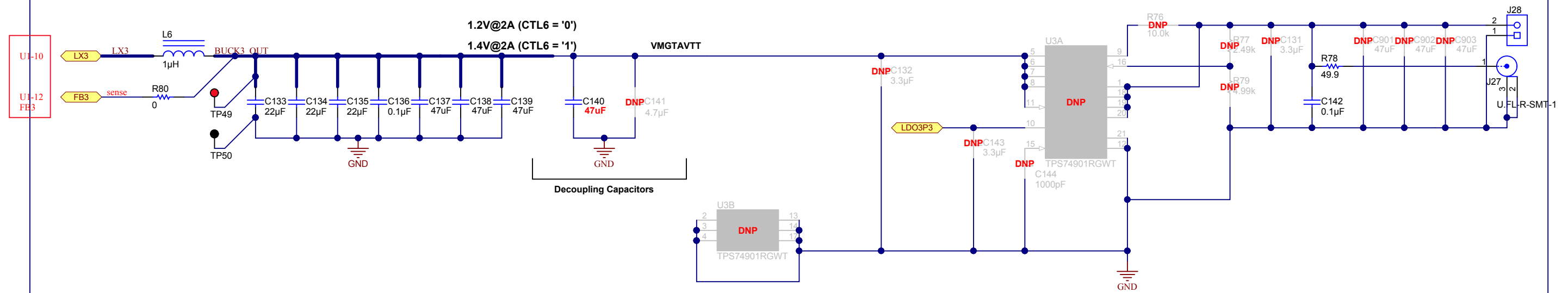


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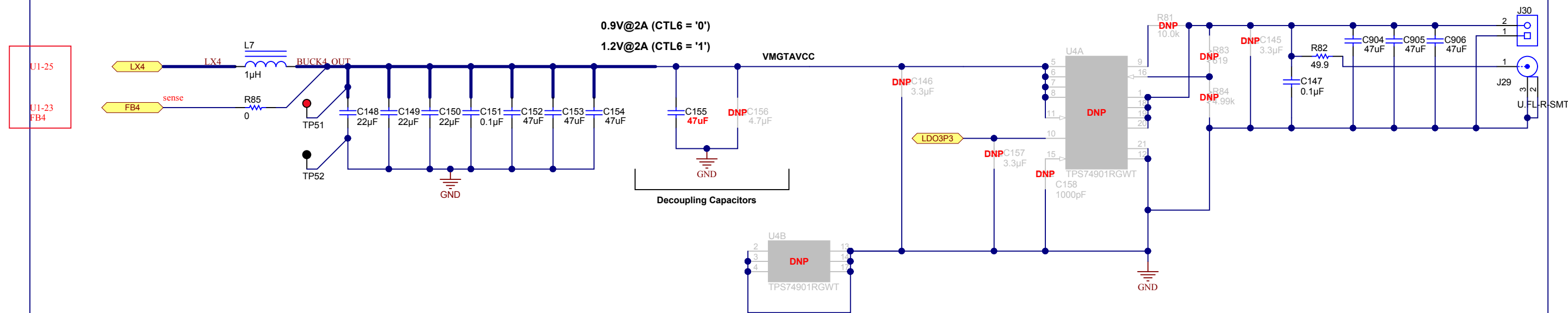
Orderable: N/A	Designed for: Xilinx	Mod. Date: 3/29/2016
TID #: PMP12004-HE	Project Title: XILINX RRH & WIRELESS BH	
Number: PMP12004-HE Rev: B	Sheet Title: 3.3V & VCCPINT Rails	
SVN Rev: Version control disabled	Assembly Variant: 003	Sheet: 2 of 7
Drawn By:	File: PMP12004-HE_sh2.SchDoc	Size: B
Engineer: R Sheikh/M Battan	Contact: http://www.ti.com/support	



BUCK3



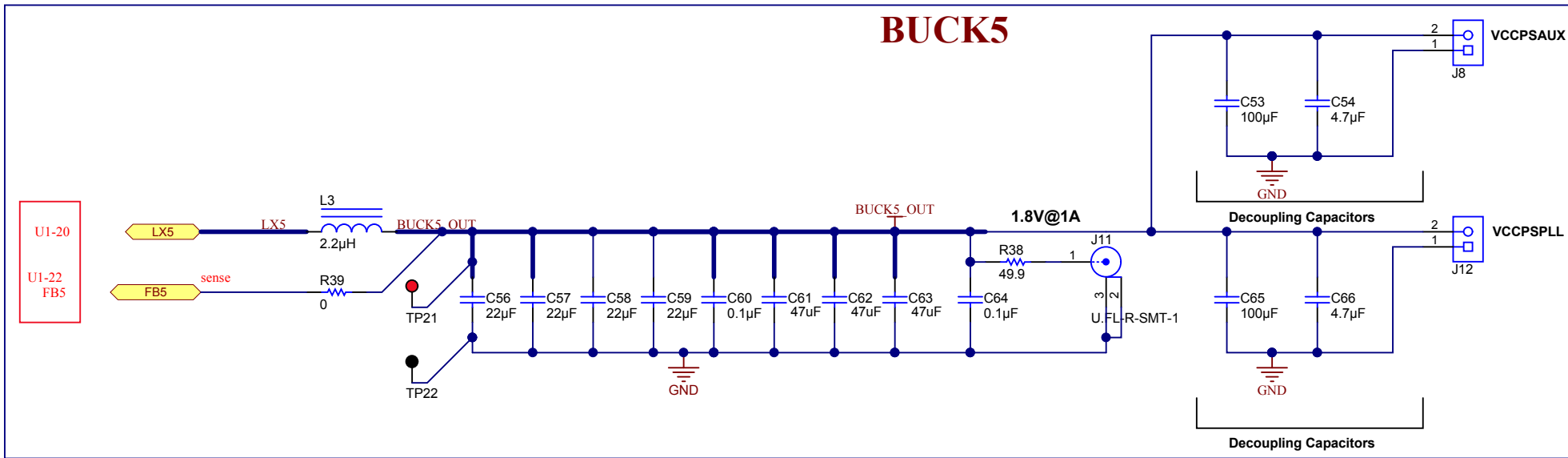
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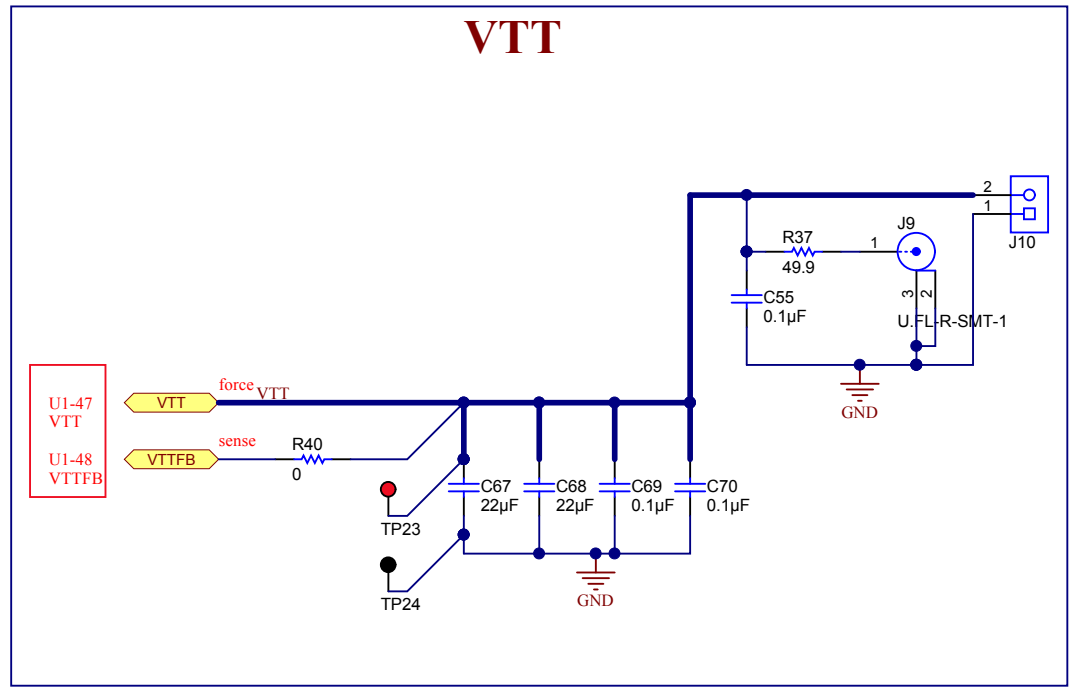
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TID #: PMP12004-HE	Project Title: XILINX RRR & WIRELESS BH	Sheet: 3 of 7	
Number: PMP12004-HE Rev: B	Sheet Title: VMGTA Rails	Size: B	http://www.ti.com © Texas Instruments 2015
SVN Rev: Version control disabled	Assembly Variant: 003		
Drawn By: R Sheikh/M Battan	File: PMP12004-HE_sh3.SchDoc	Contact: http://www.ti.com/support	

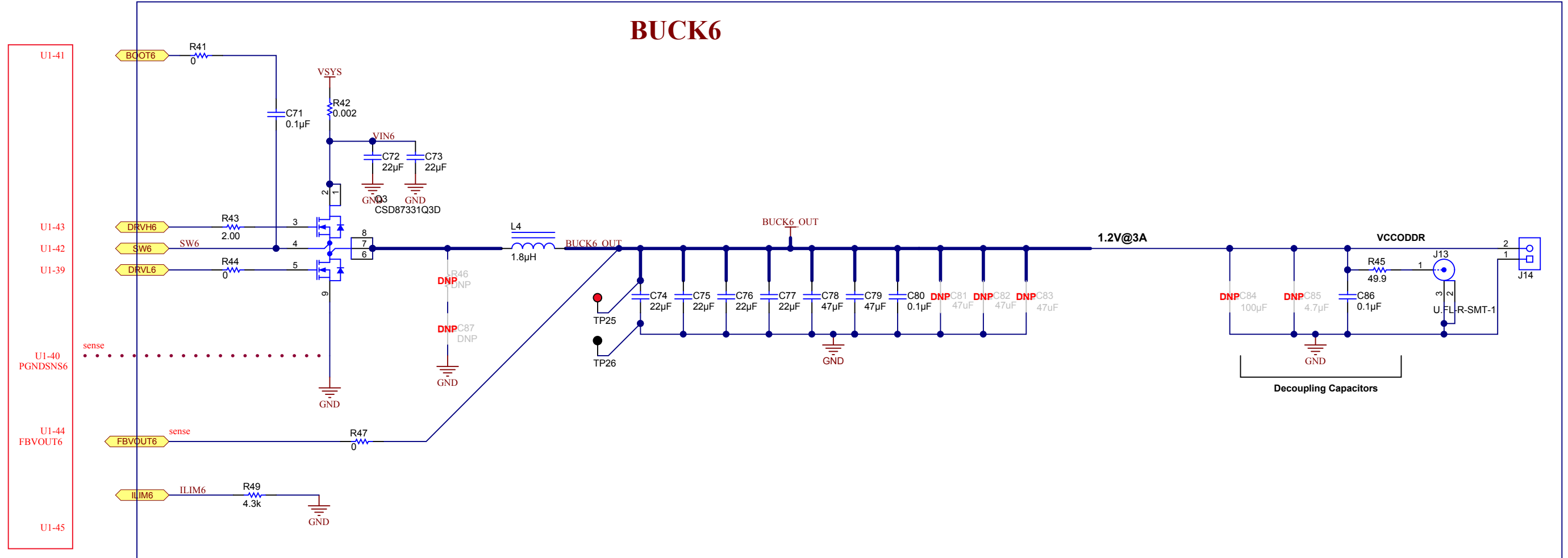
BUCK5



VTT



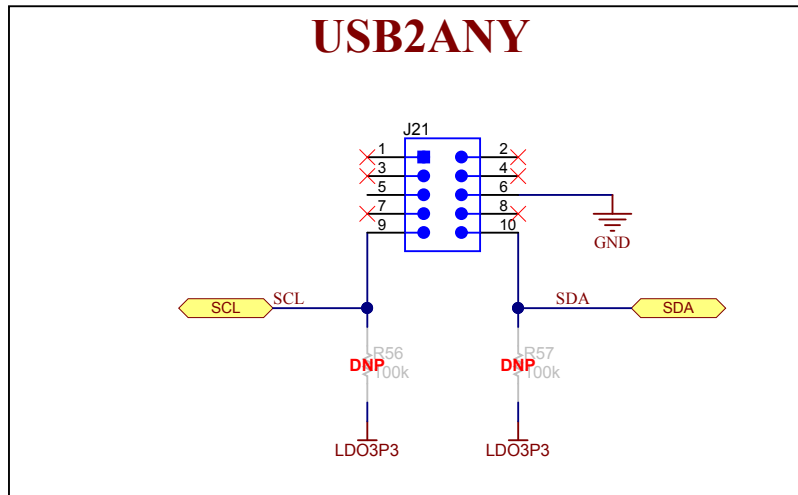
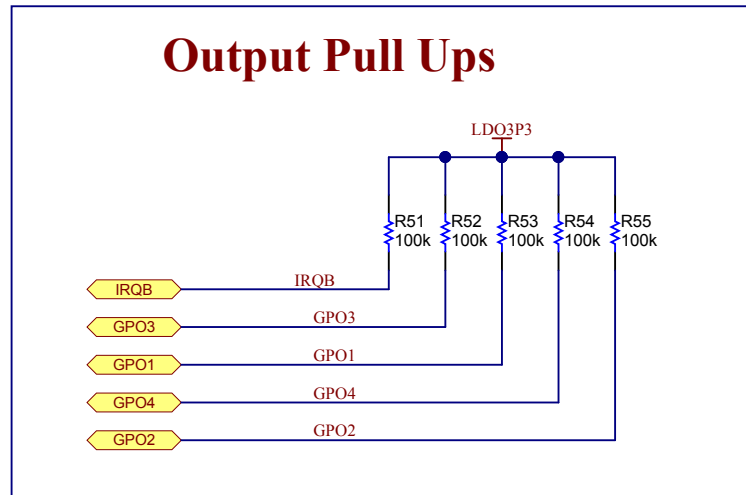
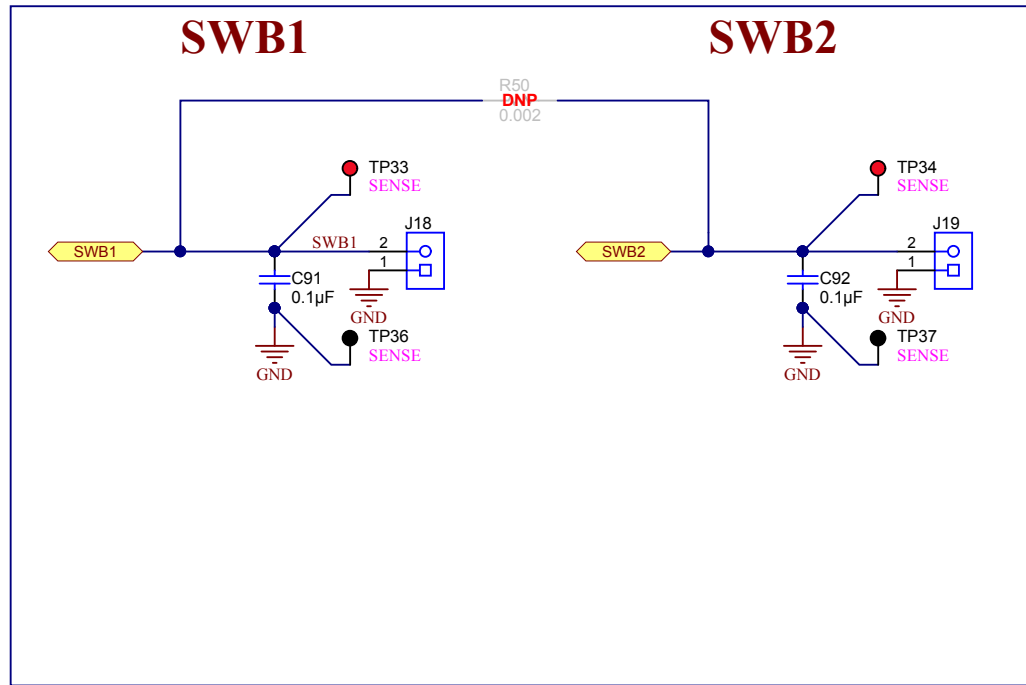
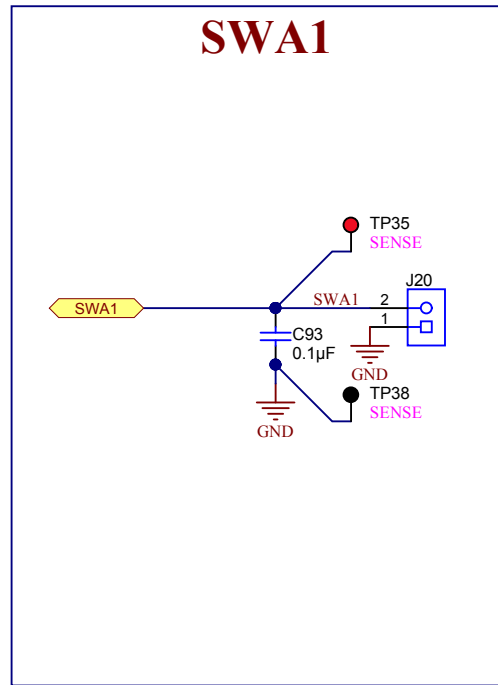
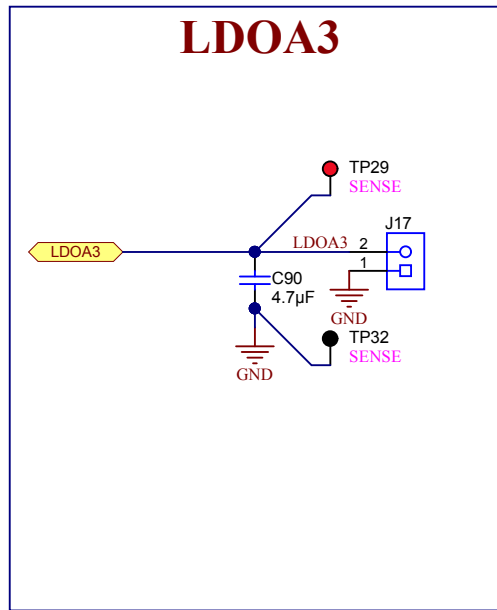
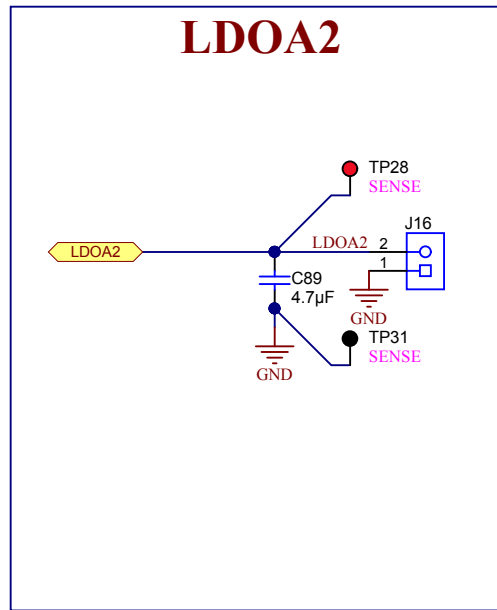
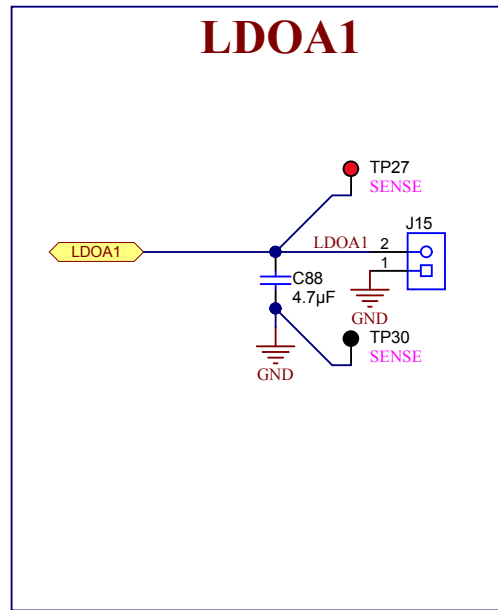
BUCK6



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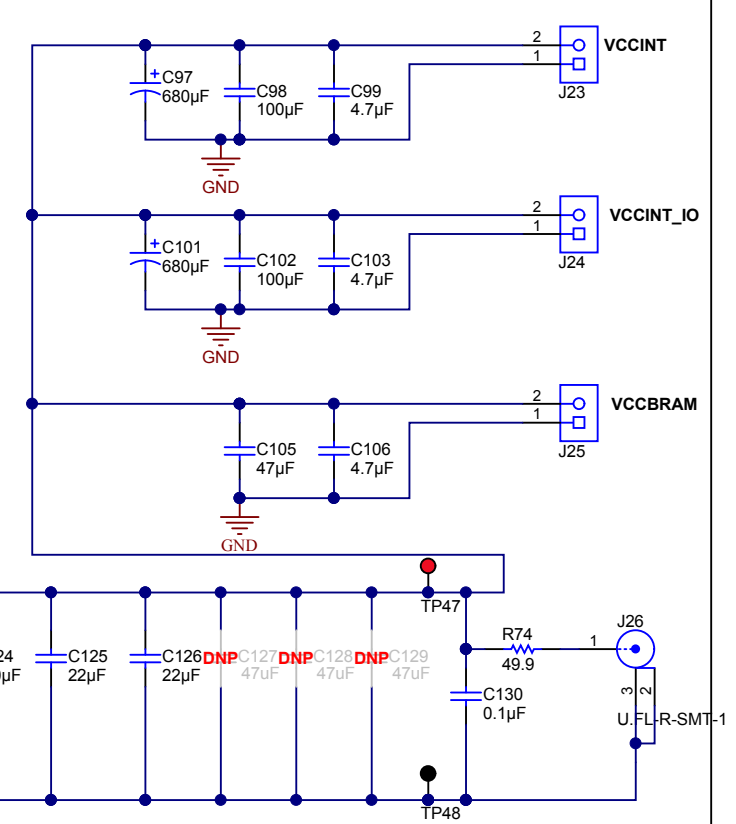
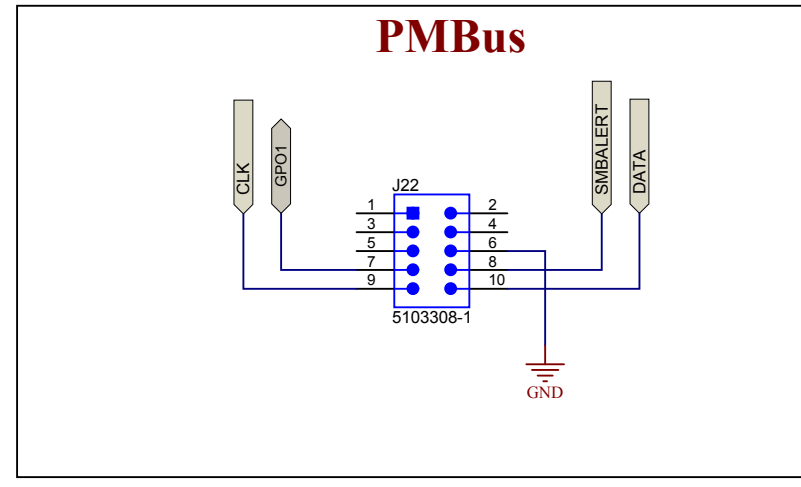
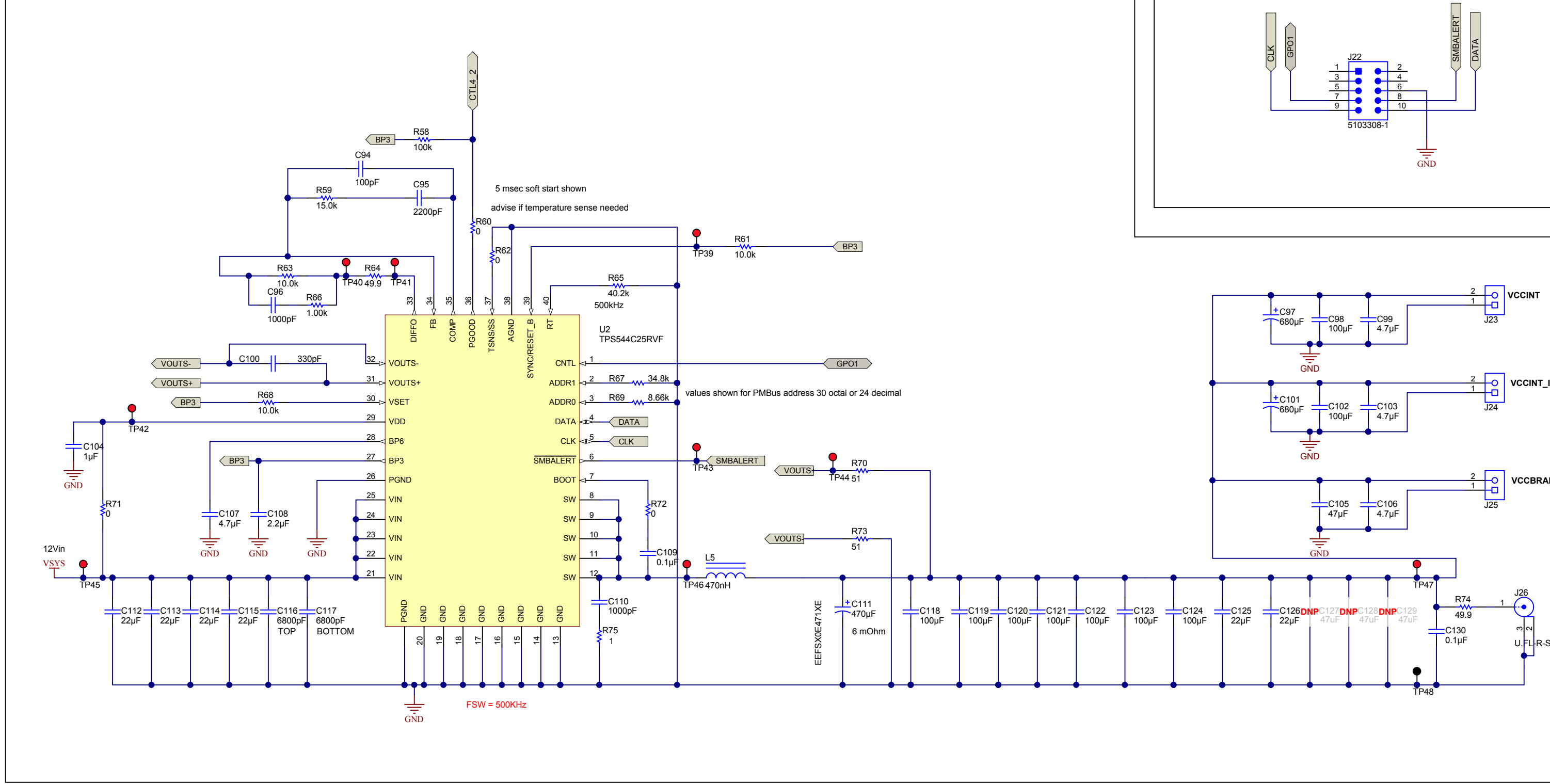
Orderable: N/A	Designed for: Xilinx	Mod. Date: 3/29/2016
TID #: PMP12004-HE	Project Title: XILINX RRR & WIRELESS BH	
Number: PMP12004-HE Rev: B	Sheet Title: 1.8V & DDR Rails	
SVN Rev: Version control disabled	Assembly Variant: 003	Sheet: 4 of 7
Drawn By:	File: PMP12004-HE_sh4.SchDoc	Size: B
Engineer: R Sheikh/M Battan	Contact: http://www.ti.com/support	





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TID #: PMP12004-HE	Project Title: XILINX RRR & WIRELESS BH	
Number: PMP12004-HE Rev: B	Sheet Title: VCCINT Core Rail	
SVN Rev: Version control disabled	Assembly Variant: 003	Sheet: 6 of 7
Drawn By: R Sheikh/M Battan	File: PMP12004-HE_sh6.SchDoc	Size: B
Engineer: R Sheikh/M Battan	Contact: http://www.ti.com/support	



H1 SJ-5303 (CLEAR) H2 SJ-5303 (CLEAR) H3 SJ-5303 (CLEAR) H4 SJ-5303 (CLEAR)

FID1 FID2 FID3 FID4 FID5 FID6

PCB Number: PMP12004-HE
PCB Rev: RevA

PCB
LOGO
Texas Instruments

PCB
LOGO
Pb-Free Symbol

ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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TID #: PMP12004-HE	Project Title: XILINX RRH & WIRELESS BH		
Number: PMP12004-HE Rev: B	Sheet Title:		
SVN Rev: Version control disabled	Assembly Variant: 003	Sheet: 7 of 7	
Drawn By: R Sheikh/M Battan	File: PMP12004-HE_Hardware.SchDoc	Size: B	
Engineer: R Sheikh/M Battan	Contact: http://www.ti.com/support		

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