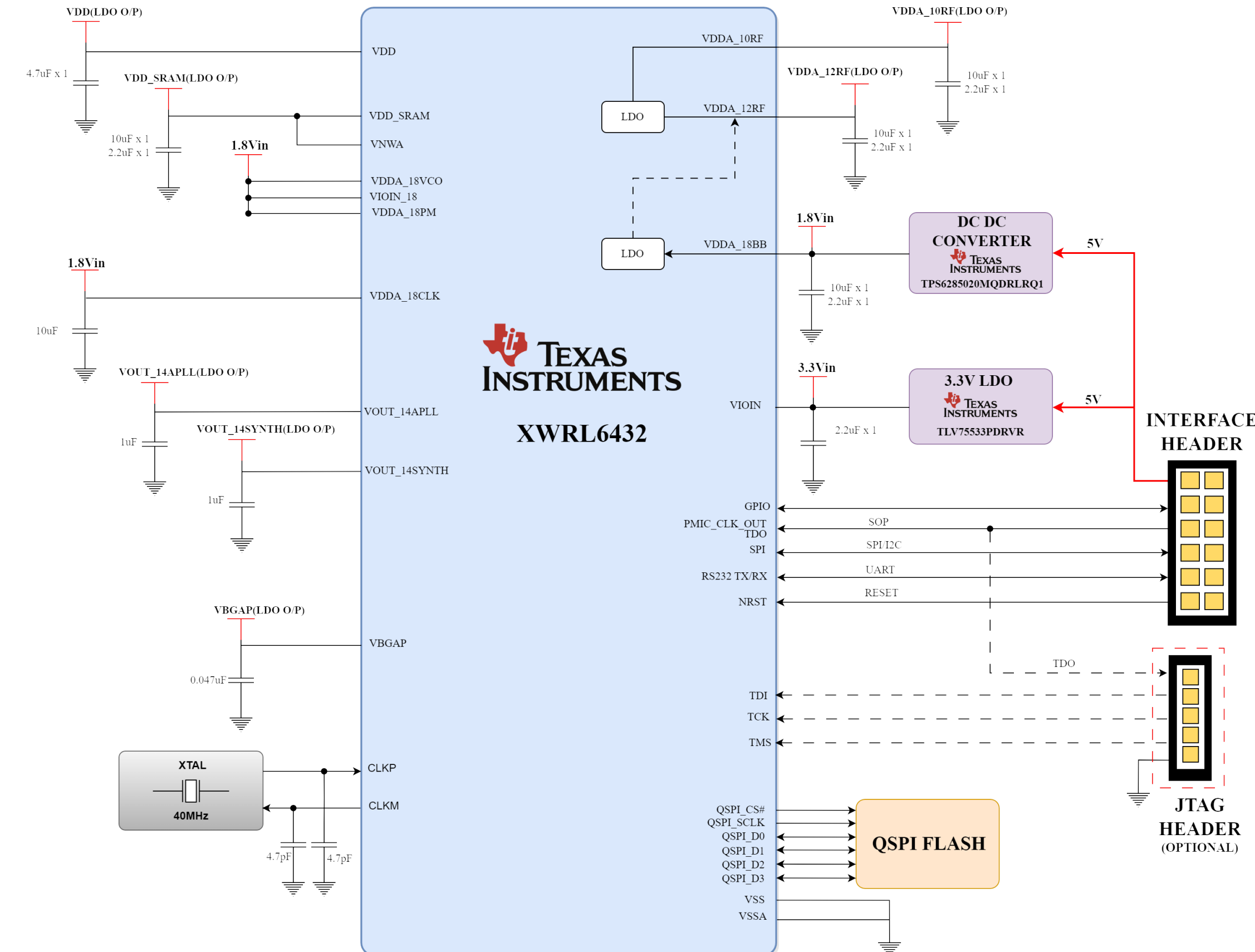


BLOCK DIAGRAM

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
NA	NA	NA	Chethan Kumar	Baseline Schematics

A
B
C
D



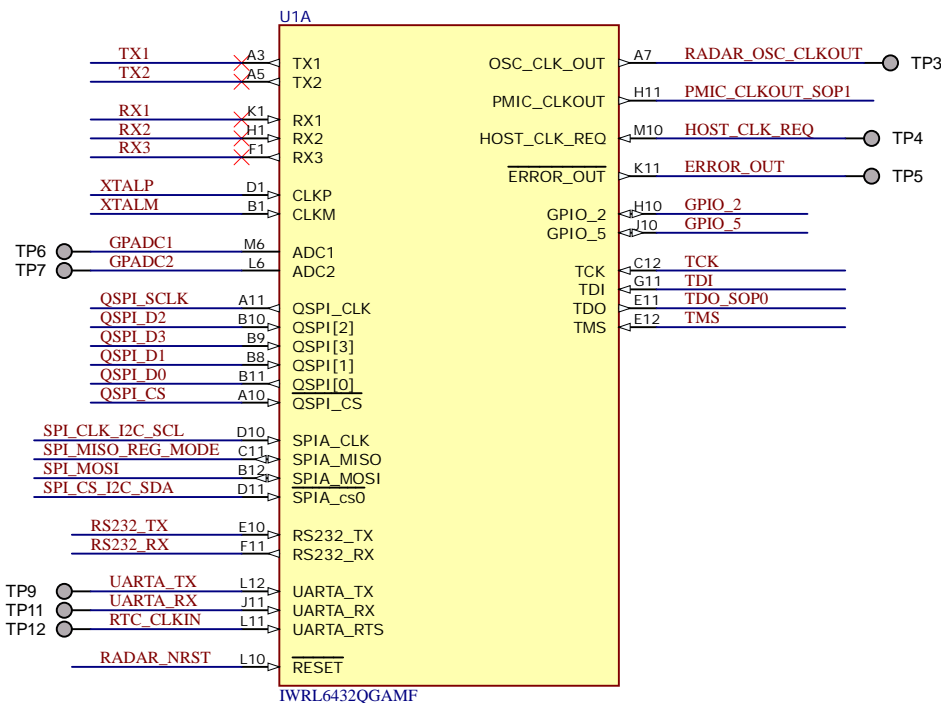
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Orderable: N/A	Designed for: Public Release	Mod. Date: 9/23/2024
TID #: TIDEP-01033	Project Title: IWRL6432 FCCSP REFERENCE DESIGN	
Number: TIDEP-01033 Rev: A	Sheet Title: BLOCK DIAGRAM	
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 1 of 2
Drawn By: Texas Instruments	File: IWRL6432 FCCSP_REF_Block_Diagram.Sch	Size: B
Engineer: Texas Instruments	Contact: http://www.ti.com/support	

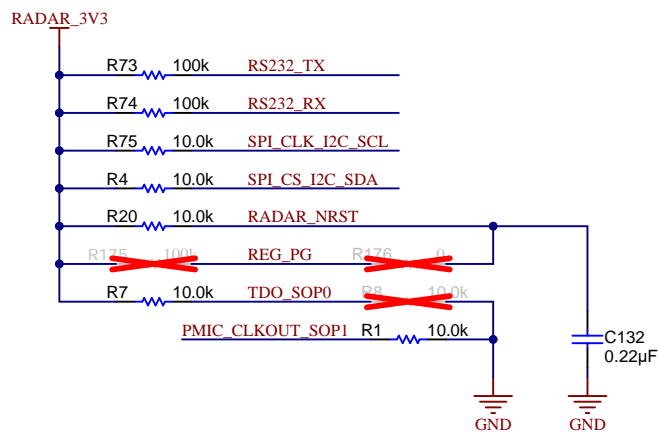


IWR6432 FCCSP REFERENCE DESIGN

IWR6432 FCCSP IO INTERFACE



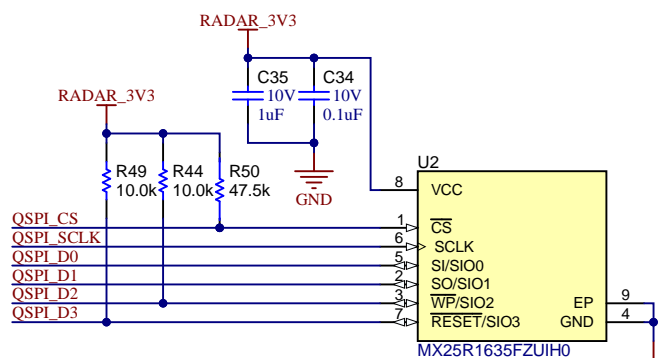
Design Note:
 1. Antenna traces are GCPW traces
 2. 'Generic No ERCs' were placed intentionally on Single Port RF Tx, Rx lines



SOP CONFIGURATION

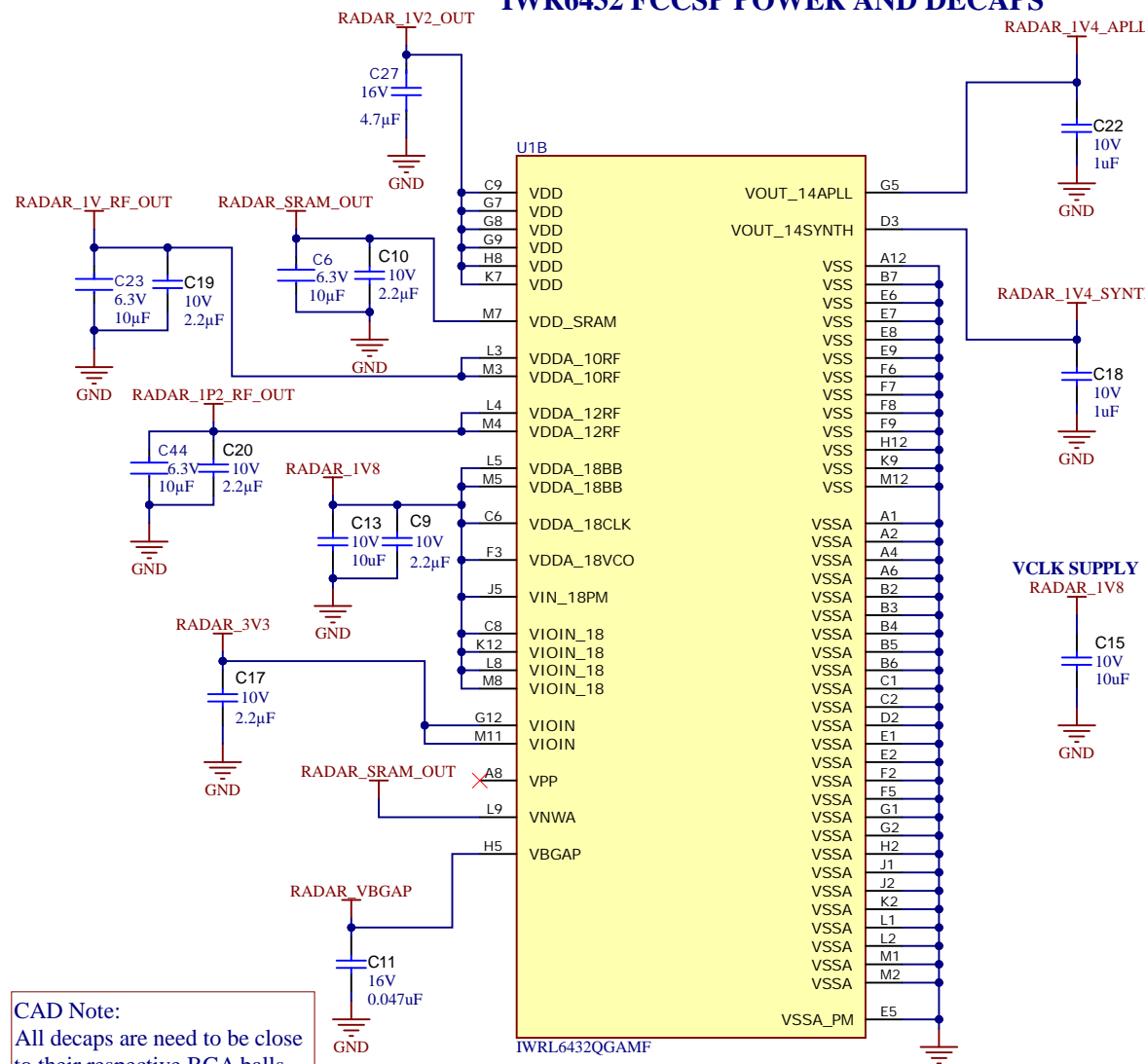
SOP Mode	PMIC_CLK_OUT, TDO	Combination
SOP_MODE1	Device management mode / QSPI Flashing mode	0 0
SOP_MODE2	Application mode / Functional mode	0 1(Default)

QSPI FLASH



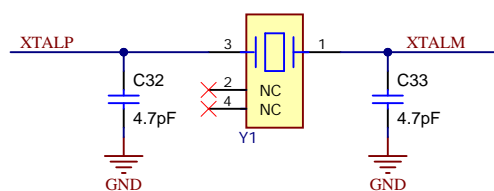
Design note:
 Current design MX25R1635FZUIH0 Flash supports VCC from 1.65V to 3.3V
 Alternate Flash part is MX25U1632FZUI02 supports VCC from 1.65V to 2.0V

IWR6432 FCCSP POWER AND DECAPS

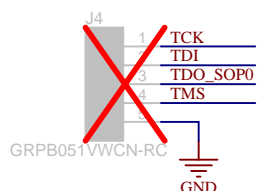


CAD Note:
 All decaps are need to be close to their respective BGA balls

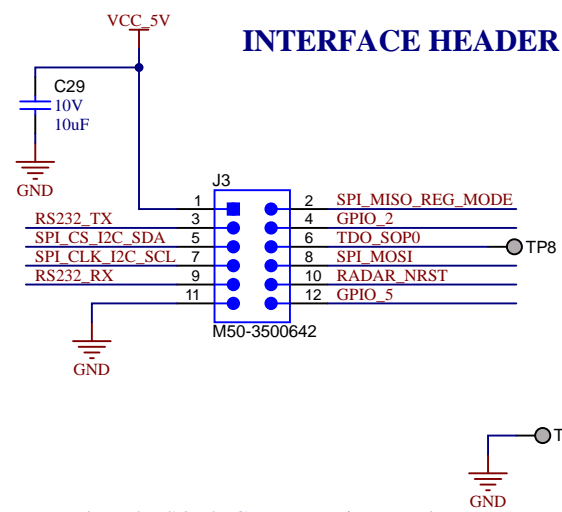
40 MHz CRYSTAL OSCILLATOR



JTAG HEADER

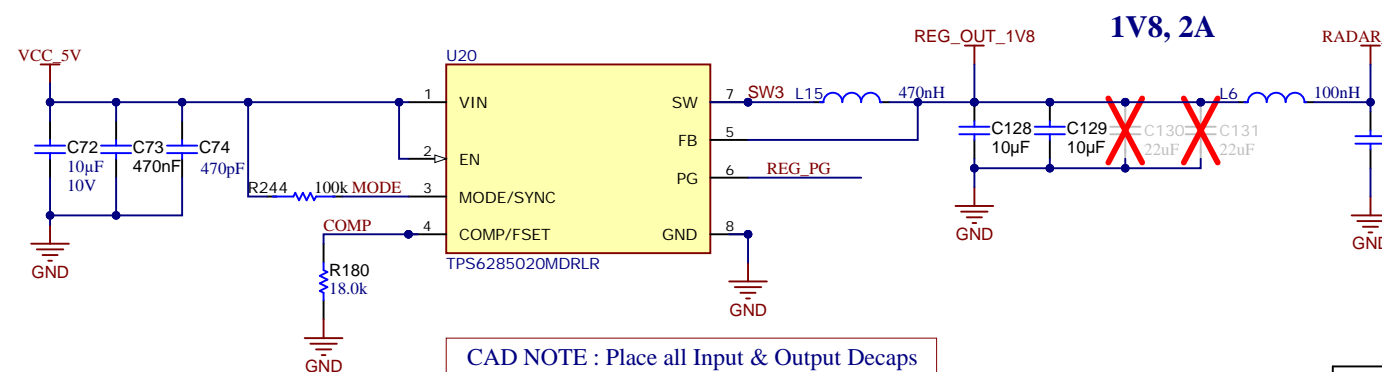


INTERFACE HEADER



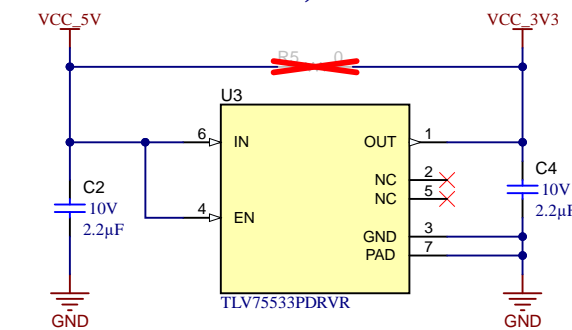
Design Note: Place the SOP0, GND testpoints nearby

DC DC REGULATOR - 1.8V



CAD NOTE: Place all Input & Output Decaps close to Regulator Pins - U20

3.3V LDO, 500mA



Orderable: N/A	Designed for: Public Release	Mod. Date: 9/23/2024
TID #: TIDEP-01033	Project Title: IWR6432 FCCSP REFERENCE DESIGN	
Number: TIDEP-01033 Rev: A	Sheet Title: IWR6432FCCSP_CHIP	
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 2 of 2
Drawn By: Texas Instruments	File: IWR6432 FCCSP_REF_Chip_SchDoc	Size: B
Engineer: Texas Instruments	Contact: http://www.ti.com/support	

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