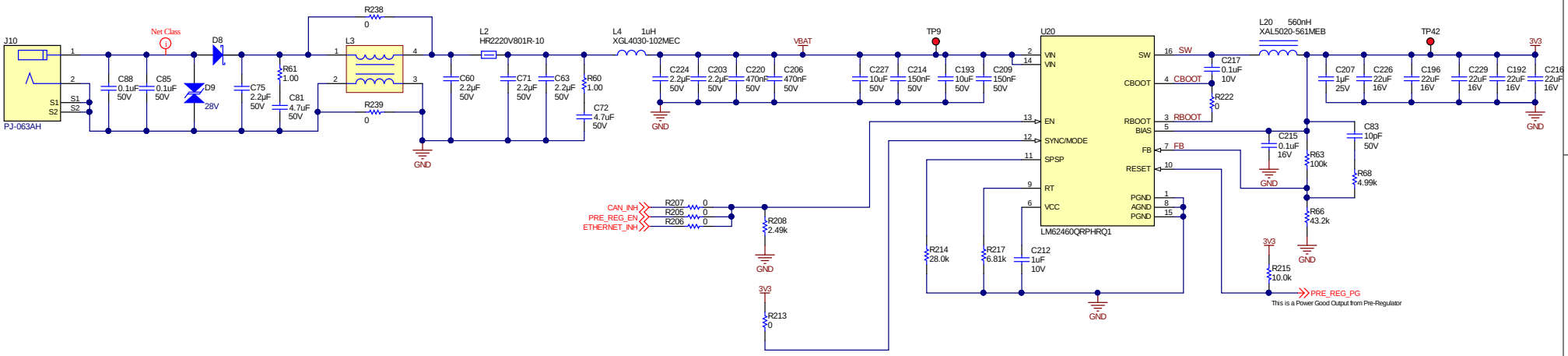
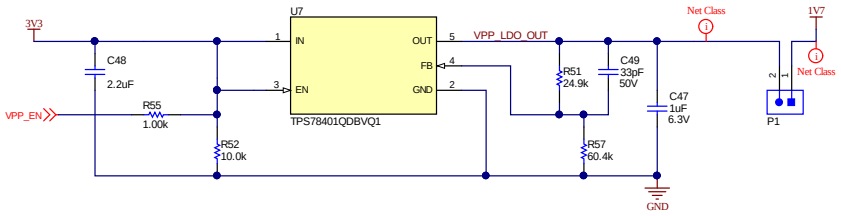
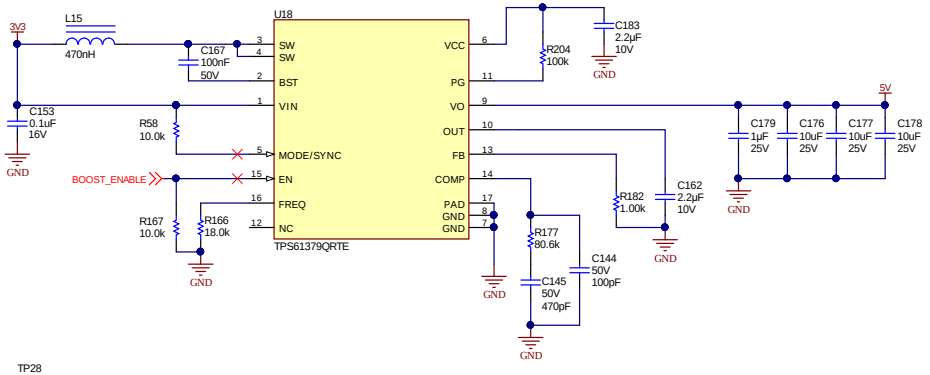
Pre-Regulator



VPP LDO



5V Boost



TP41 TP1 TP28 GND

Assembly Variants:

812: DP83TC812 Ethernet and CAN present. WAKE Controlled by Ethernet (DP83TC812)
CAN: DP83TC812 Ethernet and CAN present. WAKE Controlled by CAN (TCAN1043)
811: DP83TC811 Ethernet and CAN present. WAKE Controlled by CAN (TCAN1043)

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 11/1/2022
TID #: TIDA-020047		Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047	Rev: 2	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 1 of 17
Drawn By: B. Shaffer		File: Pre_Reg.SchDoc	Size: B
Engineer: B. Shaffer		Contact: http://www.ti.com/support	

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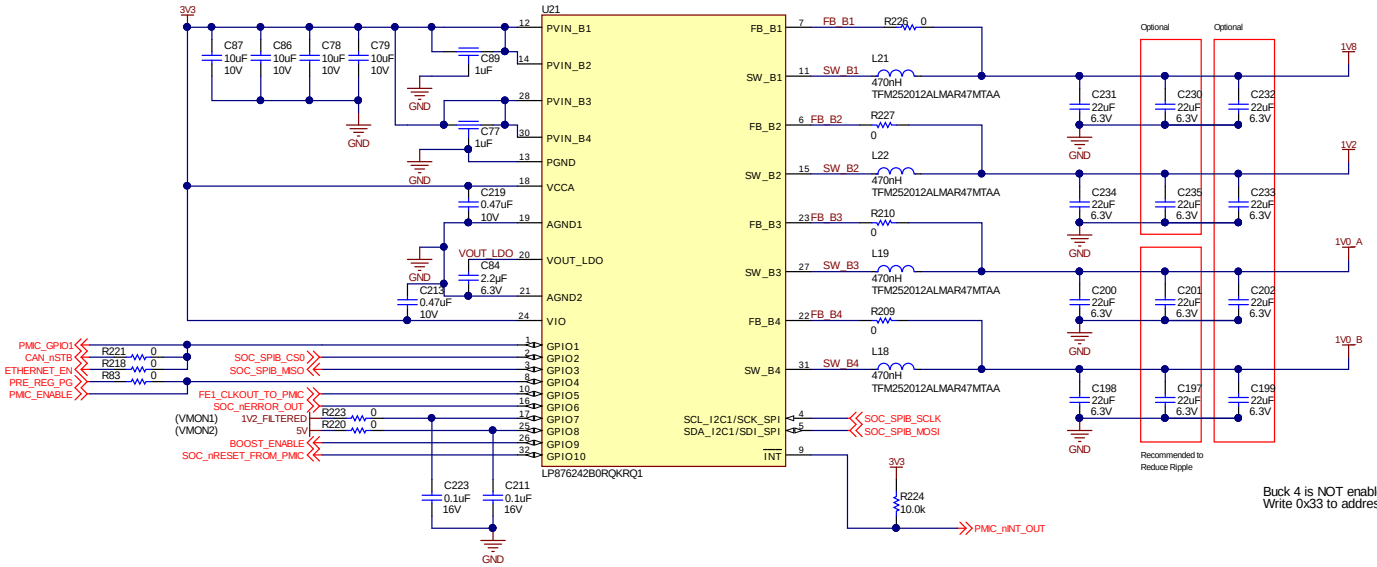
PMIC



Buck 4 is NOT enabled by default. It must be enabled over SPI.
Write 0x33 to address 0x0A

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047		Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047	Rev: 2	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 2 of 17
Drawn By: B. Shaffer		File: PMIC.schdoc	Size: B
Engineer: B. Shaffer		Contact: http://www.ti.com/support	

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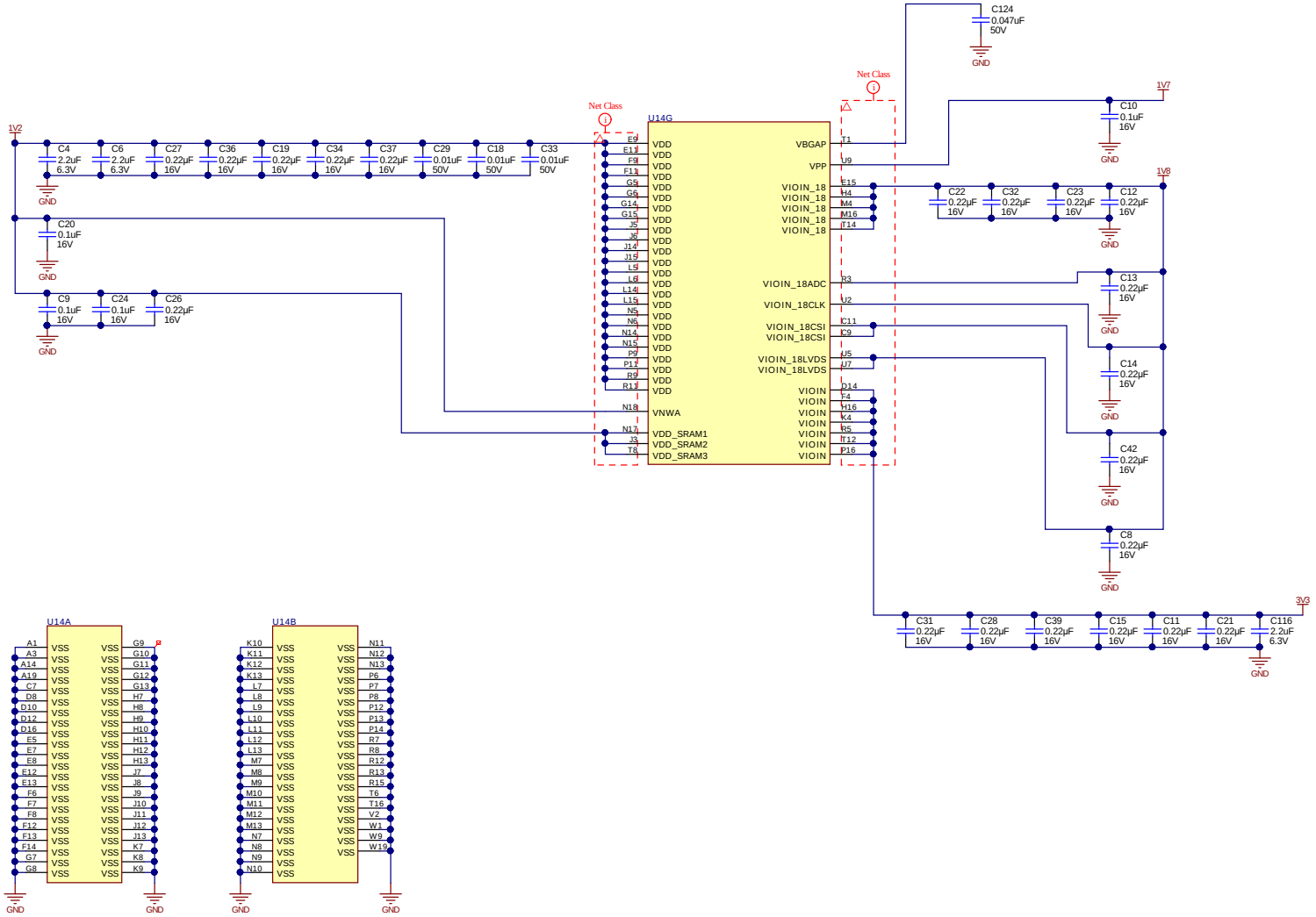
SOC POWER



Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047		Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047	Rev: 2	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 3 of 17
Drawn By: B. Shaffer		File: SOC_PWR.SchDoc	Size: B
Engineer: B. Shaffer		Contact: http://www.ti.com/support	

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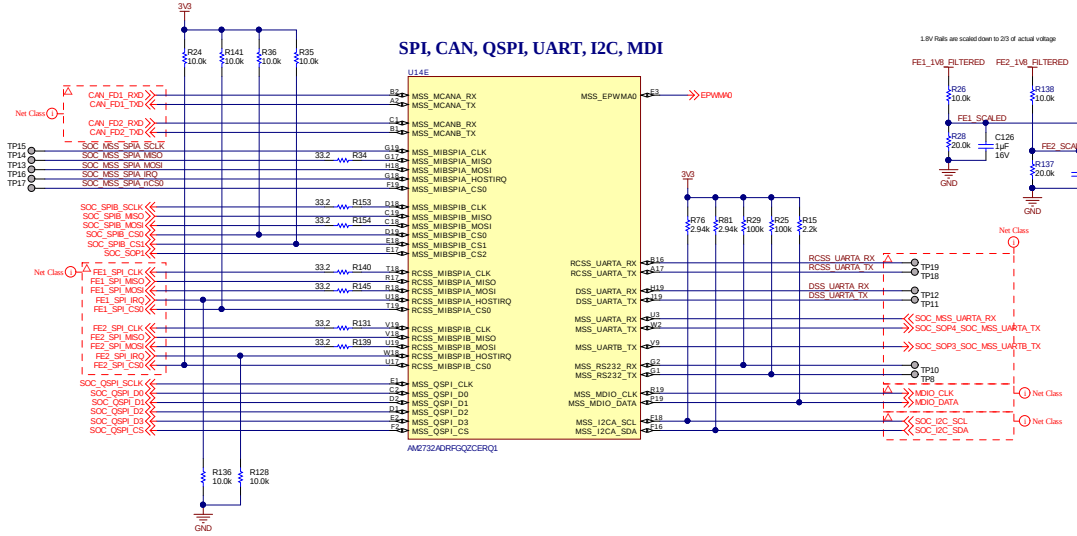
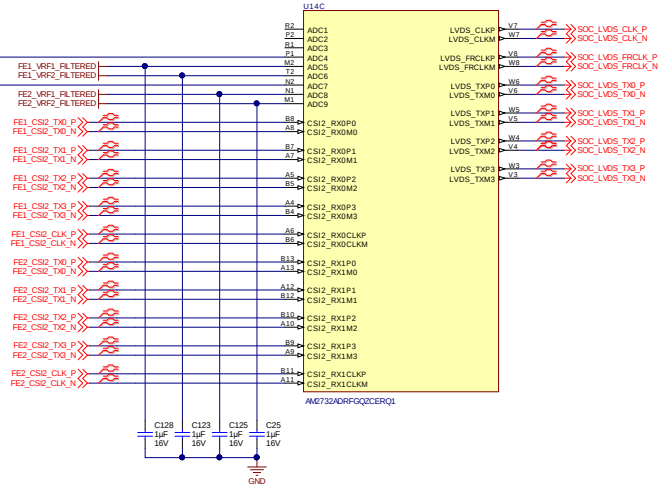
SoC IO

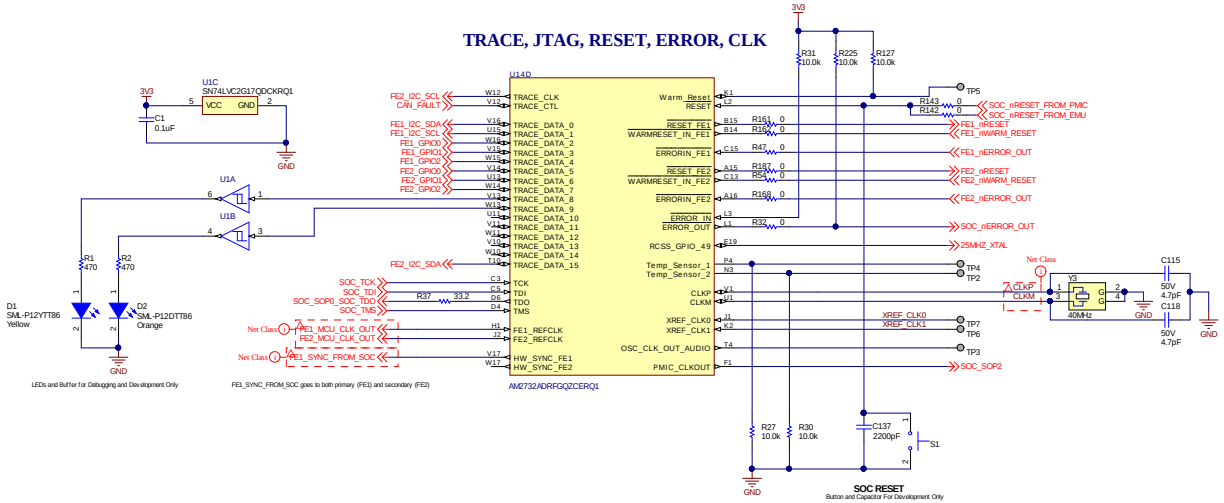
SPI, CAN, QSPI, UART, I2C, MDI



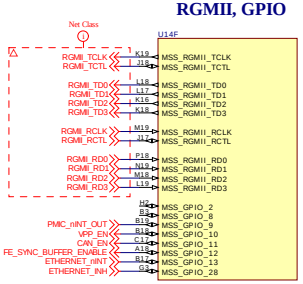
GPADC, HIGH SPEED INTERFACES



TRACE, JTAG, RESET, ERROR, CLK

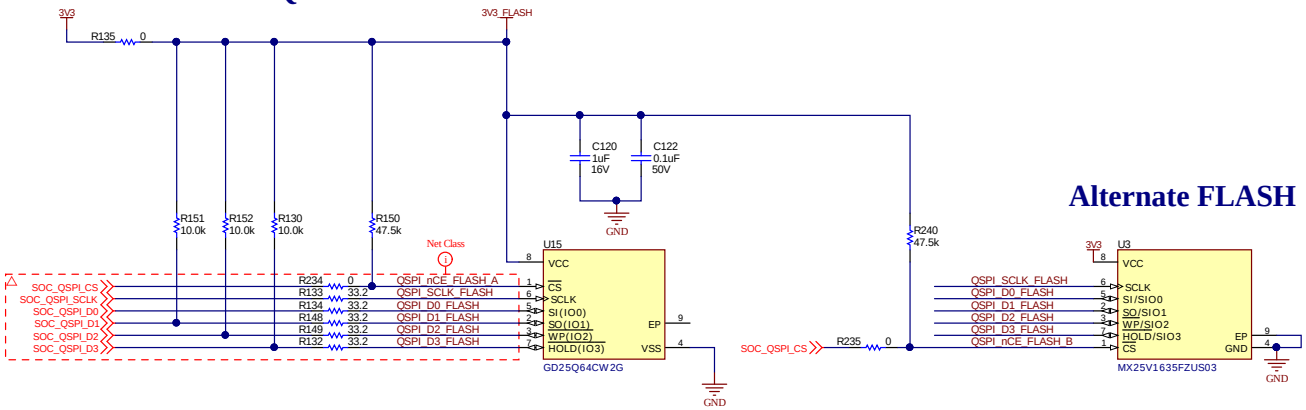


RGMII, GPIO



Orderable: EVM orderable	Designed for: Public Release	Mod. Date: 11/2/2022	
TID #: TIDA-020047	Project Title: Dual MMC cascade radar reference design		
Number: TIDA-020047 Rev 2	Sheet Title:		
SVN Rev Version control disabled	Assembly Variant: [No Variations]	Sheet: 4 of 17	
Drawn By: B. Shaffer	File: SOC_IO.schdoc	Size: A2	http://www.ti.com
Engineer: B. Shaffer	Contact: http://www.ti.com/support		

QSPI FLASH



Alternate FLASH

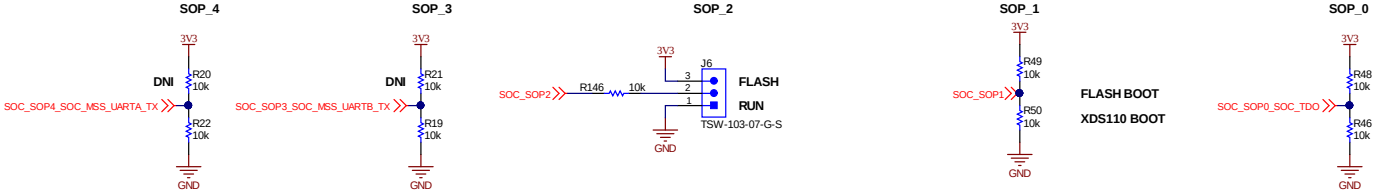
SoC SOP

XTAL DETECT SOP CONFIG

	SOP4, SOP3
40 MHz	00
45.1584 MHz	01
49.152 MHz	10
50 MHz	11

SOP2, SOP1, SOP0

SOP_MODE1	SCAN/ATPG	010
SOP_MODE2	DEV/FLED/ORBIT	011
SOP_MODE3	THB	000
SOP_MODE4	FUNC	001
SOP_MODE5	DEV MANAGEMENT	101



Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047	Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047 Rev: 2	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 5 of 17
Drawn By: B. Shaffer	File: SOC_FLASH_SOP.SchDoc	Size: B
Engineer: B. Shaffer	Contact: http://www.ti.com/support	

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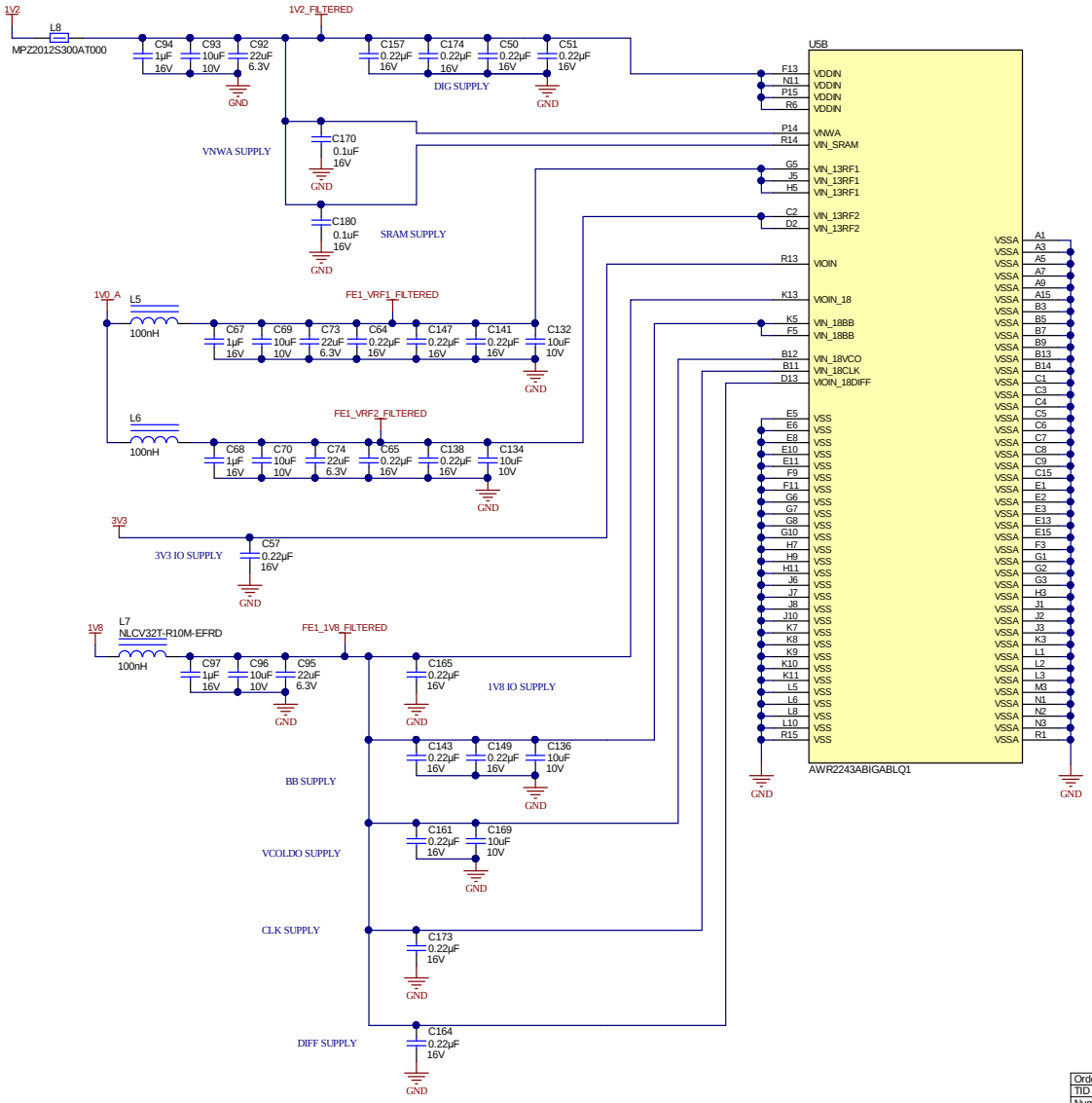
FRONT END #1 POWER CONNECTIONS



Orderable: EVM orderable		Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047		Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047	Rev: 2	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 6 of 17
Drawn By: B. Shaffer		File: FE1_PWR.SchDoc	Size: B
Engineer: B. Shaffer		Contact: http://www.ti.com/support	

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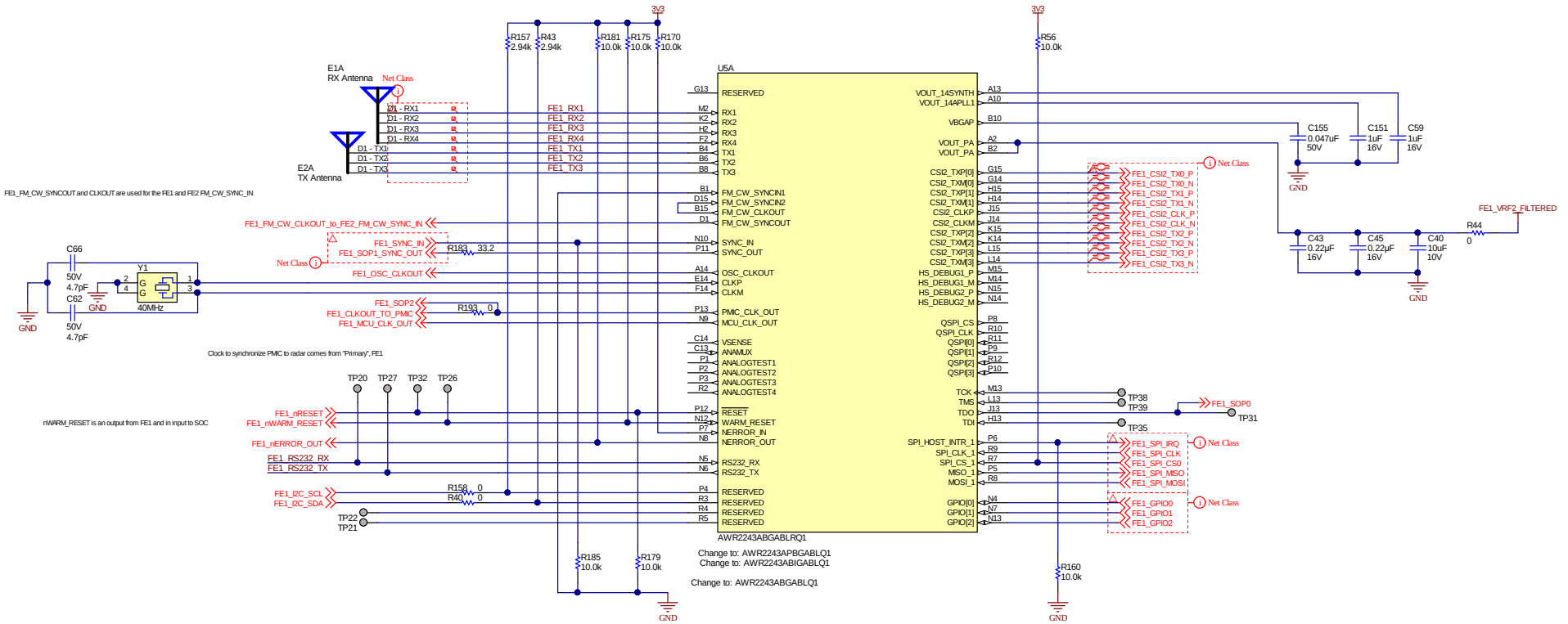
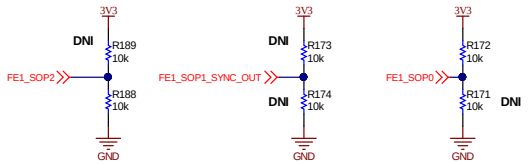
FRONT END 1





SOP_MODE1	"010"	SCAN/ATPG
SOP_MODE2	"011"	DEV/FLED/ORBIT
SOP_MODE3	"000"	TBD
SOP_MODE4	"001"	FUNC - > DEFAULT VALUE FOR OUTPUTS
SOP_MODE5	"101"	DEV MANAGEMENT -> FOR FLASHING

Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047	Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047 Rev: 2	Sheet Title: XDS110 Interface_1B	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 7 of 17
Drawn By: B. Shaffer	File: FE1_IO.schdoc	Size: B
Engineer: B. Shaffer	Contact: http://www.ti.com/support	

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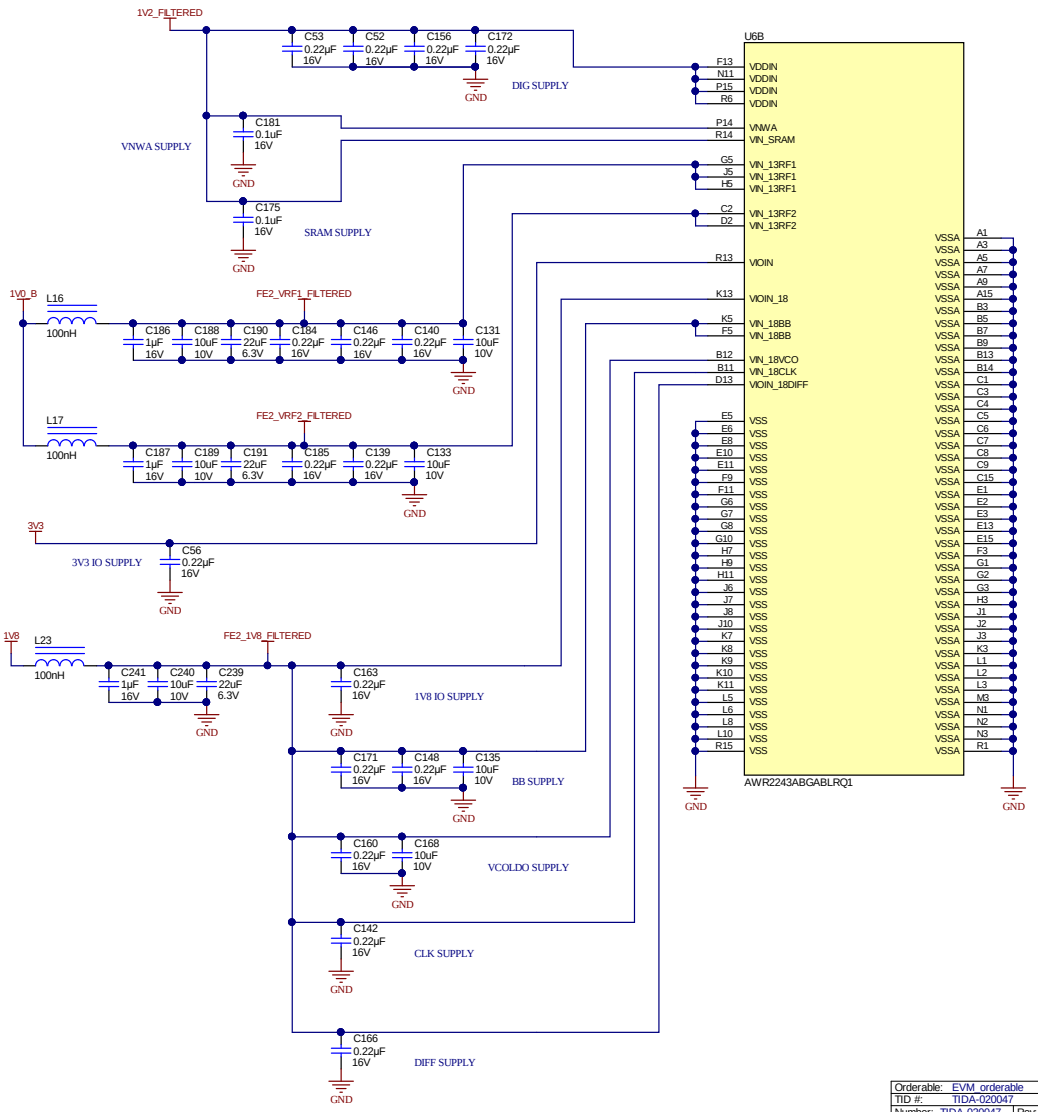
FRONT END #2 POWER CONNECTIONS



Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 11/1/2022
TID #: TIDA-020047		Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047	Rev: 2	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 8 of 17
Drawn By: B. Shaffer		File: FE2_PWR.SchDoc	Size: B
Engineer: B. Shaffer		Contact: http://www.ti.com/support	

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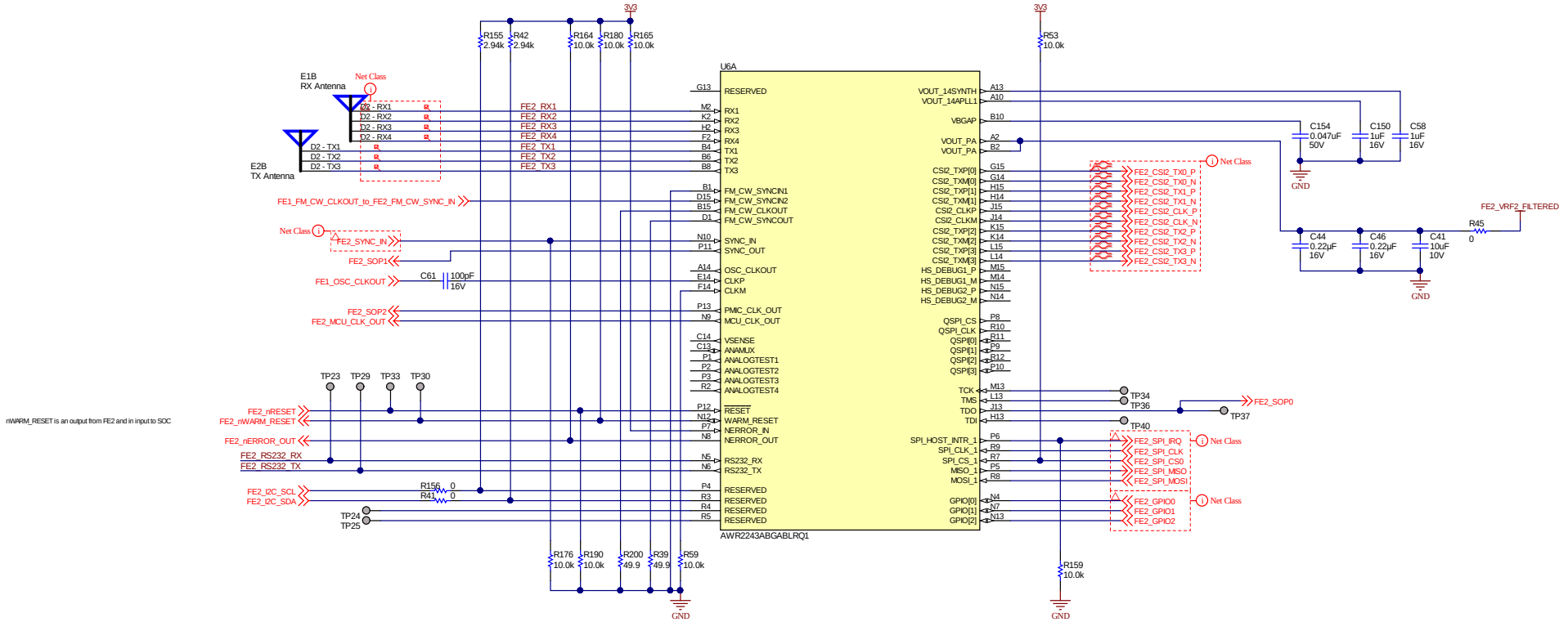
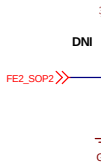
FRONT END 2

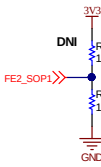


nWARM_RESET is an output from FE2 and in input to SOC

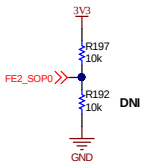
SOP_2



SOP_1



SOP_0



SOP_MODE1	"010"	SCAN/ATPG
SOP_MODE2	"011"	DEV/FLED/ORBIT
SOP_MODE3	"000"	TBD
SOP_MODE4	"001"	FUNC - > DEFAULT VALUE FOR OUTPUTS
SOP_MODE5	"101"	DEV MANAGEMENT -> FOR FLASHING

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047		Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047	Rev: 2	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 9 of 17
Drawn By: B. Shaffer		File: FE2_IO.schdoc	Size: B
Engineer: B. Shaffer		Contact: http://www.ti.com/support	

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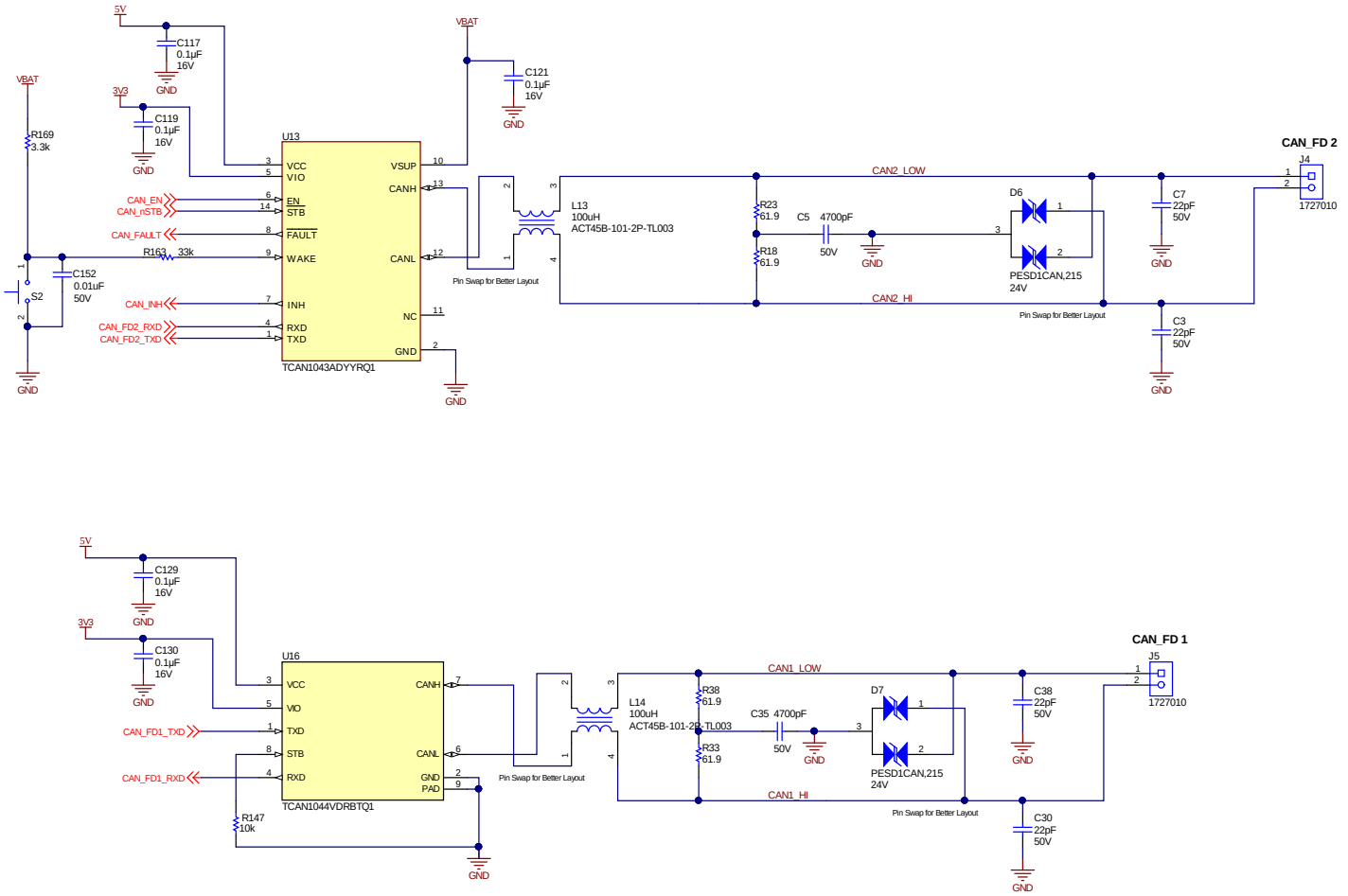
CAN INTERFACE



Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 11/1/2022
TID #: TIDA-020047	Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047 Rev: 2	Sheet Title: CAN Interface	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 10 of 17
Drawn By: B. Shaffer	File: 2CAN.SchDoc	Size: B
Engineer: B. Shaffer	Contact: http://www.ti.com/support	

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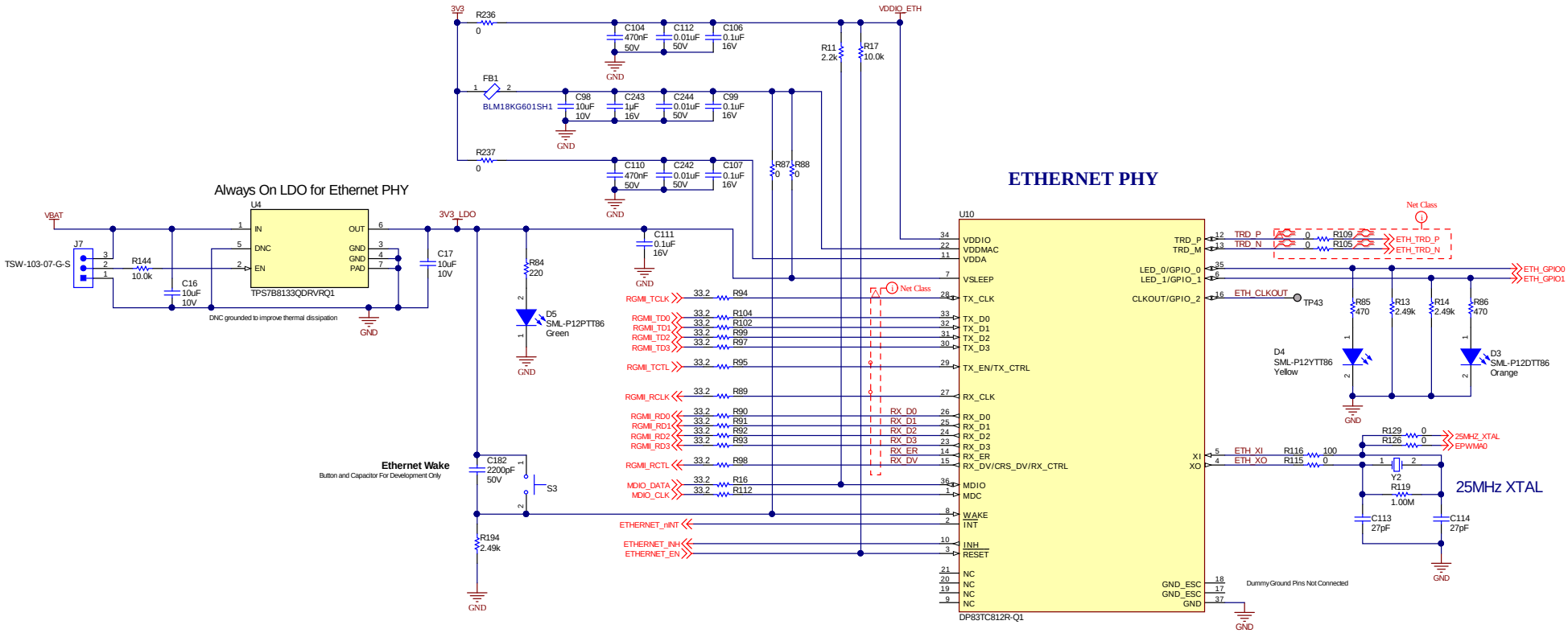
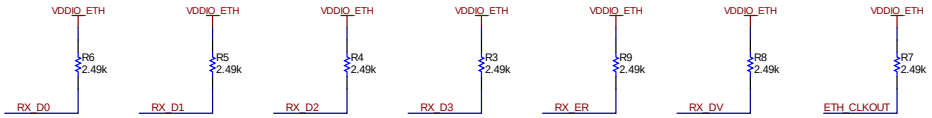
ETHERNET



BOOTSTRAP CONFIGURATION PINS

Resistor Values must be changed to change Modes, refer to datasheet for proper values



Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 11/1/2022
TID #: TIDA-020047		Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047	Rev: 2	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 11 of 17
Drawn By: B. Shaffer		File: Enet_PHY.SchDoc	Size: B
Engineer: B. Shaffer		Contact: http://www.ti.com/support	

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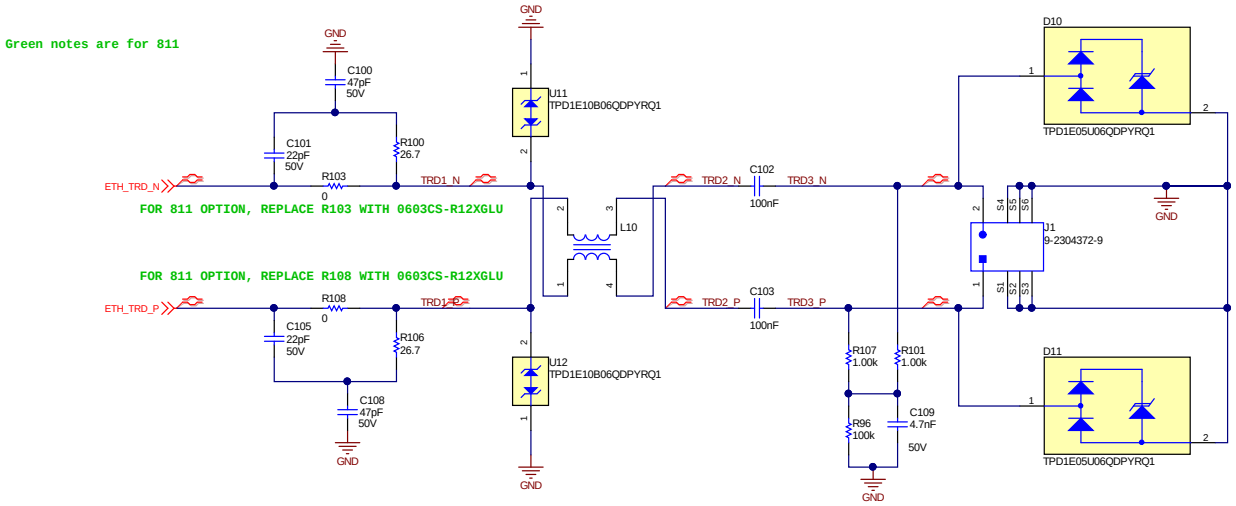
ETHERNET CONNECTOR



Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 11/1/2022
TID #: TIDA-020047	Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047 Rev: 2	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 12 of 17
Drawn By: B. Shaffer	File: Enet_Conn.SchDoc	Size: B
Engineer: B. Shaffer	Contact: http://www.ti.com/support	

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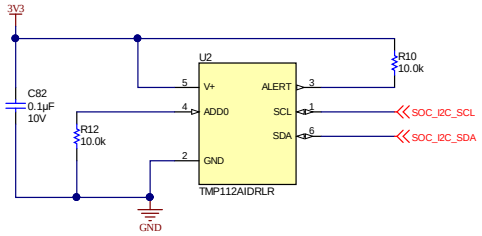
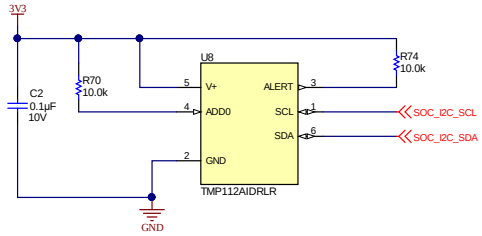
MISC

ONBOARD TEMP SENSORS

TEMP SENSOR AWAY FROM PMIC
I2C ADDRESS 1001000x



TEMP SENSOR CLOSE TO PMIC
I2C ADDRESS 1001001x



Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047	Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047 Rev: 2	Sheet Title: XDS110 Interface_1A	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 13 of 17
Drawn By: B. Shaffer	File: Temp.schdoc	Size: B
Engineer: B. Shaffer	Contact: http://www.ti.com/support	

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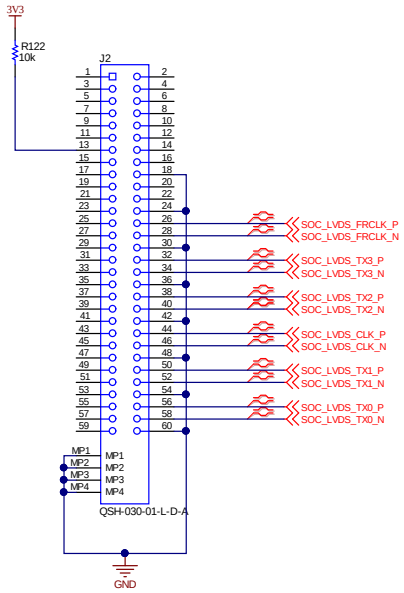
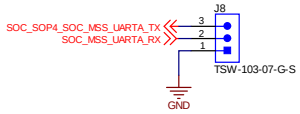
Connectors

60 PIN DEBUG CONNECTOR

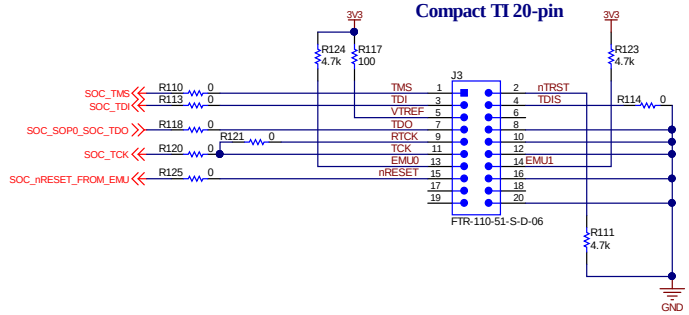


UART Test Pins

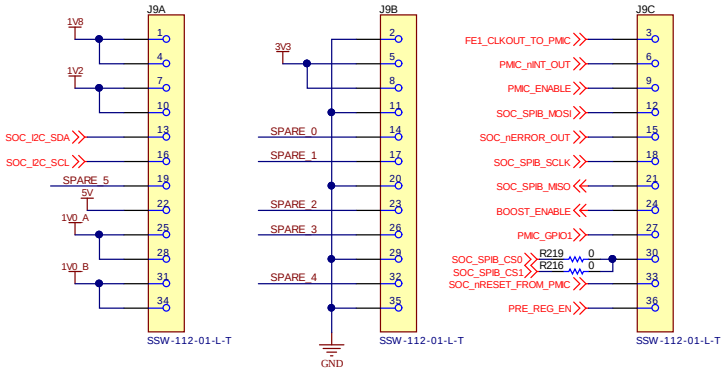


Off Board Emulator

Compact TI 20-pin



Power Reference Connector



Orderable: EVM orderable	Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047	Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047 Rev: 2	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 14 of 17
Drawn By: B. Shaffer	File: Connectors.schdoc	Size: B
Engineer: B. Shaffer	Contact: http://www.ti.com/support	

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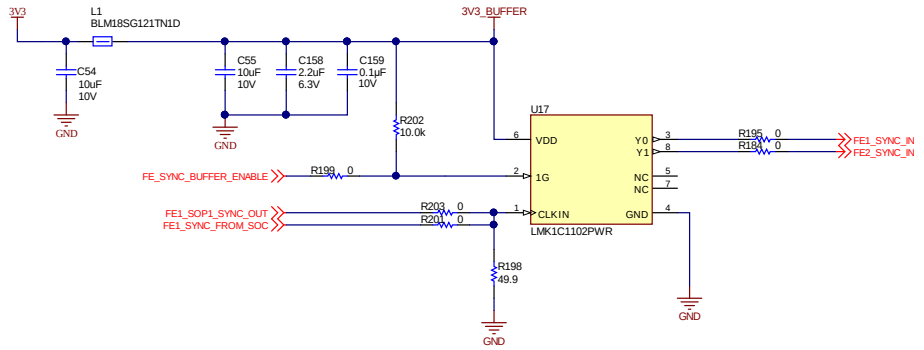
Clock Distribution



Digital SYNC from FE1 or SOC is buffered and fed into FE1 and FE2

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047		Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047	Rev: 2	Sheet Title: PMIC	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 15 of 17
Drawn By: B. Shaffer		File: Clock_Buff.SchDoc	Size: B
Engineer: B. Shaffer		Contact: http://www.ti.com/support	

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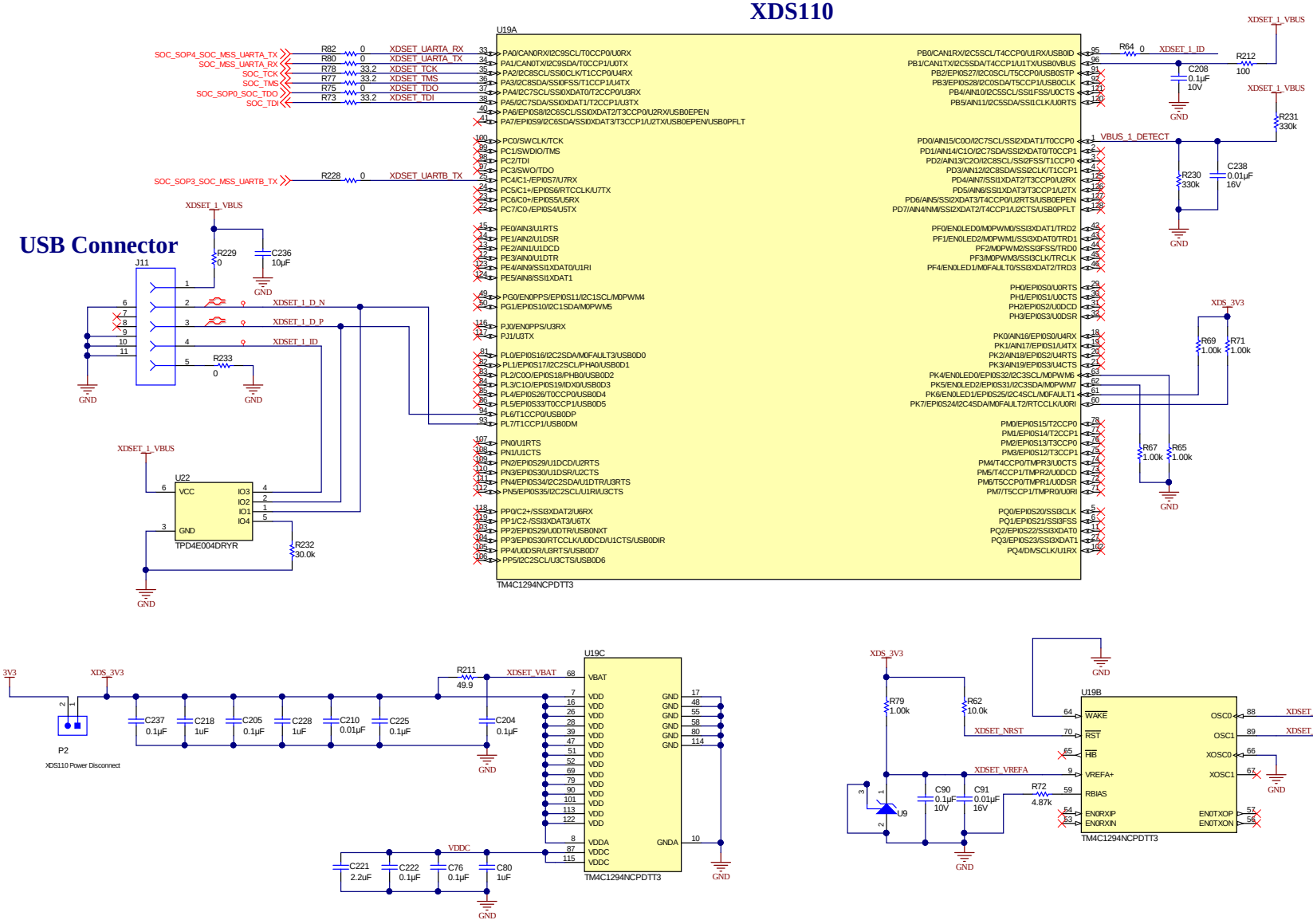
On Board Emulator
XDS110



Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047		Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047	Rev: 2	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 16 of 17
Drawn By: B. Shaffer		File: XDS110.schdoc	Size: B
Engineer: B. Shaffer		Contact: http://www.ti.com/support	

FID2 FID1 FID3 FID4 FID5 FID6

PCB Number: TIDA-020047
PCB Rev: E2

PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

PCB LOGO
ESD Susceptible

Shunt Table		
Shunt	Pinheader	Contacts
Z1	P2	1-2
Z2	J7	2-3
Z3	J6	1-2

Z1 SPC02SYAN
Z2 SPC02SYAN
Z3 SPC02SYAN

Variant/Label Table	
Variant	Label Text
CAN WITH 812	CAN WITH 812
CAN WITH 811	CAN WITH 811
812 WITH CAN	812 WITH CAN

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

H1 NY PMS 440 0025 PH
H2 NY PMS 440 0025 PH
H4 NY PMS 440 0025 PH
H3 NY PMS 440 0025 PH

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

MP1 1902D
MP4 1902D
MP3 1902D
MP2 1902D

Orderable: EVM orderable	Designed for: Public Release	Mod. Date: 11/2/2022
TID #: TIDA-020047	Project Title: Dual MMIC cascade radar reference design	
Number: TIDA-020047 Rev: 2	Sheet Title: Hardware	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 17 of 17
Drawn By: B. Shaffer	File: Hardware.SchDoc	Size: B
Engineer: B. Shaffer	Contact: http://www.ti.com/support	

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