TSC2013
Application Note

July 1, 2014

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1 TSC2013 Application Note

1.1 TSC2013 Power-On-Reset and Reset Consideration.

There are three ways to reset the TSC2013 to its default working state. Power-on-Reset (POR) discussed in section 1.1.1, Hardware Reset discussed in section 1.1.2 and Software Reset discussed in section 1.1.3.

As shown in section 1.1.1, the requirements for ensuring a proper TSC2013 POR are very stringent and may be very hard to meet in many applications. To workaround, users should apply a proper hardware or software reset, instead or additionally.

1.1.1 TSC2013 Power-On-Reset

Based on design principles and extensive tests with TSC2013, the device's power must meet a specific ON/OFF timing and sequence in order to make sure the **Power-On-Reset** (POR) is implemented at each and every time the TSC2013 is powered on and a lockup is prevented.

During the TSC2013 SNSVDD powering on, the POR will bring TSC2013 into a known default working state by initializing the internal state machine, data and control registers, and output pins' condition. Without the POR, TSC2013 may start up in a random state and may even cause the TSC /PINTDAV pin does not response correctly.

The TSC2013 POR circuit was designed that it does not consume power during the TSC normal operation; and the power-down current is kept as low as possible (max power-down supply current: 0.8uA).

Such a POR circuit in TSC2013 requires a certain specific power-up/down ramps and sequences.

The following Figure 1 and Table 1 contain the recommended power-off times and ON/OFF ramp specifications:

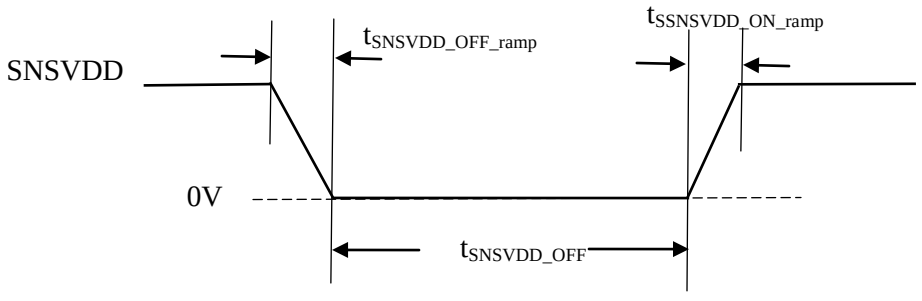


Figure 1-1 POR Sequence

Temperature Range	Minimal $t_{SNSVDD\text{-}OFF\text{-}ramp}$	Minimal $t_{SNSVDD\text{-}ON\text{-}ramp}$	Minimal $t_{SNSVDD\text{-}OFF}$ [*]
-40^{O}C to -21^{O}C	12kV/sec	12kV/sec	1.2sec

-20°C to +85°C	2kV/sec	12kV/sec	200msec

[*] $t_{SNSVDD-OFF}$ time starts when TSC2004/5/6 SNSVDD reaches and stays at 0V.

Table 1-1 Requested POR Timings

Why Request a Minimal t_{SNSVDD_OFF} Time

The POR circuit of the TSC2013 contains a capacitor that is charged when the device powers up, generating an internal reset signal, and discharged after the TSC2013 supply is switched off. The TSC2013 is designed for low power operation, therefore the POR takes time to charge and discharge the capacitor, especially under cold temperatures (<-20 ℃). If the SNSVDD OFF time is not sufficient, the device may lock up, and only a power recycle will resolve this lockup condition.

Why Request a Minimal $t_{SNSVDD\_OFF\_ramp}$ and $t_{SNSVDD\_ON\_ramp}$ Ramp

To guarantee the proper initialization of the TSC2013 it is required that the device reaches a certain voltage before the internal POR signal is released. If the power supply on ramp is too slow the device might come up in a random state and may cause a lock up.

The capacitor inside the POR circuit needs to be discharged through the TSC2013 SNSVDD pin. To support a proper discharge it is recommended to have a certain SNSVDD off ramp and also provide a low resistance path on the SNSVDD pin, when TSC2013 supply is switched off.

1.1.2 TSC2013 Hardware Reset

The Hardware Reset Pin /RESET, is available to perform a system reset to reset the device if the pulse width meets the timing requirement (at least 10µs wide; SNSVDD/IOVDD ≥ 1.6V). Any /RESET pulse less than 5µs will be rejected. To accommodate the timing drift between devices because of process variation, a /RESET pulse width between 5µs to 10µs falls into the gray area that is not recognized, and the result is undetermined; this situation should be avoided. A good reset pulse must be low for at least 10µs (SNSVDD/IOVDD ≥ 1.6V). There is an internal spike filter to reject spikes up to 20ns wide.

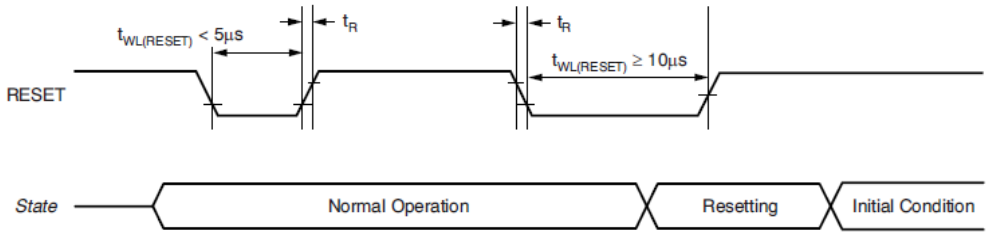


Figure 1-2 Hardware Reset Timing

1.1.3 TSC2013 Software Reset

During normal operation a Software Reset can be sent by the host processor to the TSC through setting '1' the SWRST bit in Control Byte 1, bit D1.

Table 6. Control Byte 1 Bit Register Description (D7 = 1)

BIT	NAME	DESCRIPTION
D7	Control Byte ID	1
D6-D3	C3:C0	Converter Function Select as detailed in Table 7
D2	RM	0: 10 Bit 1: 12 Bit
D1	SWRST	Software Reset. This bit is self-clearing. 1: Reset all register values to default
D0	STS	Stop bit for all converter functions. This bit is self-clearing.

Figure 1-3 Screenshot from TSC2013 Data Sheet Control Byte 1 Description

1.2 TSC2013 Power Up Considerations

1.2.1 Power OFF Cycles during Normal Operation

The TSC2013 is a low power device and therefore it is not necessary and not recommended to switch OFF the TSC2013 device during normal operation.

Every power cycle (power ON → power OFF → power ON) needs to meet the requirements described in section 1.1.1. If that can't be avoided if is recommended to issue a Hardware Reset after every power cycle.

1.2.2 Glitches on TSC2013 Supply during Normal Operation

A TSC2013 SNSVDD or IOVDD power glitch during normal operation may cause a lockup condition. Therefore it is important that the system is able to either recycle the power in the system following the requirements stated section 1.1.1 or issue a Hardware Reset described in section 1.1.2.

1.2.3 Affections from TSC2013 regarding Digital Pins

In many applications, users use the same power supply for both analog and digital supplied to TSC2013. SNSVDD is connected with the IOVDD. Under such cases, the logic high status on the TSC2013 digital pins before power-up become a concern for the proper TSC2013 POR.

TSC2013 has several digital IO pins, as listed in table below.

TSC2013 pin name	Description
/PINTDAV	Digital Output. An interrupt on pen/data status
/RESET	Digital input. Hardware reset to the TSC.
SCL	Open drain/collector. I2C bus clock.
SDA	Open drain/collector. I2C bus data.
A0	Digital input. TSC address A0 for I2C bus.
A1	Digital input. TSC address A1 for I2C bus.

Table 1-2 TSC2013 Digital Pin List

Every TSC2013 pin is well protected against ESD strikes. The TSC2013 /RESET, A0, A1 pins have the same protection as the SDA and SCL pins. That means /RESET, A0 and A1 can be pulled high before the TSC2013 is powered up, without activating an internal ESD diode and causing a power up of the TSC2013. The output pin /PINTDAV is a digital output pin. The host processor has to define the /PINTDAV pin as an input to the host processor without any pullup/pulldown feature. In some cases the default of the host processor might be an output with an enabled pullup/pulldown feature and the host processor firmware is changing this definition later to an input. If the TSC2013 is not powered up yet it could also cause a power up through the ESD cells as shown in Figure 1-4 through the yellow line. Such a "false" power up could not ensure a proper power supply to the TSC2013 and TSC2013's correct POR could not be ensured.

In case the TSC2013 is already powered up, both parts might drive different levels on the same line and cause high power consumption.

The TSC2013 /PINTDAV pin should be connected to the correct pin on the host processor to avoid bus conflicts and illegal powering up the TSC2013.

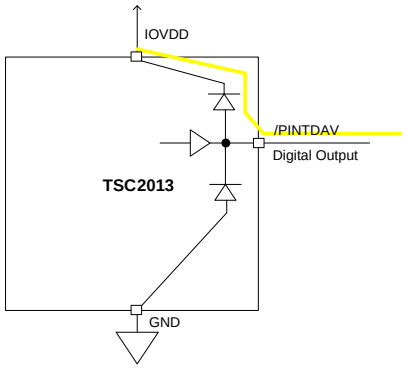


Figure 1-4 Internal ESD Protection Diodes at TSC2013 /PINTDAV pin

1.2.4 Suggested Hardware Reset during Power-On

The suggested sequence during power up would be to keep /RESET pin low, wait for the supplies to settle and then wait for at least 10µs before releasing the /RESET pin. The waveform is shown below.

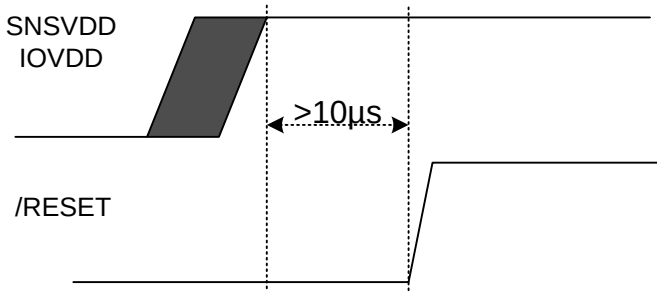


Figure 1-5 Suggested /RESET waveform during Power-On

1.3 PWB Layout Guidance

1.3.1 Common Practises

It is recommended to follow commonly accepted design practices for PWB layout, such as the *Generic Standard on PWB Design* IPC 2221A [1]. Also refer to [2].

Some of the more important and widely accepted points for PWB layout include:

- Use a ground plane where possible, and connect the signal ground through vias to the ground plane rather than printed traces;
- Keep the analog ground and digital ground separate at each power-supply stage, and connect them together at a single point;
- Use large trace for power supply lines to provide low impendence, and add bypass capacitors to each power supply, located as close as possible to the power pins;
- Avoid wiring digital lines under the device;
- Avoid cross-wiring between analog and digital signals;
- Minimize the area and length of loops for the required analog wiring.

1.3.2 Analog Connection

In the specific case of a resistive touch screen system, additional care should be given to the connection between the TSC2013 and the touch screen. This connection is also known as the *analog interconnection* or *analog interface*. Figure 1-6 shows a typical connection diagram for the TSC2013 in a touch application, as given in the TSC2013 data sheet. Note the analog connection here.

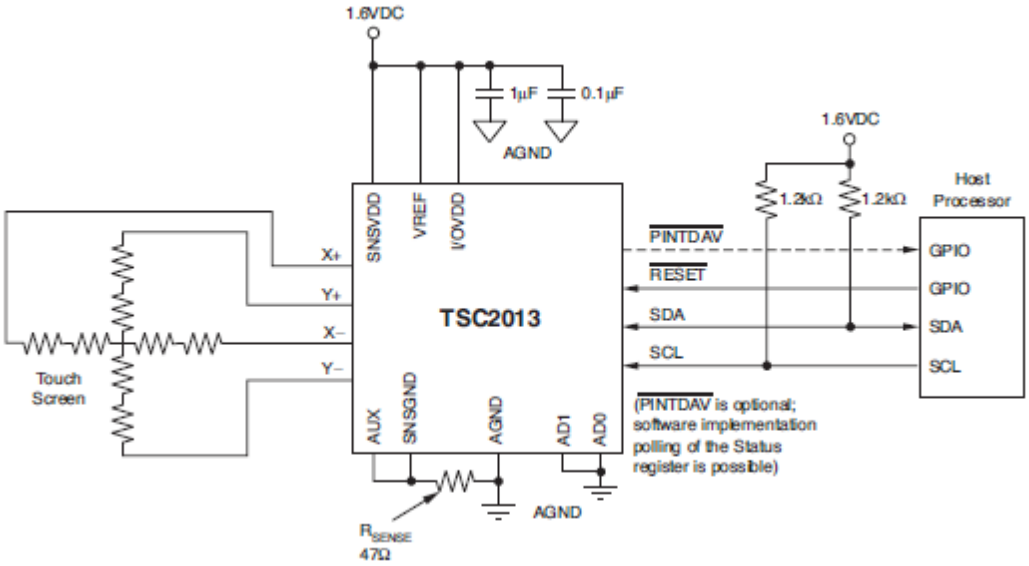


Figure 1-6 Typical Circuit Configuration

The Analog Interface should be kept as short, as simple, and as secure as possible because resistive touch screens have fairly low resistance (usually several hundred ohms). Longer connections can not only bring in

possible pigtail resistance between the TSC2013 and the touch screen, but also increase the chance for noise, ESD and other interferes to affect the analog input lines. Poor connections can be another source of noise and error when the contact resistance changes with flexing or vibrations, and can even cause the entire touch screen system to malfunction or fail.

Electromagnetic interference (EMI) noise can be a major source of error in touch screen applications that require an LCD panel with backlighting. This type of noise can couple through the LCD panel to the touch screen and enter the TSC2013 through the analog interface, causing the converted ADC data to flicker. To reduce this type of error, use a touch screen with a bottom-side metal layer connected to ground. This configuration couples most of the noise to ground, and has been shown to be very helpful in a range of embedded touch screen applications. Additionally, display interface and touch interface should be separated to avoid crosstalk. Remember to use TSC2013 internal MAV filtering capabilities!

1.3.3 R_{SENSE} Resistor Selection

To detect two touches, an external R_{SENSE} resistor must be added, as shown in Figure 1-6. The value of R_{SENSE} depends on the touch panel resistance. The ratio between the lowest touch panel resistance and R_{SENSE} should be approximately 4.5.

See chapter 2 for more details about dual touch functionality.

1.3.4 Power and Grounding

Care should be taken with the physical layout on power and grounding of the TSC2013 circuitry.

The analog-to-digital converter (ADC) in TSC2013 device is a successive-approximation-register (SAR) architecture ADC. The generic SAR architecture is sensitive to glitches or sudden changes in the power supply, ground connections, and digital inputs that occur before latching the output of the analog comparator. Therefore, during any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. Once the SAR ADC has made a decision to keep or reject a bit-value, the converter cannot go back in time and change the previous decision.

With this consideration in mind, power to the TSC2013 should be clean and well-bypassed, with bypass capacitors between power and ground. In a single supply system VDD as shown in Figure 1-6 SNSVDD is connected to VREF and also IOVDD. A 0.1μF ceramic bypass capacitor should be added between (VDD and GND). A 1μF to 10μF capacitor may also be needed if the impedance of the connection between VDD and the power supply is high. These bypass capacitors must be placed as close as possible to the VDD pins, optimally right up against the TSC2013. From the ESD protection point of view, the traces connecting the VDD bypass capacitors to ground should be as short as possible. The VDD side of the capacitors needs to be placed right on the VDD trace and the other side of the capacitors right on the ground plane.

The ground pins of the TSC2013 device and its analog surrounding circuit should be connected to a clean ground point. In many cases, this point is the analog ground. Avoid connections that are near the grounding point of a microcontroller or digital signal processor. If needed, it is recommended to have a separate ground trace directly from the converter to the power-supply entry or battery connection point. The ideal layout

includes an analog ground plane dedicated to the converter and associated analog circuitry. From the ESD protection point of view, provide more ground vias to the ground plane right below the TSC2013 ground and the VDD bypass capacitors. It is important to ensure there is ample ground path to the system ground to allow ESD discharge current if the touch screen subsystem is implemented on a flex.

1.3.5 ESD Protection Considerations

- If possible, place TSC device on the main PWB to mitigate possible ground bouncing problem
- Do not connect resets & interrupts to long traces or cables.
- The TSC2013 has an internal counter which makes sure that glitches on the /RESET line are not causing an internal reset. To trigger a reset the pulse width has to be at least 10µs. All pulses less than 5µs are ignored. If there is a noise coupling on the reset line which could cause longer glitches consider adding a filter (capacitor 1~10nF) right next to the reset pin.
- If there is a need for filters on TSC2013 analog input lines, place filters close to the TSC2013, right next to the TSC2013 pin.
- Avoid direct connection between the chassis ground (metal frame) and the PWB signal ground near the touch screen device
- Design extra space for ESD protection circuits that might be needed into the original layout (these extra components can be added later when needed)
- Transient voltage suppressor selection guidelines
- When selecting transient voltage suppressors, consider the maximum capacitance that can be placed on a signal while keeping the intended signal integrity
- Select devices with low breakdown voltage and low clamping voltage to reduce voltage/current going to receiver circuits
- Suppressors need to turn on within 1 ns to be effective against the fast rising ESD currents: IEC ESD current rise time ~0.8 nsec

Additional Notes

- Connect the analog input pin AUX to ground if not used.
- Avoid any active trace going under the TSC2013 analog pin, unless they are shielded by a ground or power plane.

As the last line of defense, an nFs ~ 100nFs cap may be added to an analog input line to provide a low-pass filter and extra ESD path for the TSC2013 analog pin (X+/X-/Y+/Y-). As repeatedly mentioned, the cap should be put right next and as close as possible to the TSC2013 pin. Note that the added capacitance on the analog line would increase the settling time of the touch signal, especially under weak touch when the equivalent “R” there could be in 100K-ohm to M-ohm. Refer to the Section of the application note [3] on the capacitance affect and selection.

Even though the above suggestions are based on the widely accepted PWB design practices for today's resistive touch screen systems, each layout must be carefully reviewed, because touch applications might have conflicting requirements with respect to power, cost, size, and weight, and each application and design is unique.

1.3.6 Summary for PWB layout design

Ground wiring should be done by using wide traces as possible. Especially AGND pin which is the ESD ground pin. Connection to system ground should done firmly. Avoid cutting ground planes near TSC2013 which may loose ground effectiveness in ESD situations. Ground connection by using only via is not good method to connect TSC2013 to system ground. Vias have resistance which is effecting in ESD situations.

Plan clear ground path to system ground. System ground can be battery ground or separate ground layer(s) inside main PWB.

Route power to TSC2013 by using wide traces. Even if power consumption do not require that. Place bypass capacitors nearby TSC2013. Consider also bypass caps nearby voltage source is trace is long and thin. Avoid cutting ground planes during power line tracing or any other traces as common PWB practices guide.

If external ESD filtering components are used those should be connected firmly to touchlines and ground for optimum ESD current suppression.

If digital and analog signals are routed in adjacent layers, one on top of the other, try to route them in 90 degree angles to avoid crosstalking.

2 Dual Touch functionality

2.1 Principle and system requirements

Resistive dual touch by using TC2013 is based to principle to measure resistance changes between X and Y panel. Resistive touch screen has two ITO layers which are apart each other. When user uses single finger only minor parallel connection is happening between these two layers.

During dual touch when fingers are a part of each other parallel connection is much higher and then reducing panel resistance. As TSC2013 is measuring both X and Y layer panel resistances finger distance can be easily calculated from resistance change. This is achieved by using one external resistor which is connected internally to series with measured X/Y panel.

System level requirements:
-Normal 4-wire resistive touch screen with low activation force (from center area down to 0.1-0.3N) to enable smooth dual touch operation
-Rsense resistor value is lowest panel resistance (X or Y layer) / ~4.5. This gives best dynamic range for dual touch separation.
-Use highest operation voltage with TSC2013 which is compatible to your system to achieve best possible SNR.

TSC2013 enables dual touch function by using following methods:
-Measuring all four nodes and using those to calculate center point of touch / touches.
-Also touch positions are placed correctly to right quadrants by using four node information
-Two layer panel resistances are measured by using single external resistor which is connected internally series with measured panel layer. Resistance change is interpreted as a finger distance change.
-Host side processor is doing all the calculations. TSC2013 provides only data.

2.2 Single touch operation

TSC2013 can be used also only for single touch operation. By measuring all 4-wire nodes (X+ / X- / Y+ /Y-) we can achieve even more precise touch accuracy than normal resistive touch screen controllers.

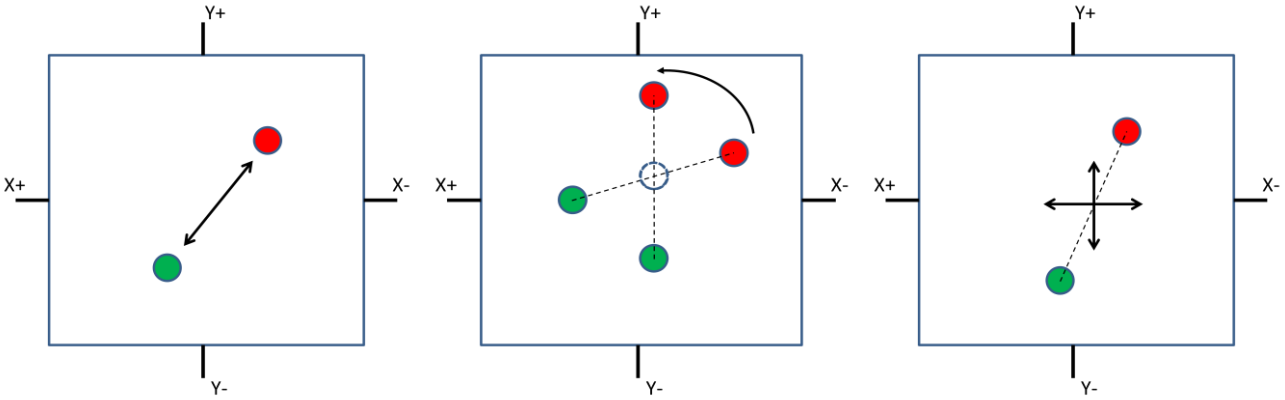
TI advises to calculate center point of touch by using both node values. For example X = 0.5x(X+ - X-) + X+. This same method is used on dual touch middle point calculation.

2.3 Dual touch operation

Dual touch function requires all triplets (X, Y and panel currents) to be measured. Z1 & Z2 information can be used to set threshold for robust touch as in single touch operation.

Dual touch accuracy is not same as actual two touches. TSC2013 dual touch function provides gesture type of addition to normal single touch.

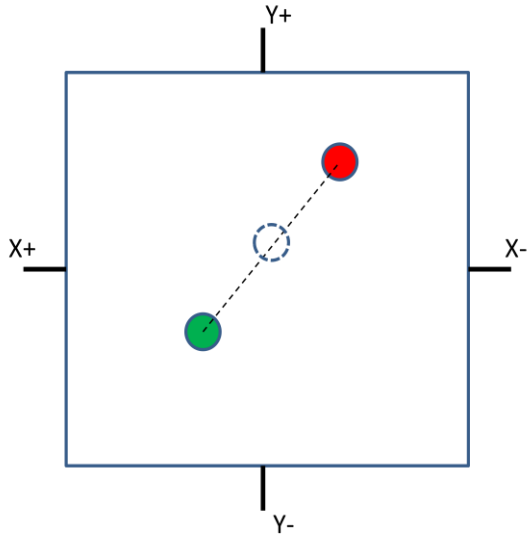
Supported gesture types which can be in operation at the same time:
-Zoom in/out.
-Rotation. Depending from system calibration movement tracking over main axis might vary.
-Dual finger movement (finger distance can be same or vary)



2.4 Calculating dual touch positions

2.4.1 Touch middle point

Dual touch center point is first measured. Red and green spots are actual touches. Resistive 4-wire reports dual touch middle point by nature.

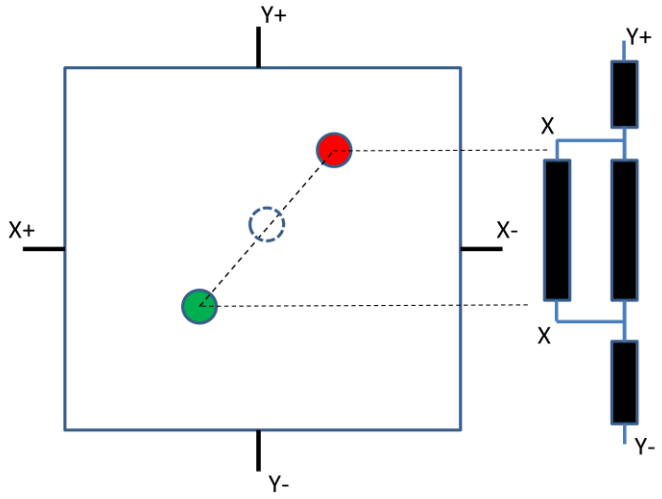


Calculation of dual touch middle point:
Xmp = (X+ - X-)/2 + X-
Ymp = (Y+ - Y-)/2 + Y-

2.4.2 Finger distance

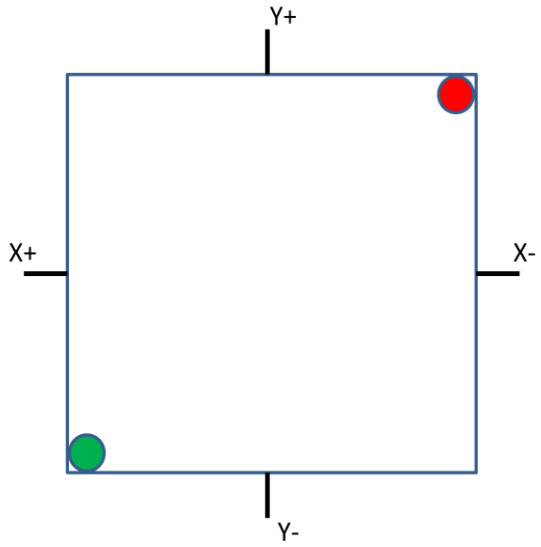
Parallel connection between two ITO layers reduces panel resistances versus distance of these two touches.

Both X and Y panel has idle current corresponding current flow through touch without actual touch. Unless panel shape is exactly square Ix and Iy have different idle current values



Y-panel current is measured while X-panel parallel connection is reducing Y-panel resistance.

To calculate finger distance we need to know what is minimum panel resistance when fingers are at maximum distance from each other. Below picture shows that situation.

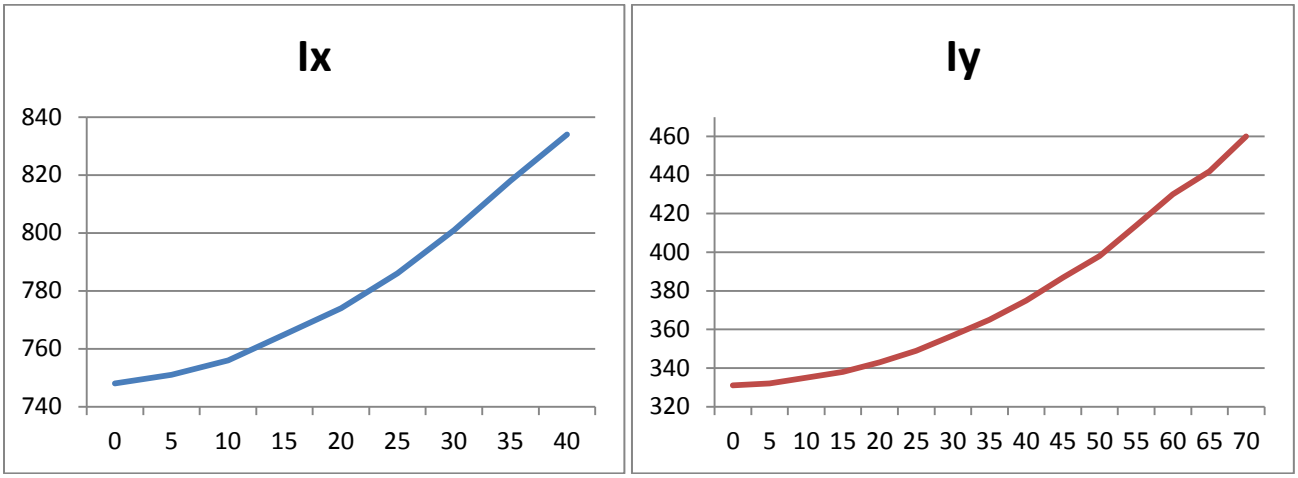


Ix and Iy have minimum value in this situation.

Finger distance can be now calculated by using this method:
Xfd = (Ixmax – Ix) x Xscale
Yfd = (Iymax – Iy) x Yscale

Xfd and Yfd are scaled to fit touch screen dimensions.

Finger distance vs panel resistance change is not linear. See example measurement from actual panel.

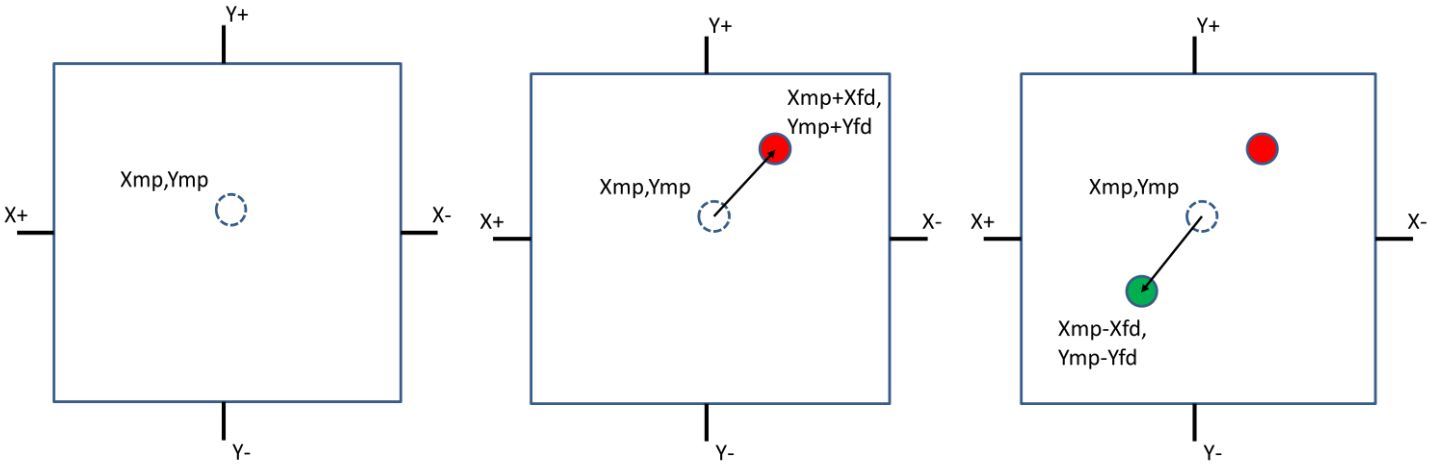


To improve dual touch usability linearization algorithm can be used.

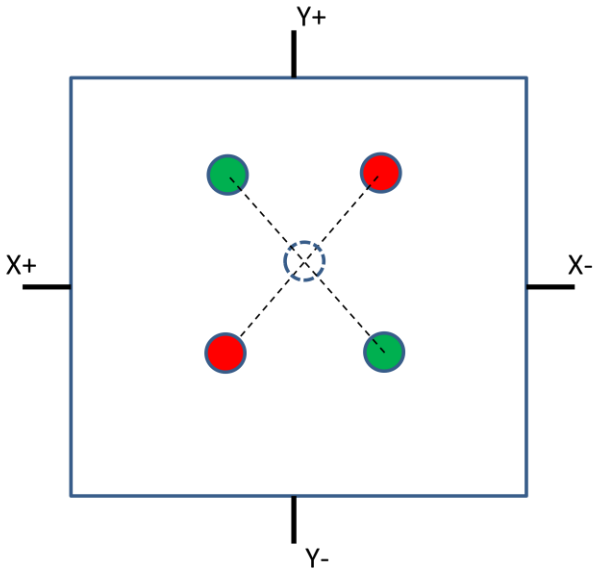
2.4.3 Calculating touches to coordinate system and placing them to correct quadrant

Procedure to calculate dual touch positions:

1. Measured middle points Xmp and Ymp is starting point
2. First touch point is calculated from middle point + Xfd & Yfd
3. Second touch point is opposite side from calculated 1st touch



Finally we need to locate touches and place them in correct quadrants. At this point system cannot detect following situation.



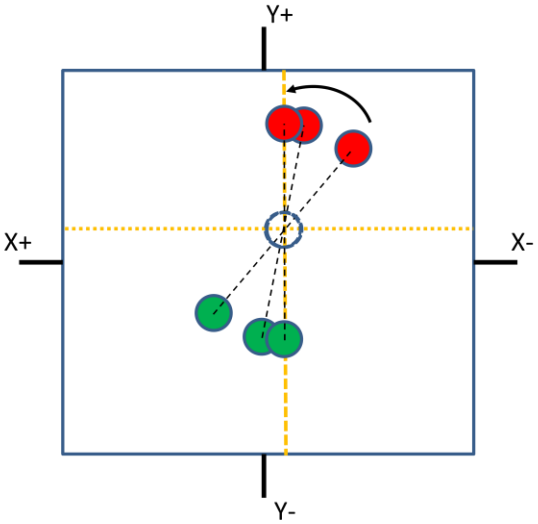
System cannot detect which dual touch set is correct. Red or green touches.

To overcome this problem data from X+ / X- / Y+ / Y- nodes are used to select correct dual touch set. Principle is to compare X+ vs X- and Y+ vs Y- voltages.

Red dots are correct touches if X+ < X-, similarly Y+ < Y-
Green dots are correct touches if X+ > X- and Y+ > Y-

2.4.4 Special cases

If system has high noise and robust finger tracking is needed during rotation gesture over main axis hysteresis is needed nearby main axis. This avoids touch jumping/jitter. Hysteresis in this area should be tuned case by case.



3 References

[1] "IPC-2221A, Generic Standard on Printed Board Design", Association Connecting Electronics Industries. February 1998. http://www.lg-advice.ro/pdf/IPC-2221A-cuprins.pdf

[2] "PWB Design for Real-World EMI Control", Bruce R. Archambeault, July 2002.

[3] “Reducing Analog Input Noise in Touch Screen Systems”, TI Application Report SBAA155A. http://focus.ti.com/lit/an/sbaa155a/sbaa155a.pdf

[4] “Operation Schemes of Touch Screen Controllers”, TI Application Report SLAA359. http://focus.ti.com/lit/an/slaa359/slaa359.pdf

4 Revision History

Date	Editor	Brief Description
3/22/11	HB	Initial Version
3/23/11	MS	Updated
2/19/13	MS	Dual Touch chapter added
7/01/14	JL	Revised for TI Design

End Of Document

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