Errata

AWR6843AOP Device Silicon Errata Silicon Revision 2.0

Table of Contents

Copyright © 2022 Texas Instruments Incorporated

1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (AWR6843AOP).

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / mmWave sensor devices. Each of the Radar devices has one of the two prefixes: XAx or AWRx (for example: **XA6843A**RBGALP). These prefixes represent evolutionary stages of product development from engineering prototypes (XI) through fully qualified production devices (AWR).

Device development evolutionary flow:

XA —	Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
AWR —	Production version of the silicon die that is fully qualified.

XA devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

Copyright © 2022 Texas Instruments Incorporated

3 Device Markings

Figure 3-1 shows an example of the AWR6843AOP Radar Device's package symbolization.

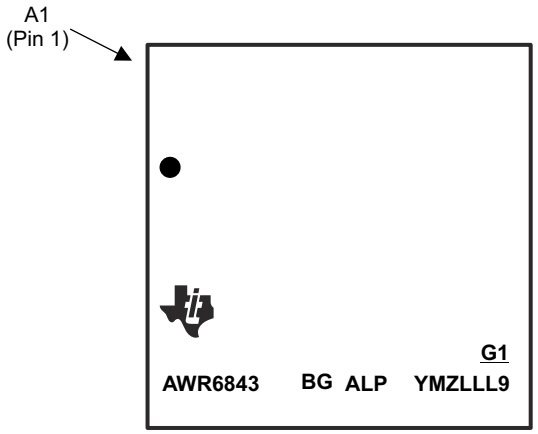


Figure 3-1. Example of Device Part Markings

This identifying number contains the following information:

- **Line 1:** TI Logo
- **Line 2:** G1 = "Green" Package Build (must be underlined)
- **Line 3:**
  - XAWR6843 = xAWR6843 Device Identifier (Pre-Production Automotive), AWR6843 ES2.0 Device Identifier (Production Automotive)
  - BG ALP = Package Identifier
  - YM = Year/Month Code
  - Z = Assembly Site Code
  - LLL = Assembly Lot Code
  - 9 = Primary Site Code

Copyright © 2022 Texas Instruments Incorporated

4 Usage Notes

Usage notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These usage notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

4.1 MSS: SPI Speed in 3-Wire Mode Usage Note

The maximum SPI speed under 3-wire operation was only tested up to 33 MHz. This affects AWR6843AOP ES2.0.

Copyright © 2022 Texas Instruments Incorporated

5 Advisory to Silicon Variant / Revision Map

Table 5-1. Advisory to Silicon Variant / Revision Map

Advisory Number	Advisory Title	AWR6843AOP ES2.0
Main Subsystem		
MSS#25	Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs	X
MSS#26	DMA Requests Lost During Suspend Mode	X
MSS#27	MibSPI in Slave Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1	X
MSS#28	A Data Length Error is Generated Repeatedly in Slave Mode When IO Loopback is Enabled	X
MSS#29	Spurious RX DMA REQ From a Slave Mode MibSPI	X
MSS#30	MibSPI RX RAM RXEMPTY Bit Does Not Get Cleared After Reading	X
MSS#31	CPU Abort Generated on a Write to Implemented CRC Space After a Write to Unimplemented CRC Space	X
MSS#32	DMMGLBCTRL BUSY Flag Not Set When DMM Starts Receiving A Packet	X
MSS#33	MibSPI RAM ECC is Not Read Correctly in DIAG Mode	X
MSS#34	HS Device Does Not Reboot Successfully on Warm Reset Getting Triggered by Watchdog Expiry	X
MSS#36	DMA Read From an Unimplemented Address Space is not Reported as a BUS Error	X
MSS#37B	DCC Module Frequency Comparison can Report Erroneous Results	X
MSS#38A	GPIO Glitch During Power-Up	X
MSS#39	The state of the MSS DMA is left pending and uncleared on any DMA MPU fault	X
MSS#40	Any EDMA Transfer That Spans ACCEL_MEM1 +ACCEL_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC	X
MSS#41	Issuing WARM_RESET can Cause Bootloader Failure Which Results in Failure to Load the Application From Serial Flash	X
MSS#42A	DSP L2 memory initialisation can reoccur on execution DSP self test (STC) OR DSP Power cycling execution by application	X
MSS#43A	Read-data from internal registers of PCR is not reliable. Shared PCS region protection is also not supported	X
MSS#44A	SYNC IN input pulse wider than 4usec can cause a FRC lockstep error	X
MSS#45	Bootup failure during the serial flash busy state	X
MSS#50	Occasional EDMA self-test failures	X
MSS#51	Spurious toggle on nERROR OUT signal during powerup due to undefined state in ESM block.	X
Analog / Millimeter Wave		
ANA#11B	TX, RX Gain Calibrations Sensitive to Large External Interference	X
ANA#12A	Second Harmonic (HD2) is Present When Receiver is Tested Standalone Using CW Input	X
ANA#13B	Phase Mismatch Variation Across Temperature in TX3/TX1 and TX3/TX2 Combinations are higher than that of TX2/TX1 Combination	X
ANA#14	Doppler Spurs Observed for Narrow Chirps	X
ANA#16	LVDS Coupling to Clock System	X
ANA#17A	On-Board Supply Ringing Induced Spur	X
ANA#18B	Spurs Caused due to Digital Activity Coupling to XTAL	X
ANA#19	Bandgap Decoupling Capacitor On-Board	X
ANA#20	Occasional Failures Observed During Calibration of the Radar Subsystem	X
ANA#22A	Overshoot and Undershoot During Inter-Chirp Idle Time	X
ANA#27A	Digital Temperature Sensor Readings Differ From Analog Temperature Sensors	X
ANA#30	Inter-Channel Mismatch Variation Across Angle of Arrival	X
ANA#31	Increase in Rx effective isotropic noise figure when Tx chains are turned ON	X
PACKAGE		
PACKAGE#02	Surface Wave Artifact from PCB	X

Copyright © 2022 Texas Instruments Incorporated

6 Known Design Exceptions to Functional Specifications

MSS#25	***Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	If a system reset (nRST goes low) occurs while the debugger is performing an access on the system resource using system view, a slave error should be replied to the debugger. If the access was a read, instead the response might indicate that the access completed successfully and return unpredictable data. This issue occurs under this condition: when a system reset is asserted (nRST low) on a specific cycle, while the debugger is completing an access on the system, using the system view. An example would be, when a debugger, like the CCS-IDE memory browser window, is refreshing content using the system view. This is not an issue for a CPU only reset and, this is not an issue during a power-on-reset (nPORRST) either.
Workaround(s):	Avoid performing debug reads and writes while the device might be in reset.

Copyright © 2022 Texas Instruments Incorporated

MSS#26 ***DMA Requests Lost During Suspend Mode***

Revision(s) Affected: AWR6843AOP ES2.0

Description: While the device is halted in suspend mode by the debugger, the DMA is expected to complete the remaining transfers of a block, if the DEBUG MODE bit field of the GCTRL register is configured to '01'. Instead, the DMA does not complete the remaining transfers of a block but, rather stops after two more frames of data are transferred. Subsequent DMA requests from a peripheral to trigger the remaining frames of a block can be lost.

This issue occurs only in the following conditions:

- The device is suspended by a debugger
- A peripheral continues to generate requests while the device is suspended
- The DMA is setup to continue the current block transfer during suspend mode with the DEBUG MODE bit field of the GCTRL register set to '01'
- The request transfer type TTYPE bit in the CHCTRL registers is set to frame trigger ('0')

Workaround(s):

Workaround #1:

Use TTYPE = block transfer ('1'), when the DEBUG MODE bit field is '01' (*finish current block transfer*)

or

Workaround #2:

Use the DMA DEBUG MODE = '00' (ignore suspend), when using TTYPE = frame transfer ('0') to complete the block transfer, even after suspend/halt is asserted.

Copyright © 2022 Texas Instruments Incorporated

MSS#27	***MibSPI in Slave Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	The MibSPI module, when configured in multibuffered slave mode with 3-functional pins (CLK, SIMO, SOMI) or 4-functional pins (CLK, SIMO, SOMI, nENA), could transmit incorrect data when all the following conditions are met: • MibSPI module is configured in multibuffered mode, • Module is configured to be a slave in the SPI communication, • SPI communication is configured to be in 3-pin mode or 4-pin mode with nENA, • Clock phase for SPICLK is 1, and • SPICLK frequency is MSS_VCLK frequency / 12 or slower
Workaround(s):	The issue can be avoided by setting the CSHOLD bit in the control field of the TX RAM (Multi-Buffer RAM Transmit Data Register). The nCS is not used as a functional signal in this communication; hence, setting the CSHOLD bit does not cause any other effect on the SPI communication.

Copyright © 2022 Texas Instruments Incorporated

MSS#28	***A Data Length Error is Generated Repeatedly in Slave Mode When IO Loopback is Enabled***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	When a DLEN error is created in Slave mode of the SPI using nSCS pins in IO Loopback Test mode, the SPI module re-transmits the data with the DLEN error instead of aborting the ongoing transfer and stopping. This is only an issue for an IOLPBK mode Slave in Analog Loopback configuration, when the intentional error generation feature is triggered using CTRLDLENERR (IOLPBKTSTCR.16).
Workaround(s):	After the DLEN_ERR interrupt is detected in IOLPBK mode, disable the transfers by clearing the SPIEN (bit 24) in the SPIGCR1 register and then, re-enable the transfers by resetting the SPIEN bit.

Copyright © 2022 Texas Instruments Incorporated

MSS#29	*Spurious RX DMA REQ From a Slave Mode MibSPI*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	A spurious DMA request could be generated even when the SPI slave is not transferring data in the following condition sequence: • The MIBSPI is configured in standard (non-multibuffered) SPI mode, as a slave • The DMAREQEN bit (SPIINT0.16) is set to enable DMA requests • The Chip Select (nSCS) pin is in an active state, but no transfers are active • The SPI is disabled by clearing the SPIEN (SPIGCR1.24) bit from '1' to '0' The above sequence triggers a false request pulse on the Receive DMA Request as soon as the SPIEN bit is cleared from '1' to '0'.
Workaround(s):	Whenever disabling the SPI, by clearing the SPIEN bit (SPIGCR1.24), first clear the DMAREQEN bit (SPIINT0.16) to '0', and then, clear the SPIEN bit.

Copyright © 2022 Texas Instruments Incorporated

MSS#30	***MibSPI RX RAM RXEMPTY bit Does Not Get Cleared After Reading***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	The RXEMPTY flag may not be auto-cleared after a CPU or DMA read when the following conditions are met: • The TXFULL flag of the latest buffer that the sequencer read out of transmit RAM for the currently active transfer group is 0, • A higher-priority transfer group interrupts the current transfer group and the sequencer starts to read the first buffer of the new transfer group from the transmit RAM, and • Simultaneously, the Host (CPU/DMA) is reading out a receive RAM location that contains valid received data from the previous transfers.
Workaround(s):	If at all possible, avoid transfer groups interrupting one another. If dummy buffers are used in lower-priority transfer groups, select the appropriate "BUFMODE" for them (like, SKIP/DISABLED) unless, there is a specific need to use the "SUSPEND" mode.

Copyright © 2022 Texas Instruments Incorporated

MSS#31	*CPU Abort Generated on a Write to Implemented CRC Space After a Write to Unimplemented CRC Space*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	An abort could be generated on a write to a legal address in the address offset region (0x0000–0x01FF) of the CRC register space when a normal mode write to an unimplemented address region (0x0200–0xFFFF) of the CRC register space is followed by a write to a legal address region (0x0000–0x01FF) of the CRC register space.
Workaround(s):	None.

Copyright © 2022 Texas Instruments Incorporated

MSS#32	***DMMGLBCTRL BUSY Flag Not Set When DMM Starts Receiving A Packet***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	The BUSY flag in the DMMGLBCTRL register should be set when the DMM starts receiving a packet or has data in its internal buffers. However, the BUSY flag (DMMGLBCTRL.24) may not get set when the DMM starts receiving a packet under the following condition: • The BUSY bit is set only after the packet has been received, de-serialized, and written to the internal buffers. It stays active while data is still in the DMM internal buffers. If the internal buffers are empty (meaning that no data needs to be written to the destination memory) then, the BUSY bit will be cleared.
Workaround(s):	Wait for a number of DMMCLK cycles (for example, 95 DMMCLK cycles) beyond the longest reception and deserialization time needed for a given packet size and DMM port configuration, before checking the status of the BUSY flag, and after the DMM ON/OFF bit field (DMMGLBCTRL.[3:0]) has been programmed to OFF.

Copyright © 2022 Texas Instruments Incorporated

MSS#33	*MibSPI RAM ECC is Not Read Correctly in DIAG Mode*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	A Read operation to the ECC address space of the MibSPI RAM in DIAG mode, does not return the correct ECC value for the first 128 buffers, if the Extended Buffer support is implemented but, the Extended Mode is disabled for the particular MibSPI instance.
Workaround(s):	None.

Copyright © 2022 Texas Instruments Incorporated

MSS#34	***HS Device Does Not Reboot Successfully on Warm Reset Getting Triggered by Watchdog Expiry***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	A warm reset triggered by a watchdog expiry (MSS Wdog) , a software register write (SOFTSYSRST), or an external warm reset pin does not ensure a successful reboot of the device in a secure device (HS device).
Workaround(s):	A warm reset should not be triggered externally or internally by a watchdog expiry, a software write, or other trigger mechanisms. To initiate a reset cycle, external circuitry should be used on the sensor design. The external circuitry uses the watchdog, nERROR OUT monitoring, or other kinds of GPIO signaling to trigger a reset using the nRST pin of the device.

Copyright © 2022 Texas Instruments Incorporated

MSS#36	***DMA Read From an Unimplemented Address Space is not Reported as a BUS Error***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	The MSS DMA should generate a Bus Error (BER) interrupt when the DMA detects an error due to a read from an unimplemented address location. This interrupt is not available on any of the VIM Interrupt Channels for DMA1 and DMA2. *Implication: A DMA read from an unimplemented address can go undetected.*
Workaround(s):	The DMA MPU has to be engaged with valid address range to ensure no occurrence of any read from an invalid address location happens. DMA transfers have to be covered with end-to-end CRC from source to destination.

Copyright © 2022 Texas Instruments Incorporated

MSS#37B	***DCC Module Frequency Comparison can Report Erroneous Results***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	The Dual-clock Comparator module, which is used to monitor a clock frequency while comparing with a known clock reference, could stop earlier than expected, and, thus, indicating the measured clock frequency to be lower. This is due to a clock domain crossing issue causing a preset to the error detection logic to get triggered.
Workaround(s):	Multiple measurements can be taken for the same clock pairs and abnormal frequencies reported can be ignored Application code, where possible, could compare the clocks using an alternate clock comparator module (CCC).

Copyright © 2022 Texas Instruments Incorporated

MSS#38A	*GPIO Glitch During Power-Up*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	During the 3.3-V supply ramp, the GPIO outputs could possibly see a short glitch (*rising above the 0 V for a short duration*), if the 3.3V supply powers up before the 1.8V supply. This GPIO glitch cannot be avoided by just a pulldown resistor. If the GPIO glitch during boot-up is high enough, it could be falsely detected as a “high”.
Workaround(s):	Powering up the 1.8V supply before the 3.3V supply resolved the issue. Incase that is not feasible, AND the GPIO is used for critical controls where glitch cannot be tolerated, the GPIO output should be gated by the nRESET signal of the xWR device. Using a tri-state buffer (for example: SN74LVC1G126-Q1) externally to isolate the GPIO output from the system until the nRESET of xWR device is released. At this point, all the supplies are expected to be stable.

Copyright © 2022 Texas Instruments Incorporated

MSS#39	*The state of the MSS DMA is left pending and uncleared on any DMA MPU fault*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	The state of the MSS DMA is left pending and uncleared on any DMA MPU fault. The transfer that caused this MPU fault is left pending inside the DMA IP. Any trigger on DMA REQ lines (could be caused by any module/IP that is hooked up to DMA in h/w) can re-trigger DMA to start executing the above pending transfer irrespective of whether that trigger is actually valid/enabled in DMA or that module/IP
Workaround(s):	For devices where the Boot ROM is executing the MSS DMA MPU Self tests. As part of application initialization, if the MSS DMA will be used, the following register field should be used to reset the MSS DMA IP so that the uncleared transfer is reset 1. Write MSS_RCM:SOFTRST1[31:24] 0xAD 2. Write MSS_RCM:SOFTRST1[31:24] 0x0 It is not recommended to use this configuration at any another instance other than that recommended here in this Errata. On an actual Real time MPU Error, this error should be treated as a non-recoverable error and a warm reset should be issued to recover.

Copyright © 2022 Texas Instruments Incorporated

MSS#40	***Any EDMA Transfer That Spans ACCEL_MEM1 +ACCEL_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	As per TPTC IP Spec, a Transfer request (TR) is supposed to access a single slave end point. ACCEL_MEM0/ACCEL_MEM1 memory banks of HWA are available via single slave point and ACCEL_MEM2/ ACCEL_MEM3 memory banks of HWA are available as another slave point (different from that of ACCEL_MEM0/ ACCEL_MEM1). Hence if a single TR is used to access a buffer spanning ACCEL_MEM1 and ACCEL_MEM2 memories of the HWA (i.e. a single buffer spanning 2 different slave points), the spec is not being adhered to. This errata is explicitly highlighting this spec requirement
Workaround(s):	TBSplit the access into 2 TRs so that a single TR does not span ACCEL_MEM1 +ACCEL_MEM2. The 2 TRs can be chained.

Copyright © 2022 Texas Instruments Incorporated

MSS#41 ***Issuing WARM_RESET can Cause Bootloader Failure Which Results in Failure to Load the Application From Serial Flash***

Revision(s) Affected: AWR6843AOP ES2.0

Description: WARM_RESET issued by application software (via register write), internal watchdog trigger, or external pin invocation can cause bootloader failure. This results in failure to load the application from serial flash

1. Occurrence of WARM_RESET resets all configuration registers to default pre boot ROM values.
2. Change in register values can affect settings of APLL clock, resulting in the PLL clock leaking into digital subsystems of device. This can create an invalid state of a specific clock divider in the PLL clock domain which is subsequently not initialized by the WARM_RESET functionality.
3. Once this clock divider state is reached the subsequent bootloader execution hangs while trying to read the QSPI serial flash for program load (the QSPI is dependent upon the clock divider). This necessitates a power-cycle or nRESET for a successful recovery.

Workaround(s): Avoid WARM_RESET. Use an external nRESET to initiate device reset with either an external watchdog or PMIC initiated reset sequence.

Copyright © 2022 Texas Instruments Incorporated

MSS#42A ***DSP L2 memory initialisation can reoccur on execution DSP self test (STC) OR DSP Power cycling execution by application.***

Revision(s) Affected: AWR6843AOP ES2.0

Description: MSS Boot ROM Powers on DSP, Performs a Memory Initialisation of DSP L2 and downloads the program code to L2 memory. If the user application executes the STC or DSP power cycle, memory init is triggered again, hence erasing the L2 memory contents.

Workaround(s): The workaround for Mem init would be to perform a Dummy mem init to reset a latch within the IP while keeping the destination domain in reset. This can be done by the application using the below sequence before running STC or DSP power cycling:

1. Set the GEM_CLK_EN_BYPASS_CTRL bit in the TOPRCM-> GEMPWRSMCFG2 register Bit 9 as ‘1’.
2. Set the GEM_GRSTN_GATE_BYPASS_CTRL bit in the TOPRCM-> GEMPWRSMCFG1 Bit 9 register as ‘1’.
3. Set the GEM_CLK_EN_BYPASS_CTRL bit in the TOPRCM-> GEMPWRSMCFG1 Bit 7 register as ‘1’.
4. Write a value of 0xFFFF in , DSS_REG ->L2MEMINITCFG1 register.
5. Write a value of 0xF in , DSS_REG ->L2MEMINITCFG2 register
6. Write a value of 0x0 in TOPRCM-> GEMPWRSMCFG1-> PWRSMOUTBYPCTRL register.

Copyright © 2022 Texas Instruments Incorporated

MSS#43A	***Read-data from internal registers of PCR is not reliable. Shared PCS region protection is also not supported***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	The main subsystem has PCR interconnect that manages the accesses to the peripheral registers and peripheral memories, and provides a global reset for all peripherals. The read-data from PCR is getting corrupted before handing it of to VBUSP interconnect. So any partial write to PCR-registers is not reliable. Peripheral access is blocked by writing to internal registers which is not feasible. Shared PCS region protection is also not supported
Workaround(s):	No workaround

Copyright © 2022 Texas Instruments Incorporated

MSS#44A	***SYNC IN input pulse wider than 4usec can cause a FRC lockstep error***
Revision(s) Affected:	AWR6243 ES1.0
Description:	In hardware based frame triggered mode of operation, external SYNC IN pulse is provided to the radar device. If the width of the pulse if > 4usec, it could cause MSS ESM group 1 fault with FRC lockstep error.
Workaround(s):	The pulse width of the external SYNC IN signal should be >25nsec and < 4usec

Copyright © 2022 Texas Instruments Incorporated

MSS#45	***Bootup failure during the serial flash busy state***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	If the radar device is rebooted internally or externally while the serial flash is busy completing a previous operation, like erase, format etc, the radar device might fail to bootup since the serial flash would not respond to the commands from the bootloader during the bootup process.
Workaround(s):	The user application should make sure if its triggering an internal reset due to watch dog expiry or other reasons, it should reset the serial flash to bring it to a known state or wait for completion of any pending issued commands to serial flash before it resets the XWR device.

Copyright © 2022 Texas Instruments Incorporated

MSS#50	*Occasional EDMA self-test failures*
Revisions Affected	AWR6843AOP ES2.0
Details	During the first powerup, there could be occasional failures in the EDMA self-test. It is reported as part of the "AWR_AE_MSS_BOOTERRORSTATUS_SB" flag during bootup. This is due to the undefined states of certain flops during first powerup. This blocks the EDMA channel and eventually fails any subsequent EDMA transfers as well. EDMA is also used to transfer out ADC/CP/CQ data on the CSI or LVDS interface as well, so this data transfer would also fail in that case. **Note** This failure is not seen with subsequent nReset cycles after powerup.
Workaround	The host application needs to monitor the BOOTERRORSTATUS flag. If the EDMA_Self Test flag is set to ‘1’, indicating failure, it should issue an nReset to the mmWave device. This should be done without power cycling the device, i.e. disabling the power supplies to the mmWave device.

Copyright © 2022 Texas Instruments Incorporated

MSS#51	***Spurious toggle on nERROR OUT signal during powerup due to undefined state in ESM block.***
Revisions Affected	AWR6843AOP ES2.0
Details	When the mmWave device powers up (nReset is released), the internal state machine starts on internal RC oscillator clock before the 40MHz clock is available. Inside the ESM module (Error Signaling Module), at least 3 cycles of RCOSC CLK cycles are needed to clear the internal states because the Flip Flops (FFs) are non-resettable. In silicon, the ESM reset might get released before these three RCOSC CLK cycles and at that moment an undefined state of nError out flip flop could get latched. This could be either 0 or 1 since its undefined at that point. Once an error value gets latched, it would be retained until the software clears it. The bootloader then boots up and initializes the ESM block, which then clears the error. Hence, the nError out goes low for about 13msec after the power up, until it is initialized by the bootloader.
Workaround	1. The Host processor can ignore the nERROR OUT status until the device has fully booted up i.e. until the Host IRQ is raised and the mmWave device is ready to receive the command from the host processor over the SPI interface. 2. The Host processor could also put a timer from the nRESET release to ensure the nERROR OUT does not remain low beyond a certain time after nRESET release. For example, a 25 msec timer after the nReset release. By this time, the bootloader should have ideally cleared the ESM block and nERROR OUT should go high. If the nERROR OUT still remains low post the timer, then it could indicate a real fault.

Copyright © 2022 Texas Instruments Incorporated

ANA#11B	***TX, RX Calibrations Sensitive to Large External Interference***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	External interference present on the RX or TX pins, during the period of the device calibration at RfInit, can lead to degraded accuracy or errors in the calibration results. If the interference changes its level while these calibrations are actively running, the calibration algorithm may interpret this as a change in signal power, leading to incorrect convergence. This applies to boot-time PD, Rx IQ mismatch calibration, Rx gain calibration, Tx power calibration, and phase-shifter calibration.
Workaround(s):	Workaround is to save the boot time calibrations at production (done in a clean environment without interference) and during operation, the calibrations can be restored.

Copyright © 2022 Texas Instruments Incorporated

ANA#12A	*Second Harmonic (HD2) Present in the Receiver*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	There is a finite isolation between the RF pins/package and the FMCW synthesizer. This can create spurious tones at the synthesizer output and lead to appearance of 2nd order harmonics and inter-modulations of expected IF frequencies at RX ADC output. The amplitude of the 2nd harmonic could be as high as -55 dBc , referenced to the power level of the intended tone at the LNA input.
Workaround(s):	No workaround available at this time. However, in many typical radar use-cases the HD2 does not affect the system performance due to two reasons: 1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (that is, phase noise and phase spur suppression effect at the mixer). 2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

Copyright © 2022 Texas Instruments Incorporated

ANA#13B	***Phase Mismatch Variation Across Temperature in TX3/TX1 and TX3/TX2 Combinations are higher than that of TX2/TX1 Combination***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	TX3/TX1 and TX3/TX2 combinations exhibit a higher phase mismatch variation across the complete recommended operating temperature range per the data manual as compared to TX2/TX1 combination over the same temperature range.
Workaround(s):	In applications requiring high phase accuracy across TX channels, a background angle calibration can be used to control phase variation over temperature

Copyright © 2022 Texas Instruments Incorporated

ANA#14	***Doppler Spurs Observed for Narrow Chirps***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	There is a non-linearity of the synthesizer when crossing certain frequencies: 60.3-, 60.75-, 61.2-, 61.56-, 62.1-, 62.64-, 63-, and 63.45-GHz. Implication: There will be a spur in the non-zero Doppler bin when the synthesizer crosses any of these frequencies during a chirp. The exact Doppler bin depends on the slope and ramp timings. The spur will be spread across multiple range bins.
Workaround(s):	Avoid narrow bandwidth ramps around frequencies with high-spur levels.

Copyright © 2022 Texas Instruments Incorporated

ANA#16	*LVDS Coupling to Clock System*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	The digital activity in the High-Speed Serial Interfaces (HSI) state machine can couple to the clock system/FMCW synthesizer and can cause spurs in its clock output. The spur frequency is HSI rate dependent (for example, for a 600-MHz HSI clock rate, 6.25-MHz and 12.5-MHz spurs can be observed on TX/RX output, and for a 900-MHz HSI clock rate, 7-MHz and 14-MHz spurs can be observed on the TX/RX output). The spur levels are low (*near or below -65 dBc*).
Workaround(s):	The spur will not be present, when the LVDS is not used.

Copyright © 2022 Texas Instruments Incorporated

ANA#17A	*On-Board Supply Ringing Induced Spur*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	Turning OFF and ON front-end modules can cause on-board supply ringing and slow the settling of the power supply. This supply ringing can manifest as a spur (~130KHz) in the FMCW synthesizer output spectrum.
Workaround(s):	**Workaround #1:** Disable inter-chirp duty cycling of the RX. ***or*** **Workaround #2:** Design the power supply to damp out the ringing on the rails to the device.

Copyright © 2022 Texas Instruments Incorporated

ANA#18B ***Spurs Caused due to Digital Activity Coupling to XTAL***

Revision(s) Affected: AWR6843AOP ES2.0

Description: Digital filtering activity can potentially couple to XTAL pins and lead to spurs in the LO, which would also be seen in the Rx data. The spur in the Rx data would be seen at the spur frequency offset around a strong object. For example if the spur frequency is 500Khz and there is a strong object at 2Mhz , the Rx ADC spectrum could have a spike at 1.5Mhz or 2.5Mhz. Note that the Tx – Rx antenna coupling would also form a strong object close to DC. The spur frequency depends on the sampling rate (Fs). The strongest of these spurs have been observed when Fs is close to 10, 12.5, 18, 18.75,20, 25, Msps. In these ranges, an IF spur can appear at Fs-10 Mhz, 2Fs-40MHz, 4Fs-40 MHz, 4Fs-100 MHz, 8Fs-100 MHz , 2Fs-37.5 MHz, 2Fs-36 MHz. The spur is observable when the spur frequency falls within 1.5 MHz, beyond that it gets heavily filtered out. Please refer the device datasheet for max usable sampling rate.

Workaround(s):

Workaround #1:

Avoid sampling rates close to these numbers (10, 12.5, 18, 18.75, 20, 25 Msps) or use exactly these numbers (spur is at 0 Hz in the latter case).

Workaround #2:

Using external TCXO, instead of XTAL, with voltage swing between 1.4-1.8 Vpp can avoid these spurs.

Copyright © 2022 Texas Instruments Incorporated

ANA#19	***Bandgap Decoupling Capacitor On-Board***
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	A 47-nF capacitor is needed on the bandgap pin. Not having correct capacitor on this pin, can cause boot up issues, especially, at negative temperatures. This requirement is being Included in the errata, as it is a recent change which may not be updated in older reference designs.
Workaround(s):	Use the recommended 47-nF capacitor. For example: part - GRM155R71E473KA88 (see the device-specific EVM and Reference Design files for updated part).

Copyright © 2022 Texas Instruments Incorporated

ANA#20	*Occasional Failures Observed During Calibration of the Radar Subsystem*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	Rare occurrences of failures have been observed in the Dual-Clock Comparator (DCC) module, as a result the APLL or Synthesizer may report a failure.
Workaround(s):	**Workaround #1:** Any APLL calibration failure needs to be responded with a reset cycle. ***or*** **Workaround #2:** Any SYNTH calibration failure reported by the BSS will require an RFinit.

Copyright © 2022 Texas Instruments Incorporated

ANA#22A	*Overshoot and Undershoot During Inter-Chirp Idle Time*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	At the end of the chirp , when the synthesizer starts to go back to the start frequency of the next chirp, there is some overshoot and undershoot. The undershoot/overshoot is proportional to the chirp bandwidth. Negative slope chirps have a worse undershoot than positive slope chirps.
Workaround(s):	To ensure the TX power amplifier is OFF during chirp idle time and not causing "on-air" emissions during the undershoot/overshoot period, keep the inter-chirp power savings ON.

Copyright © 2022 Texas Instruments Incorporated

ANA#27A	*Digital Temperature Sensor Readings Differ From Analog Temperature Sensors*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	The local heating in the digital circuitry can cause the readings from digital temperature sensor to differ from that of the analog temperature sensors (Tx, Rx, and PM). Implication: The temperature monitor API computes the maximum temperature difference across different sensors and compares against the programmed threshold (TEMP_DIFF_THRESH). Higher difference between analog and digital temperature sensors can cause the monitor to fail.
Workaround(s):	In temperature monitor configuration API (AWR_MONITOR_TEMPERATURE_CONF_SB), if the thresholds for the digital temperature sensors (DIG_TEMP_THRESH_MIN and DIG_TEMP_THRESH_MAX) are both set to zero, the BSS will ignore the digital sensor while computing the temperature difference across sensors to compare against the programmed threshold value (TEMP_DIFF_THRESH). The digital temperature values (verbose output) from the API need to be validated externally by the processor.

Copyright © 2022 Texas Instruments Incorporated

ANA#30	*Inter-channel mismatch variation across angle of arrival*
Revision(s) Affected:	AWR6843AOP ES2.0
Description:	The inter-channel gain and phase mismatch may vary significantly across different angles of arrival, leading to reduced accuracy of angle estimation (~8 deg error).
Workaround(s):	The inter-channel gain and phase mismatch is typically calibrated at a system level using an object (such as a corner reflector) at boresight. Due to the high variation across different angles of arrival, the customer may calibrate the inter-channel mismatch at multiple angles within the field of view. This can be compensated using DSP algorithms.

Copyright © 2022 Texas Instruments Incorporated

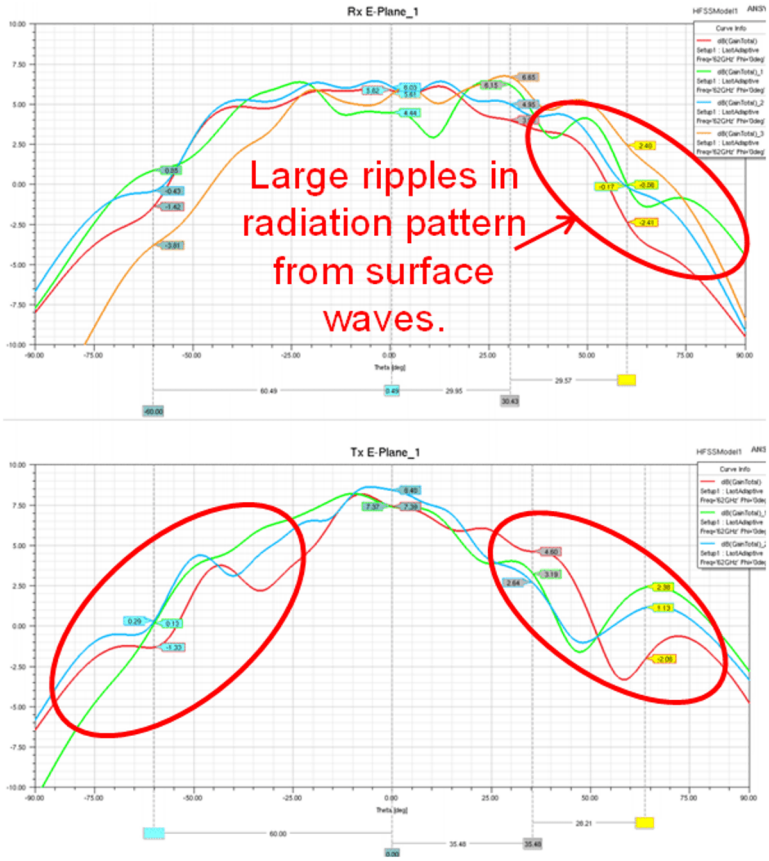
ANA#31	***Increase in Rx effective isotropic noise figure when Tx chains are turned ON***
Revisions Affected	AWR6843AOP ES2.0
Details	When all the Tx chains are turned ON with full power (0dB Backoff), due to antenna coupling there is a degradation in noise figure of about 2.7dB for Rx2 & Rx4.
Workaround	None. However, the noise figure degradation will be correspondingly lower when TX output power is backed off.

Copyright © 2022 Texas Instruments Incorporated

PACKAGE#02 ***Surface Wave Artifact from PCB***

Revisions Affected AWR6843AOP ES2.0

Description: Large PCBs area around the E-plane causes surface waves that create large ripples in the elevation direction of the AoP antenna radiation pattern.



Workaround #1 Keep the Edge of PCB close to the edge of the AoP device in the E-plane to minimize the surface wave ripples.

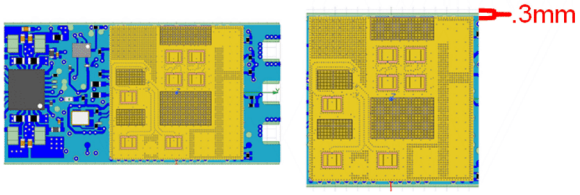


Figure 6-1. Small form factor board with PCB edge less than 0.3mm

Workaround #2 If a larger board is needed for the solution, a trapezoid cutout with the PCB edge less than <0.3mm from the edge of the AoP should be implemented to minimize the ripples caused by surface waves.

Copyright © 2022 Texas Instruments Incorporated

PACKAGE#02 (continued) ***Surface Wave Artifact from PCB***

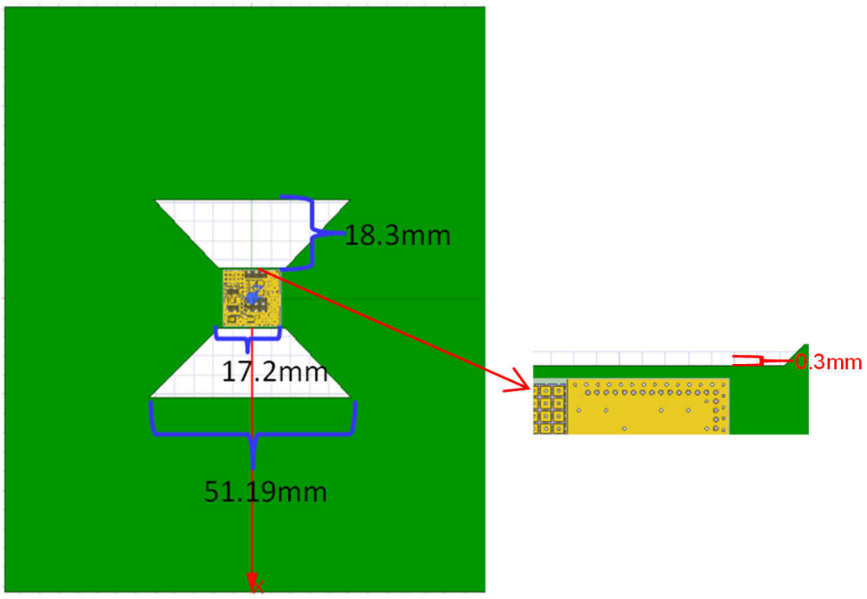


Figure 6-2. Large form factor board with trapezoidal cutout and PCB edge less than 0.3mm

7 Trademarks

All trademarks are the property of their respective owners.

Copyright © 2022 Texas Instruments Incorporated

8 Revision History

Changes from October 31, 2021 to May 31, 2021 (from Revision * (October 2020) to Revision A (May 2022)) **Page**

- Device Markings: Updated/Changed device marking description and figure 3
- Advisory to Silicon Variant / Revision Map: Updated/modified ANA#17A, ANA#18B, ANA#22A, MSS#37B, MSS#38A advisories under Analog / Millimeter Wave and Main Subsystem, all silicon revisions..... 5
- Advisory to Silicon Variant / Revision Map: Added ANA#30, ANA#31, MSS#42 , MSS#43A , MSS#44 , and MSS#45 advisories under Analog / Millimeter Wave and Main Subsystem, all silicon revisions.....5
- Advisory to Silicon Variant / Revision Map: Added PACKAGE#02 advisories under package, all silicon revisions.....5

Copyright © 2022 Texas Instruments Incorporated

Changes from June 1, 2021 to March 31, 2022 (from Revision A (June 2021) to Revision B (March 2022)) **Page**

- (Advisory to Silicon Variant/Revison Map): Added MSS#50 and MSS#51 advisories, all silicon revisions in "Main Subsytem"....5
- (Advisory to Silicon Variant/Revison Map): Updated/Revised ANA#11B, all silicon revisions in "Analog/ Millimeter Wave" category....5
- (Advisory to Silicon Variant/Revison Map): Updated/Revised MSS#42A and MSS#44A, all silicon revisions in "Main Subsytem"....5
- *MSS#42A*: Updated/Revised the Workaround to include item #3 and replace bit '7' by '9' in item #1....22
- *MSS#44A*:Rephrased the workaround 24
- *ANA#11B :* Description and workaround rephrased 28

Copyright © 2022 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated