CC2400 Errata Note 001, rev. 1.0

When using the CC2400 in buffered mode at data rates below 250 kbps, the last bit in a packet will not be sent. A software fix solves the problem.

Description and reason for the problem

When the CC2400 is used in buffered mode with an over-the-air data rate lower than 250 kbps, the PA is shut off before the last bit is sent. This will cause problems when automatic CRC checking is used, as well as if the last byte in a packet contains data.

Suggested workarounds

Alternative 1:

If the protocol used does not use automatic CRC generation/checking, a “dummy” byte should be written as the last byte in a packet. This will ensure that no data is lost.

Alternative 2:

If automatic CRC generation/checking is used, automatic CRC generation should be turned off during transmit and a dummy byte should be written as the last byte in a packet. If the microcontroller software inserts a CITT CRC-16 checksum behind the data in a packet, then automatic CRC checking can be used in receive mode. Otherwise, CRC generation and detection should be done in entirely in software.

Fix

This problem is solved by a software workaround.

Batches affected

This errata note applies to all chip batches and revisions of the chip.

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Document History

Revision	Date	Description/Changes
1.0	2003-10-02	Initial release.

CC2400 Errata Note 002, rev. 1.0

Slow receive start up times for the CC2400 can lead to packet loss. A software workaround fixes the problem.

Description and reason for the problem

Long start-up times (up to a millisecond) of the CC2400 receiver chain have been observed. This happens mainly at low temperatures and low supply voltage, but might also occur at other operating conditions.

No fix is needed if the receiver is put in RX for a minimum of 1ms before any data is to be received. Otherwise, the following workaround should be used:

Suggested workaround

Turn the LNA and MIXERs on at least 10us before the start of RX by using the MANAND register (set the first bit to zero).

Example:

1. Before RX, set bit 0 in the MANAND register to 0. This overrides the power down signal to the LNA and MIXERs, and turns them on.
2. Wait 10us.
3. Turn on RX.
4. Set the bit back to 1. The LNA and MIXERs will now be turned off after RX, as normal.

For applications that are not power critical, the LNA and MIXERs can be kept on during TX and standby to simplify the design. This does not affect TX in any way other than the related increase in current consumption.

Fix

This problem is solved by a software workaround.

Batches affected

This errata note applies to all chip batches and revisions of the chip.

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Document History

Revision	Date	Description/Changes
1.0	2003-12-11	Initial Release.

CC2400 Errata Note 003, rev. 1.0

Bit number 5, *CS_ABOVE_THRESHOLD_N*, in the status byte returned during address transfer will always return a static "1".

Description and reason for the problem

The *CS_ABOVE_THRESHOLD_N* bit will return a value equal to "1" under all operating conditions although the actual RSSI level is above the user defined RSSI threshold. This implies that *CS_ABOVE_THRESHOLD_N* cannot be used as a carrier sense flag indicating whether the RSSI is above the threshold set by *RSSI_CS_THRES[7:2]* within the RSSI Status and Control Register.

One of the following workarounds can be used:

Suggested workaround

Alternative 1:

The RSSI features a programmable carrier sense indicator that can be made available as an output on either the GIO1 or the GIO6 pin by using the IOCFG-register. One of these pins can be used to indicate when the RSSI value exceeds the user-programmed threshold. This method is the fastest way of evaluating the RSSI as it appears almost instantaneously.

Alternative 2:

The RSSI level is available in digital format and can be read via the 4-wire SPI interface. Within a microcontroller this value can be stored and then compared with the threshold value. Storing the threshold value within the microcontroller will save one read operation, thus providing a faster carrier sense flag indication than the alternative approach implying that also the threshold value is read from the CC2400.

Fix

Using one of the above-suggested workarounds solves this problem.

Batches affected

This errata note applies to all chip batches and revisions of the chip.

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Document History

Revision	Date	Description/Changes
1.0	2004-06-10	Initial Release

CC2400 Errata Note 004, rev. 2.0

March 18, 2005

For CC2400 devices marked with lot codes ranging from WA4196.00 to WB7519 correct operation of the SPI interface is not guaranteed at I/O-voltages below 2.1 V. This problem is now fixed and operation down to 1.6 V is ensured for devices with lot codes succeeding WB7519.00.

Description and reason for the problem

When using I/O-voltages below 2.1 V a limitation in the digital pads has been observed to cause reduced SPI speed and in some cases loss of functionality. This will only occur for I/O pins configured as inputs and at I/O-voltages below 2.1 V.

Suggested workaround

Using I/O-voltages at or above 2.1 V will ensure reliable operation and unaffected SPI speed.

Fix

Using voltages above 2.1 V solves the problem for those CC2400 devices affected.

Batches affected

This errata note applies to all CC2400 devices marked with lot codes ranging from WA4196.00 through WB7519.00. For devices with lot codes succeeding WB7519.00 this problem is resolved.

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Document History

Revision	Date	Description/Changes
2.0	2005-03-18	Problem fixed on lot codes higher than WB7519.00
1.0	2004-10-18	Initial release