User's Guide
SWRU458–February 2017

CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines

The CC3120 and CC3220 devices are part of the SimpleLink™ microcontroller (MCU) platform, which consists of Wi-Fi®, *Bluetooth*® low energy, Sub-1 GHz and host MCUs, which all share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink platform enables you to add any combination of the portfolio's devices into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit www.ti.com/simplelink.

Contents

1 Introduction

This document provides the design guidelines of the 4-layer PCB used for the CC3120 and CC3220 SimpleLink Wi-Fi family of devices from Texas Instruments™. The CC3120 and CC3220 devices are easy to lay out and are available in quad flat no-leads (QFNS) packages. When designing the board, follow the suggestions in this document to optimize performance of the board.

This guide includes the following:

- A brief overview of the SimpleLink Wi-Fi family of devices
- Overview of the PCB specification, components placement, and board layer information
- Layout guidelines that describe the main sections of the board such as radio frequency (RF), power, clock, digital input and output, and the ground

Each section can be independently read. This document focuses on the CC3220-LAUNCXL board as the layout for the CC3220, which is a super set among the CC3120 and the CC3220. Any exceptions to this layout are explained separately. The CC3220-LAUNCXL is also referred to as LaunchPad™ (LP).

In addition to this document, TI recommends verifying the schematic board design with the *CC3120, CC3220 SimpleLink™ Wi-Fi® and Internet of Things Design Checklist*.

Start the design with the industry's first Internet-on-a chip™. Created for the Internet of Things (IoT), the SimpleLink Wi-Fi family has several variants. The CC3120 SimpleLink Wi-Fi and IoT solution dramatically simplify the implementation of Internet connectivity. This product integrates all protocols for Wi-Fi and internet, which greatly minimizes host microcontroller (MCU) software requirements. The CC3220 device is a wireless MCU that integrates a high-performance ARM® Cortex®-M4 MCU with the CC3120 network processor subsystem, allowing customers to develop an entire application with a single integrated chip (IC). With on-chip Wi-Fi, internet, and robust security protocols, no prior Wi-Fi experience is needed for faster development. SimpleLink Wi-Fi is a complete platform solution that includes:

- Various tools and software
- Sample applications
- User's guides and programming guides
- Reference designs
- TI E2E™ support community

The devices are available in a QFN package that is easy to lay out.

2 PCB Specification

2.1 PCB Stack-Up

Figure 1 shows an example stack-up used to construct the CC3220-LAUNCHXL RevB. The user can alter the layer stack-up based on their requirements, but the impedance of the 50-Ω lines must be recalculated. Reducing the Layer 1 (L1) to Layer 2 (L2) distance helps improve the power grounding and the RF decoupling, because it lowers the overall through inductance. TI recommends keeping the L1 to L2 distance similar, or lower than the recommended value.

TYPE	LAYER	Height (um)
Mask		25
Copper	L1	35
FR-4		255
Copper	L2	35
FR-4		700
Copper	L3	35
FR-4		255
Copper	L4	35
Mask		25
	Total	1400

Total Thickness ~ 1.4 mm (+/- 10%)

Figure 1. Example Stack-Up

2.2 PCB Design Rules

Table 1 lists the PCB design rules.

Table 1. PCB Design Rules

Parameter	Value	Comments
Number of layers	4	—
Thickness	1.4 mm ± 10%	For greater thickness, increase the distance between L2 and L3.
Size of PCB	2.3” × 4.1”	Can be altered to suit the customer requirement. A smaller PCB size results in poor antenna performance. A size of 2.3” × 1.7” is verified for the CC3120 device.
Dielectric	FR4	—
Surface finish	ENIG	Not critical
Minimum track width	6 mils	Minimum track width can be reduced, but the cost would increase.
Minimum spacing	6 mils	Minimum spacing can be reduced, but the cost would increase.
Mid drill diameter	8 mils	8-mil diameter drill is used on the CC3220-LAUNCHXL Rev B board. 12-mil diameter drill is used on the CC3120 device because it has less pins to route.
Copper thickness	1 oz	—
Lead free / ROHS	Yes	—
Impedance control	Yes	50-Ω controlled impedance trace of 18 mils wide on the L1 with respect to L2 ground (GND). Air gap = 15 mils.(1)
Impedance variation	< 5%	—

(1) These calculations are based on a coplanar waveguide with ground (CPW-G) not microstrip. The estimation could be performed using tools like AWR TX Line, Saturn PCB Toolkit, and Agilent ADS, among others.

2.3 Layer Information

Table 2 describes the 4-layer PCB configuration.

Table 2. 4-Layer PCB

Layer	Usage	Notes
1	Signal plus RF	RF trace is a coplanar waveguide (CPW) with ground, routed on the L1 with respect to L2 ground.
2	GND	Reference plane for the RF and power ground. The power plane has special routing to improve the spectral mask performance.
3	Power plus signal	The power planes for the power amplifier, analog blocks, and the main input supply are routed on this layer.
4	Power plus signal	All remaining signals are routed on this layer.

3 Layout Information

The complete layout package in Altium format is available for download from *CC3220 SimpleLink™ Wi-Fi® and Internet of Things Hardware Design Files*.

CAUTION

TI recommends copying the exact layout of the engine area, which is marked by a box on the silkscreen, to ensure optimum performance as measured on the CC3x20 reference boards. Failure to adhere to this recommendation can lead to performance degradation, including spectral mask degradation, error vector magnitude (EVM) failures, and power supply instability.

3.1 Components Placement

Figure 2 shows the placement of the CC3220 LaunchPad components. This placement provides optimum performance of the device. Users must take great care of the power inductors components to ensure reduced emissions and optimum EVM and mask performance. Place the power inductors very close to the device, and minimize the length of the power traces. The CC3x20 device is sensitive to the layout of the DC-DC converters components, and placement can impact the performance of the device.

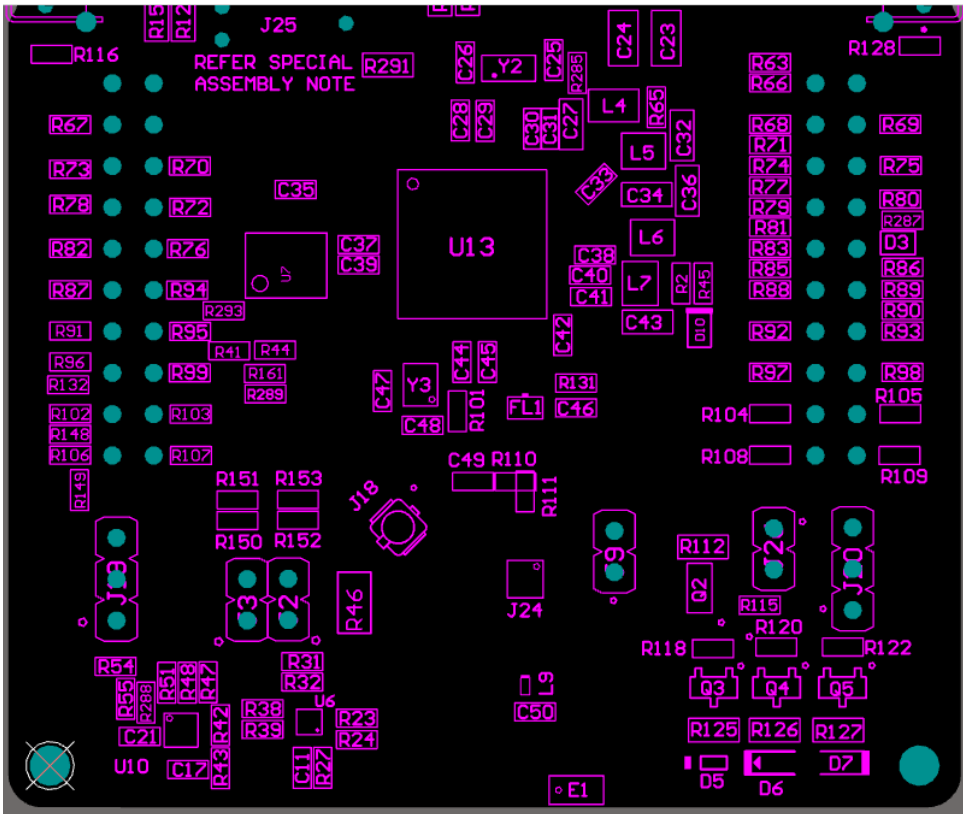

Figure 2. CC3220XX-LAUNCXHL RevB Placement Diagram

3.2 Layer Information

3.2.1 Layer 1

Figure 3 shows layer 1 (L1) where most of the routing is performed, to avoid vias on the board. The trace widths are maximized for high current pins and minimized for signal pins. For example, the signal pins can be routed with 6 mils (4 mils if possible), and the power pins with 12 mils and greater.

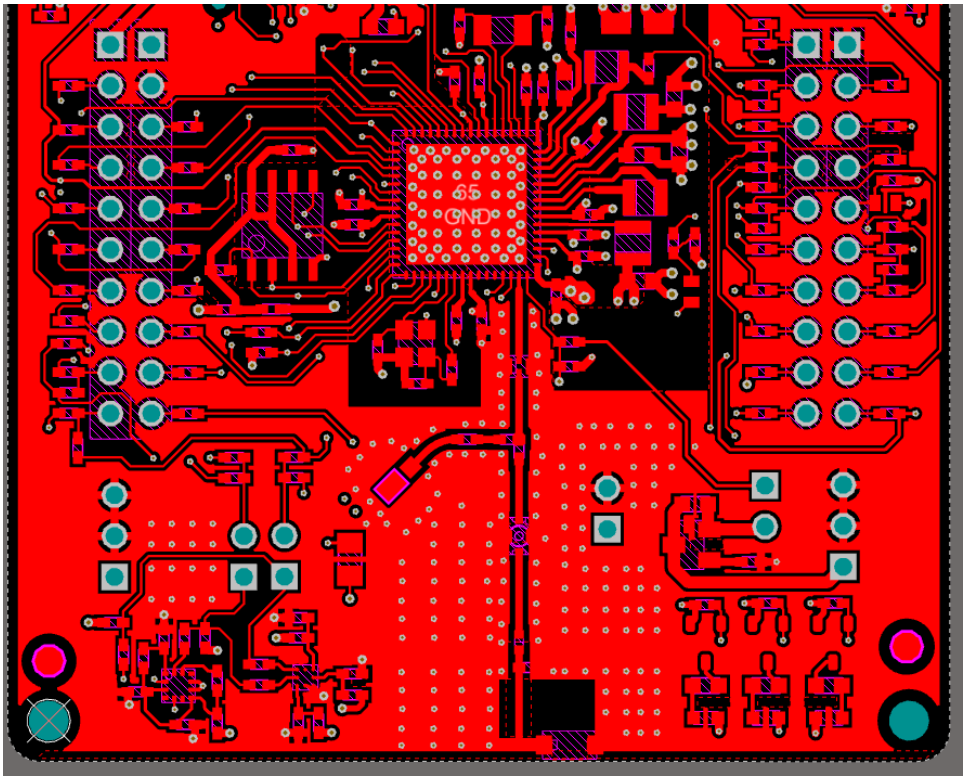

Figure 3. Layer 1

3.2.2 Layer 2

Figure 4 shows layer 2 (L2), the primary ground plane for the board reference. L2 has a void for the antenna section which is reflected on all the layers, per the antenna guidelines. Three traces are routed on the GND layer. These traces are return current path for the input decoupling capacitors (C11, C13, and C18) routed on L2 using thick traces, to isolate the RF ground from the noisy supply ground. This routing is an example of single-point grounding where the return currents are not made to flow on the ground plane. This grounding avoids the common impedance coupling between the DC-DC and RF sections, which is required to improve the IEEE spectral mask margins.

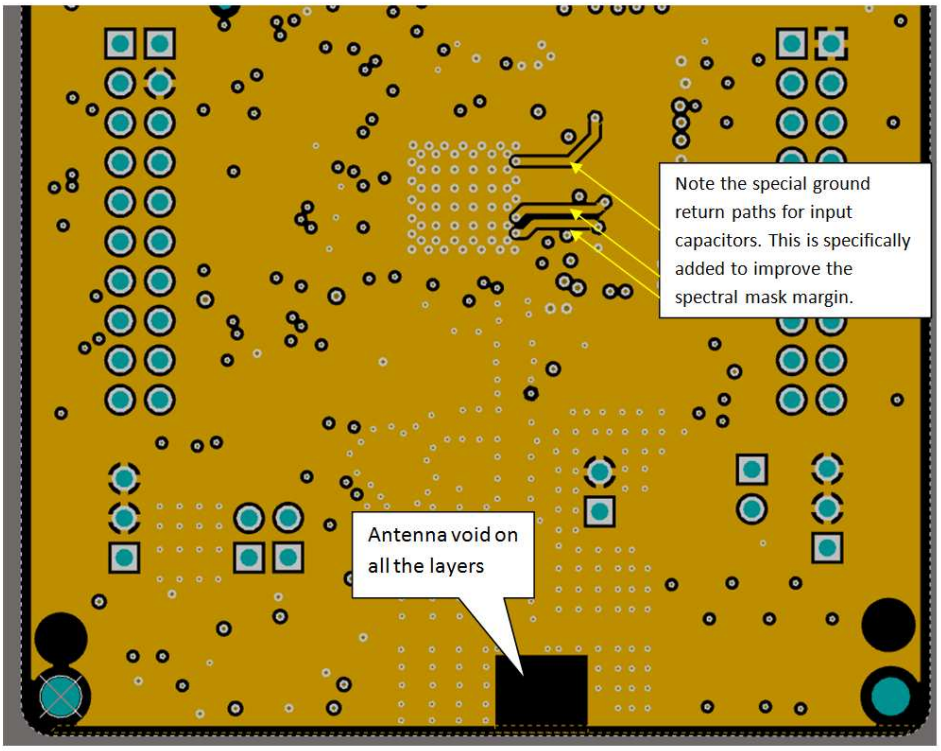

Figure 4. Layer 2

3.2.3 Layer 3

Figure 5 shows layer 3 (L3) which routes the power lines to the device. Power planes are necessary for the power amplifier (PA), and the main supply input to the device. More details are available in subsequent sections.

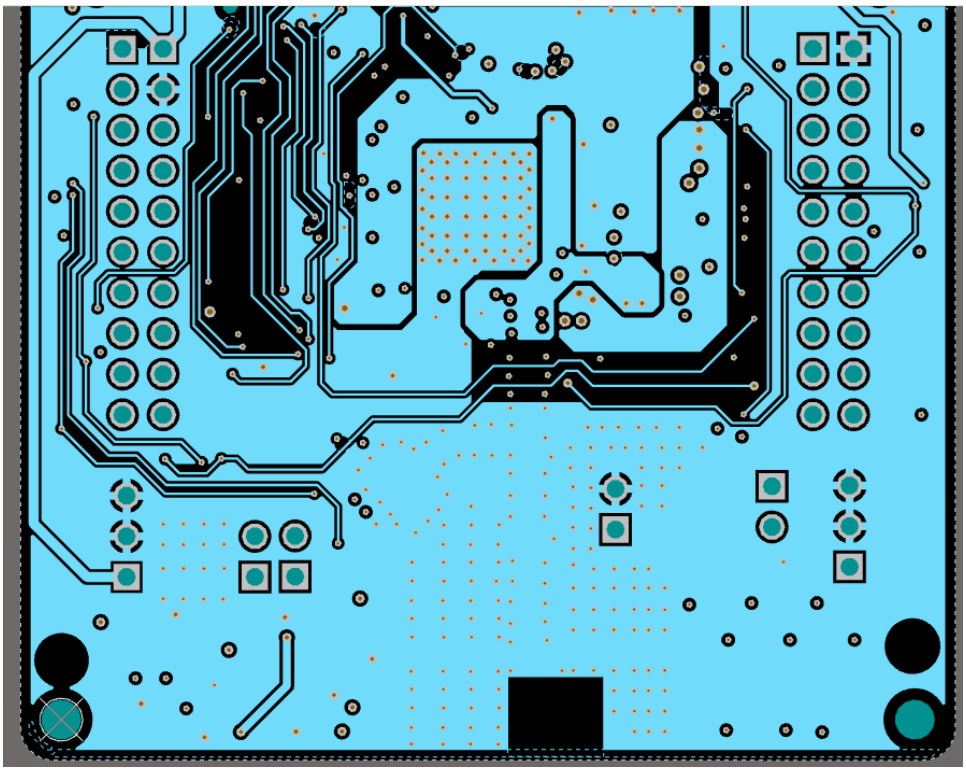

Figure 5. Layer 3

3.2.4 Layer 4

Figure 6 shows layer 4 (L4) which routes the power and signal lines on the board. L4 is also the main power dissipation GND layer for the QFN package. Users must maximize the bottom GND plane for the best thermal performance. The solder mask is kept open below the QFN device to improve the heat dissipation and yield.

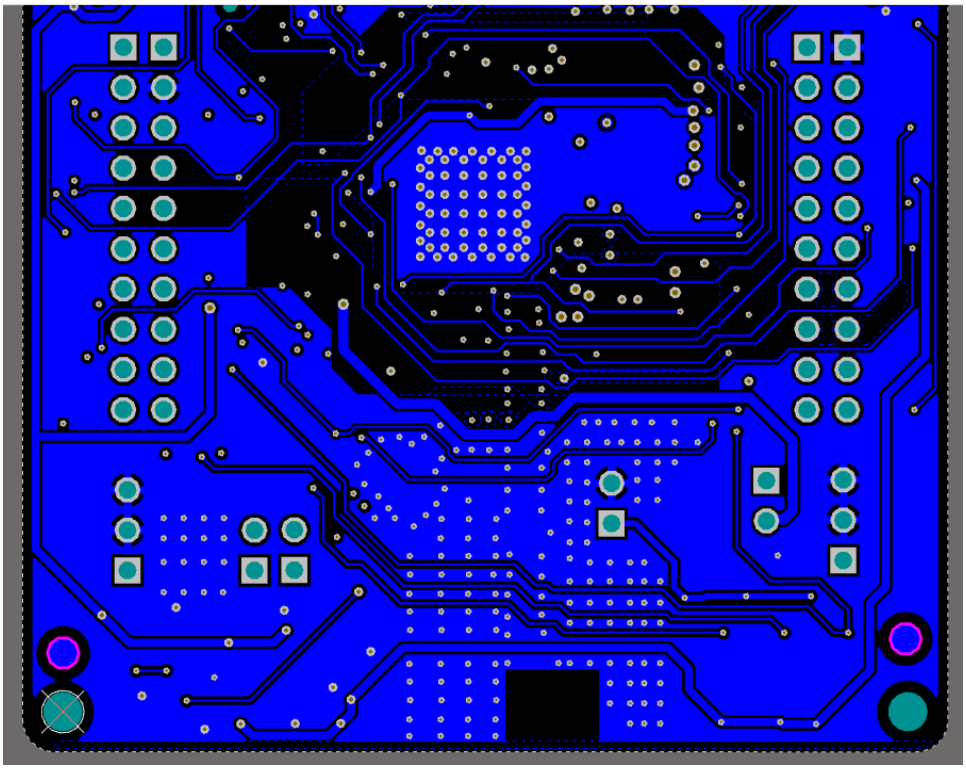

Figure 6. Layer 4

4 Layout Guidelines

4.1 RF Section

Figure 7 shows the RF section, which as a wireless device gets the top priority in terms of layout. The RF section must be laid out correctly to get the optimum performance from the device. A poor layout can cause performance degradation for the output power, EVM, sensitivity, and spectral mask.

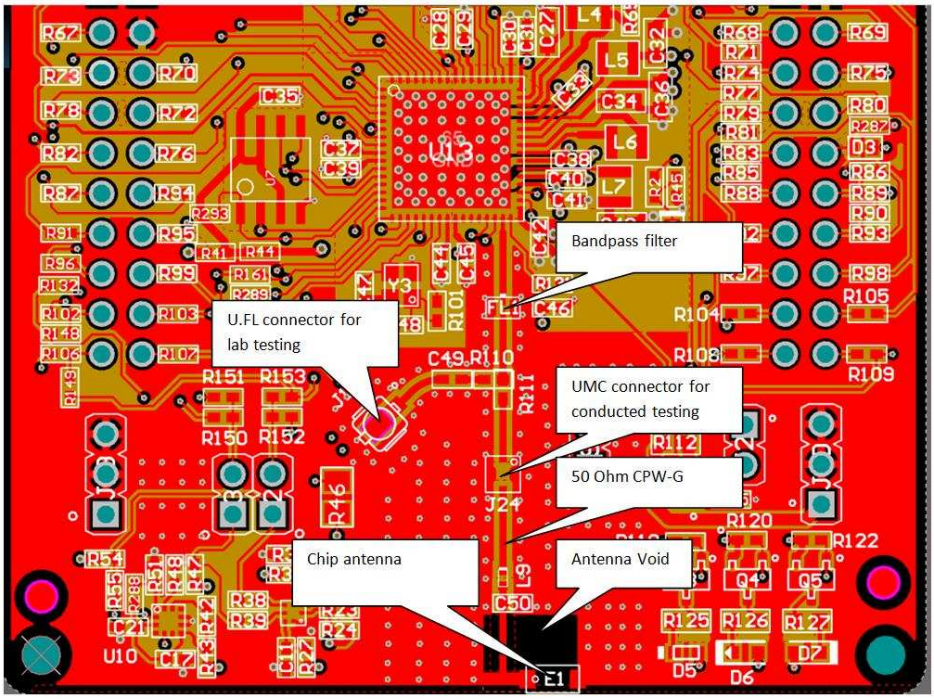

Figure 7. RF Section Layout

4.1.1 Antenna Placement and Routing

The antenna is the element which converts the guided waves on the PCB traces to the free-space electromagnetic radiation. The placement and layout of the antenna is key to increased range and data rates.

Table 3 explains the guidelines that must be observed for the antenna.

Table 3. Antenna Guidelines

Sr No.	Guidelines
1	Place the antenna on an edge or corner of the PCB, depending on the manufacturer's recommendation.
2	Ensure no signals are routed across the antenna element, or void space, on all layers of the PCB.
3	Most antennas, including the chip antenna used on the TI reference designs, require ground clearance on all the layers of the PCB. Ensure that the ground is cleared on inner layers as well.
4	Ensure there is provision to place matching components for the antenna. The antenna must be tuned for best return loss when the complete board is assembled. Any plastic or casing must also be mounted while tuning the antenna, because this can impact the impedance.
5	Ensure the antenna impedance is 50 Ω, because the device is rated to work only with a 50-Ω system. A voltage standing-wave ratio (VSWR) of 2:1 is acceptable.
6	For a printed antenna, ensure that the simulation is performed with the solder mask considered.
7	Ensure the chosen antenna has a near omnidirectional pattern. Peaks and nulls could cause reception problems if the access point is aligned with the null of the CC3220 board antenna.

Table 4 describes the recommended components.

Table 4. Recommended Components

Choice	Part Number	Manufacturer	Notes
1	AH316M245001-T	Taiyo Yuden	Can be placed on the edge of the PCB, and uses less PCB space
2	RFANT5220110A2T	Walsim	Must be placed on the corner of the PCB

Table 5 describes the characteristics of the recommended antenna.

Table 5. Characteristics of Recommended Antenna

Parameter	Specification
Frequency bandwidth	2.4 GHz to 2.5 GHz
Typical peak gain	+1.9 dBi
Average gain at OMNI plane	0 dBi
Efficiency (typical)	–1.3 dB (73%)
VSWR	2:1

4.1.2 Filter Placement and Routing

The RF filter on the board performs the important function of attenuating the out-of-band emissions from the device. Table 6 lists the recommended part numbers.

Table 6. Recommended Part Numbers

Choice	Part Number	Manufacturer	Notes
1	DEA202450BT-1294C1-H	TDK/Epcos	Lowest insertion loss (used on TI EVM)
2	RFBPF2012080AC2T00	Walsin/Passive components	Evaluated by TI to meet emission norms

Figure 8 shows the RF filter routing.

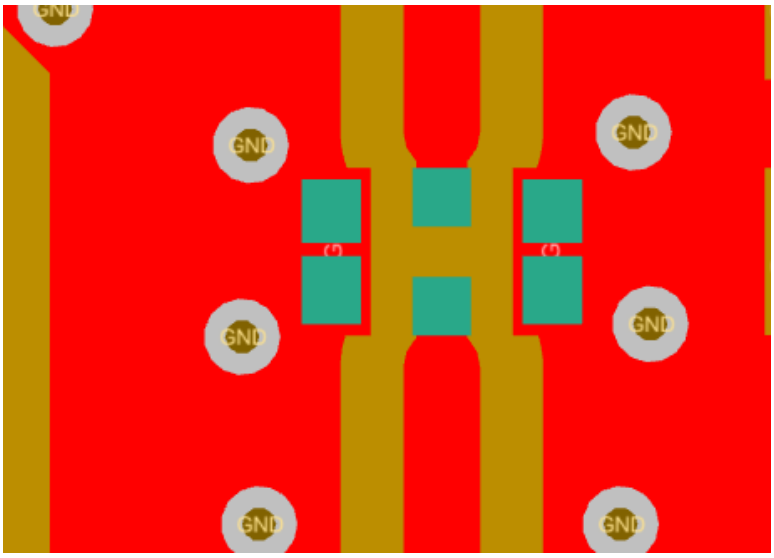

Figure 8. Filter Routing

The RF filter must be placed close to the device pin, between the antenna and the device. The RF filter should have a good ground connection to the L2 ground plane. TI recommends adding at least two ground vias near the ground pins to ensure good RF grounding.

The ground pin of the filter is split into halves for the solder paste. This method improves the overall solder reliability during reflow. Testers observed that a single paste for the ground pin causes the component to lift during assembly.

Table 7 explains the filter routing guidelines.

Table 7. Filter Guidelines

Sr No	Guidelines	Notes
1	Route the RF lines at the input and output of the filter using a CPW with ground structure. This structure offers the best isolation between the input and output due to reduced field fringing.	—
2	Use via stitching along the RF trace to reduce emissions, and keep the fields confined to the trace boundary.	CPW with GND and via stitching can be accurately simulated using 3D EM tools like EESOF.
3	Use a Zo of 50 Ω with only a tolerance of 10%. Use the stack-up and trace width provided for reference in Table 1.	—
4	Add multiple ground vias for the filter ground pads, as close as possible. A minimum of two vias ⊢ per GND pad is recommended.	—
5	To achieve the specifications of the filter attenuation, the minimum isolation between the input and output ports of the filter must be at least 60 dB (measured without the filter).	—
6	If a conducted test is required on the PCB, TI recommends adding a U.FL connector, or a Murata switch type connector (MM8030 series).	—
7	The solder paste on the ground pin is split into halves to ensure a reliable solder joint. Having a single ground on the paste causes the component to lift up during reflow.	—

Table 8 describes the characteristics of the recommended filter.

Table 8. Characteristics of Recommended Filter

Parameter	Frequency (MHz)	Specification
Return loss	2412 to 2484	10 dB (minimum)
Insertion loss	2412 to 2484	1.5 dB (maximum)
Attenuation	800 to 830	30 dB (minimum)
	1600 to 1670	20 dB (minimum)
	3200 to 3300	30 dB (minimum)
	4000 to 4150	45 dB (minimum)
	4800 to 5000	20 dB (minimum)
	5600 to 5800	20 dB (minimum)
	6400 to 6600	20 dB (minimum)
	7200 to 7500	35 dB (minimum)
	7500 to 10000	20 dB (minimum)
Reference impedance	2412 to 2484	50 Ω
Filter type	—	Band pass

4.1.3 Transmission Line

The RF signal from the device is routed to the antenna using a CPW-G structure. This structure offers the maximum isolation across the filter gap, and the best possible shielding to the RF lines. In addition to the ground on L1, placing GND vias along the line also provides additional shielding.

Figure 9 shows the CPW-G with via stitching.

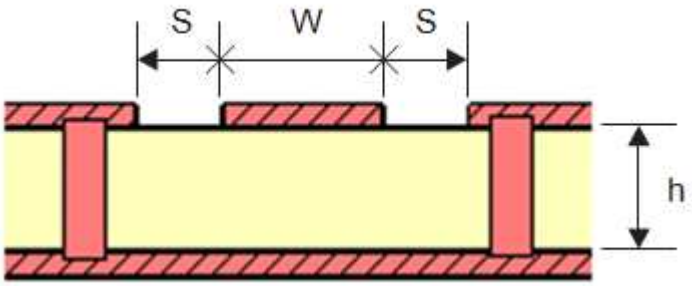

Figure 9. Coplanar Waveguide (Cross Section) With GND and Via Stitching

Figure 10 shows the top view of the CPW-G.

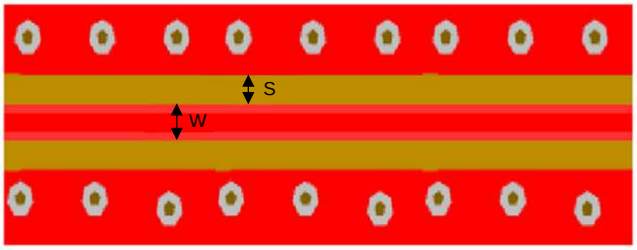

Figure 10. Coplanar Waveguide With GND (Top View)

Table 9 provides the recommended values for the PCB.

Table 9. Recommended Values for the PCB

Parameter	Value	Units and Comments
W	18	mils
S	15	mils
H	10	mils
Ɛr (1)	3.9	Dielectric constant

(1) Ɛr is assumed to be of an FR-4 substrate.

4.2 DC to DC Loop Considerations

Three critical DC to DC converters must be considered for the CC31xx and CC32xx devices:

- Analog DC to DC converter
- PA DC to DC converter
- Digital DC to DC converter

Each converter requires an external inductor and capacitor that must be laid out with care. When laying out the power components, DC current loops are formed.

Figure 11 shows the two loops that are formed.

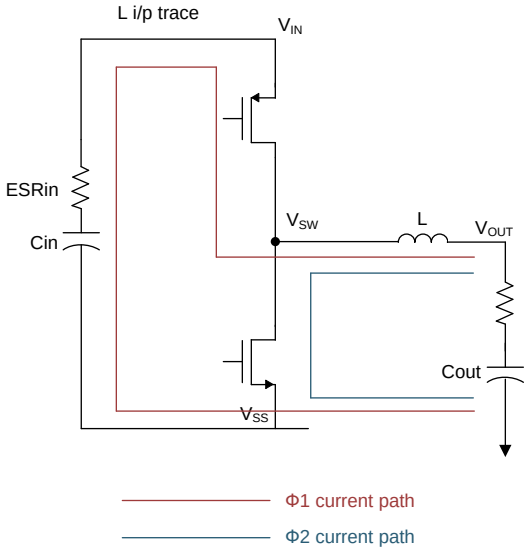

Figure 11. DC Loop Currents

The most important loop is shown in red. This loop travels from V_{SS}, through Cin and finally thru the inductor L that is on the switching node (V_{SW}) before returning to V_{SS}. On this loop there is a lot of high-frequency switching current, and therefore it must be localized to the shortest possible loop, which in turn also minimizes the loop area. Reducing the loop area is important because the higher the loop area, the higher the radiated magnetic field, causing a major source of noise propagation on the board. In addition the input capacitor must be as close as possible to both V_{IN} and the V_{SW} pin. Also, the ground node of the input capacitor must have its return path, the thermal pad of the device with its inductance of the trace minimized. Figure 12 shows the critical trace inductances that must be minimized.

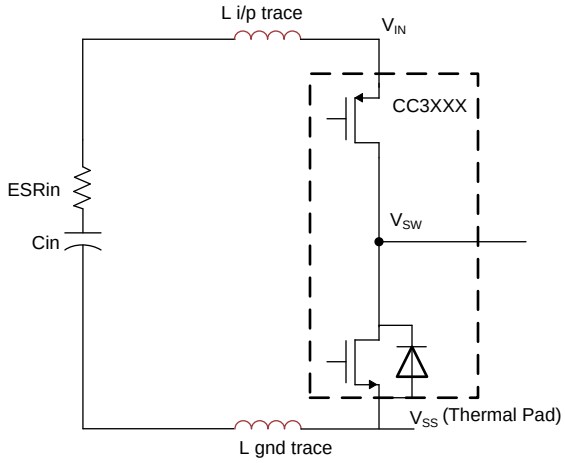

Figure 12. Critical Trace Inductances

Table 10 describes the maximum allowable trace inductance for the three DC to DC converters.

Table 10. Critical Board Trace Inductances

Device Pin Number	Pin Name	Maximum Trace Inductance Pin To Cin (L i/p trace)	Maximum Trace Inductance Cin Ground to V_{ss} (L GND trace)
37	VIN_DCDC_ANA	2 nH	0.5 nH
39	VIN_DCDC_PA	2 nH	0.5 nH
44	VIN_DCDC_DIG	3 nH	0.8 nH

4.2.1 Inductors and Capacitors for DC-to-DC Converters

The components used in the power-management section of the design are critical to achieving the required performance. Table 11 shows the recommendations that should be chosen.

Table 11. Recommended Inductor and Capacitors

Reference Designator	Critical BOM	Value	Size	Current or Voltage Rating	Recommended PN	Description
L7	ANA DCDC OUT	2.2 µH	1008	1.3 A	LQM2HPN2R2MG0L	Inductor 2.2 µH 20% 1008
L6	PA DCDC OUT	1 µH	1008	1.6 A	LQM2HPN1R0MG0L	Inductor 1 µH 20% 1008
L5	DIG DCDC OUT	2.2 µH	1008	1.3 A	LQM2HPN2R2MG0L	Inductor 2.2 µH 20% 1008
L4	FLASH DCDC OUT	10 µH	1007	0.68 A	CBC2518T100M	Fixed Ind 10 UH 680 mA 468 MOHM, ±20%
			0805	0.35 A	MLZ2012M100W	FIxed Ind 10 UH 350 mA 470 MOHM ±20%
C40, C38, C33	Input supply decap	4.7 µF	0402	6.3 V	C1005X5R0J475M050BC	CAP CER 4.7 µF 6.3 V X5R 0402, ±20%
C43	ANA DCDC OUT	10 µF	0603	6.3 V	GRM188R60J106ME47	CAP CER 10 µF 6.3 V X5R 0603, ±20%
C32	DIG DCDC OUT	10 µF	0603	6.3 V	GRM188R60J106ME47	CAP CER 10 µF 6.3 V X5R 0603, ±20%
C27	FLASH DCDC OUT	10 µF	0603	6.3 V	GRM188R60J106ME47	CAP CER 10 µF 6.3 V X5R 0603, ±20%
C34, C36	PA DCDC OUT	22 µF	0603	4 V	C1608X5R0G226M080AA	CAP CER 22UF 4 V X5R 0603

4.2.2 Design Considerations

The following design guidelines must be followed when laying out the CC31xx or CC32xx device:

- Route all of the input decoupling capacitors (C11, C13, and C18) on L2 using thick traces, to isolate the RF ground from the noisy supply ground. This step is also required to meet the IEEE spectral mask specifications.
- Maintain the thickness of power traces to be greater than 12 mils. Take special consideration for power amplifier supply lines (pin 33, 40, 41, and 42), and all input supply pins (pin 37, 39, and 44).
- Ensure the shortest grounding loop for the PLL supply decoupling capacitor (pin 24).
- Place all decoupling capacitors as close to the respective pins as possible.
- Power budget: The CC3x20 device can consume up to 450 mA for 3.3 V, 670 mA for 2.1 V, and 700 mA for 1.85 V, for 24 ms during the calibration cycle.
- Ensure the power supply is designed to source this current without any issues. The complete calibration (TX and RX) can take up to 17 mJ of energy from the battery over a time of 24 ms.

- The CC3X20 device contains many high-current input pins. Ensure the trace feeding these pins is capable of handling the following currents:
  - PA DCDC input (pin 39) maximum 1 A
  - ANA DCDC input (pin 37) maximum 600 mA
  - DIG DCDC input (pin 44) maximum 500 mA
  - PA DCDC switching nodes (pin 40 and pin 41) maximum 1 A
  - PA DCDC output node (pin 42) maximum 1 A
  - ANA DCDC switching node (pin 38) maximum 600 mA
  - DIG DCDC switching node (pin 43) maximum 500 mA
  - PA supply (pin 33) maximum 500 mA

Figure 13 shows the ground routing for the input decoupling capacitors.

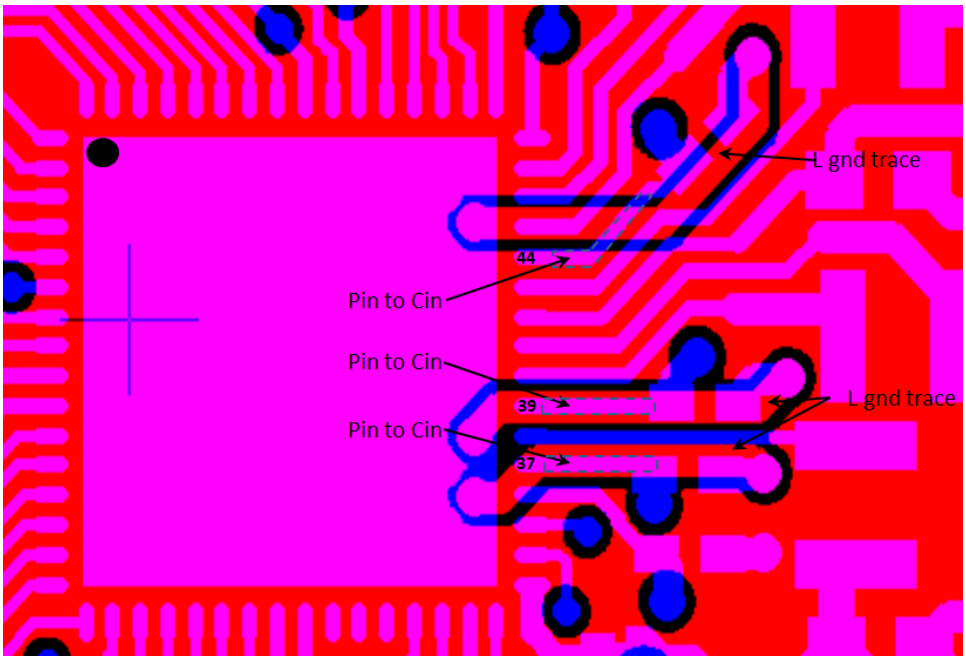

Figure 13. Ground Routing for the Input Decoupling Capacitors

The ground return for the input capacitors are routed on L2 to reduce the EMI and improve the spectral mask. This routing must be strictly followed because it is critical for the overall performance of the device.

4.3 Clock Section

4.3.1 32-kHz RTC Crystal

The 32.768-kHz crystal should be placed close to the QFN package. Ensure the load capacitance is tuned based on the board parasitic, so that the frequency tolerance is within ±150 ppm.

Table 12 describes the characteristics of the recommended 32K XTAL.

Table 12. Characteristics of Recommended 32K XTAL

Parameter	Specification
Nominal frequency	32.768 kHz
Tolerance with temperature and aging	±150 ppm
ESR	70 kΩ (maximum)

4.3.2 40-MHz Crystal

The 40-MHz crystal should be placed closer to the QFN package. Ensure the load capacitance is tuned based on the board parasitic, so that the frequency tolerance is within ±10 ppm at room temperature. The total frequency accuracy for the crystal across parts, temperature, and with aging, should be ±25 ppm to meet the WLAN specifications. In addition, ensure no high-frequency lines are routed closer to the XTAL routing, to avoid any phase noise degradation. Refer to CC31xx and CC32xx Frequency Tuning for frequency tuning information.

Table 13 describes the characteristics of the recommended 40 MHz crystal.

Table 13. Characteristics of Recommended 40-MHz Crystal

Parameter	Specification
Nominal frequency	40 MHz
Tolerance	±10 ppm
Load capacitance	8 pF
Temperature stability	±10 ppm
Aging	1 ppm/year (assuming 5-year life)
ERS	60 Ω (maximum)

4.4 Digital Input and Output (I/O) Section

Route the serial peripheral interface (SPI) and universal asynchronous receiver and transmitter (UART) lines away from any RF traces, because these digital I/O lines are high-frequency lines, and can cause interference to the RF signal.

Keep the length of the high-speed lines as short as possible to avoid transmission line effects. Keep the line lower than 1/10 of the rise time of the signal, to ignore transmission line effects. This recommendation is required only if the traces cannot be kept short. Place the resistor at the source end, closer to the device driving the signal.

Add series-terminating resistors for each high-speed line (for example, SPI_CLK, SPI_DATA) to match the driver impedance to the line. Typical terminating resistor values range from 27 Ω to 36 Ω for a 50-Ω line impedance.

Route high-speed lines with a ground reference plane continuously below it to offer good impedance throughout, and help shield the trace against EMI.

Avoid stubs on high-speed lines to minimize the reflections. If the line must be routed to multiple locations, use a separate line driver for each line.

If the lines are longer compared to the rise time, add series terminating resistors near the driver for each high-speed line (for example, SPI_CLK, SPI_DATA) to match the driver impedance to the line. Typical terminating resistor values range from 27 Ω to 36 Ω for a 50-Ω line impedance.

4.5 QFN Ground

Figure 14 shows ground vias placed on the ground pad to ensure optimal thermal dissipation. The via drill size can be from 8 mils to 12 mils.

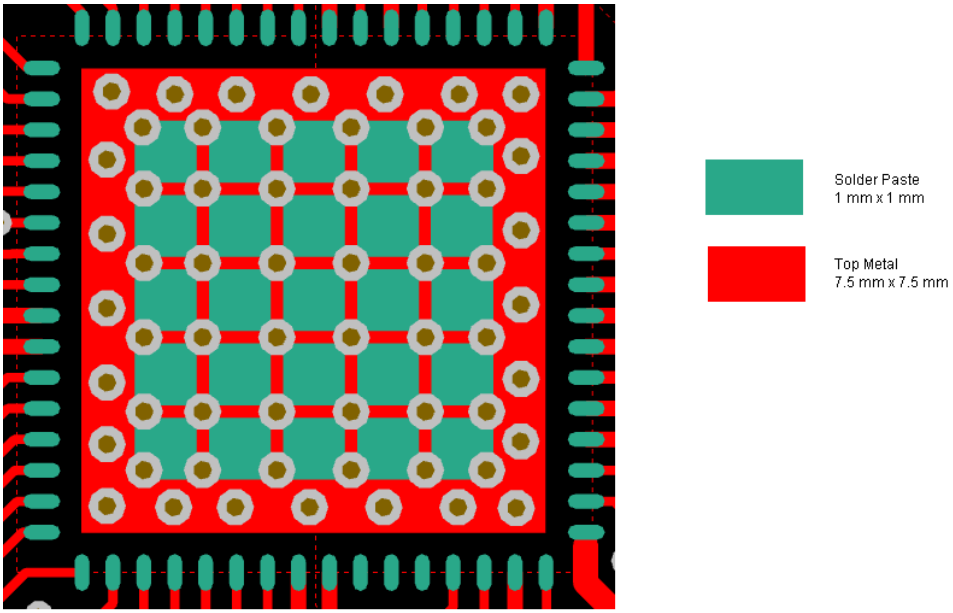

Figure 14. Ground Vias on Ground Pad

- Open the solder mask on the vias on the bottom side for better soldering yield. This process is called *via encroaching*.
- Figure 15 shows solder paste split into smaller blocks to avoid component lifting while soldering or reflow.
- Solder paste should cover at least 75% of the ground tab of the QFN.
- The metal layers on L1 under the device are expanded beyond the thermal pad dimensions. This step specifically improves the spectral mask and EVM performance. Also, the additional vias placed along the edge of the package help suppress EMI emissions.
- Although the metal on L1 below the QFN is oversized, the solder mask remains smaller to fit the thermal pad dimensions on the device.

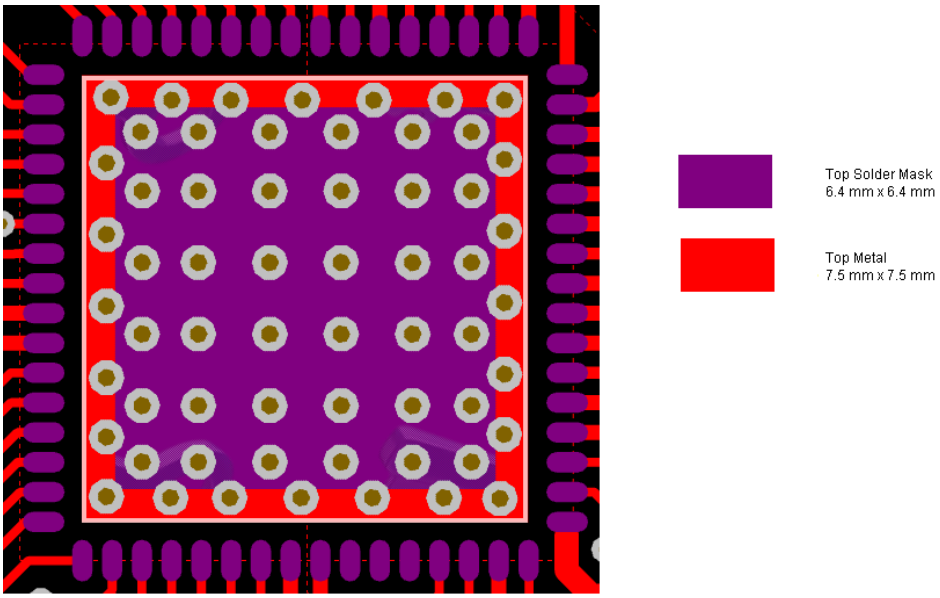

Figure 15. Top Metal and Solder Mask (Reduced Mask Area)

For the exact dimensions of the metal pad, solder mask, and the paste layers, refer to the CC3120 SimpleLink Wi-Fi and IoT Solution BoosterPack™ design files, and the CC3220 SimpleLink Wi-Fi and IoT Solution With MCU LaunchPad board design.

5 Summary

This document presented an introduction to designing a 4-layer PCB for the CC3120 and CC3220 SimpleLink Wi-Fi, easy to lay out QFN packaged family of devices. In addition to the recommendations presented here, see the CC3120 SimpleLink Wi-Fi and IoT Solution BoosterPack Design Files, and the CC3220 SimpleLink Wi-Fi and IoT Solution With MCU LaunchPad Board Design.

6 Additional References

1. Texas Instruments, CC31xx and CC32xx main landing page
2. *CC3120 SimpleLink™ Wi-Fi® and IoT Solution for MCU Applications Data Sheet*
3. *CC3220 SimpleLink™ Wi-Fi® and IoT Solution, a Single Chip Wireless MCU Data Sheet*
4. CC3120 SimpleLink Wi-Fi and IoT Solution BoosterPack Design Files
5. CC3220 SimpleLink Wi-Fi and IoT Solution With MCU LaunchPad Board Design

Revision History

Date	Revision	Notes
February 2017	SWRU458*	Initial release

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