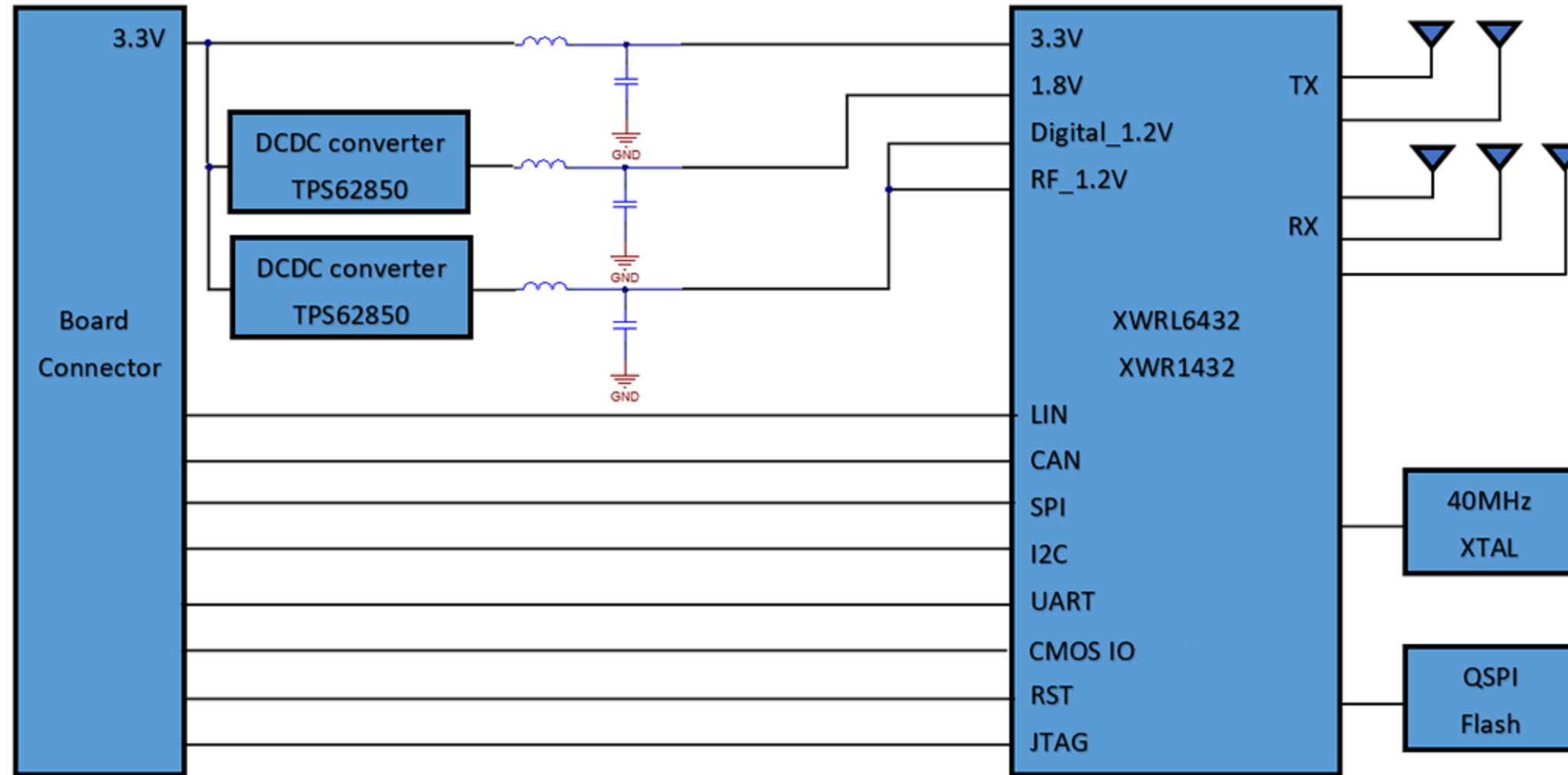


Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
B	N/A	2024/6/28	Kumar Y. B., Chethan	Optimize changes for low power mode, and stackup material changes.

### BLOCK DIAGRAM



Orderable: IWRL6432FSPEVM	Designed for: Public Release	Mod. Date: 6/26/2024
TID #: N/A	Project Title: IWRL6432 FCCSP Power optimized design	
Number: PROC198	Rev: B	Sheet Title: BLOCK DIAGRAM
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 1 of 8
Drawn By: Justin Yin	File: PROC198_Diagram.SchDoc	Size: B
Engineer: Justin Yin	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

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### TABLE OF CONTENTS

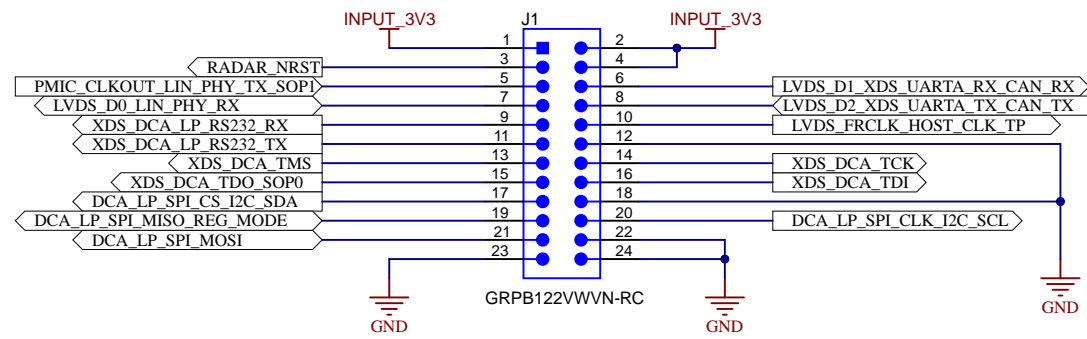
SHEET NO.	SHEET NAME
1	BLOCK DIAGRAM
2	TABLE OF CONTENTS
3	PWR_CONNECTOR
4	DC REGULATORS
5	xWRL6432_CHIP
6	DECOUPLING CAPS
7	QSPI_FLASH
8	HARDWARE

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Orderable: <a href="#">IWRL6432FSPEVM</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 6/26/2024
TID #: N/A	Project Title: <a href="#">IWRL6432 FCCSP Power optimized design</a>	
Number: <a href="#">PROC198</a>	Rev: <a href="#">B</a>	Sheet Title: <a href="#">TABLE OF CONTENTS</a>
SVN Rev: Not in version control	Assembly Variant: <a href="#">001_IWR</a>	Sheet: <a href="#">2</a> of <a href="#">8</a>
Drawn By: <a href="#">Justin Yin</a>	File: <a href="#">PROC198_Table_Of_Contents.SchDoc</a>	Size: B
Engineer: <a href="#">Justin Yin</a>	Contact: <a href="#">http://www.ti.com/support</a>	



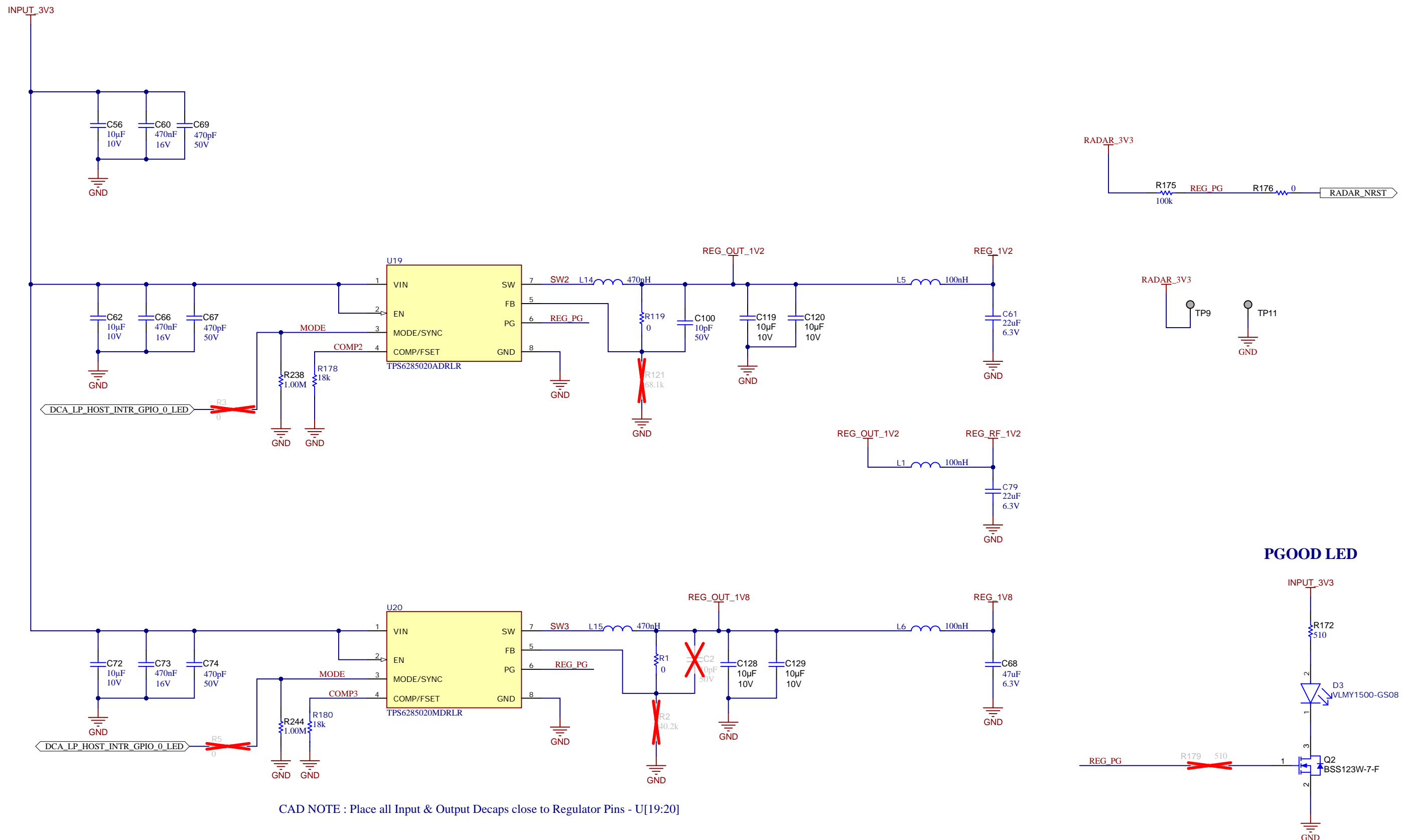
### Connectors



Orderable: IWRL6432FSPEVM	Designed for: Public Release	Mod. Date: 6/26/2024
TID #: N/A	Project Title: IWRL6432 FCCSP Power optimized design	
Number: PROC198	Rev: B	Sheet Title: PWR Connector
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 3 of 8
Drawn By: Justin Yin	File: PROC198_PWR_Connector.SchDoc	Size: B
Engineer: Justin Yin	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

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# DC-DC REGULATORS - 3.3V, 1.2V & 1.8V OUTPUTS



CAD NOTE : Place all Input & Output Decaps close to Regulator Pins - U[19:20]

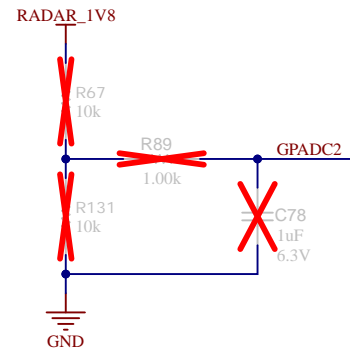
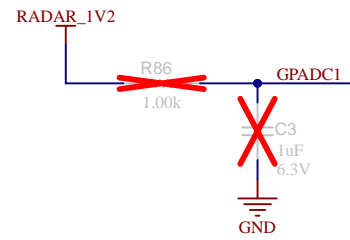
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Orderable: IWRL6432FSPEVM	Designed for: Public Release	Mod. Date: 6/28/2024
TID #: N/A	Project Title: IWRL6432 FCCSP Power optimized design	
Number: PROC198	Rev: B	Sheet Title: DC REGULATORS
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 4 of 8
Drawn By: Justin Yin	File: PROC198_DC_Regulators.SchDoc	Size: B
Engineer: Justin Yin	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

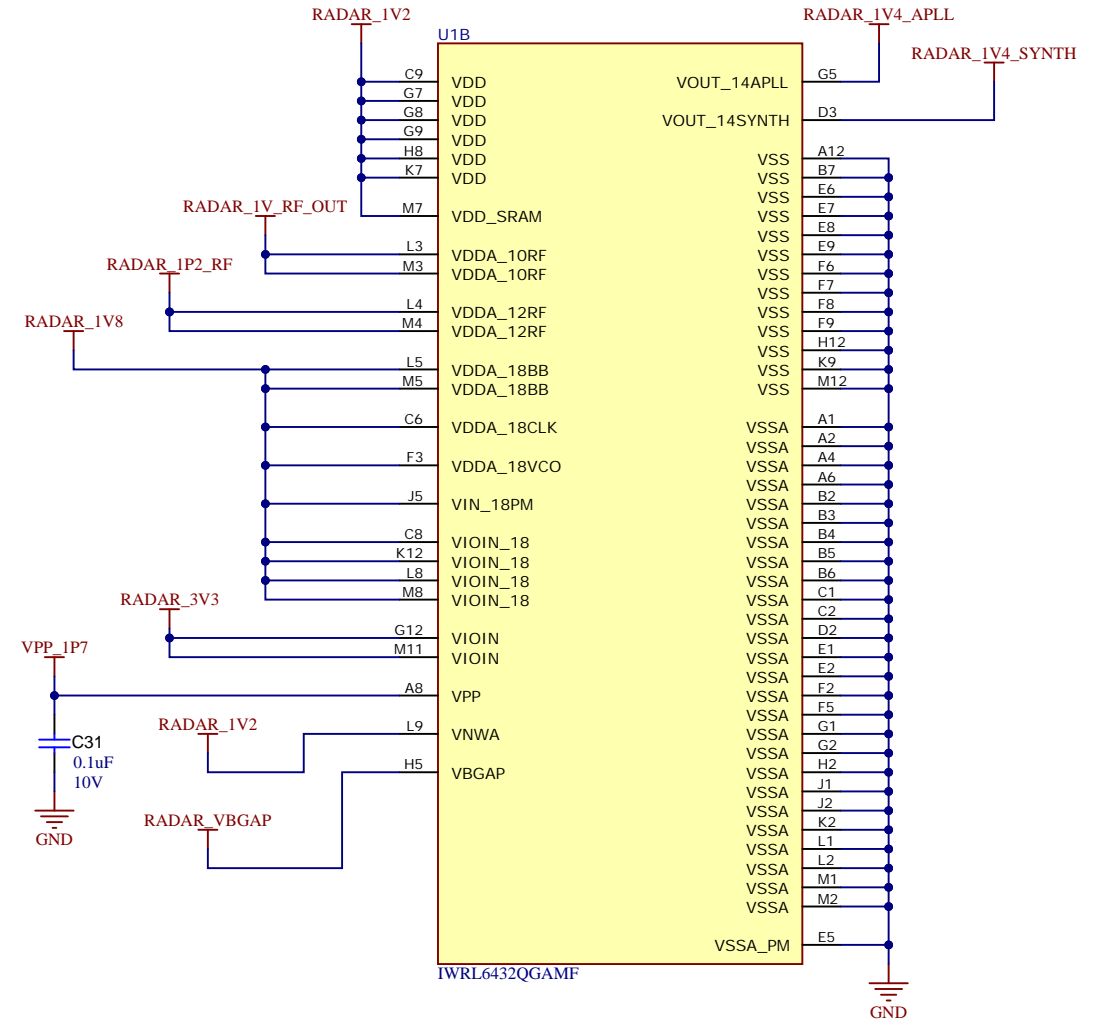
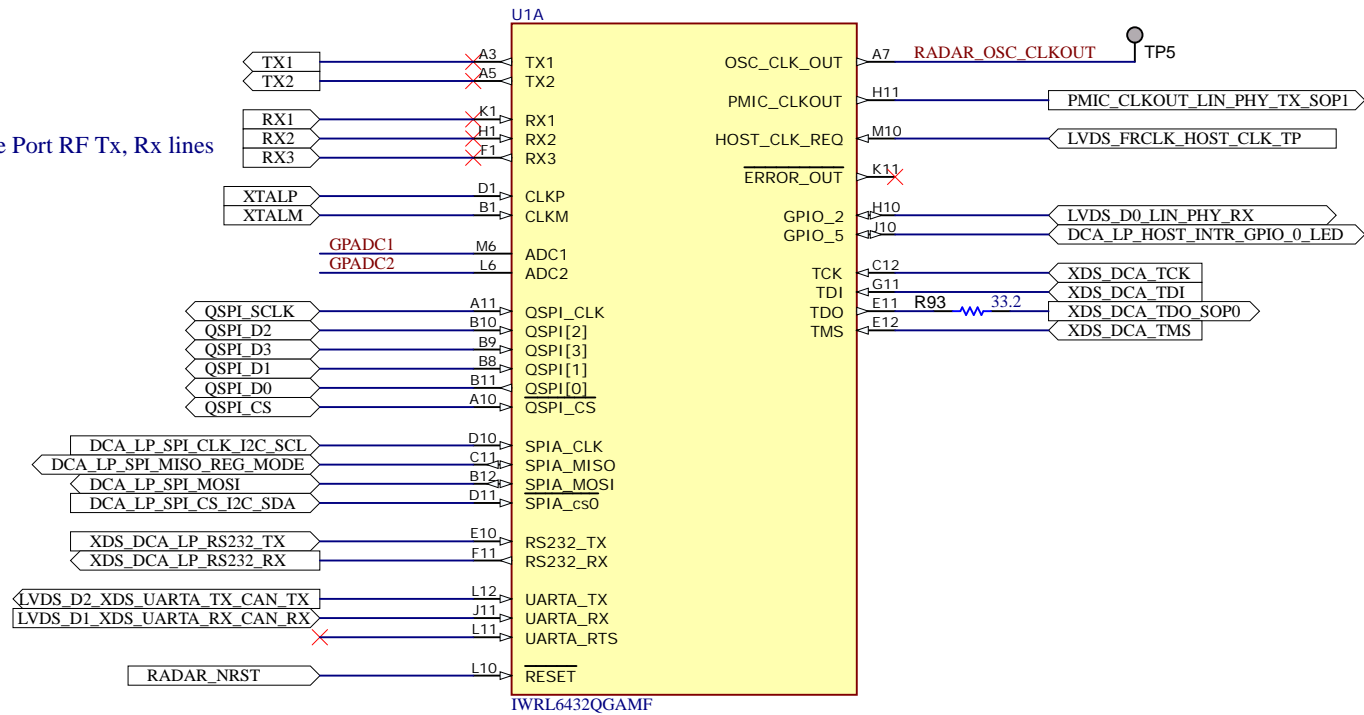
# xWRL6432 CHIP

**Design Note:**

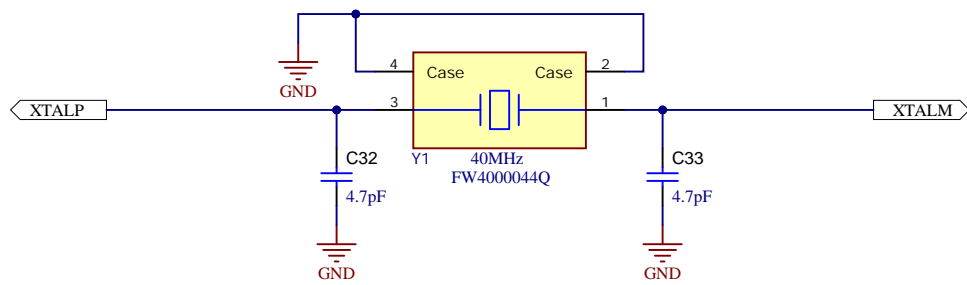
1. Antenna traces are GCPW traces
2. 'Generic No ERCs' were placed intentionally on Single Port RF Tx, Rx lines



CAD Note: Place C3 and C78 close to xWRL6432 IC

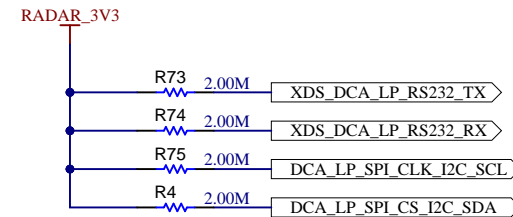
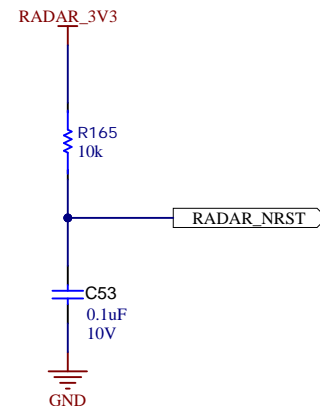


### 40 MHz CRYSTAL OSCILLATOR



Alternate Crystal part number : CX2016SA40000D0PTWC1

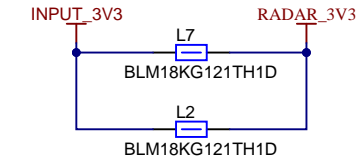
### RESET



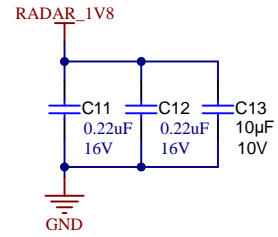
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TID #: N/A	Project Title: IWRL6432 FCCSP Power optimized design	
Number: PROC198	Rev: B	Sheet Title: xWRL6432_CHIP
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 5 of 8
Drawn By: Justin Yin	File: PROC198_xWRL6432_Chip_SchDoc	Size: B
Engineer: Justin Yin	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

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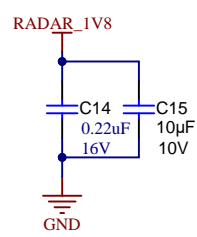
# SUPPLY\_DECOUPLING\_CAPS



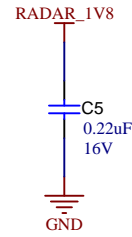
BB SUPPLY



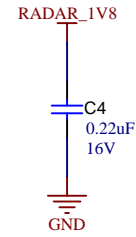
VCLK SUPPLY



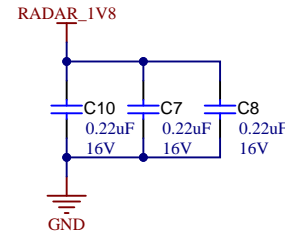
VCO\_LDO SUPPLY



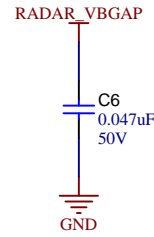
PM SUPPLY



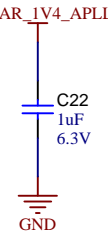
1P8V IO SUPPLY



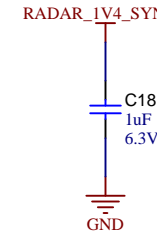
VBGAP SUPPLY



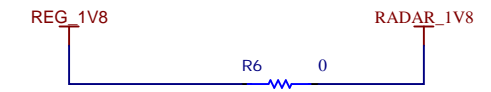
VOUT\_PLL SUPPLY



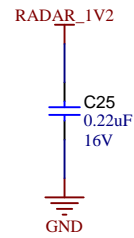
VOUT\_SYNTH SUPPLY



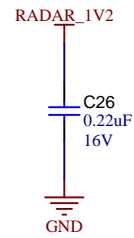
## DC-DC CURRENT MEASUREMENT



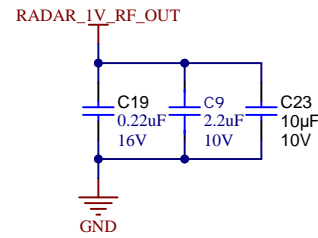
VNWA SUPPLY



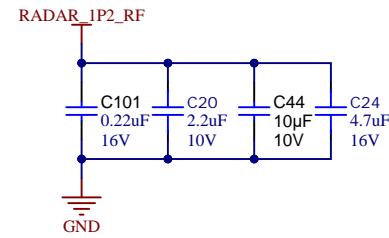
SRAM SUPPLY



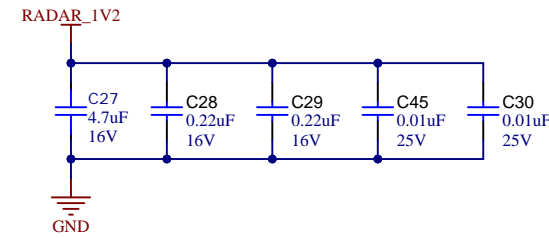
1V\_RF\_OUT SUPPLY



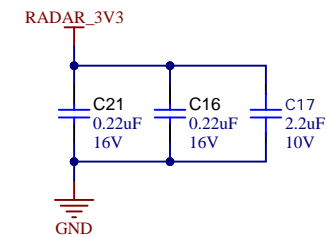
1V2\_RF SUPPLY



1V2 DIG SUPPLY



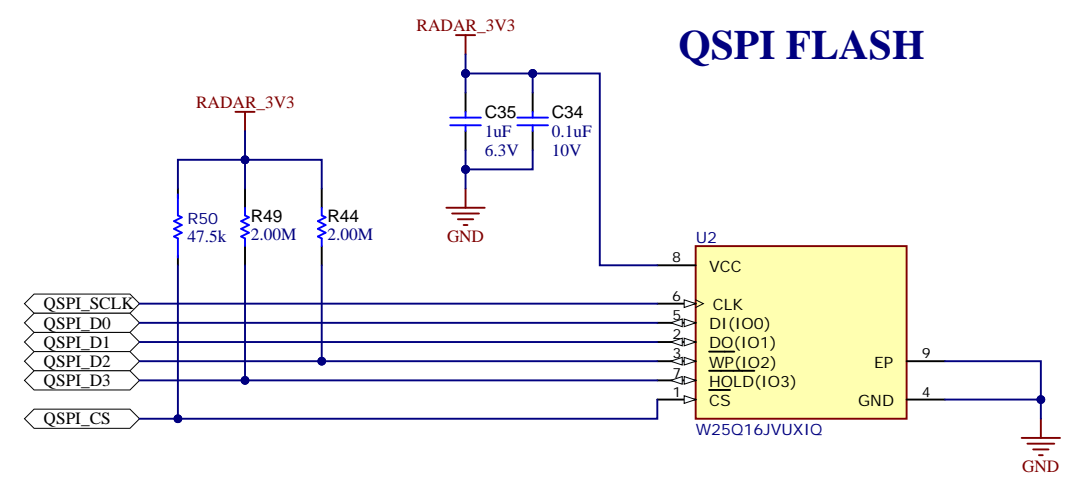
3V3\_IO SUPPLY



Orderable: IWRL6432FSPEVM	Designed for: Public Release	Mod. Date: 7/4/2024
TID #: N/A	Project Title: IWRL6432 FCCSP Power optimized design	
Number: PROC198	Rev: B	Sheet Title: DECOUPLING_CAPS
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 6 of 8
Drawn By: Justin Yin	File: PROC198_Decoupling_caps.SchDoc	Size: B
Engineer: Justin Yin	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

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Orderable: IWRL6432FSPEVM	Designed for: Public Release	Mod. Date: 6/27/2024
TID #: N/A	Project Title: IWRL6432 FCCSP Power optimized design	
Number: PROC198	Rev: B	Sheet Title: QSPI_FLASH
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 7 of 8
Drawn By: Justin Yin	File: PROC198_QSPI_Flash.SchDoc	Size: B
Engineer: Justin Yin	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	





PCB Number: PROC198  
PCB Rev: B

PCB  
LOGO  
Texas Instruments

Variant/Label Table	
Variant	Label Text
001_IWR	IWRL6432FSEVM
002_AWR	AWRL6432FSEVM

CAPACITORS HIGHLIGHTED IN THE RED COLOR BOXES ARE ADDED FOR IMPROVEMENT AND THOSE ARE NOT MANDATORY.

ZZ1

Label Assembly Note  
This Assembly Note is for PCB labels only

ZZ2

Assembly Note  
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3

Assembly Note  
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4

Assembly Note  
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5

Assembly Note  
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: IWRL6432FSPEVM	Designed for: Public Release	Mod. Date: 7/3/2024
TID #: N/A	Project Title: IWRL6432 FCCSP Power optimized design	
Number: PROC198	Rev: B	Sheet Title: HARDWARE
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 8 of 8
Drawn By: Justin Yin	File: PROC198_Hardware.SchDoc	Size: B
Engineer: Justin Yin	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

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