

# **TPS659039-Q1 User's Guide to Power DRA74x, DRA75x, TDA2x, and AM572x**

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This User's Guide can be used as a guide for integrating the TPS659039-Q1 power-management integrated circuit (PMIC) into a system powering the DRA74x, DRA75x, TDA2x, or AM572x device.

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## Trademarks

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## 1 Introduction

This user's guide can be used as a guide for connectivity between the TPS659039-Q1 PMIC and a processor. This guide describes the platform connections as well as the power-up, power-down, and sleep entry and exit sequences along with the OTP configurations. In addition, this user's guide describes the initialization software and advises how to get started with the TPS659039-Q1 PMIC. This document does not provide details about the power resources, external components, or the functionality of the device. For such information, see the TPS659038-Q1 and TPS659039-Q1 data sheet, [TPS65903x-Q1 Automotive Power Management Unit \(PMU\) for Processor](#).

In the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material, the data sheet specification will be the definitive source.

## 2 Device Versions

Three different versions of the TPS659039-Q1 device are available and the OTP settings for each version are described in this document. The three different versions of the device can be used to power the DRA74x, DRA75x, TDA2x, and AM572x processor devices. The OTP version can be read from the SW\_REVISION register. In this user's guide, each device version is distinguished either by the part number or the SW\_REVISION value which are both listed in [Table 1](#).

In addition, the TPS65917-Q1 device can be used to power the DRA74x, DRA75x, and TDA2x devices as described in the [TPS65917-Q1 User's Guide to Power DRA7xx and TDA2x/TDA2Ex](#). See [Table 1](#) to determine the recommended part number based on the load current requirements of the MPU, DSPEVE, GPU, and IVA domains of the processor.

Texas Instruments recommends having 15% margin in the load current. Therefore the current requirements listed in [Table 1](#) are 15% lower than the maximum capability of the regulator. If the load currents in the application are unknown, select the O9039A385IZWSRQ1 because it supports the maximum performance of the processors.

**Table 1. TPS659039-Q1 OTP Settings Differentiation**

LOAD CURRENT REQUIREMENT	SLEEP MODE	POWERGOOD	SPECIAL FEATURES	ORDERABLE PART NUMBER	CONTENT OF SW_REVISION REGISTER
MPU > 3 A or DSPEVE + GPU + IVA > 3.4 A	Yes	Yes	Integrated DDR regulator	<a href="#">O9039A385IZWSRQ1</a>	0x85
MPU > 3 A or DSPEVE + GPU + IVA > 3.4 A	Yes	Yes	Same configuration as <a href="#">DRA74x EVM</a> External DDR regulator	<a href="#">O9039A387IZWSRQ1</a>	0x87 <sup>(1)</sup>
MPU > 3 A or 3 A < DSPEVE + GPU + IVA < 3.4 A	Yes	Yes	2 SMPS regulators for external use Integrated DDR regulator	<a href="#">O9039A389IZWSRQ1</a>	0x89
MPU < 3 A and DSPEVE + GPU + IVA < 3 A	No	Yes	Smaller, lower-power solution	<a href="#">O917A132TRGZRQ1</a>	See <a href="#">User's Guide</a>
MPU < 3 A and DSPEVE + GPU + IVA < 3 A	Yes	No	Smaller, lower-power solution	<a href="#">O917A133TRGZRQ1</a>	

<sup>(1)</sup> TI only recommends 0x87 if copying the DRA74x EVM reference design.

[Table 2](#) lists the older OTP versions and the differences compared to the current OTP versions. The older versions are not recommended for new designs (NRND). The newer versions should be used instead because they meet the latest specifications of the processor, and are pin-to-pin replacements for the older versions with no schematic or layout change required.

**Table 2. Differences from Older OTP Versions**

OLDER OTP VERSION	NEWER OTP VERSION	CHANGES IMPLEMENTED IN NEWER VERSION
O9039A344IZWSRQ1	O9039A387IZWSRQ1	SMPS123 voltage increased from 1.10 V to 1.15 V SMPS7 voltage increased from 1.06 V to 1.15 V
O9039A360IZWSRQ1	O9039A385IZWSRQ1	SMPS12 voltage increased from 1.10 V to 1.15 V SMPS7 voltage increased from 1.06 V to 1.15 V
O9039A36BIZWSRQ1	O9039A389IZWSRQ1	SMPS12 voltage increased from 1.10 V to 1.15 V SMPS6 voltage increased from 1.06 V to 1.15 V

### 3 Platform Connection

Figure 1 shows the detailed connections between a processor and the O9039A387IZWSRQ1 (0x87). In this configuration, the VIO\_IN of the PMIC is supplied by SMPS9 at 1.8 V. If the VIO\_IN of the PMIC is supplied by 3.3 V, it can be supplied by an externally switched 3.3-V rail enabled by SMPS9.

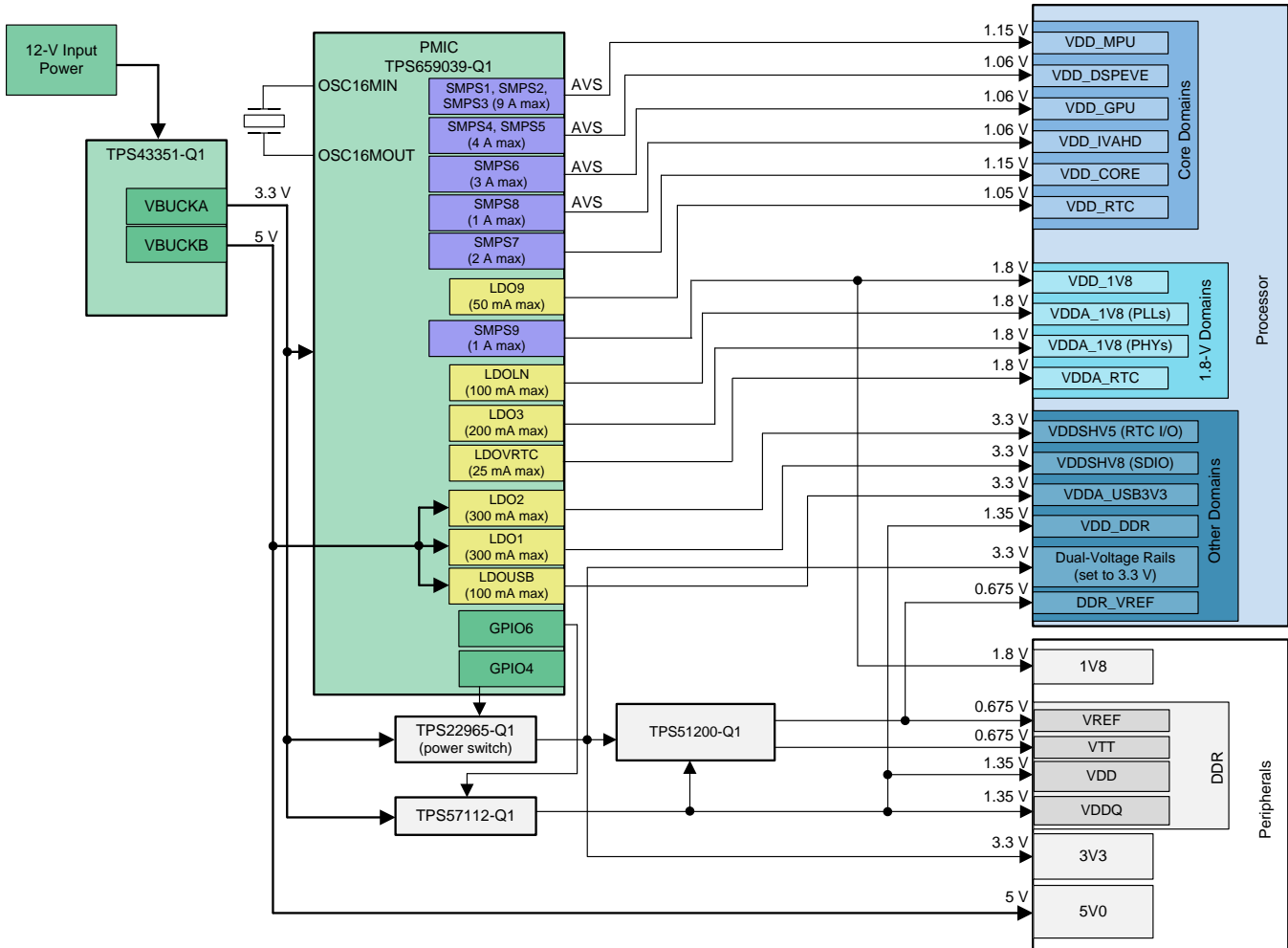


Figure 1. Processor Connection With O9039A387IZWSRQ1

Figure 2 shows the detailed connections between the processor and the O9039A385IZWSRQ1 (0x85). The main difference between 0x85 and 0x87 is that the DDR voltage is supplied by the SMPS3 of the PMIC instead of an external regulator. The configuration allows selection between a 1.35-V output on SMPS3 supporting DDR3L and a 1.5-V output supporting DDR3. Additionally, this PMIC device does not use an external crystal. In this configuration, VIO\_IN of the PMIC is driven by the 3.3-V output of the load switch, TPS22965-Q1.

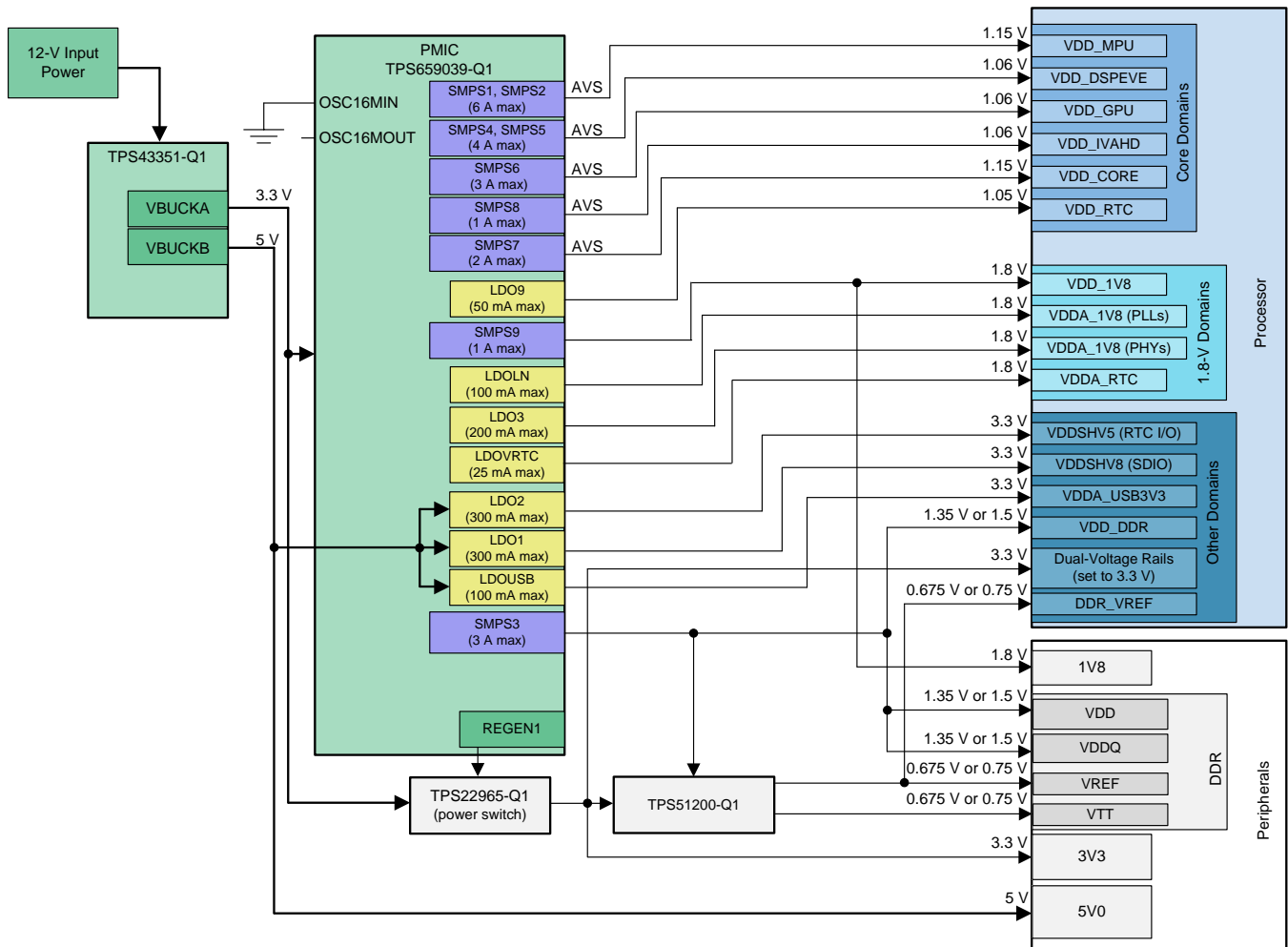


Figure 2. Processor Connection With O9039A385IZWSRQ1

Figure 3 shows the detailed connections between the processor and O9039A389IZWSRQ1 (0x89). This configuration uses a different power mapping where the DSPEVE, GPU, and IVAHD domains of the processor are powered from the single output SMPS45. The core domain of the processor is powered by SMPS6. The VDD\_1V8 domain of the processor is powered by SMPS8. This configuration allows selection between a 1.35-V output on SMPS3 supporting DDR3L and a 1.5-V output supporting DDR3. Additionally, this PMIC device does not use an external crystal. In this configuration, VIO\_IN of the PMIC is driven by the 3.3-V output of the load switch, TPS22965-Q1.

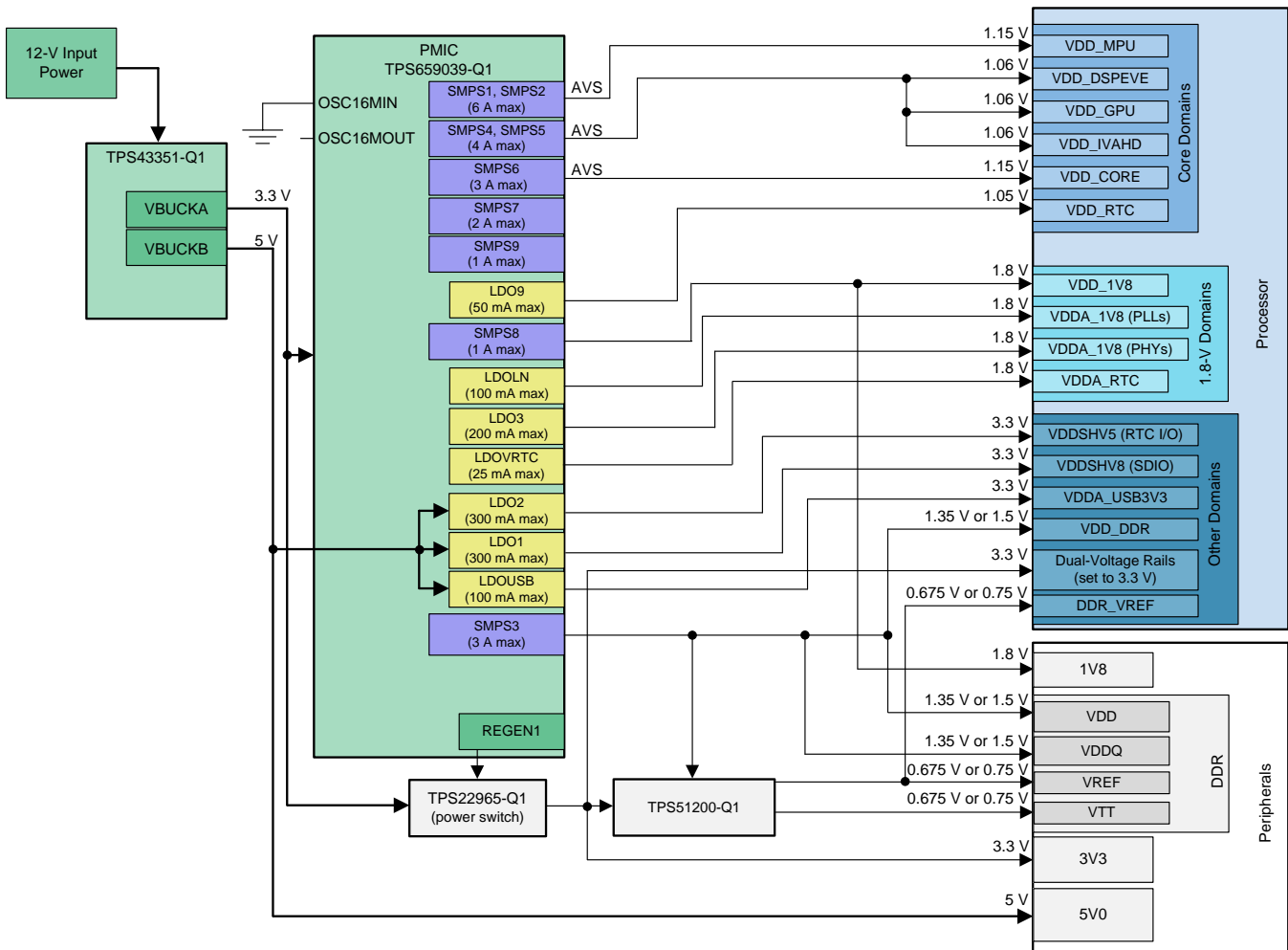


Figure 3. Processor Connection With O9039A389IZWSRQ1

Figure 4 and Figure 5 show the reset connections required between the TPS659039-Q1 and the processor. All of the OTP configurations have the same reset connections to the processor, along with one of the two options for enabling the power supply; either POWERHOLD or PWRON. Enabling either of these signals turns on the TPS659039-Q1 device and starts the startup sequence for the processor. Figure 4 shows the POWERHOLD configuration for the TPS659039-Q1 and the processor. GPIO\_7 is configured as POWERHOLD in the OTP memory. To turn on the TPS659039-Q1, GPIO\_7 must be set to a high logic level. When using POWERHOLD, the PWRON signal can be left floating.

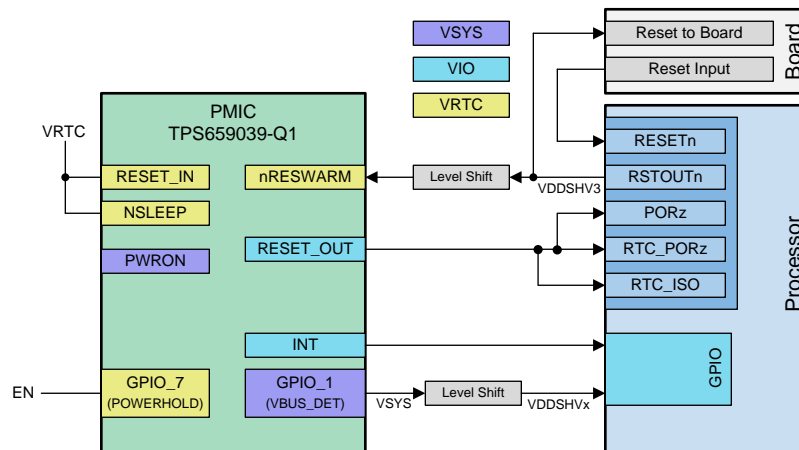


Figure 4. Reset Connections With POWERHOLD Configuration

Figure 5 shows the PWRON configuration for the TPS659039-Q1 and the processor. This configuration is used when a push button enables the system. As shown, PWRON is connected to a switch that pulls PWRON to a low logic level when the switch is pressed on.

In some applications, a warm reset is required. This allows for the TPS659039-Q1 to reset to its default settings without turning off first. To complete a warm reset correctly, POWERHOLD must be kept at a high logic level so the TPS659039-Q1 does not turn off. One solution for this scenario is that GPIO\_5 is tied to GPIO\_7 and pulled up to VDDSD1V8 from the processor. Pulling GPIO\_7 to VDDSD1V8 ensures that POWERHOLD is kept high during a warm reset. Tying GPIO\_5 to POWERHOLD provides a method to set POWERHOLD low, which is necessary to turn off the device.

For this solution to work, a few software writes must occur:

1. First, enable the TPS659039-Q1 by the push button.
2. Second, set GPIO\_5 to a high logic level.
3. Third, set GPIO\_5 as an output.

When ready to disable the TPS659039-Q1, set GPIO\_5 to a low logic level.

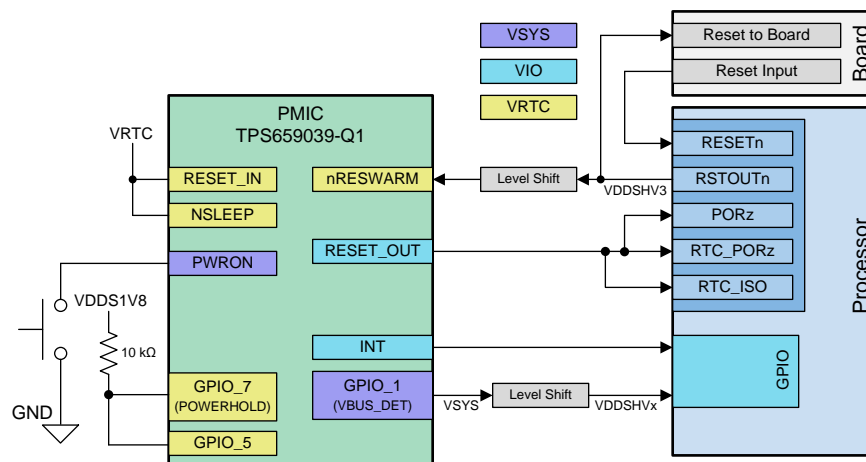


Figure 5. Reset Connections With PWRON Configuration

## 4 BOOT OTP Configuration

All TPS659039-Q1 resource settings are stored in the form of registers. Therefore, all platform-related settings are linked to an action altering these registers. This action can be a static update (register initialization value) or a dynamic update of the register (either from the user or from a power sequence).

Resources and platform settings are stored in nonvolatile memory (OTP). These settings are defined as follows:

**Static platform settings** — These settings define, for example, SMPS or LDO default voltages, and GPIO functionality. Most static platform settings can be overwritten by a power sequence or by the user.

**Sequence platform settings** — These settings define the TPS659039-Q1 power sequences between state transitions, such as the OFF2ACT sequence when transitioning from OFF mode to ACTIVE mode. The power sequence is composed of several register accesses that define which resources (and the corresponding registers) must be updated during the respective state transition. The state of these resources can be overwritten by the user after the power sequence completes execution.

## 5 Static Platform Settings

Each device has predefined values stored in OTP which control the default configuration of the device. The tables in this section list the OTP-programmed values for each device, distinguished by the SW\_REVISION.

### 5.1 System Voltage Monitoring

**Table 3. System Voltage Monitoring OTP Settings**

REGISTER	BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE	UNIT
VSYS_MON	VSYS_HI	System voltage rising-edge threshold		3.1		V
VSYS_LO	VSYS_LO	System voltage falling-edge threshold		2.75		V

The power state-machine of the TPS659039-Q1 device is controlled by comparators monitoring the voltage on the VCC\_SENSE and VCCx pins. For electrical parameters refer to the data sheet.

**VSYS\_LO** — When the voltage on the VCC1 pin rises above VSYS\_LO, the device enters from the BACKUP to the OFF state. When the device is in the ACTIVE, SLEEP, or OFF state and the voltage on the VCC1 pin decreases below VSYS\_LO, the device enters BACKUP mode. The VSYS\_LO level is OTP programmable.

**VSYS\_HI** — During power up, the VSYS\_HI OTP value is used as a threshold for the VSYS\_MON comparator which is gating the PMIC startup (as a threshold for transition from the OFF to ACTIVE state). The VSYS\_MON comparator monitors the VCC\_SENSE pin. After power up, the user can use software to configure the comparator threshold in the VSYS\_MON register.



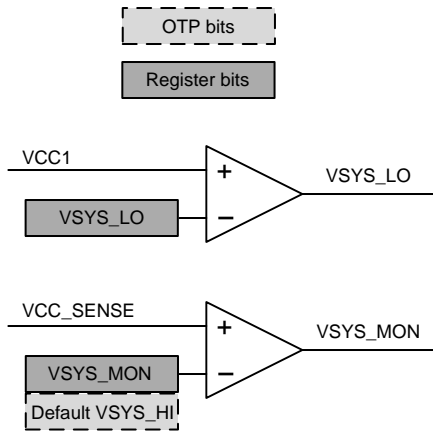


Figure 6. PMIC Comparators

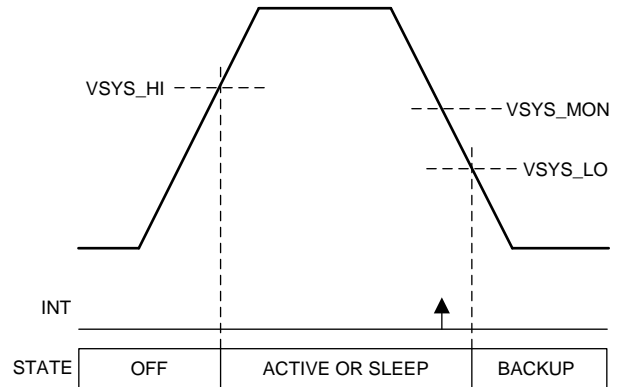


Figure 7. State Transitions

**NOTE:** The maximum input voltage of the VCC\_SENSE and VCC\_SENSE2 pins depend on the OTP setting of PMU\_CONFIG [HIGH\_VCC\_SENSE] as listed in the *Recommended Operating Conditions* table of the TPS659039-Q1 data sheet. This configuration is set as HIGH\_VCC\_SENSE = 0 with the VCC\_SENSE and VCC\_SENSE2 pins are connected to VCC1.

For the recommended operating conditions of the electrical parameters, see the TPS659038-Q1 and TPS659039-Q1 data sheet, *TPS65903x-Q1 Automotive Power Management Unit (PMU) for Processor*.

## 5.2 SMPS

This section describes the default voltage for each SMPS. The 0x87 OTP uses SMPS123 in triple phase. Therefore, SMPS12 and SMPS3 are combined and always output the same voltage programmed in to the SMPS12\_VOLTAGE register. The 0x85 and 0x89 OTP have two default voltages for SMPS3 based on the connection of the BOOT0 pin. If the BOOT0 pin is connected to 0 V, then SMPS3 defaults to 1.35 V. If the BOOT0 pin is connected to 1.8 V, then SMPS3 outputs 1.5 V.

By default, SMPS7 and SMPS9 remain off in OTP 0x89. SMPS7 and SMPS9 can be enabled after startup through I<sup>2</sup>C by setting the appropriate SMPSx\_CTRL and SMPSx\_VOLTAGE registers.

Table 4. SMPS OTP Settings

BIT	DESCRIPTION <sup>(1)</sup>	0x87 VALUE	0x85 VALUE		0x89 VALUE		UNIT
			BOOT0 = 0	BOOT0 = 1	BOOT0 = 0	BOOT0 = 1	
SMPS12_VOLTAGE	Default output voltage for the regulator		1.15				V
SMPS3_VOLTAGE	Default output voltage for the regulator	N/A	1.35	1.5	1.35	1.5	V
SMPS45_VOLTAGE	Default output voltage for the regulator		1.06				V
SMPS6_VOLTAGE	Default output voltage for the regulator		1.06		1.15		V
SMPS7_VOLTAGE	Default output voltage for the regulator		1.15		0		V
SMPS8_VOLTAGE	Default output voltage for the regulator		1.06		1.8		V
SMPS9_VOLTAGE	Default output voltage for the regulator		1.8		0		V
SMPS12_SMPS123_EN	SMPS3 configuration	SMPS123 triple phase	SMPS3 single phase				NA

<sup>(1)</sup> The regulator output voltage cannot be modified while active from one (0.7 to 1.65 V) voltage range to the other (1 to 3.3 V) voltage range or the other way around. The regulator must be turned off to do so.

### 5.3 LDO

This section describes the default output voltage for each LDO.

**Table 5. LDO OTP Settings**

BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE	UNIT
LDO1_VOLTAGE	Default output voltage for the regulator		3.3		V
LDO2_VOLTAGE	Default output voltage for the regulator		3.3		V
LDO3_VOLTAGE	Default output voltage for the regulator		1.8		V
LDO9_VOLTAGE	Default output voltage for the regulator		1.05		V
LDOLN_VOLTAGE	Default output voltage for the regulator		1.8		V
LDOUSB_VOLTAGE	Default output voltage for the regulator		3.3		V

**NOTE:** LDO1 and LDO2 share a single input LDO12\_IN and must be supplied by the same voltage. Refer to the input voltage parameter in the data sheet.

### 5.4 Interrupts

The interrupts are split into four register groups (INT1, INT2, INT3, and INT4). All interrupts are logically combined on a single output line, INT (default active-low). This line is used as an external interrupt line to warn the host processor of any interrupt event that has occurred within the device. The OTP settings in this section show whether each interrupt is enabled or disabled by default.

**Table 6. INT1 OTP Settings**

REGISTER	BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE
INT1_MASK	VSYS_MON	Enable and disable interrupt from the VSYS_MON comparator		1: Interrupt generation disabled	
	PWRDOWN	Enable and disable interrupt from the PWRDOWN pin		0: Interrupt generated	
	PWRON	Enable and disable interrupt from PWRON pin. A PWRON event is always an ON request.		1: Interrupt generation disabled	
	LONG_PRESS_KEY	Enable and disable interrupt from long key press on the PWRON pin		1: Interrupt generation disabled	
	RPWRON	Enable and disable interrupt from RPWRON pin. A RPWRON event is always an ON request.		0: Interrupt generated	
	HOTDIE	Enable and disable interrupt from device hot-die detection. The interrupt can be used as a pre-warning for processor to limit the PMIC load, before increasing die temperature forces shutdown.		0: Interrupt generated	

**Table 7. INT2 OTP Settings**

REGISTER	BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE
INT2_MASK	SHORT	Triggered from internal event of SMPS or LDO outputs failing. If an interrupt is enabled, it is an ON request.		0: Interrupt generated	
	WDT	Enable and disable interrupt from watchdog expiration		0: Interrupt generated	
	RTC_TIMER	Enable and disable RTC timer interrupt. Timer period preprogrammed. If an interrupt is enabled, it is an ON request.		1: Interrupt generation disabled	
	RTC_ALARM	Enable and disable RTC alarm interrupt. The alarm is preprogrammed for certain date or time. If an interrupt is enabled, it is an ON request.		0: Interrupt generated	
	RESET_IN	Enable and disable interrupt from the RESET_IN pin		0: Interrupt generated	

**Table 8. INT3 OTP Settings**

REGISTER	BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE
INT3_MASK	GPADC_EOC_SW	GPADC result ready from software-initiated conversion	1: Interrupt generation disabled		
	GPADC_AUTO_1	GPADC automatic conversion result 1 above or below the reference threshold	0: Interrupt generated		
	GPADC_AUTO_0	GPADC automatic conversion result 0 above or below the reference threshold	0: Interrupt generated		

**Table 9. INT4 OTP Settings**

REGISTER	BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE
INT4_MASK	GPIO_7	Enable and disable interrupt from the GPIO7 pin rising or falling edge	1: Interrupt generation disabled		
	GPIO_6	Enable and disable interrupt from the GPIO6 pin rising or falling edge	1: Interrupt generation disabled		
	GPIO_5	Enable and disable interrupt from the GPIO5 pin rising or falling edge	1: Interrupt generation disabled		
	GPIO_4	Enable and disable interrupt from the GPIO4 pin rising or falling edge	1: Interrupt generation disabled		
	GPIO_3	Enable and disable interrupt from the GPIO3 pin rising or falling edge	1: Interrupt generation disabled		
	GPIO_2	Enable and disable interrupt from the GPIO2 pin rising or falling edge	1: Interrupt generation disabled		
	GPIO_1	Enable and disable interrupt from the GPIO1 pin rising or falling edge	1: Interrupt generation disabled		
	GPIO_0	Enable and disable interrupt from the GPIO0 pin rising or falling edge	1: Interrupt generation disabled		

## 5.5 GPIO

TPS659039-Q1 integrates eight configurable general-purpose I/Os (GPIOs) that are multiplexed with alternative features. This section describes the default configuration of each GPIO, as well as the configuration of internal pullup or pulldown resistors on the GPIOs.

**Table 10. GPIO OTP Settings**

REGISTER	BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE
PRIMARY_SECONDARY_PAD2	GPIO_7	Select pin function	10: POWERHOLD		
	GPIO_6	Select pin function	1: SYSEN2		
	GPIO_5	Select pin function	00: GPIO_5		
	GPIO_4	Select pin function	1: SYSEN1		
PRIMARY_SECONDARY_PAD1	GPIO_2	Select pin function	00: GPIO_2		
	GPIO_1	Select pin function	00: GPIO_1		
PU_PD_GPIO_CTRL2	GPIO_7_PD	Enable and disable pulldown for GPIO_7. Applies if GPIO mode is selected	0: Pulldown not enabled		
PU_PD_GPIO_CTRL1	GPIO_3_PD	Enable and disable pulldown for GPIO_3. Applies if GPIO mode is selected	1: Pulldown enabled		
	GPIO_2_PU	Enable and disable pullup for GPIO_2. Applies if GPIO mode is selected	0: Pullup not enabled		
	GPIO_2_PD	Enable and disable pulldown for GPIO_2. Applies if GPIO mode is selected	1: Pulldown enabled		
	GPIO_1_PU	Enable and disable pullup for GPIO_1. Applies if GPIO mode is selected	0: Pullup not enabled		
	GPIO_1_PD	Enable and disable pulldown for GPIO_1. Applies if GPIO mode is selected	1: Pulldown enabled		
	GPIO_0_PD	Enable and disable pulldown for GPIO_0. Applies if GPIO mode is selected	0: Pulldown not enabled		

## 5.6 MISC

This section describes miscellaneous device configuration settings including pulldowns, polarity of signals, communication settings, and other functionality.

**Table 11. MISC1 OTP Settings**

REGISTER	BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE
PRIMARY_SECONDARY_PAD2	RESET_IN_PD	Enable and disable internal pulldown for the RESET_IN pin		1: Pulldown enabled	
	PWRDOWN_PD	Enable and disable internal pulldown for the PWRDOWN pin		1: Pulldown enabled	
POLARITY_CTRL	PWRGOOD_USB_PSELPOLARITY_	Select polarity, applies to PWRGOOD and USB_PSEL selection		0: Active high	
	PWRDOWN_POLARITY	Select PWRDOWN pin polarity: 0: Device is switched off when PWRDOWN is high. 1: Device is switched off when PWRDOWN is low.		0: Active high	
	RESET_IN_POLARITY	Select RESET_IN pin polarity: 0: Device is switched off when RESET_IN is low. 1: Device is switched off when RESET_IN is high.		0: Active low	
	GPIO_3_POLARITY	Select polarity for GPIO3 pin:		0: Active high	

**Table 12. MISC2 OTP Settings**

REGISTER	BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE
LONG_PRESS_KEY	PWRON_DEBOUNCE	Debounce time selection for PWRON pin		00: 15 ms	
I2C_SPI	I2C_SPI	Selection of control interface, I <sup>2</sup> C, or SPI		0: I <sup>2</sup> C	
	ID_I2C2	I2C_2 address for page access versus initial address (0H12)		0: Address is 0x12	
	ID_I2C1	I2C_1 address for I <sup>2</sup> C register access		I2C_1[0] = 1: 0x58 I2C_1[1] = 1: 0x59 I2C_1[2] = 1: 0x5A I2C_1[3] = 1: 0x5B	
PMU_CONFIG	HIGH_VCC_SENSE	Enable internal buffers on VCC_SENSE to allow voltage sensing above 5.25 V		0: High VCC sense not enabled	
	GATE_RESET_OUT	Gating of RESET_OUT until crystal oscillator is stable.		0: Not gated	
	AUTODEVON	Automatically set DEV_ON bit after startup sequence completes		0: AUTODEVON disabled	
	SWOFF_DLY	Delay before switch-off to allow host processor to save context. Device is maintained as ACTIVE until delay expiration then switches off.		00: No delay	
SPARE	REGEN2_OD	Configures REGEN2 to be open drain or push-pull.		0: Push-pull mode	
	REGEN1_OD	Configures REGEN1 to be open drain or push-pull.		0: Push-pull mode	
	OSC16M_CFG	16-MHz crystal is disabled and the 32K bypass is Enable	0: 16-MHz oscillator enabled	1: 16-MHz oscillator disabled	

## 5.7 SWOFF\_HWRST

This section describes whether each reset type is configured to generate a HWRST or SWORST.

**Hardware reset (HWRST)** — A hardware reset occurs when any OFF request is configured to generate a hardware reset. This reset triggers a transition to the OFF state from either the ACTIVE or SLEEP state (execute either the ACT2OFF or SLP2OFF sequence).

**Switch-off reset (SWORST)** — A switch-off reset occurs when any OFF request is configured to not generate a hardware reset. This reset acts as the HWRST, except only the SWO registers are reset. The device enters the OFF state, from either ACTIVE or SLEEP, and therefore executes the ACT2OFF or SLP2OFF sequence.

The power resource control registers for SMPS and LDO voltage levels and operating mode control are in SWORST domain. Additionally some registers control the 32-kHz, REGENx and SYSENx, watchdog, and VSYS\_MON comparator. This list is indicative only.

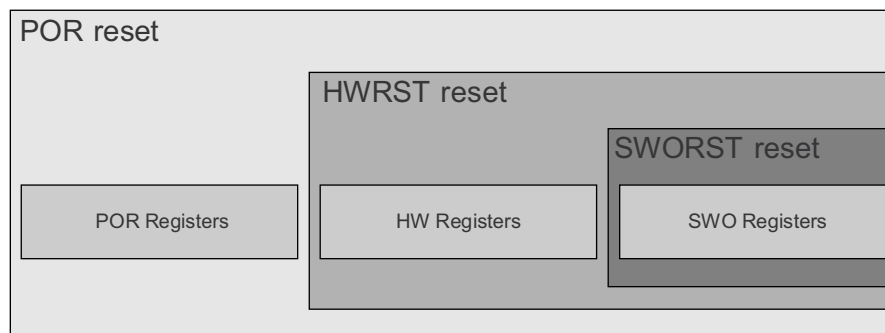


Figure 8. Reset Levels versus Registers

Table 13. SWOFF\_HWRST OTP Settings

REGISTER	BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE
SWOFF_HWRST	PWRON_LPK	Define if PWRON long key press is causing HWRST or SWORST		1: HWRST	
	PWRDOWN	Define if PWRDOWN pin is causing HWRST or SWORST		0: SWORST	
	WTD	Define if watchdog expiration is causing HWRST or SWORST		1: HWRST	
	TSHUT	Define if thermal shutdown is causing HWRST or SWORST		1: HWRST	
	RESET_IN	Define if RESET_IN pin is causing HWRST or SWORST		1: HWRST	
	SW_RST	Define if register bit is causing HWRST or SWORST		1: HWRST	
	VSYS_LO	Define if VSYS_LO is causing HWRST or SWORST		1: HWRST	
	GPADC_SHUTDOWN	Define if GPADC event is causing HWRST or SWORST		0: SWORST	

## 5.8 Shutdown\_ColdReset

These OTP settings show whether each OFF request is configured to generate a shutdown request (SD) or cold reset request (CR).

- When configured to generate an SD, the embedded power controller (EPC) executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and remains in the OFF state.
- When configured to generate a CR, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and restarts, transitioning to the ACTIVE state (OFF2ACT power sequence) if none of the ON request gating conditions are present.

**Table 14. Shutdown\_ColdReset OTP Settings**

REGISTER	BIT	DESCRIPTION	0x87 VALUE	0x85 VALUE	0x89 VALUE
SWOFF_COLDRST	PWRON_LPK	Define if PWRON long key press causes shutdown or cold reset		0: Shutdown	
	PWRDOWN	Define if PWRDOWN pin causes shutdown or cold reset		1: Cold reset	
	WTD	Define if watchdog timer expiration causes shutdown or cold reset		1: Cold reset	
	TSHUT	Define if thermal shutdown causes shutdown or cold reset		0: Shutdown	
	RESET_IN	Define if RESET_IN pin causes shutdown or cold reset		1: Cold reset	
	SW_RST	Define if SW_RST register bit causes shutdown or cold reset		1: Cold reset	
	VSYS_LO	Define if VSYS_LO causes shutdown or cold reset		0: Shutdown	
	GPADC_SHUTDOWN	Define if GPADC shutdown causes shutdown or cold reset		0: Shutdown	

## **6 Sequence Platform Settings**

A power sequence is an automatic preprogrammed sequence handled by the TPS659039-Q1 device to configure the device resources: SMPSs, LDOs, part of GPIOs, and REGEN signals into ON, OFF, or SLEEP state.

### **6.1 OFF2ACT Sequences**

When an ON request occurs in the OFF state, the device is switched on and each resource is enabled based on the programmed OFF2ACT sequence.

Figure 9 shows the OFF2ACT sequence of the O9039A387IZWSRQ1. If the BOOT0 pin is connected to 1.8 V, then RESET\_OUT generates a high pulse of 3.4 ms, a low pulse of 3.4 ms, and then transitions high. If the BOOT0 pin is connected to 0 V, then RESET\_OUT generates only one positive edge.

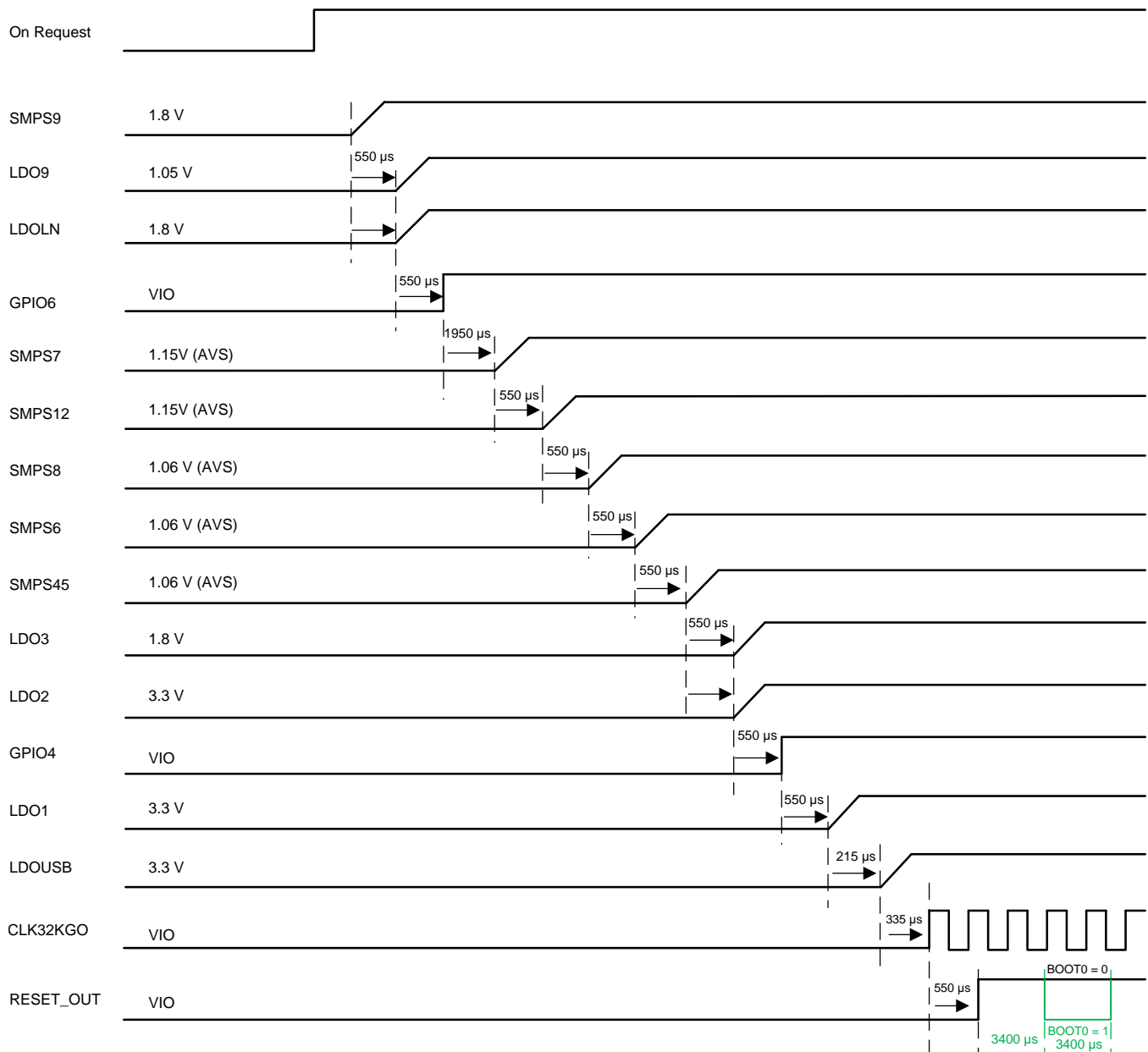


Figure 9. OFF2ACT Sequence of O9039A387IZWSRQ1



Figure 10 shows the OFF2ACT sequence of O9039A385IZWSRQ1. If the BOOT1 pin is connected to 1.8 V, then RESET\_OUT generates a high pulse of 3.4 ms, a low pulse of 3.4 ms, and then transitions high. If the BOOT1 pin is connected to 0 V, then RESET\_OUT generates one positive edge.

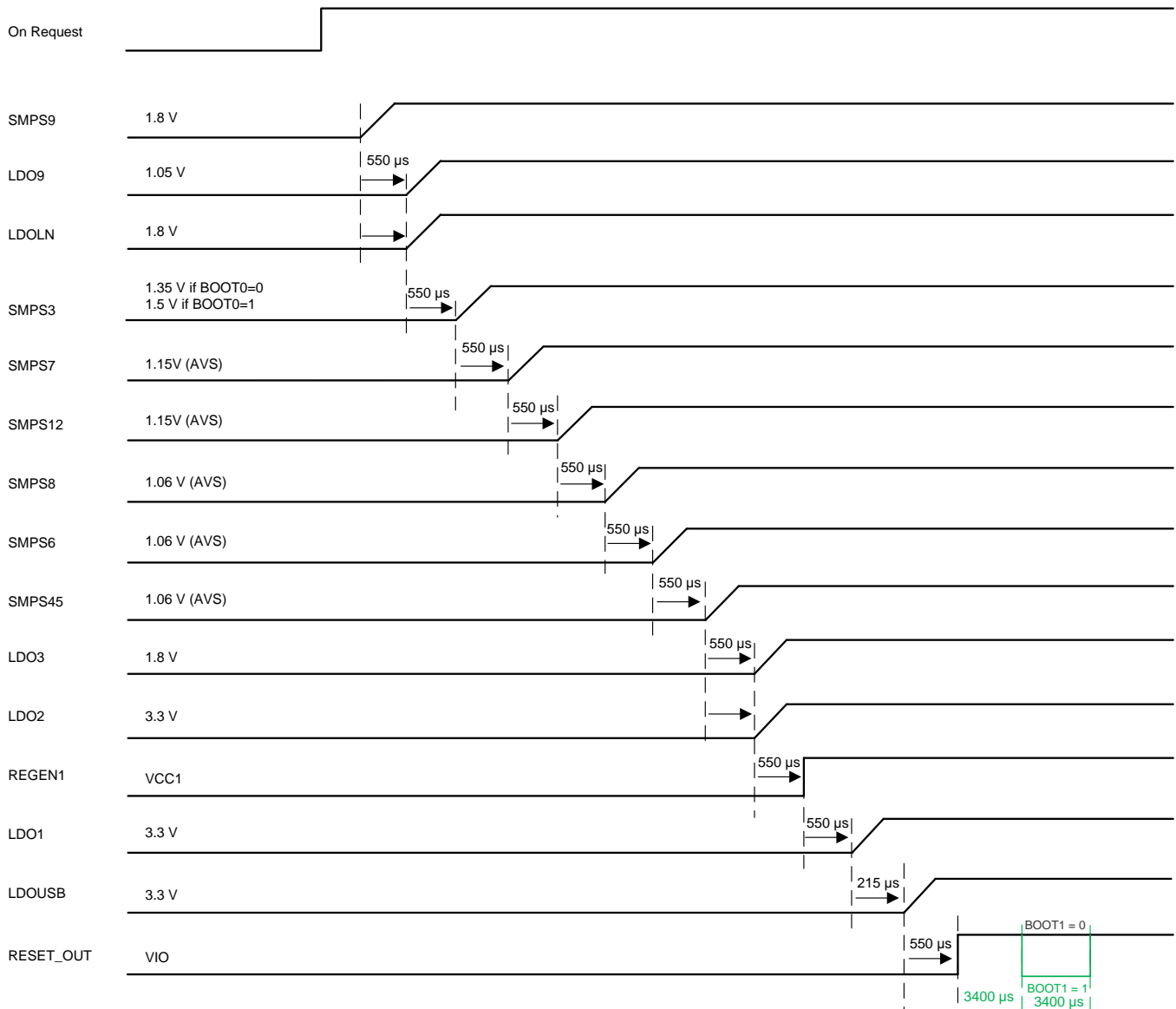
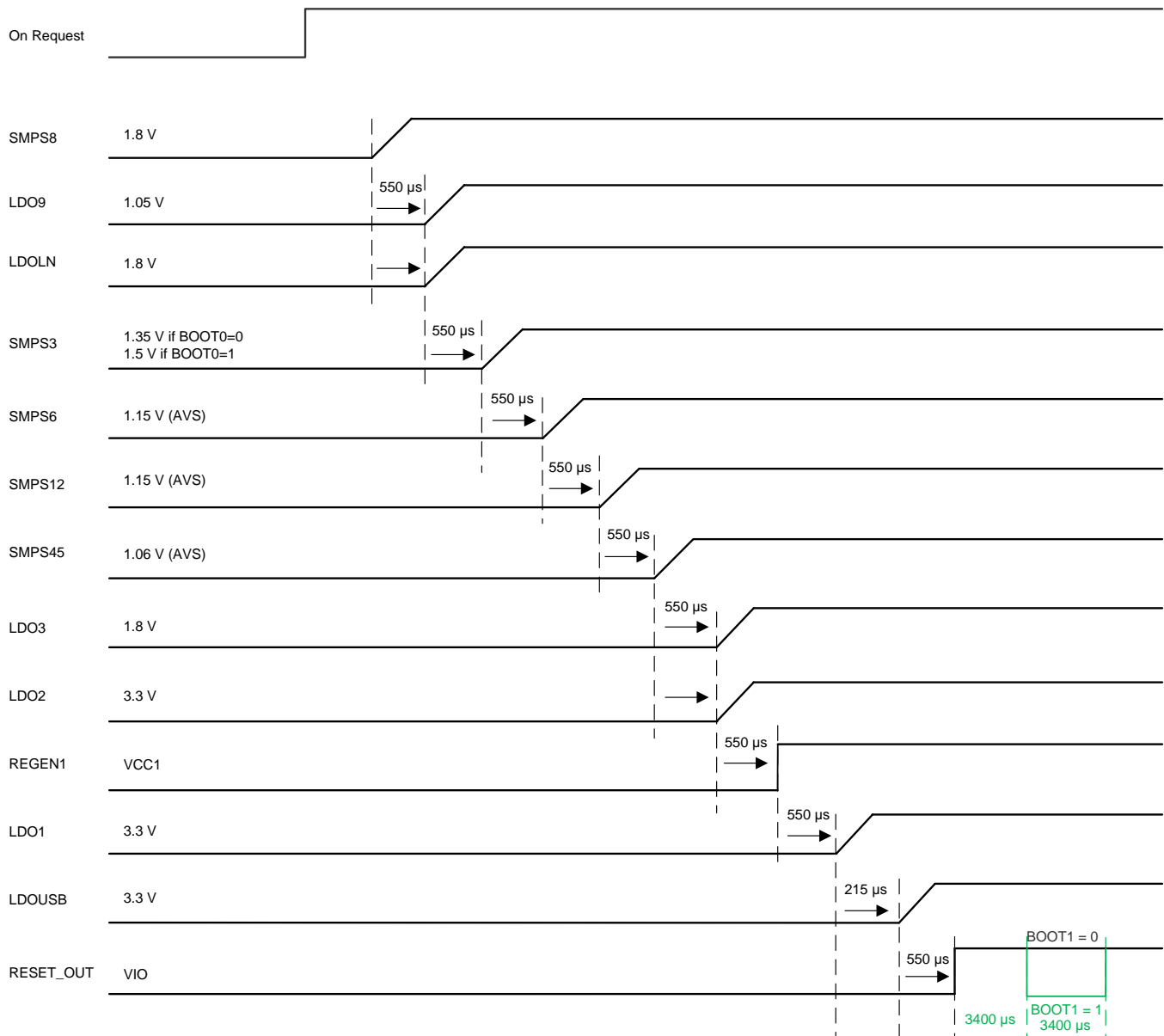


Figure 10. OFF2ACT Sequence of O9039A385IZWSRQ1

Figure 11 shows the OFF2ACT sequence of O9039A389IZWSRQ1. If the BOOT1 pin is connected to 1.8 V, then RESET\_OUT generates a high pulse of 3.4 ms, a low pulse of 3.4 ms, and then transitions high. If the BOOT1 pin is connected to 0 V, then RESET\_OUT generates one positive edge.



**Figure 11. OFF2ACT Sequence of O9039A389IZWSRQ1**

## 6.2 ACT2OFF Sequences

When an OFF request occurs during active mode, each resource is disabled based on the programmed ACT2OFF sequence. The ACT2OFF sequence of each device is the reverse of the OFF2ACT sequence, with the exception of the RESET\_OUT pulse, which does not appear in any ACT2OFF sequence.

## 6.3 ACT2SLP and SLP2ACT Sequences

When a SLEEP request occurs during active mode, each resource transitions to the sleep operating mode (MODE\_SLEEP bits of the corresponding CTRL register) based on the programmed ACT2SLP sequence. When a WAKE request occurs during sleep mode, each resource transitions to the active operating mode (MODE\_ACTIVE bits of the corresponding CTRL register) based on the programmed SLP2ACT sequence.

The following five steps must occur before a resource shuts off in sleep mode.

- Step 1. The NSLEEP pin must be unmasked through the POWER\_CTRL.NSLEEP\_MASK register bit
- Step 2. Each resource must be assigned to NSLEEP through the appropriate NSLEEP\_xxxx\_ASSIGN registers. For example, the NSLEEP\_SMPS\_ASSIGN register.
- Step 3. Each resource must be set to be OFF in sleep mode by clearing the MODE\_SLEEP bits of the appropriate xxxx\_CTRL register. For example, SMPS12\_CTRL register.
- Step 4. All interrupts must be cleared, because any pending interrupt prevents the PMIC from going to sleep mode.
- Step 5. A SLEEP request is generated through the NSLEEP pin.

OTP 0x89 automatically has the first three steps configured after startup. The user must only clear all interrupts and assert the NSLEEP pin low to transition the device to sleep mode with this OTP. For the other OTP versions, these commands must be sent to the PMIC through I<sup>2</sup>C before the device goes to SLEEP mode.

Note that RESET\_OUT and CLK32KGO are on the VIO domain, and therefore output the same voltage as VIO\_IN. When VIO\_IN is connected to SMPS9 or a switched 3.3V rail, then both RESET\_OUT and CLK32KGO will be shut off during sleep mode at the same time as VIO\_IN of the PMIC. If VIO\_IN remains supplied during sleep mode, then both RESET\_OUT and CLK32KGO will remain on.

Figure 12 shows the ACT2SLP and SLP2ACT sequences of O9039A387IZWSRQ1.

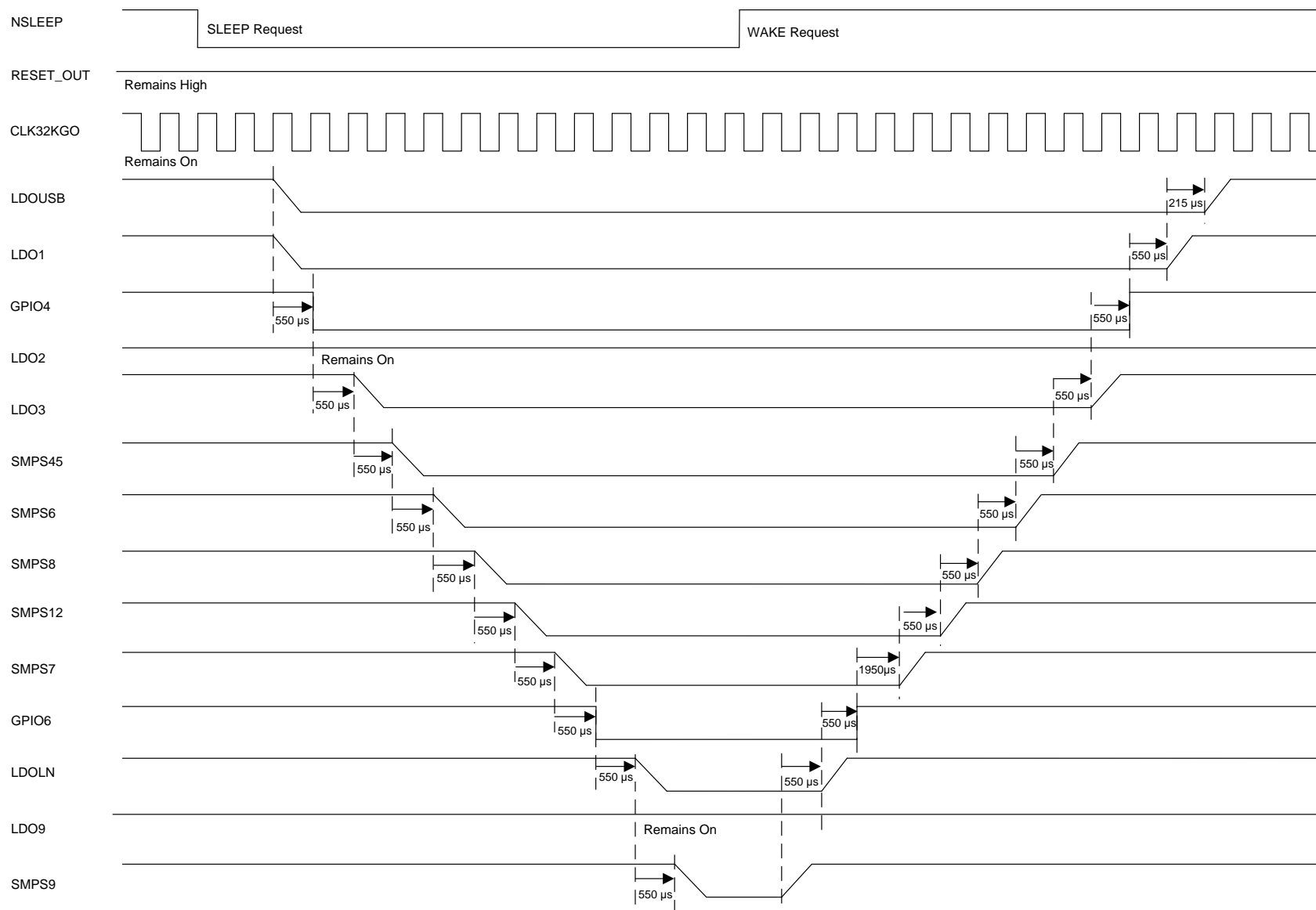


Figure 12. ACT2SLP and SLP2ACT Sequences of O9039A387IZWSRQ1

Figure 13 shows the ACT2SLP and SLP2ACT sequences of O9039A385IZWSRQ1.

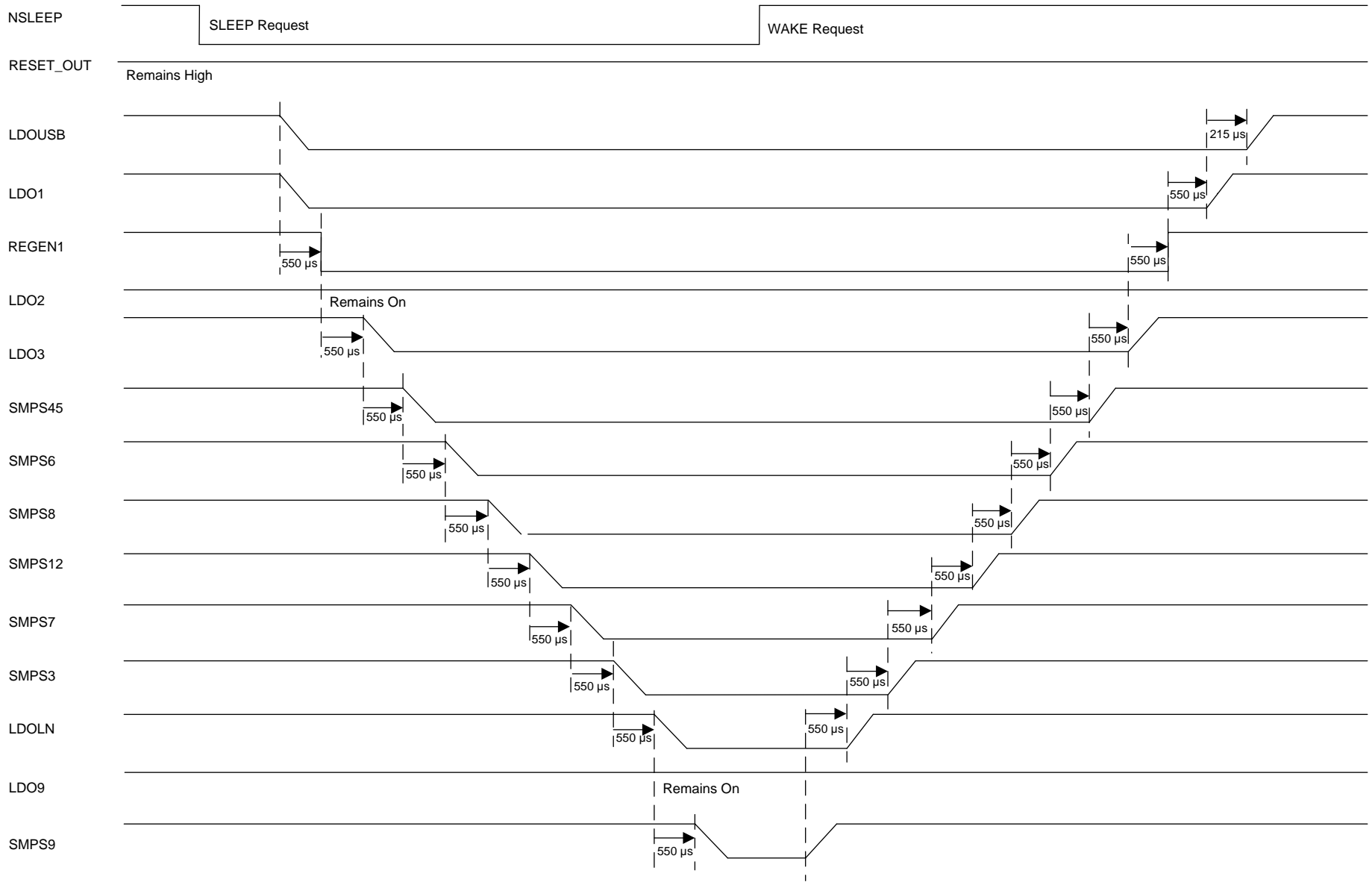


Figure 13. ACT2SLP and SLP2ACT Sequences of O9039A385IZWSRQ1

Figure 14 shows the ACT2SLP and SLP2ACT sequences of O9039A389IZWSRQ1.

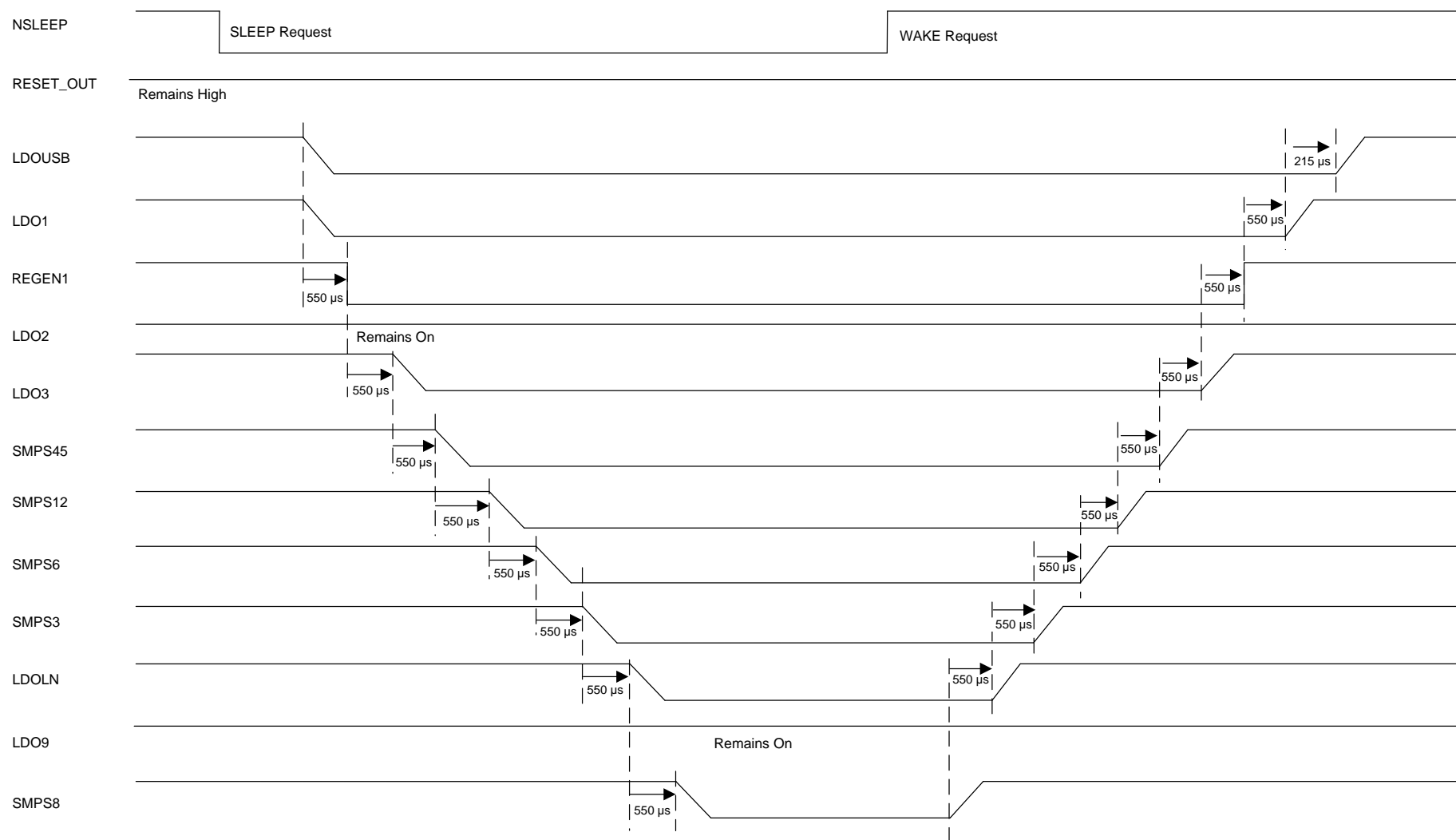


Figure 14. ACT2SLP and SLP2ACT Sequences of O9039A389IZWSRQ1

## 6.4 Warm Reset Sequences

A warm reset is triggered by the NRESWARM pin. During a warm reset, the OFF2ACT sequence is executed regardless of the actual state (ACTIVE, SLEEP) and the device returns to or remains in the ACTIVE state. Resources that are part of power-up sequence go to ACTIVE mode and the output voltage level is reloaded from OTP or kept in the previous value depending on the WR\_S bit in the SMPSx\_CTRL register or the LDOx\_CTRL register. Resources that are not part of the OFF2ACT sequence are not impacted by a warm reset and maintain the previous state. Depending on OTP version, if BOOT0 = 1 or BOOT1 = 1, then RESET\_OUT is asserted low during the warm reset sequence. If BOOT0 = 0 or BOOT1 = 0, RESET\_OUT is not asserted low.

If RESET\_OUT is asserted low during warm reset, then the PMIC must be enabled by the POWERHOLD (GPIO\_7) pin. If the PMIC will be enabled by the PWRON pin and kept on using the DEV\_ON bit, then RESET\_OUT must not be asserted low during warm reset. If POWERHOLD is set to GND and RESET\_OUT is asserted low during warm reset, the PMIC will shut off during the warm reset sequence.

Figure 15 shows the warm reset sequence of O9039A387IZWSRQ1. If any resource is on when NRESWARM is asserted, the resource remains on as shown by the solid black lines. The dashed red lines show the timing in case any resource is off before the warm reset. If VIO\_IN is switched off before the warm reset sequence, then GPIO\_4, GPIO\_6, and RESET\_OUT will be off because they are in the VIO domain. In this example, VIO\_IN is supplied by SMPS9, so RESET\_OUT follows the SMPS9 timing.

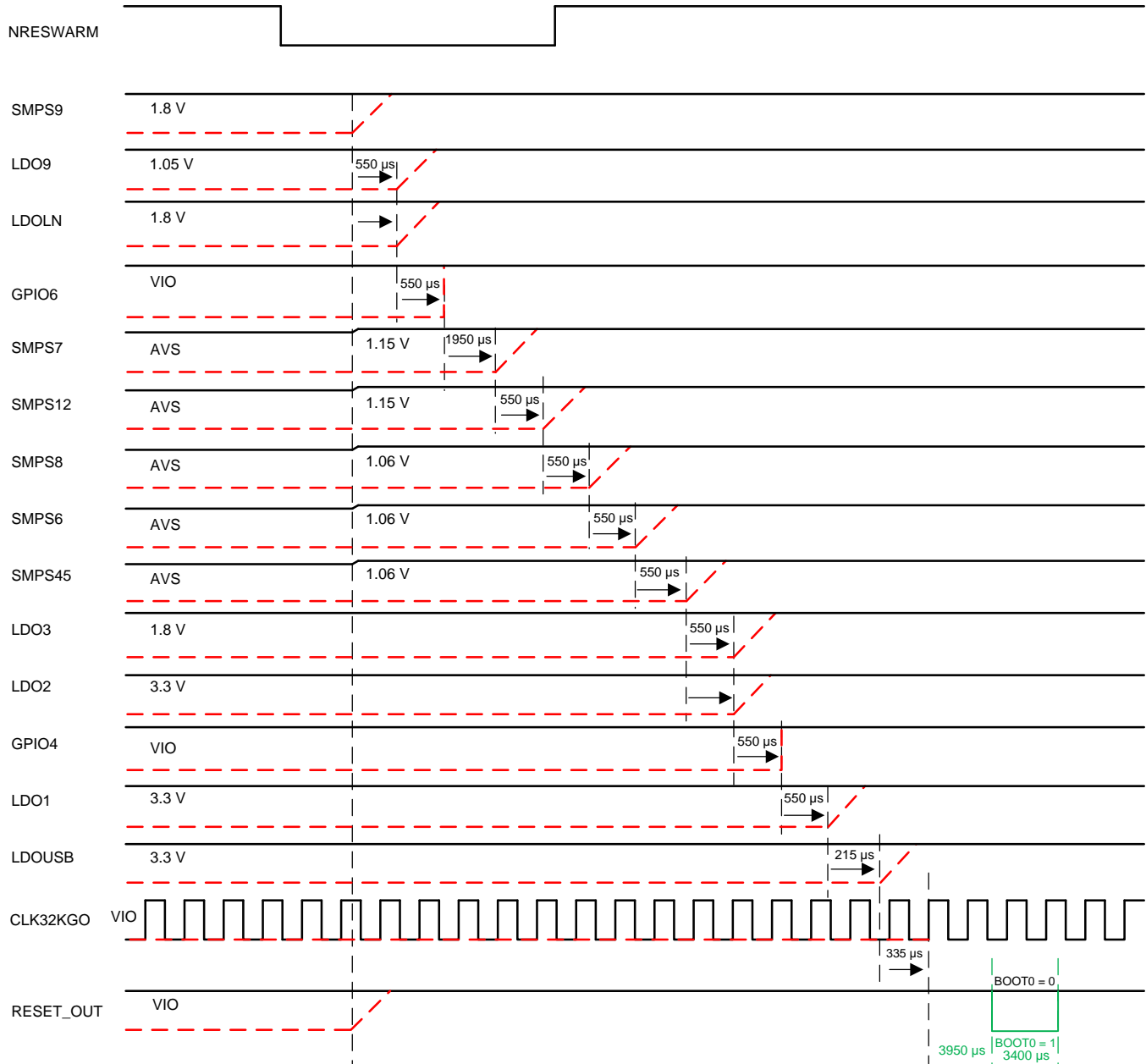


Figure 15. Warm Reset Sequence of O9039A387IZWSRQ1



Figure 16 shows the warm reset sequence of O9039A385IZWSRQ1. If any resource is on when NRESWARM is asserted, the resource remains on as shown by the solid black lines. The dashed red lines show the timing in case any resource is off before the warm reset. If VIO\_IN is switched off before the warm reset sequence, then RESET\_OUT will be off because it is in the VIO domain. In this example, VIO\_IN is supplied by SMPS9, so RESET\_OUT follows the SMPS9 timing.

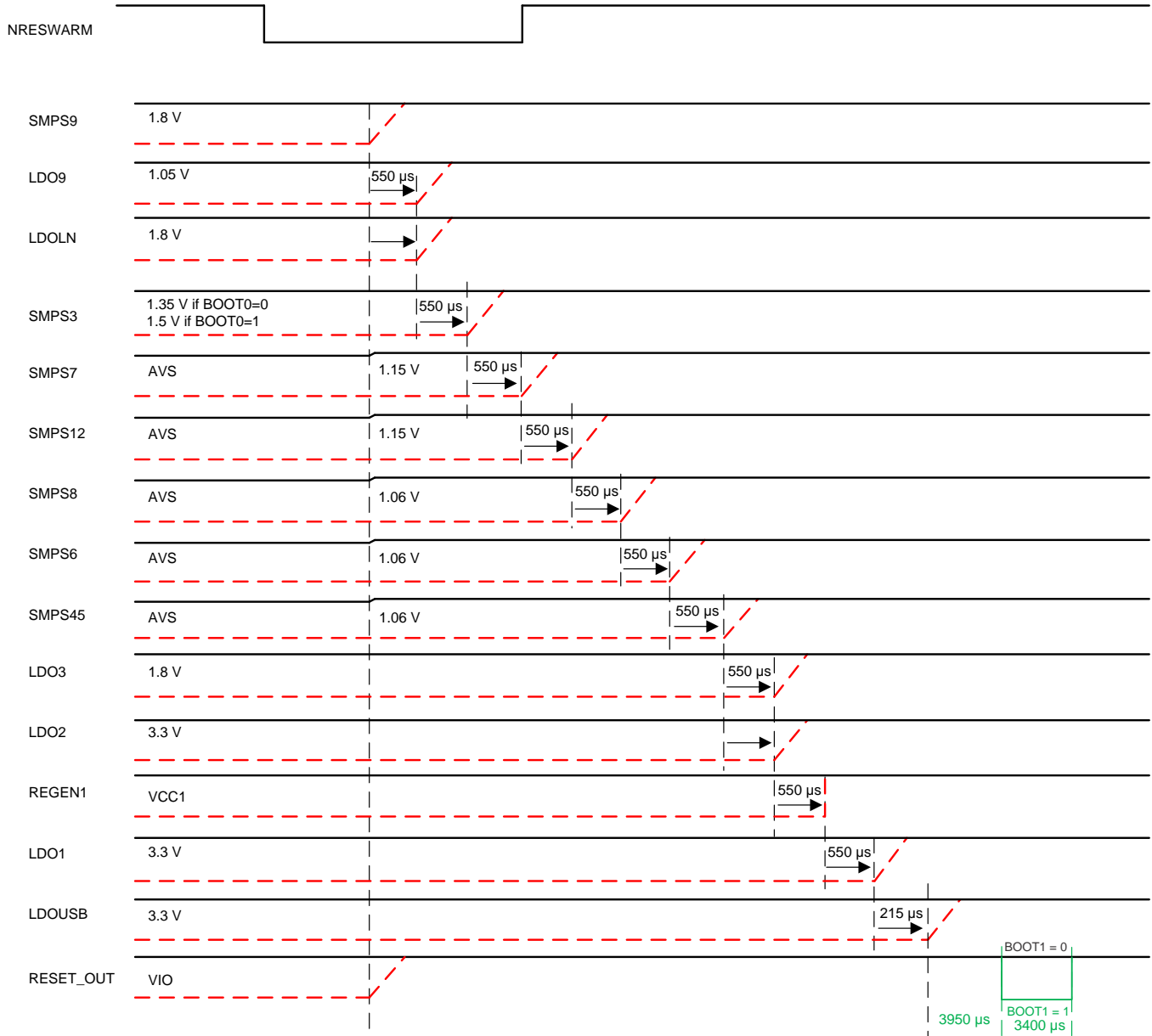


Figure 16. Warm Reset Sequence of O9039A385IZWSRQ1

Figure 17 shows the warm reset sequence of O9039A389IZWSRQ1. If any resource is on when NRESWARM is asserted, the resource remains on as shown by the solid black lines. The dashed red lines show the timing in case any resource is off before the warm reset. If VIO\_IN is switched off before the warm reset sequence, then RESET\_OUT will be off because it is in the VIO domain. In this example, VIO\_IN is supplied by SMPS8, so RESET\_OUT follows the SMPS8 timing.

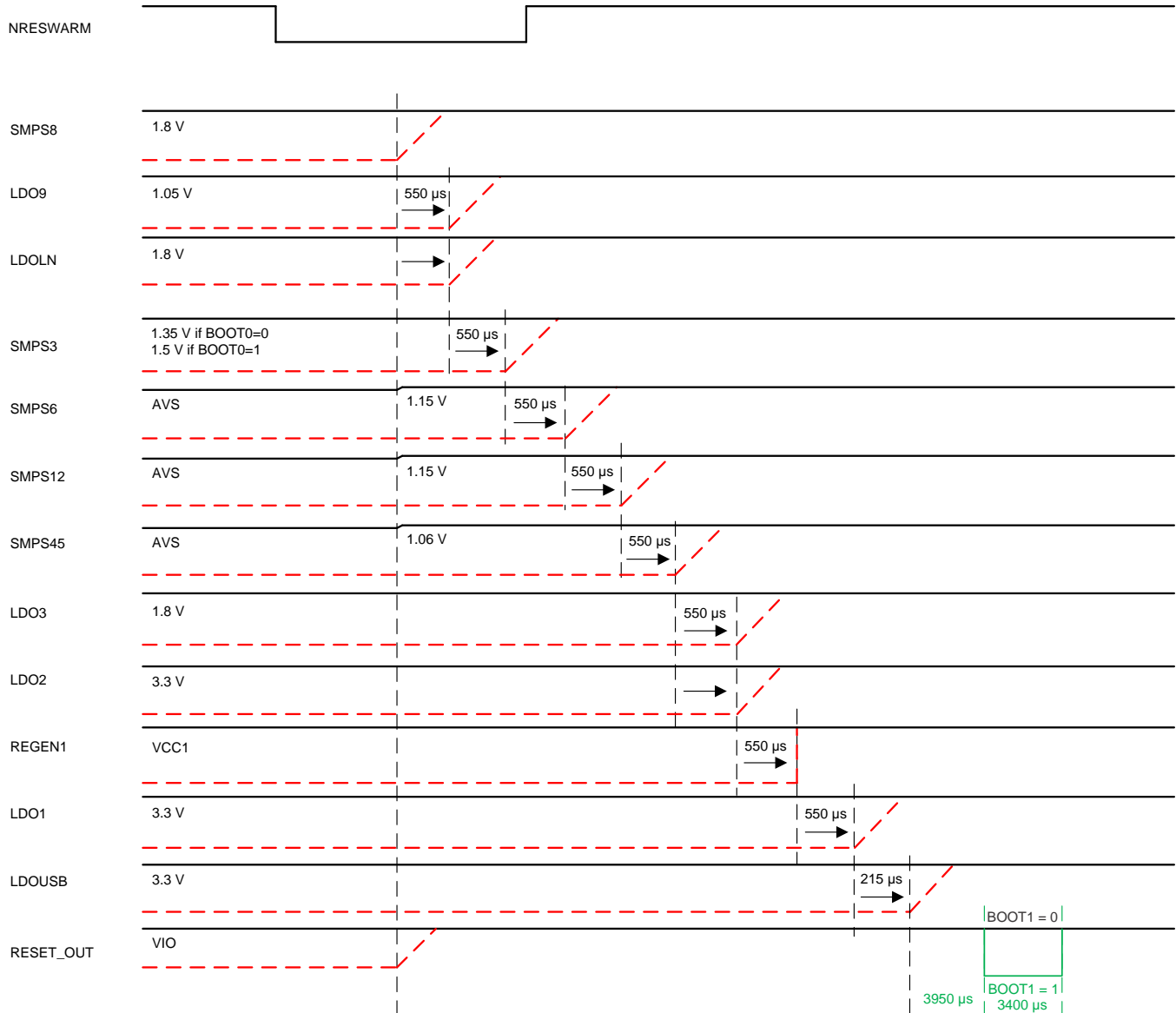


Figure 17. Warm Reset Sequence of O9039A389IZWSRQ1

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from B Revision (March 2017) to C Revision</b>	<b>Page</b>
• Added TPS65917-Q1 configurations and link to TPS65917-Q1 user's guide.....	3
• Added description of differences from older OTP versions.....	3
• Added information and diagrams on the two power up options for the TPS659039-Q1.....	6

<b>Changes from A Revision (December 2015) to B Revision</b>	<b>Page</b>
• First public release of document .....	3

<b>Changes from Original (January 2015) to A Revision</b>	<b>Page</b>
• Updated OTP versions from 0x44, 0x60, and 0x6B OTP versions to 0x87, 0x85, and 0x89 respectively with updated MPU and CORE boot voltages.....	3
• Deleted external charger control from SWORST registers.....	13
• Changed <i>CLK32KGAO</i> to <i>CLK32KGO</i> .....	16
• Changed <i>CLK32KGO domain</i> to <i>VIO domain</i> .....	16
• Changed the method of setting each resource to OFF in sleep mode from setting to clearing in the <i>ACT2SLP</i> and <i>SLP2ACT Sequences</i> section.....	19
• Added a description of the VIO signals in sleep mode when using a sequenced VIO supply .....	19
• Added <i>Warm Reset Sequences</i> section with description of warm reset behavior .....	23

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