TPS65910 User Guide for AM3517/AM3505 Processor

Application Report

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TPS65910 User Guide for AM3517/AM3505 Processor

ABSTRACT

This user's guide can be used as a reference for connectivity between the TPS65910 power-management integrated circuit (PMIC) and the AM3517/AM3505 processor.

1 Introduction

This user guide can be used as a reference for connectivity between the TPS65910 PMIC and the AM3517/AM3505 processor. For information about the power resources or the functionality of the device, see the device data sheet.

2 Platform Connection

Figure 1 shows the power supply connection between the TPS65910 PMIC and the AM3517/AM3505 processor.

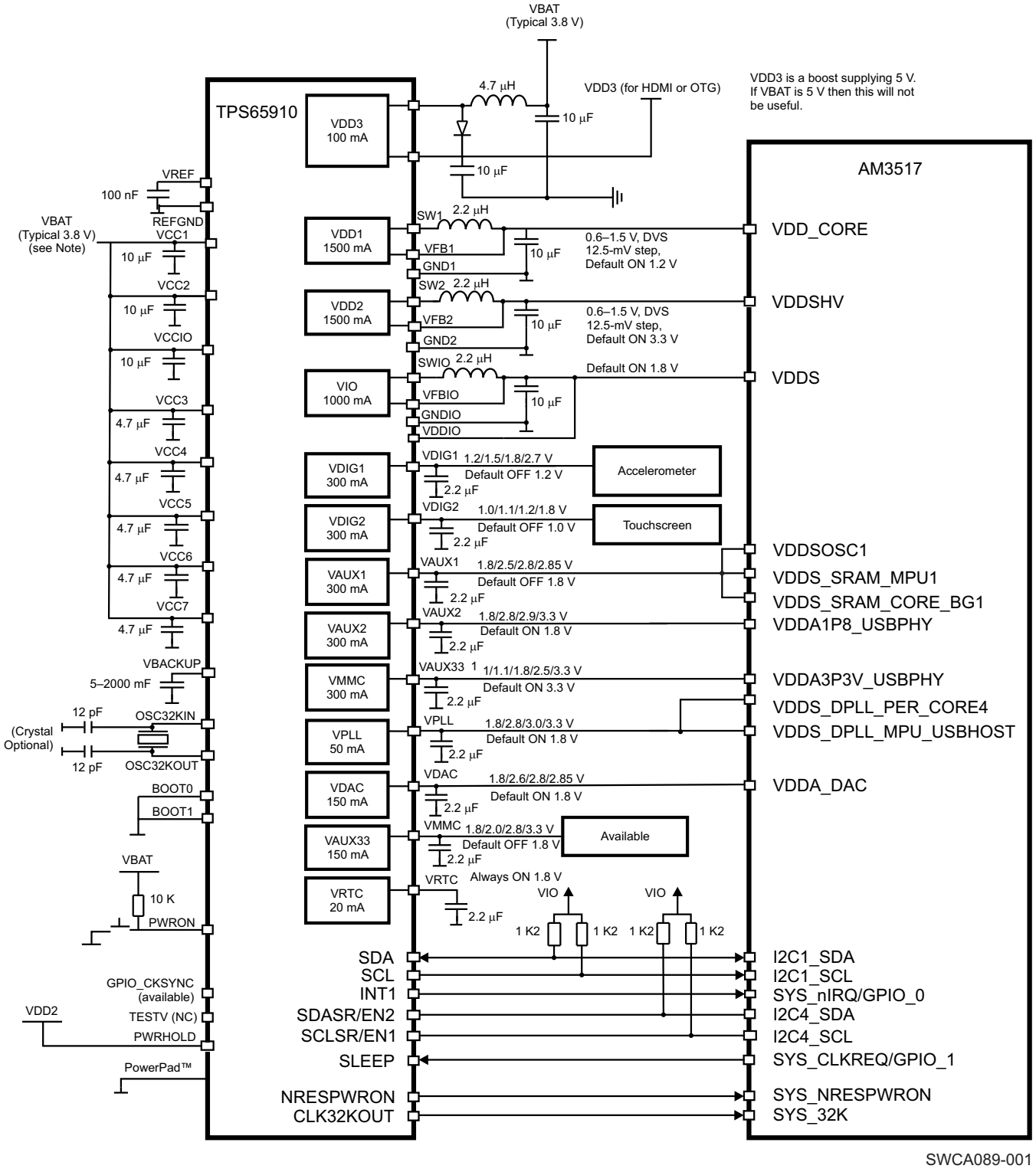

Figure 1. AM3517/AM3505 Power Supply Connection With TPS65910 (for I/O 3.3-V Operation)

NOTE: If 3.3-V operation is used, VBAT must be 4 V minimum for VDD2 SMPS to operate properly. If VDD2 is not required at 3.3 V, a lower VBAT is acceptable.

At power up, the maximum current capability (default setting) of the DCDC converters is as follows:

- VIO(max) = 500 mA
- VDD1(max) = 1000 mA
- VDD2(max) = 1000 mA

To have the maximum current capability, the user must program the following register bits:

- VIO_REG[ILMAX] = b01 for 1 A
- VDD1_REG[ILMAX] = b1 for 1.5 A
- VDD2_REG[ILMAX] = b1 for 1.5 A

3 Power-Up Sequencing

This section shows the power-up sequence for the TPS65910 power rails that match the power-up requirement for the AM3517/AM3505 processor. To power up the system, the user should press and release the PWRON switch on the platform. The PWRON switch is connected to the PWRON pad as shown in Figure 1.

The device can be operated in either 3.3-V or 1.8-V I/O operation. The power-up sequence in Figure 2 shows the 3.3-V I/O operation. For 1.8-V I/O operation, see note 3 in Table 1.

Figure 2 shows the power-up sequence for TPS65910 (where BOOT0 = 0 and BOOT1 = 0) for the AM3517/AM3505 processor.

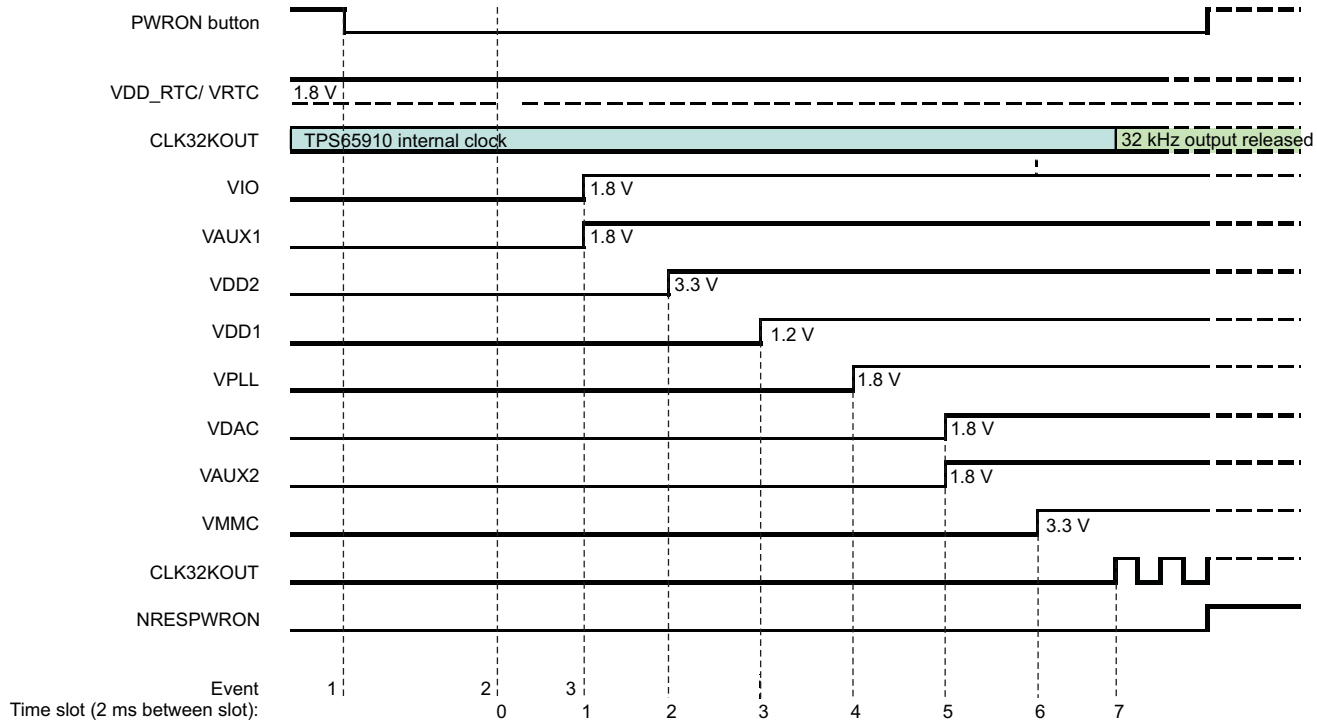

Figure 2. Power-Up Sequence for TPS65910

NOTE: For proper power up of the device, the PWRHOLD signal should be high after PWRON is pressed. For the AM3517/AM3505 configuration, PWRHOLD is connected to VDD2. PWRHOLD transitions to high when VDD2 powers up.

Table 1 lists the power domain mapping for TPS65910 and AM3517/AM3505.

Table 1. Power Domain Mapping(1)

TPS65910 POWER RESOURCE(2)	Imax (mA)	AM3517/AM3505 POWER DOMAIN(3)	Imax (mA)
VIO	1000	VDDS	200
VAUX1	300	VDDS_SRAM_CORE_BG	40
		VDDS_SRAM_MPU	40
		VDDOSC	20
VDD2 (for 3.3-V operation)	1500	VDDSHV	300
VDD1	1500	VDD_CORE	1500
VPLL	50	VDDS_DPLL_PER_CORE	25
		VDDSDPLL_MPU_USBHOST	25
VDAC	150	VDDA_DAC	65
VAUX2	300	VDDA1P8_USBPHY	50
VMMC	300	VDDA3P3V_USBPHY	10

(1) The power-up sequence for the boot mode (BOOT0 = 0 and BOOT1 = 0) is aligned with AM3517/AM3505.
(2) On TPS65910, the VIO and VAUX1 domains cannot be guaranteed to power up exactly at the same time, but there is no special requirement for timing of VDDS compared to VDD_SRAM, VDDOSC.
(3) If all I/Os are at 1.8 V, the VDDSHV domain of AM3517/AM3505 should be connected to VIO. In this case, VDD2 can be used for other system power, or software can disable it after the initial power-up sequence to save power.

Table 2 lists the default voltage levels for the power domains on TPS65910.

Table 2. TPS65910 Default Power Levels at Power Up

Power Domain on TPS65910	Voltage (V)
VDD1	1.2
VDD2	3.3
VIO	1.8
VDD3	Same as VBAT(1)
VDAC	1.8
VPLL	1.8
VAUX1	1.8
VAUX2	1.8
VMMC	3.3
VAUX33	0
VDIG1	0
VDIG2	0
VREF	0.85

(1) For VDD3 to function correctly, VAUX33 first must be enabled at 3.3 V, and then VDD3 should be enabled using the appropriate register settings.

Table 3 describes the EEPROM configuration for the TPS65910 power-up sequence where BOOT0 = BOOT1 = 0.

Table 3. EEPROM Configuration of TPS65910

Register	Bit	Description	Option Selected
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.2 V
VDD1_REG	VGAIN_SEL	VDD1 gain selection (x1 or x2)	x1
EEPROM		VDD1 time slot selection	3
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG/ VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.1 V
VDD2_REG	VGAIN_SEL	VDD2 gain selection (x1 or x3)	x3
EEPROM		VDD2 time slot selection	2
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	1
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled
EEPROM		VDD3 time slot	0
VDIG1_REG	SEL	LDO voltage selection	1.2 V
EEPROM		LDO time slot	0
VDIG2_REG	SEL	LDO voltage selection	1 V
EEPROM		LDO time slot	0
VDAC_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	5
VPLL_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	4
VAUX1_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	1
VMMC_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	6
VAUX33_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	0
VAUX2_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	5
CLK32KOUT pin		CLK32KOUT time slot	7
NRESPWRON pin		NRESPWRON time slot	7 + 1
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO is in low-power mode during OFF state. 1 = VRC LDO is in full-power mode during OFF state.	Low-power mode
DEVCTRL_REG	RTC_PWDN	0 = RTC in normal power mode 1 = Clock gating of RTC register and logic, low-power mode.	1
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is crystal/external clock. 1 = Clock source is internal RC oscillator.	Crystal
DEVCTRL2_REG	TSLOT_LENGTH	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	2 ms
DEVCTRL2_REG	IT_POL	0 = INT1 signal is active low. 1 = INT1 signal is active high.	Active low
INT_MSK_REG	VMBHI_IT_MSK	0 = Device automatically switches on at NOSUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = Start-up reason is required before switch on.	0 = Automatic switch on from supply insertion
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	3 V

4 Getting Started With TPS65910 and AM3517/AM3505

4.1 First Initialization

4.1.1 I/O Polarity/Muxing Configuration

To allow the SYS_CLKREQ signal from AM3517/AM3505 to control the SLEEP state of the device, set DEVCTRL2_REG[SLEEPSIG_POL] = 0 (active low, default). This can be set to active low or active high for SLEEP transition. The software configuration allows specific power resources to enter low-consumption state.

To allow SLEEP transition when requested, set DEVCTRL_REG.DEV_SLP = 1.

Update the GPIO0 configuration (GPIO0_REG) based on the platform requirement.

4.1.2 Define Wakeup/Interrupt Event (SLEEP or OFF)

To activate an interrupt to the processor on the INT1 line, select the appropriate bits in the INT_MSK_REG and INT_MSK2_REG registers.

4.1.3 Backup Battery Configuration

If a backup battery is used, set BBCH_REG[BBCHEN] = 1 to enable backup battery charging. The maximum voltage can be set based on the backup battery specifications (BBSEL).

4.1.4 DCDC and Voltage Scaling Resource Configuration

To configure two operating voltages for DCDC1 and DCDC2:

- VDDx_OP_REG.SEL = roof voltage (Enx ball high)
- VDDx_SR_REG.SEL = floor voltage (Enx ball low)

To assign control of DCDC1 to SCLSR_EN1 and DCDC2 to SCLSR_EN2:

- Set EN1_SMPS_ASS_REG.VDD1_EN1 = 1.
- Set EN2_SMPS_ASS_REG.VDD2_EN2 = 1.
- Set SLEEP_KEEP_RES_ON_REG.VDD2_KEEPON = 1 (allow low-power mode).
- Set SLEEP_KEEP_RES_ON_REG.VDD1_KEEPON = 1 (allow low-power mode).

4.1.5 Sleep Platform Configuration

Configure the state of the LDOs when the SLEEP signal is used. By default, all resources go to SLEEP state. In SLEEP state the LDO voltage is maintained but transient and load capability is reduced.

Resources that provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG register.

Resources that can be set off in SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG register.

4.2 Event Management Through Interrupt

4.2.1 INT_STS_REG.VMBHI_IT

INT_STS_REG.VMBHI_IT indicates that supply (VBAT) is connected. Leaving BACKUP or NO SUPPLY state, the system must be initialized (see Section 4.1, *First Initialization*).

4.2.2 INT_STS_REG.PWRON_IT

INT_STS_REG.PWRON_IT is triggered by pressing the PWRON button. If the device is in OFF or SLEEP state, then this acts as a wake-up event and resources are reinitialized.

4.2.3 INT_STS_REG.PWRON_LP_IT

INT_STS_REG.PWRON_LP_IT is the PWRON long-press interrupt and is generated when the PWRON switch is pressed for 6 seconds. The application processor can decide to acknowledge the interrupt. If this interrupt is not acknowledged in the next 2 seconds, then the device interprets this as a power-down event.

4.2.4 INT_STS_REG.HOTDIE_IT

INT_STS_REG.HOTDIE_IT indicates that the temperature of the die is reaching the limit. Software decreases power consumption before automatic shutdown.

4.2.5 INT_STS_REG.VMBDCH_IT

INT_STS_REG.VMBDCH_IT indicates that the input supply is low and the processor must prepare a shutdown to avoid losing data.

This interrupt is linked to VBAT but does not apply in a system in which the PMIC is connected to 5-V rails and not connected directly to VBAT.

4.2.6 INT_STS2_REG.GPIO_R/F_IT

The INT_STS2_REG.GPIO_R/F_IT GPIO interrupt event can be used to wake up the device from SLEEP state. This can be an interrupt coming from any peripheral or similar device. This wake-up event is not valid for a transition from OFF state.

4.2.7 INT_STS_REG.RTC_ALARM_IT

INT_STS_REG.RTC_ALARM_IT is triggered when the RTC alarm set time is reached.

Revision History

Changes from A Revision (January 2011) to B Revision **Page**

- Updated VAUX2 to 300 mA in Figure 1 5
- Corrected the Imax values to 300 for VAUX2 and VMMC 7
- VDD2_OP_REG/VDD2_SR_REG Option Selected: Replace 3.3 V by 1.1 V 8
- VDIG1_REG Option Selected: Replace N/A by 1.2 V 8
- VDIG2_REG Option Selected: Replace N/A by 1 V 8
- VAUX33_REG Option Selected: Replace N/A by 1.8 V 8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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