Technical Article
If Someone Offered You Same Video Quality for Half the Data Rate, Would You Take It?

TEXAS INSTRUMENTS

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Because that's the promise of High Efficiency Video Coding or HEVC. Also known as H.265, this is the follow-on of the H.264 / MPEG-4 Advanced Video Coding (AVC) standard. HEVC provides the same video quality but reduces the data bandwidth by up to 50 percent. This makes HEVC not only well suited for transporting SD content, but also for higher resolution and frame rate HD and UltraHD video, including 4K video at 60fps.

HEVC is an efficient but processing intensive video standard, with encoding complexity 5x to 10x that of H.264 and decoding complexity of 2x compared to H.264. This means significant processing horsepower is needed and has to be enabled in a viable power envelope for commercial and consumer systems. TI's TMS320C6678 eight core DSP capable of delivering 320GMACs and 160 GFLOPs in just 10W goes a long way in alleviating the performance issue without breaking the power-budget bank.

Another thing to note is that standards such as the ones defined for H.265 typically specify the decoding process and do not specify how encoding is implemented. It is left to the encoding system designer to consider performance/ delay/ power tradeoffs and generate a conforming bit stream. Also, just like with H.264, HEVC standard evolution can be expected over the next several years to include improvements targeting specific problem domains and / or market segments. Therefore, an important factor to consider when choosing an encoder solution and the associated processing platform is its flexibility in enabling solutions. In this regard, DSP-optimized encoding seems to provide a happy medium between a general purpose processor and hardwired solution such as an ASIC / FPGA.

To showcase the ease of implementation on TI processors, TI has recently launched a TI Design for HEVC. This free design shows how a power efficient, soft H.265 / HEVC solution, that scales across resolutions, frame rates and profiles, can be implemented in real-time using one or more C6678 DSPs. A specific use case of a single channel HEVC 720p30 real-time encoder and single channel HEVC 1080p60 real-time decoder is also included. The design includes schematics, design files, and a bill of materials for TI's TMDSEVM6678 board, as well as free software including TI's C66x optimized HEVC encoder and decoder, TI's Multicore Software Development Kit (MCSDK) framework and other software packages. TI's feature rich HEVC encoder delivers a bitrate savings of about 40 percent compared with existing H.264x encoders, all while supporting a variety of resolutions, profiles, and frame rates.

Check out more of the various configurations supported, performance benchmarks and board level power estimates in the design guide that accompanies the HEVC TI Design. We'd love to hear your views on HEVC, its adoption and any head winds it faces in the face of growing video traffic.

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