

# LDO Basics: Noise – How a Noise-reduction Pin Improves System Performance



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In the article, “[LDO basics: power supply rejection ratio](#),” Aaron Paxton discussed using a low-dropout regulator (LDO) to filter ripple voltage arising from switched-mode power supplies. That isn’t the only consideration for achieving a clean DC power supply, however. Because LDOs are electronic devices, they generate a certain amount of noise of their own accord. Selecting a low-noise LDO and taking steps to reduce internal noise are integral to generating clean supply rails that won’t compromise system performance.

## Identifying Noise

The ideal LDO would generate a voltage rail with no AC elements. Unfortunately, LDOs generate their own noise like other electronic devices. [Figure 1](#) shows how this noise manifests in the time domain.

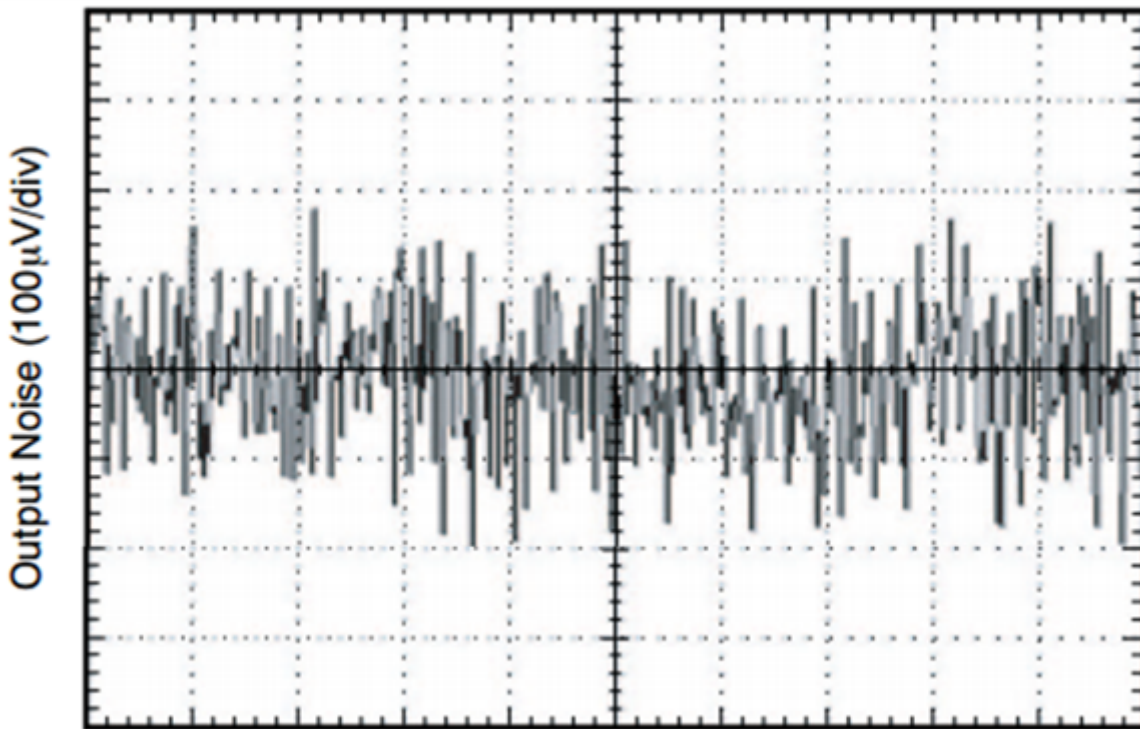
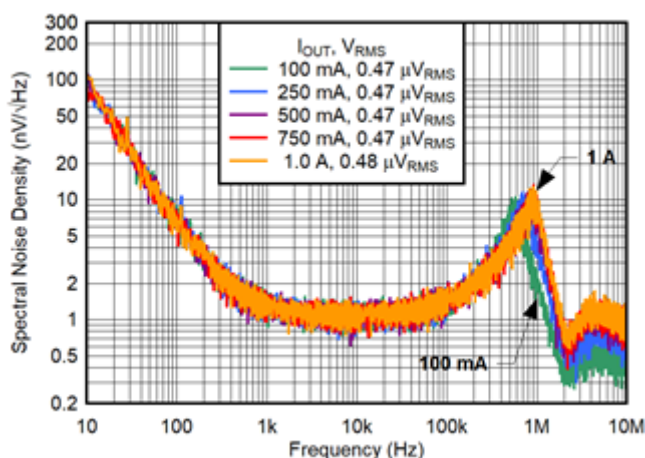


Figure 1. Scope Shot of a Noisy Power Supply

Analysis in the time domain is difficult. Therefore, there are two main ways to examine noise: across frequency and as an integrated value.

You can use a spectrum analyzer to identify the various AC elements at the output of the LDO. The application report, “[How to Measure LDO Noise](#),” covers noise measurements extensively.

[Figure 2](#) plots output noise for a 1-A low-noise LDO, the [TPS7A94](#).



**Figure 2. Noise Spectral Density of the TPS7A94 vs. Frequency and  $V_{OUT}$**

As you can see from the various curves, output noise, represented in microvolts per square root hertz ( $\mu\text{V}/\sqrt{\text{Hz}}$ ), is concentrated at the lower end of the frequency spectrum. This noise mostly emanates from the internal reference voltage, but the error amplifier, field-effect transistor (FET) and resistor divider also contribute.

It's helpful to look at output noise across frequency when determining the noise profile for a frequency range of interest. For example, audio application designers care about audible frequencies (20 Hz to 20 kHz) where power-supply noise might degrade sound quality.

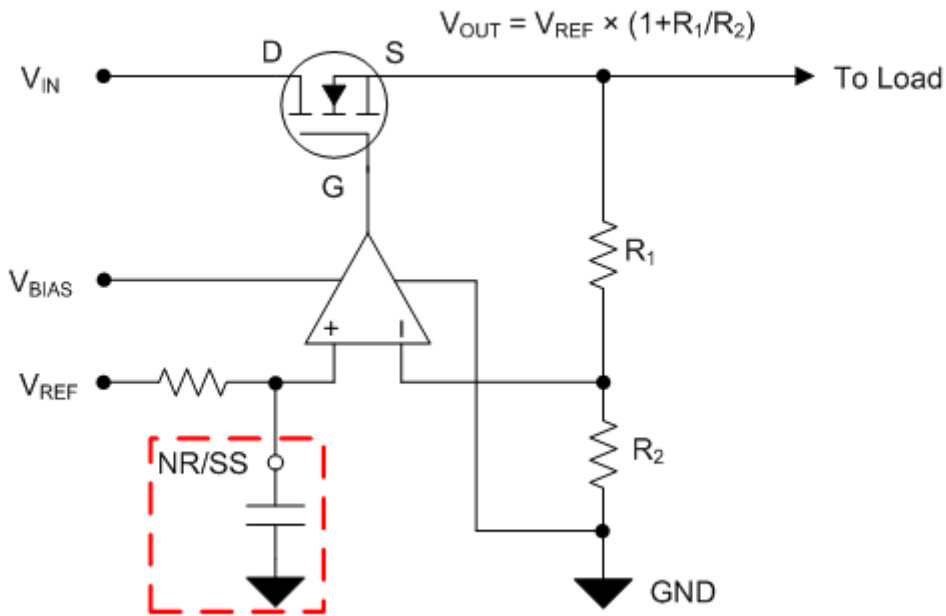
Data sheets commonly provide a single, integrated noise value for apples-to-apples comparisons. Output noise is often integrated from 10 Hz to 100 kHz and is represented in microvolts root mean square ( $\mu\text{V}_{\text{RMS}}$ ). Some semiconductor manufacturers integrate noise from 100 Hz to 100 kHz or a custom frequency range. Integrating over a select frequency range can help mask unflattering noise properties, so it's important to examine the noise curves in addition to the integrated value. Figure 2 shows integrated noise values that correspond with the various curves. Texas Instruments features a [portfolio of LDOs](#) whose integrated noise values measure as low as  $0.47 \mu\text{V}_{\text{RMS}}$ .

## Reducing Noise

In addition to selecting an LDO with low-noise qualities, you can also employ a couple of techniques to ensure that your LDO has the lowest noise characteristics. These involve the use of noise-reduction and feed-forward capacitors, discussed in the article, "[LDO basics: noise – how a feed-forward capacitor improves system performance.](#)"

## Noise-reduction Capacitors

Many low-noise LDOs in the TI portfolio have a special pin designated as "NR/SS." Figure 3 shows a common topology used to implement the noise-reduction feature.

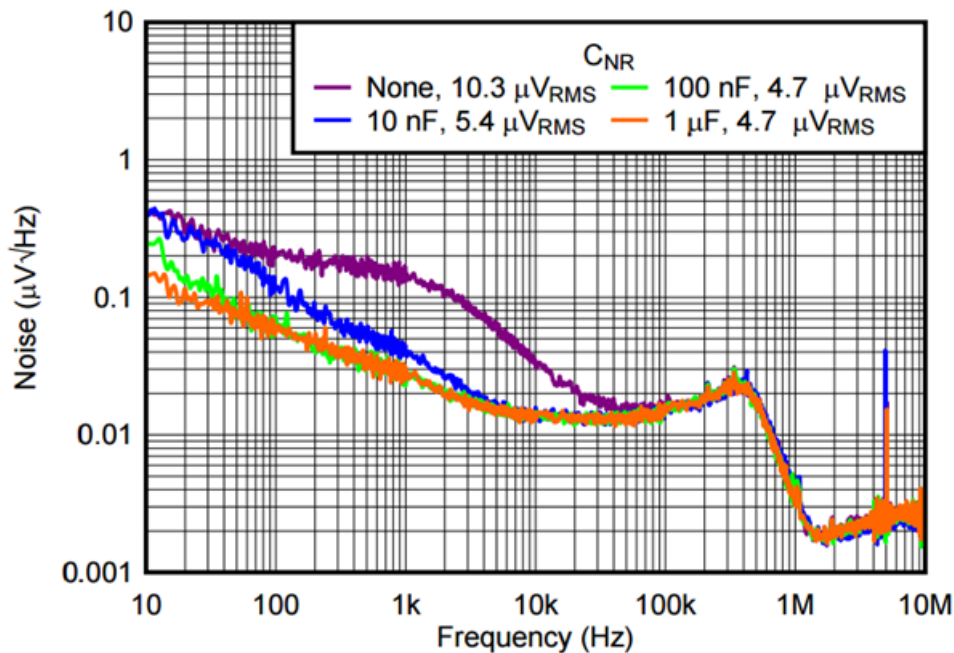


**Figure 3. An NMOS LDO with an NR/SS Pin**

The function of this pin is twofold. It's used to filter noise emanating from the internal voltage reference and to either slow the slew rate during startup or enable the LDO.

Adding a capacitor at this pin ( $C_{NR/SS}$ ) forms a resistor-capacitor (RC) filter with internal resistance, helping shunt undesirable noise generated by the voltage reference. Since the voltage reference is the main contributor to noise, increasing the capacitance helps push the cutoff frequency of the low-pass filter to lower frequencies.

Figure 4 shows the effect of this capacitor on output noise.



**Figure 4. Noise Spectral Density of the TPS7A91 vs. Frequency and  $C_{NR/SS}$**

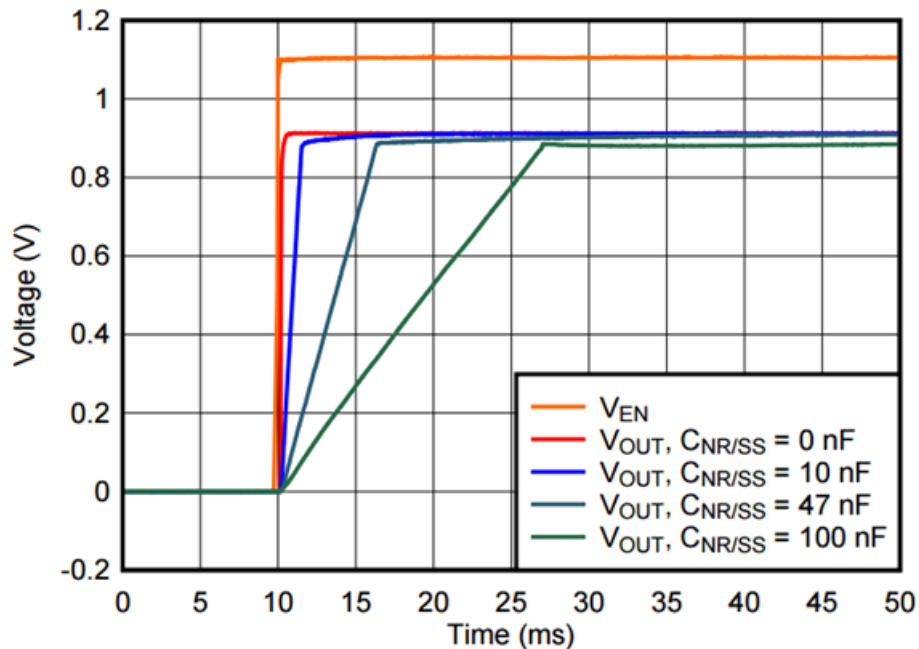
As Figure 4 shows, a greater value of  $C_{NR/SS}$  yields better noise figures. At a certain point, increasing the capacitance will no longer reduce noise. The remaining noise emanates from the error amplifier, FET, etc.

Adding a capacitor also introduces an RC delay during startup, which causes the output voltage to ramp at a slower rate. This is advantageous when bulk capacitance is present at the output or load and you need to mitigate the inrush current.

Equation 1 expresses inrush current as:

$$I_{inrush} = (C_{OUT} + C_{LOAD}) \frac{dV}{dt}$$

In order to reduce inrush current, you must either lower the output capacitance or lower the slew rate. Fortunately, a  $C_{NR/SS}$  helps achieve the latter, as [Figure 5](#) shows for the [TPS7A85](#).



**Figure 5. Startup of the TPS7A85 vs.  $C_{NR/SS}$**

As you can see, increasing  $C_{NR/SS}$  values results in longer startup times, preventing inrush current from spiking and potentially triggering a current-limit event. Note that some LDOs with an NR pin do not implement a soft-start feature. They implement a quick-start circuit, which helps achieve minimal startup times even with large noise-reduction capacitors.

## Summary

Low-noise LDOs are critical to ensuring a clean DC power supply. It is important to both select an LDO with low-noise properties and implement techniques to ensure the cleanest output possible. Using a  $C_{NR/SS}$  has two benefits: it enables you to control the slew rate and filter reference noise. For more tips on designing with LDOs, check out other articles in the [LDO basics series](#).

## Additional Resources

- Watch the “[LDO Basics](#)” [video series](#) for trainings about LDO dropout voltage, current limit, power-supply rejection ratio, noise and thermals.
- Download the [quick reference guide](#) of popular LDOs and linear voltage regulators for a wide variety of applications, including industrial, personal electronics, communications equipment and automotive.

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