*EVM User's Guide: TMDSCNCD263-PMIC*

# *AM263x Control Card with PMIC and Automotive Ethernet*

## Description

The AM263x Control Card Evaluation Module (EVM) is an evaluation and development board for the Texas Instruments Sitara™ AM263x series of microcontrollers (MCUs). This EVM provides an easy way to start developing on the AM263x MCUs with on-board emulation for programming and debugging as well as buttons and LEDs for a simple user interface. This version of the AM263x Control Card (TMDSCNCD263-PMIC) has all of the qualities of the original AM263x Control Card (TMDSCNCD263) while also incorporating a PMIC power solution and replacing two of the Industrial Ethernet PHYs plus RJ45 connectors with Automotive Ethernet PHYs plus MATEnet connectors. The control card also enables header pin access to key signals through the use of a high speed edge connector (HSEC) baseboard docking station for rapid prototyping.

## Features

- **Integrated power and safety monitoring solution that is consistent with the ISO26262 ASIL-D specification**
  - **Multirail Power Supply designed for Safety-Relevant Applications**
  - **Automotive, dual-channel voltage supervisor with very-high accuracy**
- **Two MATEnet connectors with on-board Automotive Ethernet PHYs**
- One RJ45 ethernet port with on-board Industrial Ethernet PHY
- PCB dimensions: 131.15 mm width by 92.81 mm length + 6.17 mm length of HSEC interface
- Powered through 5 V, 3 A USB type-C input
- On-board XDS110 debug probe
- 180 pin HSEC interface for rapid prototyping
- Three push buttons:
  - PORz
  - User interrupt
  - RESETz
- LEDs for:
  - Power status
  - User testing
  - Ethernet connection
  - I2C driven array
- CAN connectivity with on-board CAN transceiver
- LIN connectivity with on-board LIN transceiver
- Dedicated FSI connector
- TI Test Automation Header
- MMC interface to micro SD card connector
- On-board memory
  - 128 MB QSPI Flash
  - 1 MB I2C EEPROM

# 1 Evaluation Module Overview

## Preface: Read This First

### 1.1.1 Sitara™ MCU+ Academy

Texas Instruments™ offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

### 1.1.2 If You Need Assistance

If you have any feedback or questions, support for the Sitara™ MCUs and the AM263x Control Card development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in the Section 6.1.

### 1.1.3 Important Usage Notes

**Note**

The TMDSCNCD263-PMIC has software examples and drivers in a one-time SDK release. For more information on the installation of the SDK, refer to Section 3.1.

**Note**

The TMDSCNCD263-PMIC E1 design has various hardware modifications to make sure of proper operation of the EVM. For additional details of all modifications, refer to Section 5.2.

**Note**

The AM263x Control Card requires a 5 V, 3 A power supply to function. While a USB type-C cable is included, a 5 V, 3 A power supply is not included in the kit and must be ordered separately. For more information, refer to Section 2.3.

**Note**

TMDSCNCD263-PMIC includes a PMIC and Boost regulator, U30 and U182 which can exceed 55°C case temperature during normal operation. This user guide's statement and the PCB warning sticker from the table below have been added to alert users to these higher temperature components.

| | | |
|---|---|---|
|  | Caution | Caution hot surface.<br>Contact can cause burns.<br>Do not touch! |

**Note**

External Power Supply or Power Accessory Requirements:

- Nominal output voltage: 5-VDC
- Max output current: 3000 mA
- Efficiency Level V

**Note**

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, etc.

## 1.1 Introduction

The original AM263x Control Card (TMDSCNCD263) was developed to enable easy and rapid prototyping of the AM263x and all of the peripherals. The changes between the original Control Card and this specific version, TMDSCNCD263-PMIC, is showcased in Table 1-1.

**Table 1-1. Control Card Differences**

| Subsystem | TMDSCNCD263 | TMDSCNCD263-PMIC | TMDSCNCD263-PMIC Part Number |
|---|---|---|---|
| Power | Discrete power | Power Management Integrated Chip (PMIC) | *O3850QDCARQ1* |
| Voltage Supervisor | N/A | 1x Automotive, multichannel window supervisor with very-high accuracy for 1.2 V and 3.3 V supply rails | *TPS37042A3OFDDFRQ1* |
| Ethernet | 3x Industrial Ethernet PHYs with RJ45 connectors | 1x Industrial Ethernet PHY with RJ45 Connector | *DP83826ERHBT* |
| | | 2x Automotive Ethernet PHY with MATEnet connectors | *DP83TG720SWRHARQ1* |

This EVM supports integrated power and safety monitoring that is consistent with ISO26262 ASIL-D by using a PMIC designed for safety-relevant applications as well as an independent, automotive-grade voltage supervisor.

The Control Card described in this user guide has an E1 and E2 revision. The E1 revision of the Control Card requires Hardware modifications for proper use. The E1 design Hardware Modifications are described in Section 5.2. The E2 Design files serve as a reference for the proper implementation of the PMIC with the AM263x. Design files for both E1 and E2 versions of the TMDSCNCD263-PMIC can be found in Section 4.

## 1.2 Kit Contents

The Sitara AM263x Control Card development kit contains the following items:

- AM263x Sitara series control card development board
- Type-A to Micro-B USB cable (1 meter length)
- USB Type-C Cable (1 meter length)

**Note**

The maximum length of the IO cables shall not exceed 3 meters.

Not included:

- HSEC 180-pin Baseboard Docking Station
- Standoffs
- USB Type-C 5-V/3-A AC/DC supply and cable

## 1.3 Specification

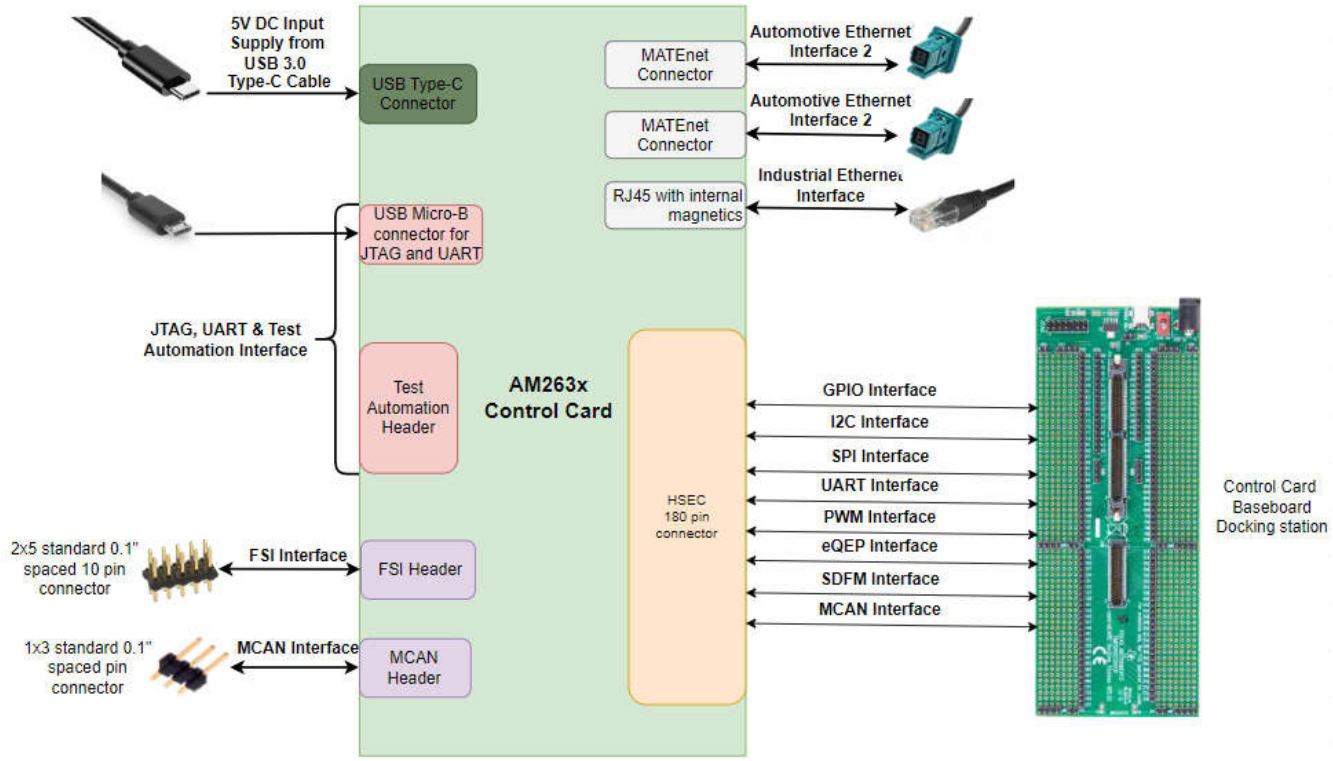



**Figure 1-1. System Architecture**

## 1.4 Device Information

The AM263x Sitara™ Arm® Microcontrollers are built to meet the complex real-time processing needs of next generation industrial and automotive embedded products. The AM263x MCU family consists of multiple pin-to-pin compatible devices with up to four 400 MHz Arm® Cortex®-R5F cores. As an option, the Arm® R5F subsystem can be programmed to run in lockstep or dual-core mode for multiple functional safety configurations. The industrial communications subsystem (PRU-ICSS) enables integrated industrial Ethernet communication protocols such as PROFINET®, TSN, Ethernet/IP®, EtherCAT® (among many others), standard Ethernet connectivity, and even custom I/O interfaces. The family is designed for the future of motor control and digital power applications with advanced analog sensing and digital actuation modules.

The multiple R5F cores are arranged in cluster subsystems with 256KB of shared tightly coupled memory (TCM) along with 2MB of shared SRAM, greatly reducing the need for external memory. Extensive ECC is included for on-chip memories, peripherals, and interconnects for enhanced reliability. Granular firewalls managed by the Hardware Security Manager (HSM) enable developers to implement stringent security-minded system design requirements. Cryptographic acceleration and secure boot are also available on AM263x devices.

For additional information about the AM263x, refer to either the data sheet: *AM263x Sitara™ Microcontrollers Data Sheet* or the Technical Reference Manual: *AM263x Sitara™ Microcontrollers Technical Reference Manual*.

## 1.5 HSEC 180-pin Control Card Docking Station

The *TMDSHSECDOCK 180-pin docking station* is available for purchase through Texas Instruments. The docking station is a baseboard that enables rapid prototyping. There is a power switch on the docking station that determines whether power to the Control Card is supplied by the 5 V connector or the USB connector.

**Note**

The docking station power switch must be toggled to the EXT-ON side to meet the power requirements of the AM263x Control Card. EXT-ON indicates that the power is being sourced from the Barrell connector of the Control Card Dock. The mini-USB (USB-ON) connector does not meet the power requirements of the AM263x Control Card.

The AM263x Control Card has a power mux (TPS2121RUXT) that supplies power from the type-C connection, as long as the voltage supplied by the type-C connection is equal to or greater than the voltage supplied by the HSEC docking station. Therefore, if both a type-C connection is present and the Control Card is connected to a powered HSEC docking station, then the power mux routes the type-C supplied voltage to VMAIN of the Control Card. If there is no type-C connection and voltage is being supplied through the HSEC docking station, then the power mux routes that voltage to VMAIN of the Control Card.

For more information on the docking station, refer to the *180-Pin Docking Station Informational Guide*.

## 1.6 Security

The AM263x Control Card features a High Security, Field Securable (HS-FS) device. An HS-FS device has the ability to use a one time programming to convert the device from HS-FS to High Security, Security Enforced (HS-SE).

The AM263x device leaves the TI factory in an HS-FS state where customer keys are not programmed and has the following attributes:

- Does not enforce the secure boot process
- M4 JTAG port is closed
- R5 JTAG port is open
- Security Subsystem firewalls are closed
- SoC Firewalls are open
- ROM Boot expects a TI signed binary (encryption is optional)
- TIFS-MCU binary is signed by the TI private key

The One Time Programmable (OTP) keyrwriter converts the secure device from HS-FS to HS-SE. The OTP keywriter programs customer keys into the device eFustes to enforce secure boot and establish a root of trust. The secure boot requires an image to be encrypted (optional) and signed using customer keys, which is verified by the SoC. A secure device in the HS-SE state has the following attributes:

- M4, R5 JTAG ports are both closed
- Security Subsystems and SoC Firewalls are both closed
- TIFS-MCU and SBL need to be signed with active customer key

# 2 Hardware

## 2.1 Functional Block Diagram

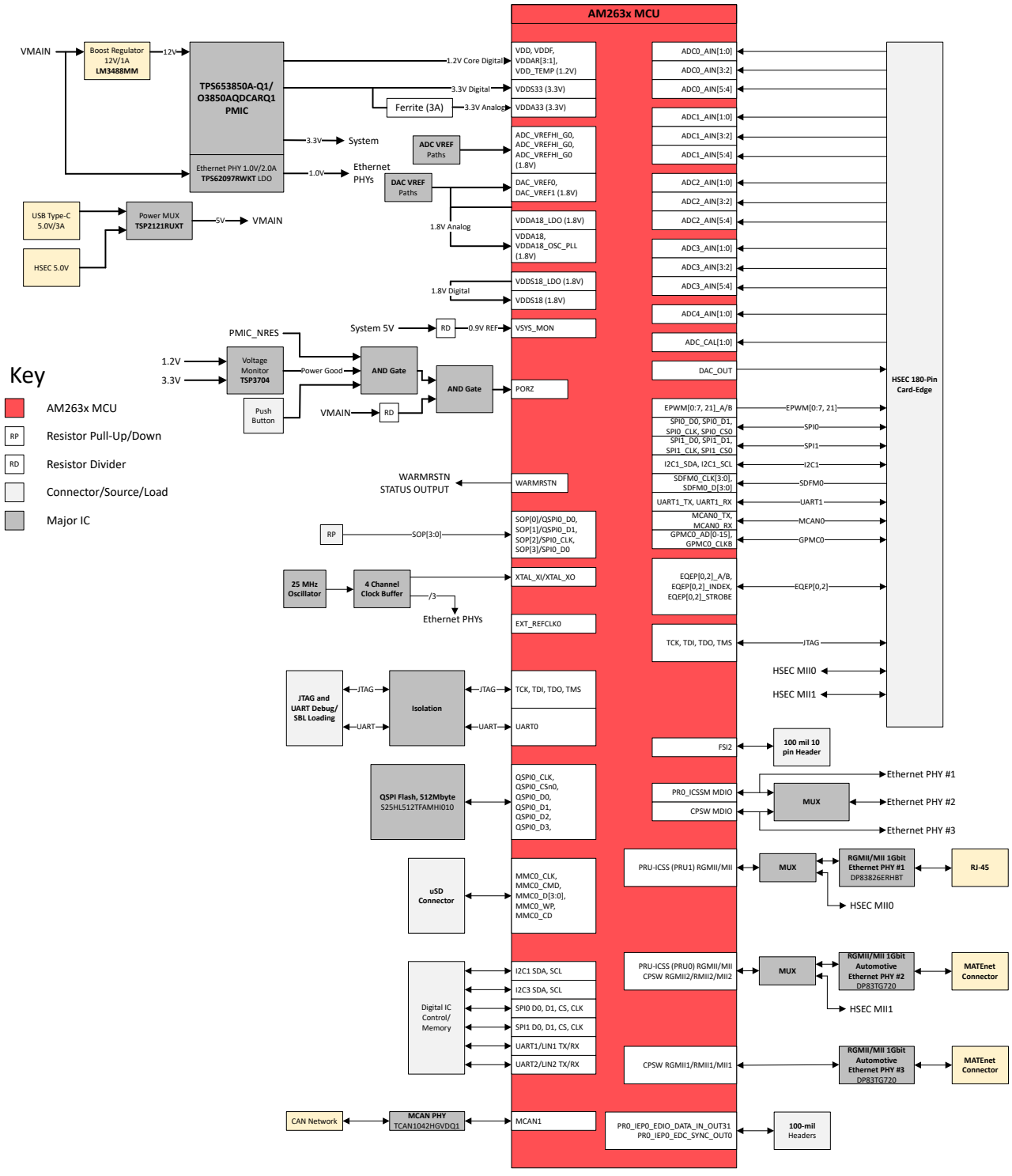



**Figure 2-1. AM263x Control Card Block Diagram**

## 2.2 Component Identification

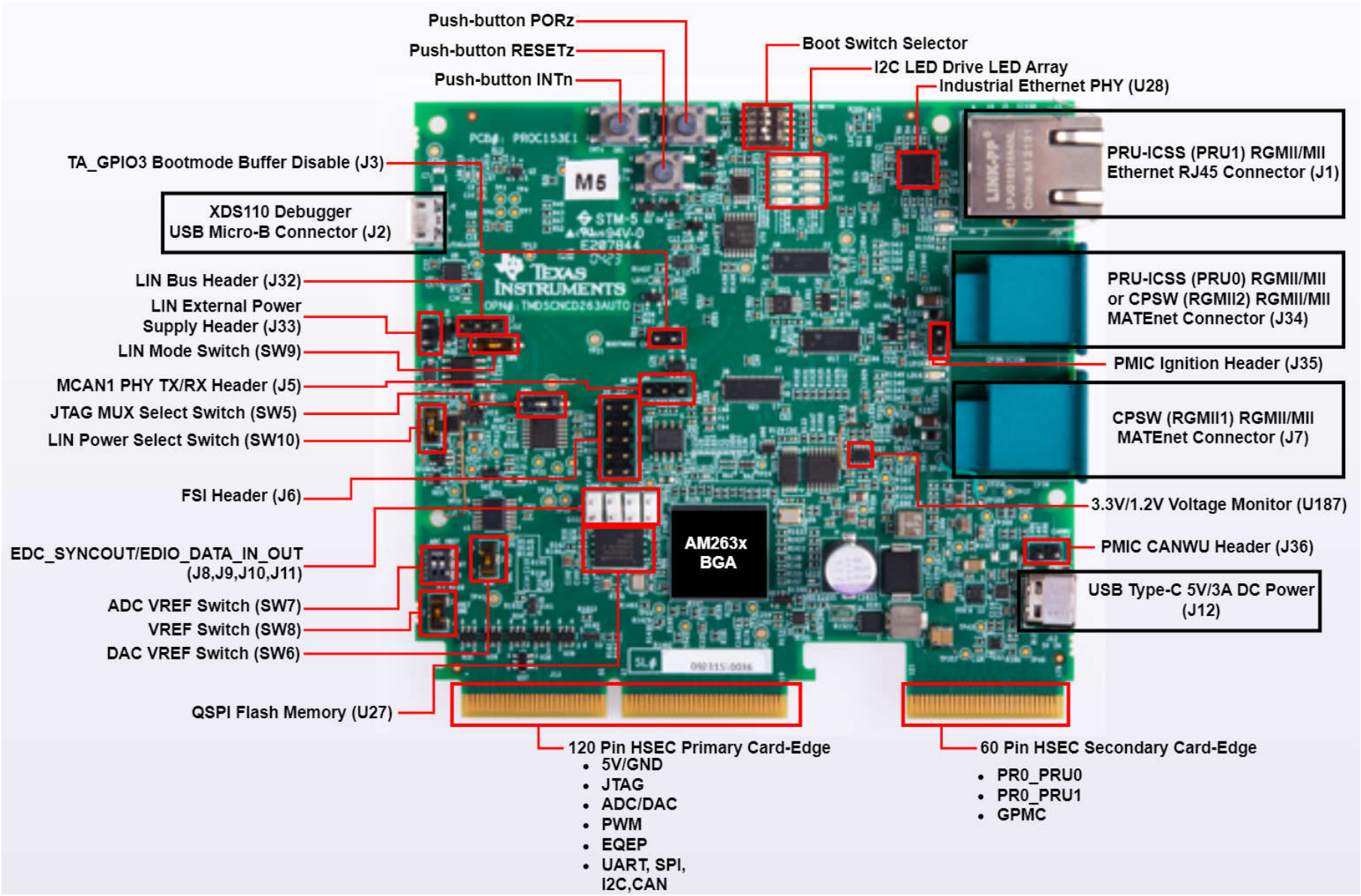



**Figure 2-2. Component Identification Front**

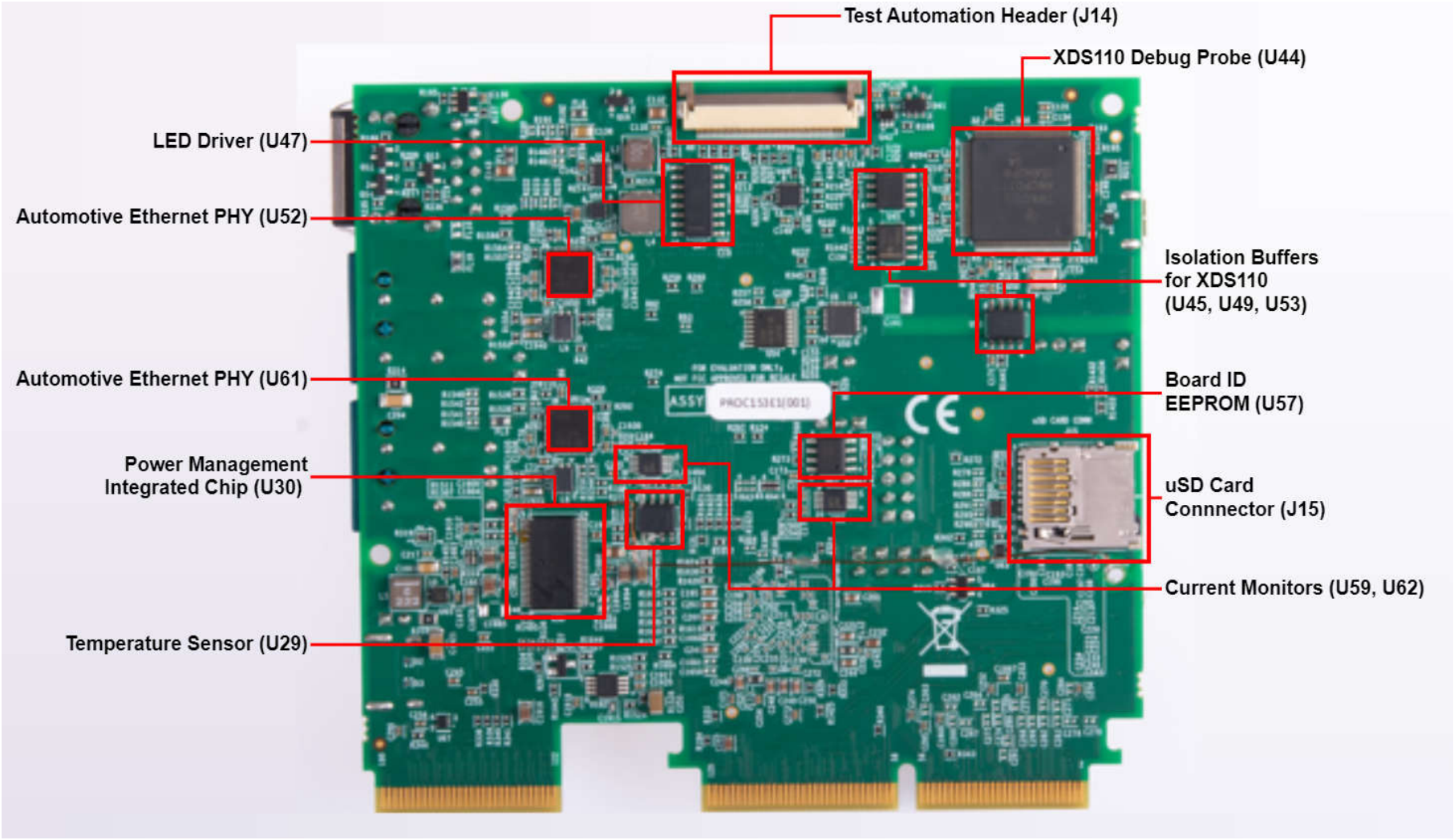



**Figure 2-3. Component Identification Back**

## 2.3 Power Requirements

The AM263x Control Card is powered from a 5 V, 3 A USB type-C input or from a 5 V, 3 A HSEC connection supplied by the docking station. The following sections describe the power distribution network topology that supplies the AM263x Control Card, supporting components, and the reference voltages.

Power supply solutions that are compatible with the AM263x Control Card:

- When using the USB type-C input:
  - 5 V, 3 A power adapter with USB-C receptacle
  - 5 V, 3 A power adapter with captive USB-C cable
  - PC USB type-C port that has Power Delivery classification
    - Thunderbolt
    - Battery behind USB logo

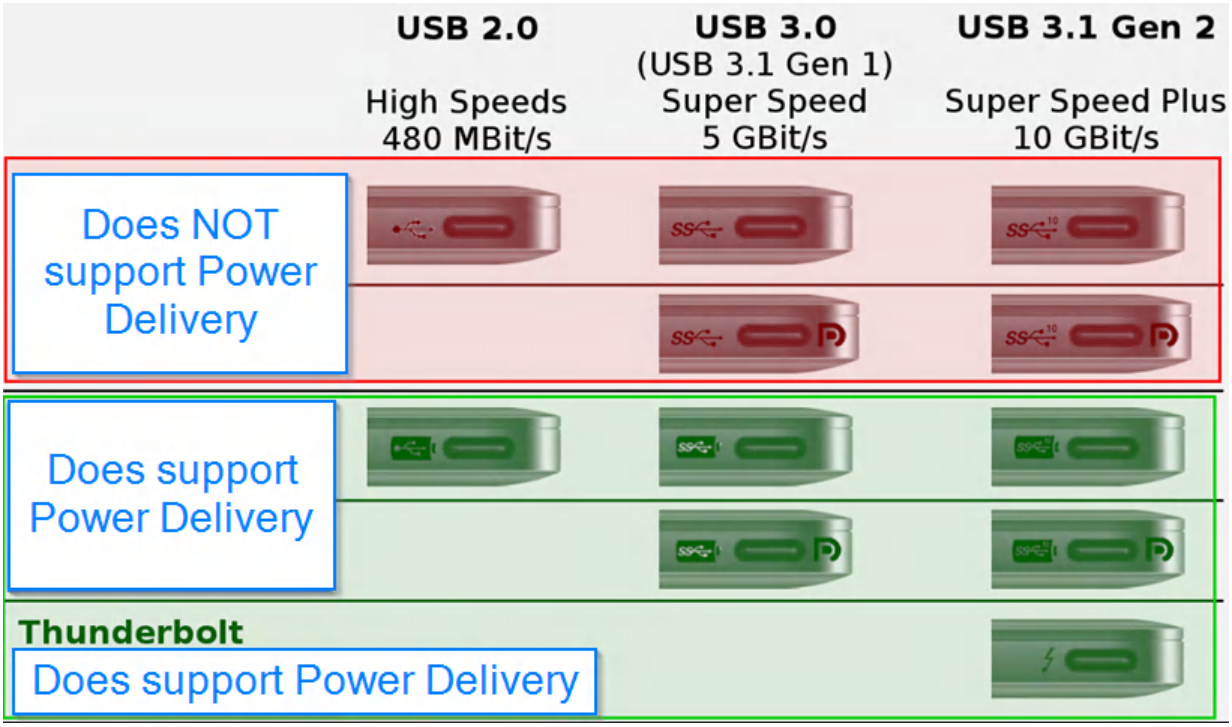



**Figure 2-4. USB Type-C Power Delivery Classification**

- When using the HSEC DC barrel jack power input:
  - A power adapter that is at least 15 W

Power supply solutions that are **NOT** compatible with the AM263x Control Card:

- When using USB type-C input:
  - Any USB adapter cables such as:
    - Type-A to type-C
    - micro-B to type-C
    - DC barrel jack to type-C
  - 5 V, 1.5 A power adapter with USB-C captive cable or receptacle
  - PC USB type-C port not capable of 3 A

### 2.3.1 Power Input Using USB Type-C Connector

The AM263x Control Card can be powered through a USB type-C connection. The USB Type-C source is capable of providing 3 A at 5 V and advertises the current sourcing capability through the CC1 and CC2 signals. On this EVM, the CC1 and CC2 from the USB type-C connector are interfaced to the port controller IC (TUSB320LAIRWBR). This device uses the CC pins to determine port attach/detach, cable orientation, role

detection, and port control for Type-C current mode. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected.

The Port pin is pulled down to ground with a resistor to configure the IC in upward facing port (UFP) mode. VBUS detection is implemented to determine a successful attach in upward facing port (UFP) mode. The OUT1 and OUT2 pins are connected to a NOR gate. Active low on both the OUT1 and OUT2 pins advertises high current (3A) in the attached state which enables the load switch (TPS22965DSGT) to provide the VBUS_MAIN supply which powers other regulators that create the power rails for the device.

In UFP mode, the port controller IC constantly presents pull-down resistors on both CC pins. The port controller IC also monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected downward facing port (DFP). The port controller IC de-bounces the CC pins and waits for VBUS detection before successfully attaching. As a UFP, the port controller device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs.

The power requirement for AM263x Control Card is 5 V at 3 A. If the source is not capable of providing the required power, then the output at the NOR gate becomes low, disabling the VBUS_MAIN power switch. Therefore, if the power requirement is not met, then all power supplies except VSYS_TA_3V3 remain in an off state. The board gets powered on completely only when the source can provide 5 V at 3 A.

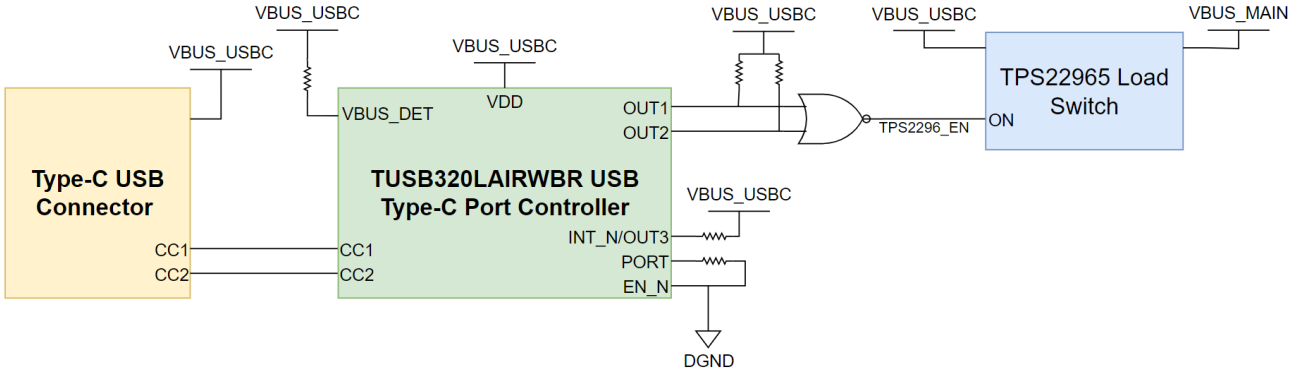



**Figure 2-5. Type-C CC Configuration**

**Table 2-1. Current Sourcing Capability and State of USB Type-C Cable**

| OUT1 | OUT2 | Advertisement |
|---|---|---|
| H | H | Default current in unattached state |
| H | L | Default current in attached state |
| L | H | Medium current (1.5A) in attached state |
| L | L | High current (3.0A) in attached state |

The AM263x Control Card includes a power source based on a Power Management Integrated Chip (PMIC) for each of the power rails. During the initial stage of the power supply, 5 V supplied by the type-C USB connector is used to generate all of the necessary voltages required by the PMIC and subsequently the rest of the board via the PMIC LDO outputs. For more information about the PMIC, refer to Section 2.3.5.

### 2.3.2 Power Status LEDs

Multiple power-indication LEDs are provided on-board to indicate to users the output status of major supplies. The LEDs indicate power across various domains as shown in the table below.

**Table 2-2. Power Status LEDs**

| Name | Default Status | Operation | Function |
|---|---|---|---|
| LD16 | OFF | SAFETY_ERROR | Power error indication for voltage - VUSB_5V0 |
| LD17 | ON | VMAIN_12V0 | Power indicator for voltage - VMAIN_12V0 |
| LD15 | ON | VSYS_3V3A | Power indicator for voltage - VSYS_3V3A |
| LD14 | ON | VSYS_1V2_PG | Power indicator for voltage -VSYS_1V2_PG |
| LD1 | ON | VSYS_TA_3V3 | Power indicator for voltage -VSYS_TA_3V3 |
| LD6 | OFF | XDS110_PROG_STAZ2 | LED glows after XDS configuration |
| LD7 | OFF | XDS110_PROG_STAZ1 | |

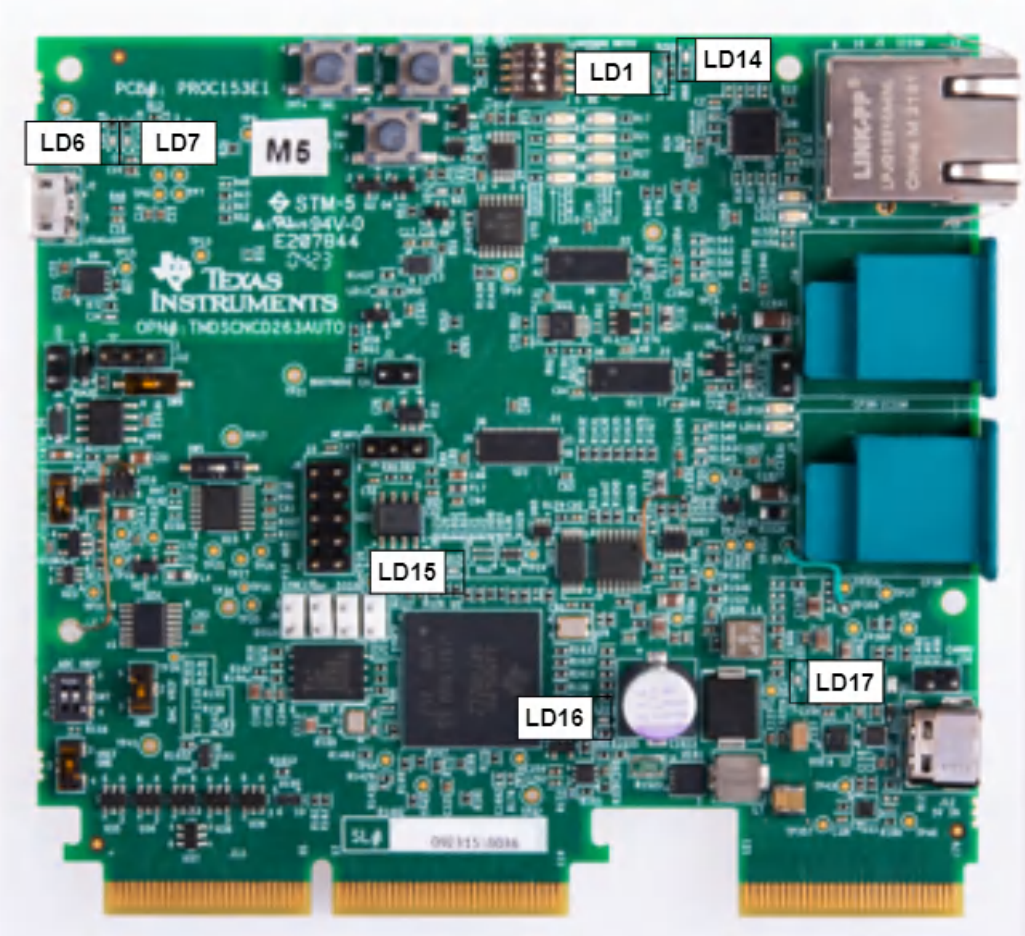



**Figure 2-6. Power Status LEDs**

### 2.3.3 Power Tree

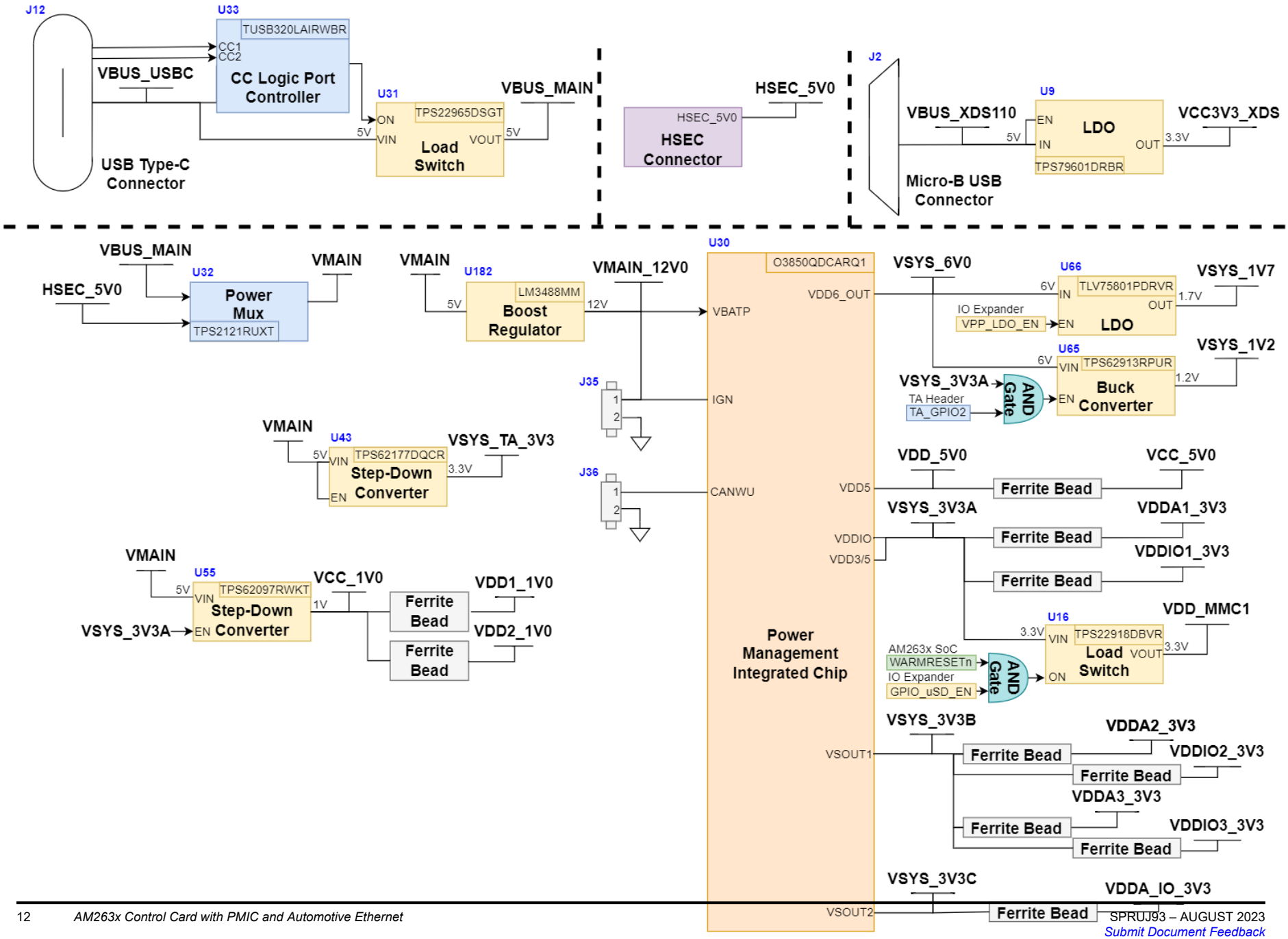







**Figure 2-7. Power Tree**

### 2.3.4 Power Sequence

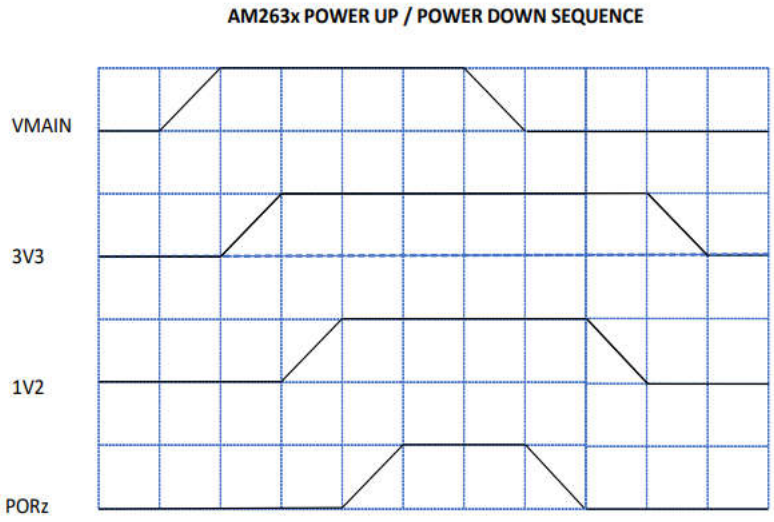



**Figure 2-8. Power Sequence Diagram**

### 2.3.5 PMIC

The TMDSCNCD263-PMIC makes use of a Multirail Power Supply for Microcontrollers in Safety-Relevant Applications (**TPS3850QDCARQ1**). The PMIC integrates multiple supply rails to power the MCU, CAN, and other on-board peripherals.

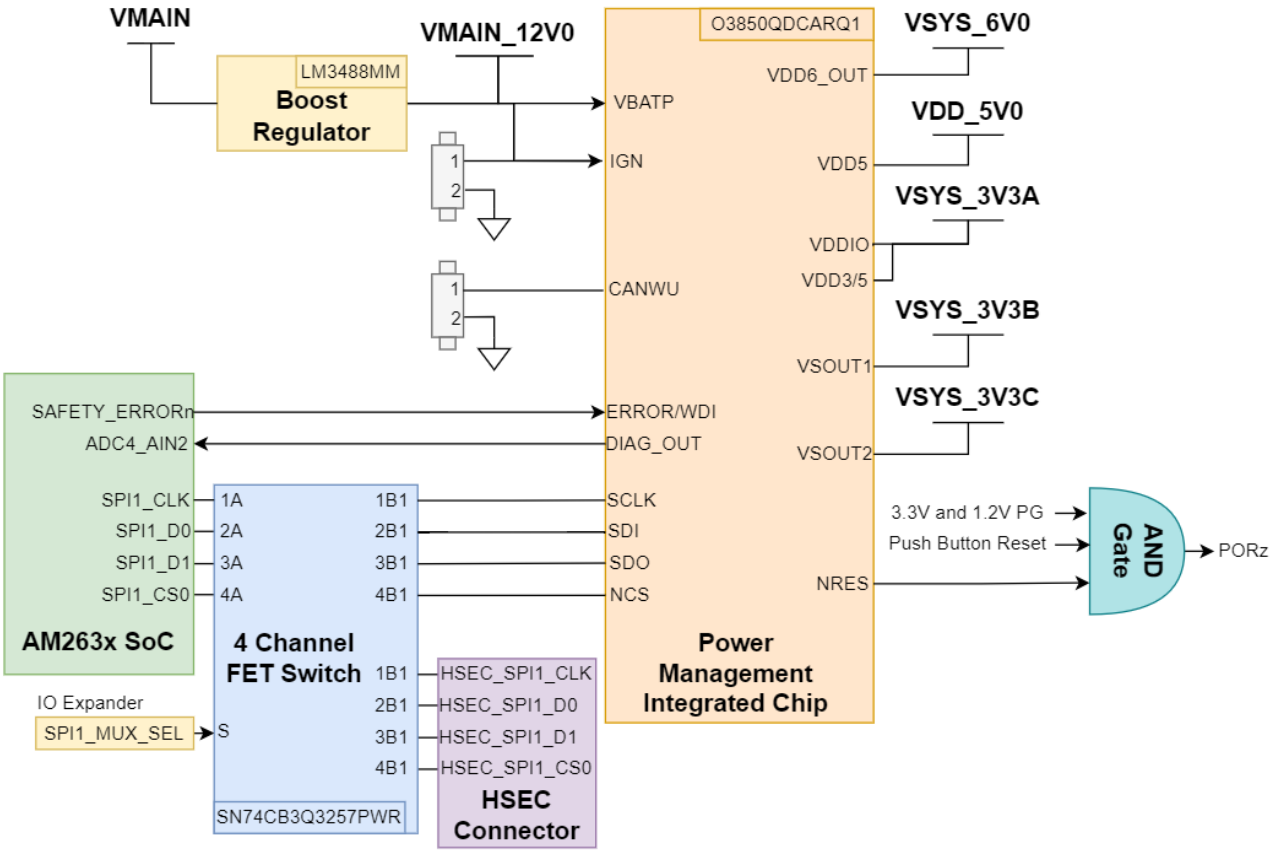



**Figure 2-9. PMIC**

**Note**

VSOUT1 and VSOUT2 are not powered on by default and requires a SPI write to enable the relevant supply rails.

The PMIC supports wake-up from an ignition signal (IGN) or wake-up from a CAN transceiver (CAN_WU).

An independent voltage monitoring unit inside the PMIC monitors undervoltage and overvoltage on all internal supply rails and regulator outputs of the battery supply. All supplies are protected with current limiting and overtemperature pre-warning and shutdown.

For more information about the PMIC and features, refer to the *PMIC Data Sheet*.

## 2.4 Reset

Figure 2-10 shows the reset architecture of the AM263x Control Card.

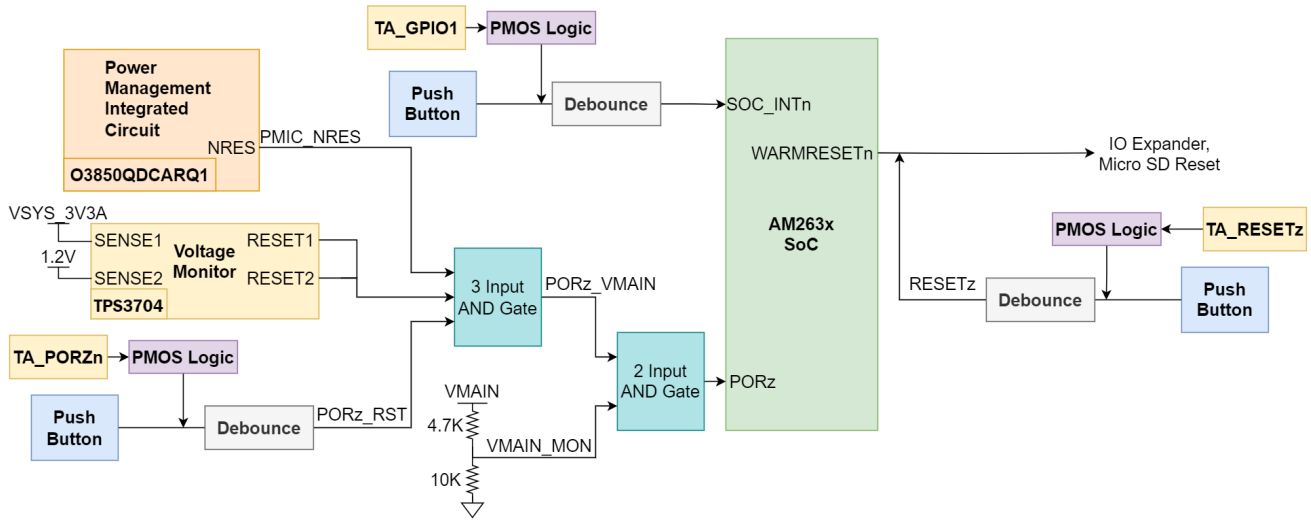



**Figure 2-10. Reset Architecture**

The AM263x SoC has the following resets:

- PORz is the Power-On-Reset for the MAIN Domain.
- WARMRESETn is the Warm Reset to MAIN Domain.

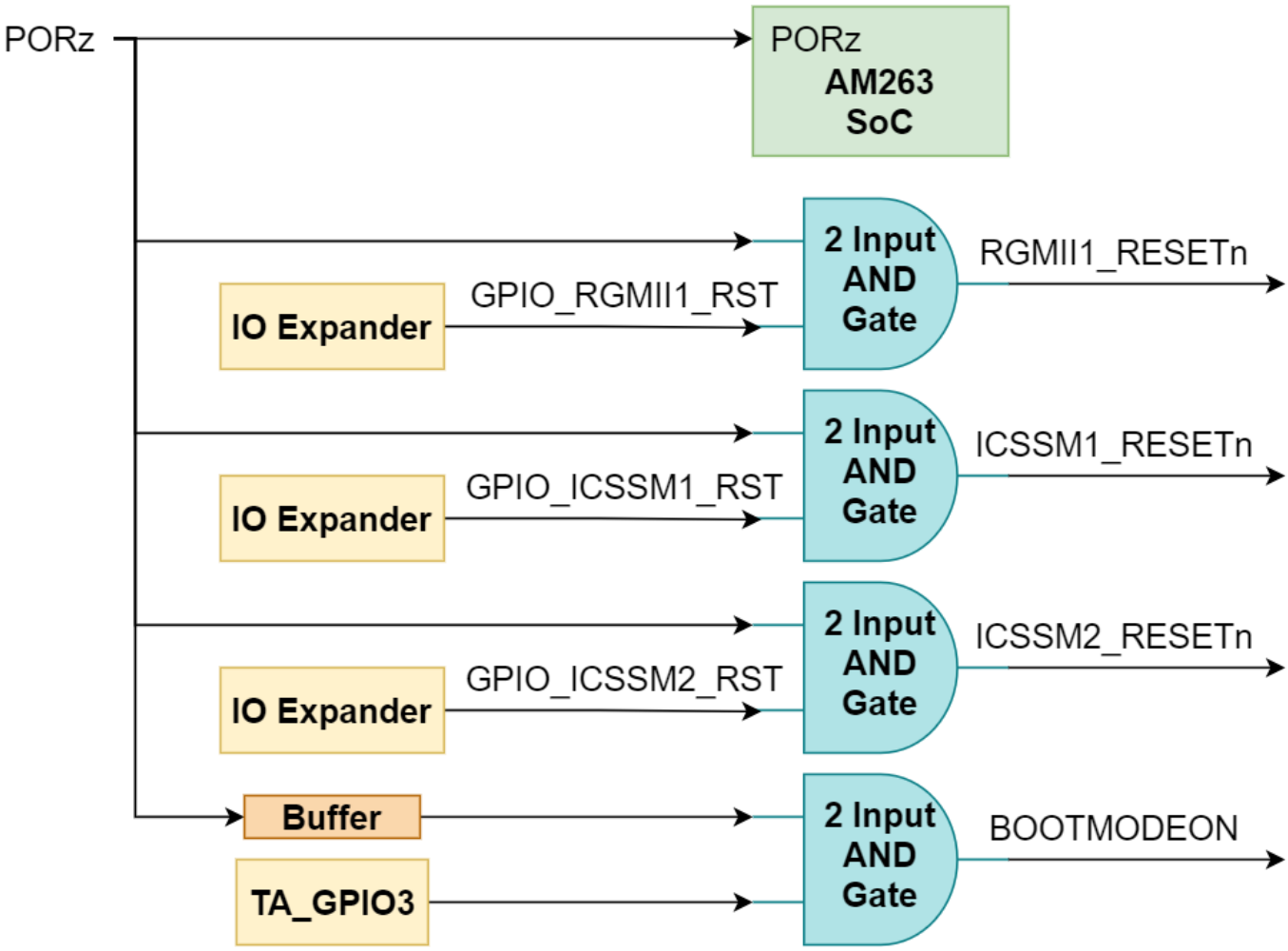



**Figure 2-11. PORz Reset Signal Tree**

The PORz signal is driven by a 3-input AND gate that generates a power on reset for the MAIN domain when:

- The PMIC drives the NRES, MCU Reset output signal low.
- The Voltage Monitor (TPS37042A3OFDDFRQ1) drives either RESET1 or RESET2 when VSYS_3V3A or VSYS_1V2 respectively are outside of the defined boundaries. For VSYS_3V3A, RESET1 is asserted when SENSE1 is either 8% above or below 3.3 V (including device accuracy). For VSYS_1V2, RESET2 is asserted when SENSE2 is either 5% above or below 1.2 V (including device accuracy.
- The user push button (SW2) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_PORZn) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero and so the PORz signal connects to the PMOS drain which is tied directly to ground.

The PORz signal is tied to:

- AM263x SoC PORz input
- RGMII1 Ethernet PHY reset
- ICSSM1 Gigabit Ethernet PHY reset
- ICSSM2 Industrial Ethernet PHY reset
- BOOTMODE buffer output enable

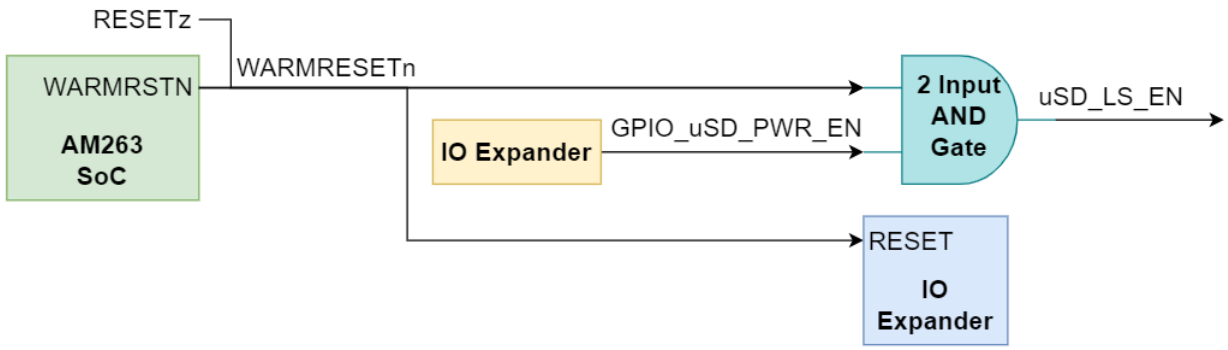



**Figure 2-12. WARMRESETn Reset Signal Tree**

The WARMRESETn signal creates a warm reset to the MAIN domain when:

- The user push button (SW4) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_RESETz) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero and so the RESETz signal connects to the PMOS drain which is tied directly to ground.

The WARMRESETn signal is tied to:

- AM263x SoC WARMRESETN output
- RESETz signal created from push button + PMOS logic
- IO Expander reset
- Micro SD reset

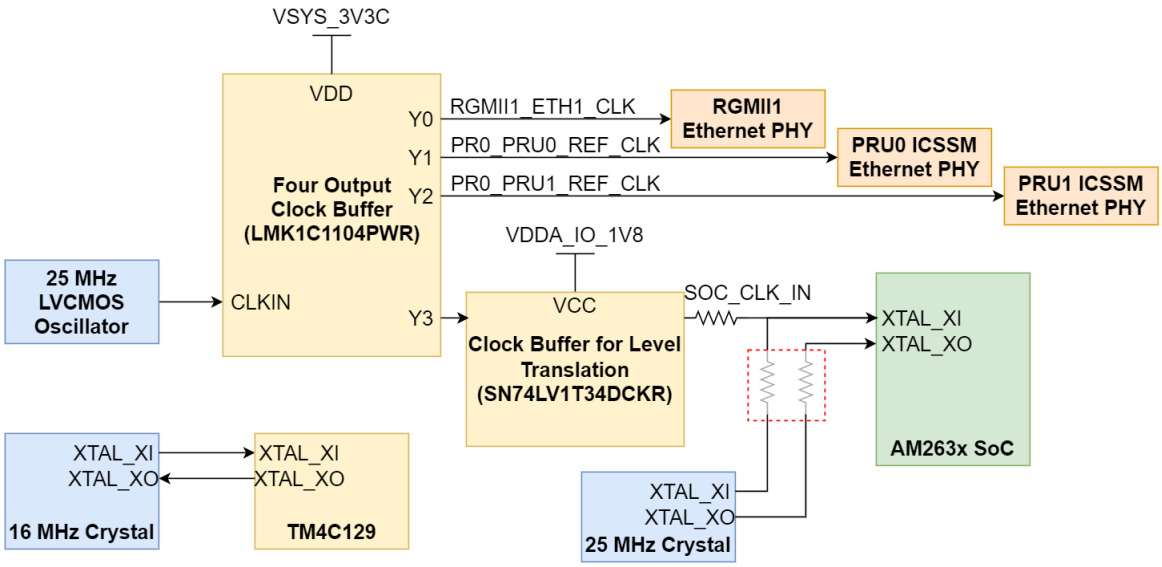
The AM263x Control Card also has an external interrupt to the SoC, INTn, that occurs when:

- The user push button (SW1) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_GPIO1) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero, connecting the INTn signal to he PMOS drain tied directly to ground.

## 2.5 Clock

The AM263x SoC requires a 25-MHz clock input for XTAL_XI. All reference clocks required for the SoC and the three Ethernet PHYs are generated from a single four output clock buffer (LMK1C1104PWR), which is sourced from a single 25-MHz LVCMOS Oscillator by default. A clock buffer is used for level translation from 3.3 V to 1.8 V.

The Control Card also requires a 16-MHz clock source for the TM4C129 microcontroller for UART-USB JTAG support.




Alternatively, the SoC clock input can be sourced from a single 25-MHz crystal. To use the crystal there must be resistors mounted and unmounted as shown in Table 2-3. When the using a crystal as the SoC clock source, then the AM263x CLKOUT0 signal is used to source the four output clock buffer for the Ethernet PHY reference clock signals.

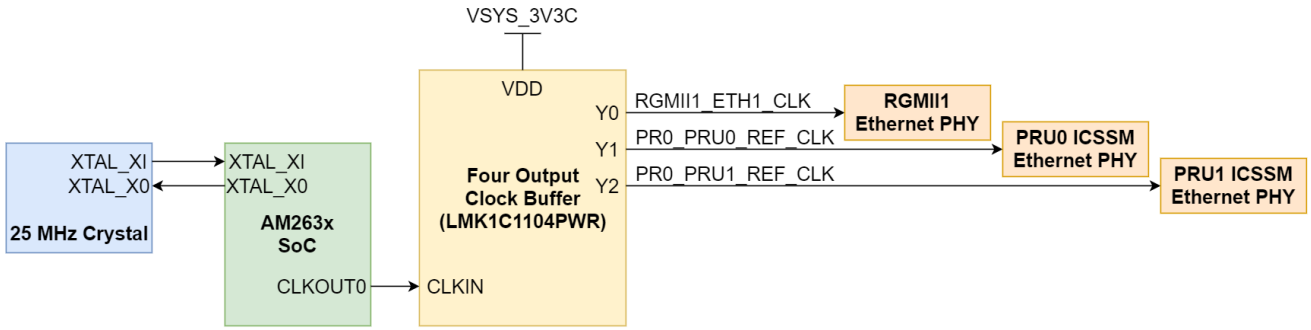



**Figure 2-13. Crystal Clock Tree**

The following table describes the proper resistors to be mounted and DNI'd for each clock source configuration.

**Table 2-3. Clock Source**

| Clock Source | Mounted | DNI |
|---|---|---|
| 25-MHz LVCMOS Oscillator (default) | R161, R135 | R158, R155, R134 |
| 25-MHz Crystal | R158, R155, R134 | R161, R135 |

## 2.6 Boot Mode Selection

The bootmode for the AM263x is selected by either the DIP switch (SW3) or the test automation header. The test automation header uses an I2C IO expansion buffer to drive the bootmode when PORz is toggled. The supported boot modes are as shown in Supported Boot Modes.

**Table 2-4. Supported Boot Modes**

| Boot Mode/Peripheral | Boot Media/Host | Notes |
|---|---|---|
| QSPI (4S) - Quad Read Mode | QSPI Flash | Download and boot SBL from QSPI flash in quad read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails. |
| UART | External Host | Download and boot SBL from UART. Device is expected to get SBL from UART. Device supports the XMODEM protocol for download over UART. |
| QSPI (1S) - Single Read Mode | QSPI Flash | Download and boot SBL from QSPI flash in single read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails. |
| QSPI (4S) - Quad Read UART Fallback Mode | QSPI Flash / External Host | Download and boot SBL from QSPI flash in quad read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails. If Secondary SBL also fails then boot from external host via UART interface. |
| QSPI (1S) - Single Read UART Fallback Mode | QSPI Flash / External Host | Download and boot SBL from QSPI flash in single read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails. If Secondary SBL also fails then boot from external host via UART interface. |
| DevBoot | N/A | No SBL. Used for development purposes only. |

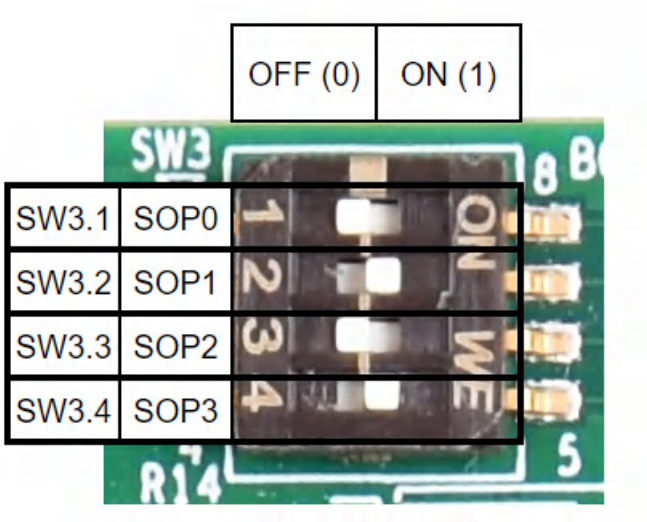



**Figure 2-14. SW3 Switch Positions**

**Table 2-5. Boot-Mode Selection Table**

| Boot Mode | SPI0_D0_pad (SOP3) | SPI0_CLK_pad (SOP2) | QSPI_D1 (SOP1) | QSPI_D0 (SOP0) |
|---|---|---|---|---|
| QSPI (4S) - Quad Read Mode | 0 | 0 | 0 | 0 |
| UART | 0 | 0 | 0 | 1 |
| QSPI (1S) - Single Read Mode | 0 | 0 | 1 | 0 |
| QSPI (4S) - Quad Read UART Fallback Mode | 0 | 1 | 0 | 0 |
| QSPI (1S) - Single Read UART Fallback Mode | 0 | 1 | 0 | 1 |
| DevBoot | 1 | 0 | 1 | 1 |
| Unsupported Boot Mode | All other combinations not defined above | | | |

## 2.7 JTAG Path Selection

The AM263x Control Card allows for JTAG connections to the SoC through the on-board XDS110 or an external emulator via the HSEC docking station. A switch (SW5) is used to drive the select line of a mux (U19) to determine the JTAG path for the SoC. Section 2.12.9 provides additional detail on JTAG pathing.

## 2.8 Header Information

This version of the AM263x Control Card has 11 different headers. For the locations of each header, refer to Section 2.2. The signal details for each header pin is detailed below.

- Test Automation Bootmode Control Header
  - For more information about the Test Automation Header, refer to Section 2.12.10

**Table 2-6. Test Automation Header**

| Designator | Pin 1 | Pin 2 |
|---|---|---|
| J3 | TA_GPIO3 | DGND |

- MCAN Header
  - For more information about the MCAN interface, refer to Section 2.12.7

**Table 2-7. MCAN Header**

| Designator | Pin 1 | Pin 2 | Pin 3 |
|---|---|---|---|
| J5 | MCAN1_CAN_H | DGND | MCAN1_CAN_L |

- FSI Header
  - For more information about the FSI Interface, refer to Section 2.12.8

**Table 2-8. FSI Header**

| Designator | Pin 1 | Pin 2 | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 | Pin 9 | Pin 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| J6 | FSIRX2_CLK | FSITX2_CLK | DGND | DGND | FSIRX2_DATA0 | FSITX2_DATA0 | FSIRX2_DATA1 | FSITX2_DATA1 | DGND | VSYS_3V3A |

- PRU-ICSS IEP Headers
  - For more information about the PRU-ICSS, refer to Section 2.12.2.2

**Table 2-9. PRU-ICSS IEP Headers**

| Designator | Pin 1 | Pin 2 |
|---|---|---|
| J8 | PR0_IEP0_EDIO_DATA_IN_OUT_31 | DGND |
| J9 | PR0_IEP0_EDC_SYNC_OUT1 | DGND |
| J10 | PR0_IEP0_EDIO_DATA_IN_OUT_30 | DGND |
| J11 | PR0_IEP0_EDC_SYNC_OUT0 | DGND |

- LIN Headers
  - For more information about the LIN interface, refer to Section 2.12.11

**Table 2-10. LIN Headers**

| Designator | Pin 1 | Pin 2 | Pin 3 |
|---|---|---|---|
| J32 | VLIN | LIN | DGND |
| J33 | VBAT_LIN | DGND | N/A |

- PMIC Headers
  - For more information about the PMIC, refer to Section 2.3.5

**Table 2-11. PMIC Headers**

| Designator | Pin 1 | Pin 2 |
|---|---|---|
| J35 | IGNITION | DGND |
| J36 | CANWU | DGND |

## 2.9 GPIO Mapping

**Table 2-12. GPIO Mapping Table**

| Sl No. | GPIO Description | GPIO | Pin Name | Functionality | Net Name | Active Status |
|---|---|---|---|---|---|---|
| 1 | Interrupt To SoC | GPIO21 | LIN2_RXD | Interrupt | SOC_INTn | LOW |
| 2 | Interrupt To DP83826E | GPIO66 | EPWM12_A | Interrupt | ICSSM2_PWDN/INTn | LOW |
| 3 | Interrupt To DP83TG720_01 | GPIO67 | EPWM11_B | Interrupt | RGMII1_INT | LOW |
| 4 | Interrupt To DP83TG720_02 | GPIO68 | EPWM12_B | Interrupt | ICSSM1_INT | LOW |
| 5 | User Defined LED | GPIO20 | LIN2_TXD | GPIO | USER_LED0 | PREFERABLE |
| 6 | PMIC DIAG OUT TO SoC | GPIO1 | QSPI0_CSn1 | GPIO | PMIC_DIAG_OUT | LOW |
| **IO Expander 01** | | | | | | |
| 7 | Standby input to CAN tranciever | | P00 | GPIO | MCAN1_STB | High |
| 8 | Enable control to clock buffer | | P01 | Enable | CLK_BUF_EN | High |
| 9 | Select line for ICSSM Mux 1 | | P02 | Mux Selection | ICSSM1_MUX_SEL | PREFERABLE |
| 10 | Select line for ICSSM Mux 2 | | P03 | Mux Selection | ICSSM2_MUX_SEL | PREFERABLE |
| 11 | Reset input to DP83869_01 | | P04 | Reset | GPIO_RGMII1_RST | LOW |
| 12 | Reset input to DP83869_02 | | P05 | Reset | GPIO_ICSSM1_RST | LOW |
| 13 | Reset input to DP83826E | | P06 | Reset | GPIO_ICSSM2_RST | LOW |
| 14 | Enable control to SD load switch | | P07 | Load SW Enable | GPIO_uSD_PWR_EN | High |
| 15 | User Defined LED | | P10 | GPIO | USER_LED1 | PREFERABLE |
| 16 | Select line for I2C0 MUX | | P11 | Mux Selection | I2C0_MUX_SEL | PREFERABLE |
| 17 | Select line for SPI1 MUX | | P12 | Mux Selection | SPI1_MUX_SEL | PREFERABLE |
| 18 | Enable control to 1.7V LDO | | P13 | LDO Enable | VPP_LDO_EN | PREFERABLE |
| 19 | Select line for MDIO/MDC MUX | | P14 | Mux Selection | MDIO/MDC_MUX_SEL | PREFERABLE |
| 20 | Select line for LIN/UART MUX | | P15 | Mux Selection | LIN_MUX_SEL | PREFERABLE |
| 21 | Select line for ADC MUX | | P16 | Mux Selection | ADC1_MUX_SEL | PREFERABLE |
| 22 | Select line for ADC MUX | | P17 | Mux Selection | ADC2_MUX_SEL | PREFERABLE |

## 2.10 Push Buttons

The control card supports multiple user push buttons that provide reset inputs and user interrupts to the processor.

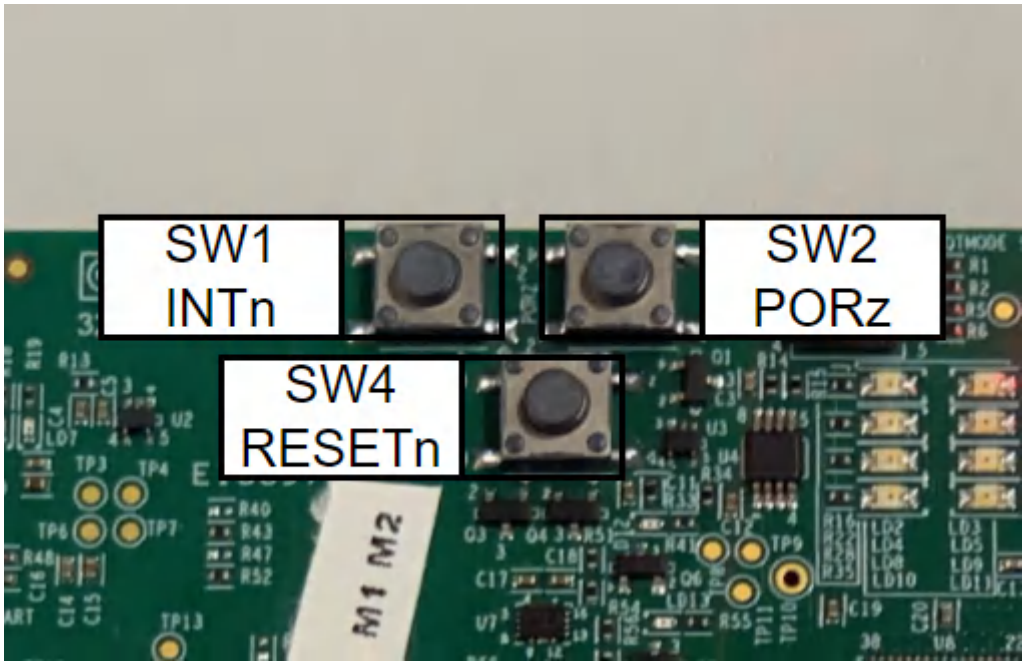



**Figure 2-15. Push Buttons**

Control Card Push Buttons lists the push buttons that are placed on the top side of the AM263x Control Card board.

**Table 2-13. Control Card Push Buttons**

| Push Button | Signal | Function |
|---|---|---|
| SW1 | INTn | User Interrupt signal |
| SW2 | PORz | SoC PORz reset input |
| SW4 | RESETn | SoC warm reset input |

## 2.11 Test Points

The following table describes all test points available on the Control Card.

**Table 2-14. Control Card Test Points**

| Designator | Signal |
|---|---|
| TP1 | VSYS_TA_3V3 |
| TP2 | VCC3V3_XDS |
| TP3 | TM4C129_TCK |
| TP4 | TM4C129_TMS |
| TP6 | TM4C129_TDI |
| TP7 | TM4C129_TDO |
| TP13 | TM4C129_RST# |
| TP14 | PRU-ICSS Ethernet PHY CLK_OUT2 |
| TP15 | VBUS_XDS110 |
| TP20 | RGMII1 Ethernet PHY CLK_OUT1 |
| TP22 | VDD_MMC1 |
| TP23 | SOC_TDI |
| TP24 | SOC_MMC0_CLK |
| TP25 | SOC_TDO |
| TP26 | SOC_TMS |
| TP27 | SOC_TCK |
| TP29 | WARMRESETn |
| TP31 | MMC0_WP |
| TP32 | PORz |
| TP33 | RSVD |
| TP35 | VDD_IO_3V3 |
| TP36 | DGND |
| TP37 | VCC_1V2 |
| TP39 | VSYS_1V2 |
| TP40 | SAFETY_ERRORn |
| TP41 | DGND |
| TP42 | VSYS_1V7 |
| TP43 | TUSB320 ID |
| TP44 | VSYS_MON |
| TP45 | RSVD |
| TP353 | PMIC_NRES |
| TP354 | PMIC_DIAG_OUT |
| TP355 | PMIC_ENDRV |
| TP356 | PMIC_ERROR-WDI |
| TP357 | VBUS_USBC |
| TP358 | VDD_5V0 |
| TP359 | VSYS_3V3A |
| TP360 | VSYS_6V0 |
| TP361 | VSYS_3V3B |
| TP362 | VSYS_3V3C |
| TP363 | VMAIN_12V0 |

## 2.12 Interfaces

### 2.12.1 Memory Interface

#### *2.12.1.1 QSPI*

The AM263x Control Card has a 128 Mbit QSPI memory device (S25FL128SAGNFI000), which is connected to the QSPI0 interface of the AM263x SoC. The QSPI supports single data rates with memory speeds up to 104 MHz. The QSPI flash is powered by the 3.3-V IO supply (VSYS_3V3A).

**Note**

There is typically a reset pin for flash memory. The reset pin is not present in the WSON package that is used in the Control Card.

The QSPI0_D0/D1 signals are also used for BOOTMODE control logic. There are 10-kΩ resistors used to isolate the BOOTMODE control logic after the value is latched.

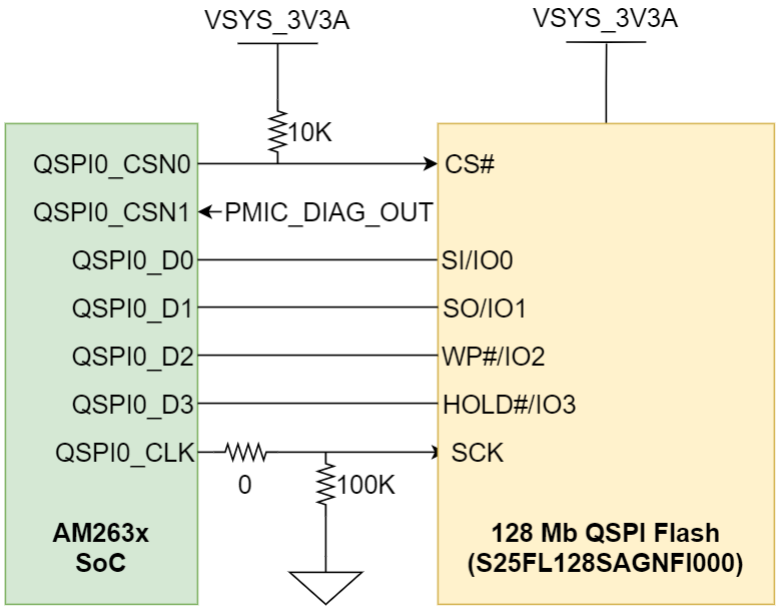



**Figure 2-16. QSPI**

### 2.12.1.2 Board ID EEPROM

The AM263x Control Card has a I2C based 1 Mbit EEPROM (CAT23M01WI-GT3) to store board configuration details. The Board ID EEPROM is connected to the I2C0 interface of the AM263x through a 1:2 mux (SN74CB3Q3257PWR). The default I2C address of the EEPROM is set to 0x50 by pulling down the address pins A1 and A2 to ground. The Write Protect pin for the EEPROM is by default pulled down to ground and therefore disabled. There is also the option to enable Write Protect by removing the 10 kΩ pull down resistor (R273) and mounting a pull up resistor (R268) to the 3.3 V IO voltage supply.

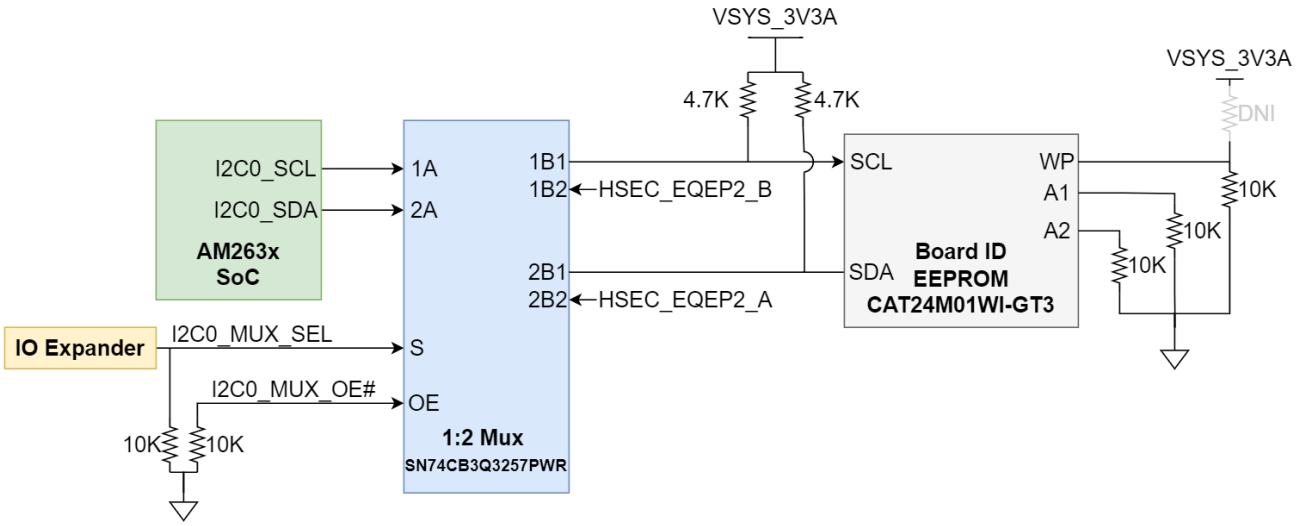



**Figure 2-17. Board ID EEPROM**

The GPIO Expander is used to control the select signal (I2C0_MUX_SEL) of the 1:2 Mux.

**Table 2-15. EEPROM Mux Table**

| Select | Condition | Mux Function |
|---|---|---|
| HIGH | HSEC EQEP Selected | A→B2 port |
| LOW | I2C0 Selected | A→B1 port |

### 2.12.2 Ethernet Interface

#### *2.12.2.1 RGMII*

The AM263x Control Card uses one port of RGMII signals to be connected to a 48-pin Ethernet PHY (DP83TG730SWRHARQ1). The PHY is configured to advertise 1-Gb operation. The Ethernet data signals of the PHY are terminated to a MATEnet Connector. LEDs are used to indicate link status and activity.

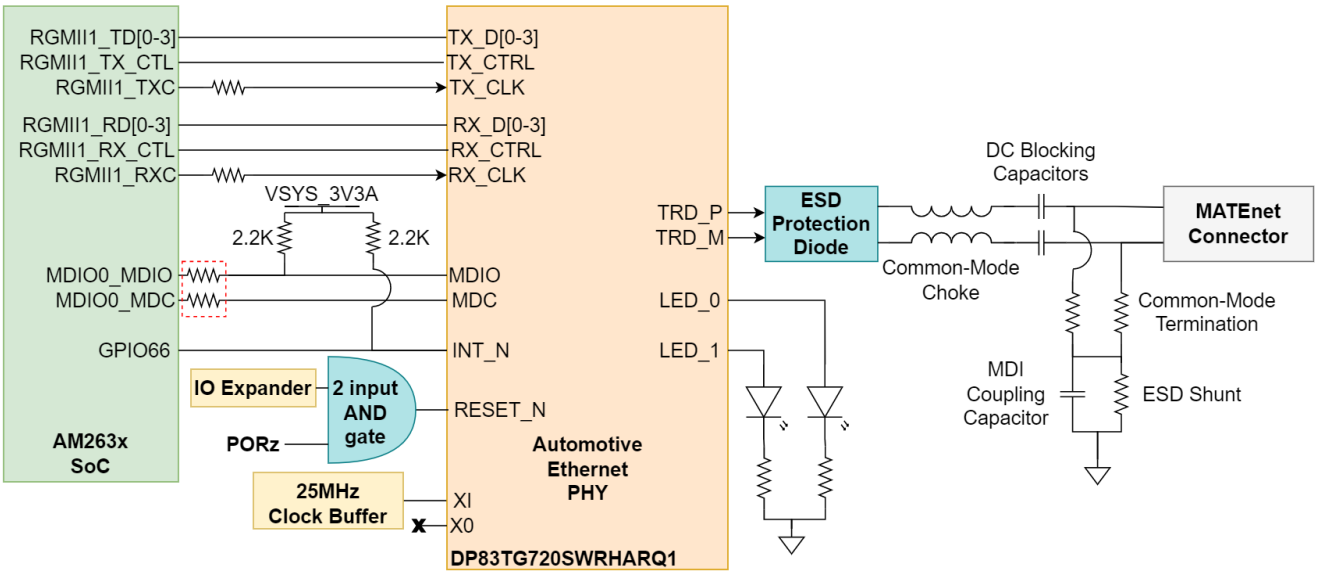



**Figure 2-18. RGMII1 Automotive Ethernet PHY**

The Ethernet PHY requires three separate power sources. VSYS_3V3A from the PMIC is filtered using two different ferrite beads to supply voltage to VDDIO and VDDA of the Ethernet PHY. There is a dedicated LDO for the 1.0 V supply for the Ethernet PHY.

There are series termination resistors on the transmit and receive clock signals located near the AM263x SoC.

The MDIO and interrupt signals from the SoC to the PHY require 2.2 kΩ pull up resistors to the I/O supply voltage for proper operation. The interrupt signal is driven by a GPIO signal that is mapped from the AM263x SoC.

The reset signal for the Ethernet PHY is driven by a 2-input AND gate. The AND gate's inputs are a GPIO signal that is generated by the IO Expander and PORz.

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

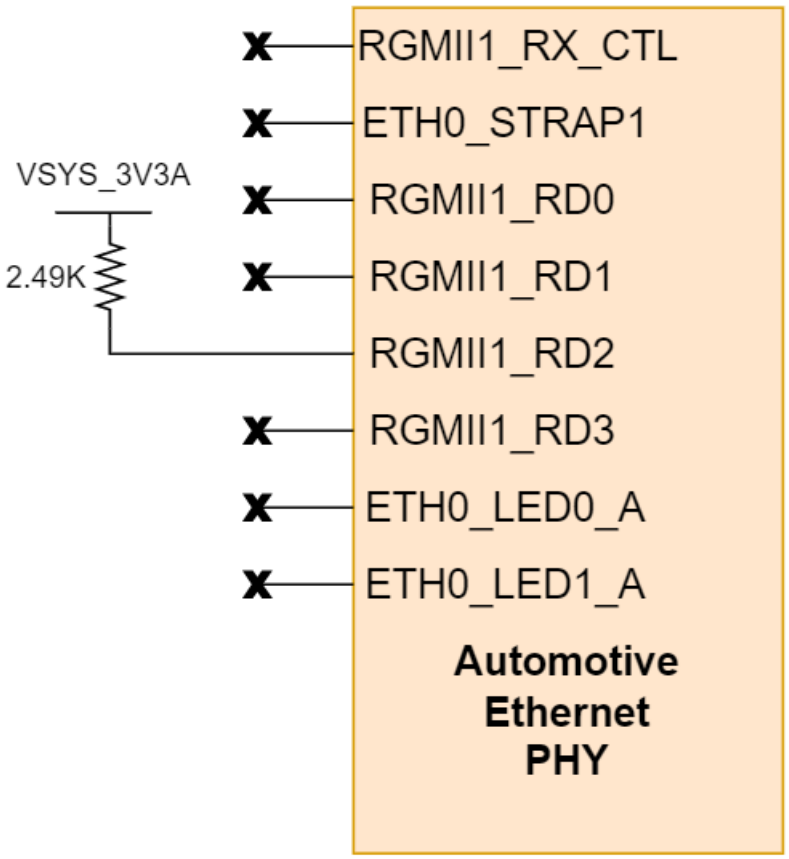



**Figure 2-19. RGMII1 Automotive Ethernet PHY Strapping Resistors**

**Note**

Each strapping has an internal pull down resistance.

**Table 2-16. RGMII1 Gigabit Ethernet PHY Strapping Resistors**

| Functional Pin | Default Mode | Mode in CC | Function |
|---|---|---|---|
| RX_D0 | 0 | 0 | RGMII (Align Mode) |
| RX_D1 | 0 | 0 | |
| RX_D2 | 0 | 1 | |
| RX_CTRL | 0 | 0 | PHY Address: 0x0000 |
| STRP_1 | 0 | 0 | |
| LED_0 | 0 | 0 | MS: Peripheral |
| LED_1 | 0 | 0 | AUTO: Autonomous |

### 2.12.2.2 PRU-ICSS

**Note**

The PRU internal pinmux mapping provided in the TRM is part of the original hardware definition of the PRU. However, due to the flexibility provided by the IP and associated firmware configurations, this is not a hard requirement. The first PRU implementation for AM65x had the MII TX pins swapped during initial SoC integration and this convention was maintained for subsequent PRU revisions to enable firmware reuse. To make use of the SDK firmware, use the SYSCONFIG generated PRU pin mapping.

The AM263x Control Card makes use of two on-die programmable real-time unit and industrial communication subsystem's (PRU-ICSS) of the AM263x SoC to interface with two Ethernet PHY transceivers. There is a Automotive Ethernet PHY transceiver (DP83TG720SWRHARQ1) connected to PRU0 of the SoC and an Industrial Ethernet PHY transceiver (DP83826ERHBT) connected to PRU1. The Ethernet data signals of the Automotive Ethernet PHY are terminated to a MATEnet Connector while the Industrial Ethernet PHY data signals are terminated to an RJ45 connector. The MATEnet Connector used on the board supports Gigabit Ethernet by the IEEE 802.3 standard 1000BASE-T1. The RJ45 connector used on the board supports 10/100 (DP83826ERHBT) Mbps connectivity with integrated magnetic and LEDs for link and activity indication.

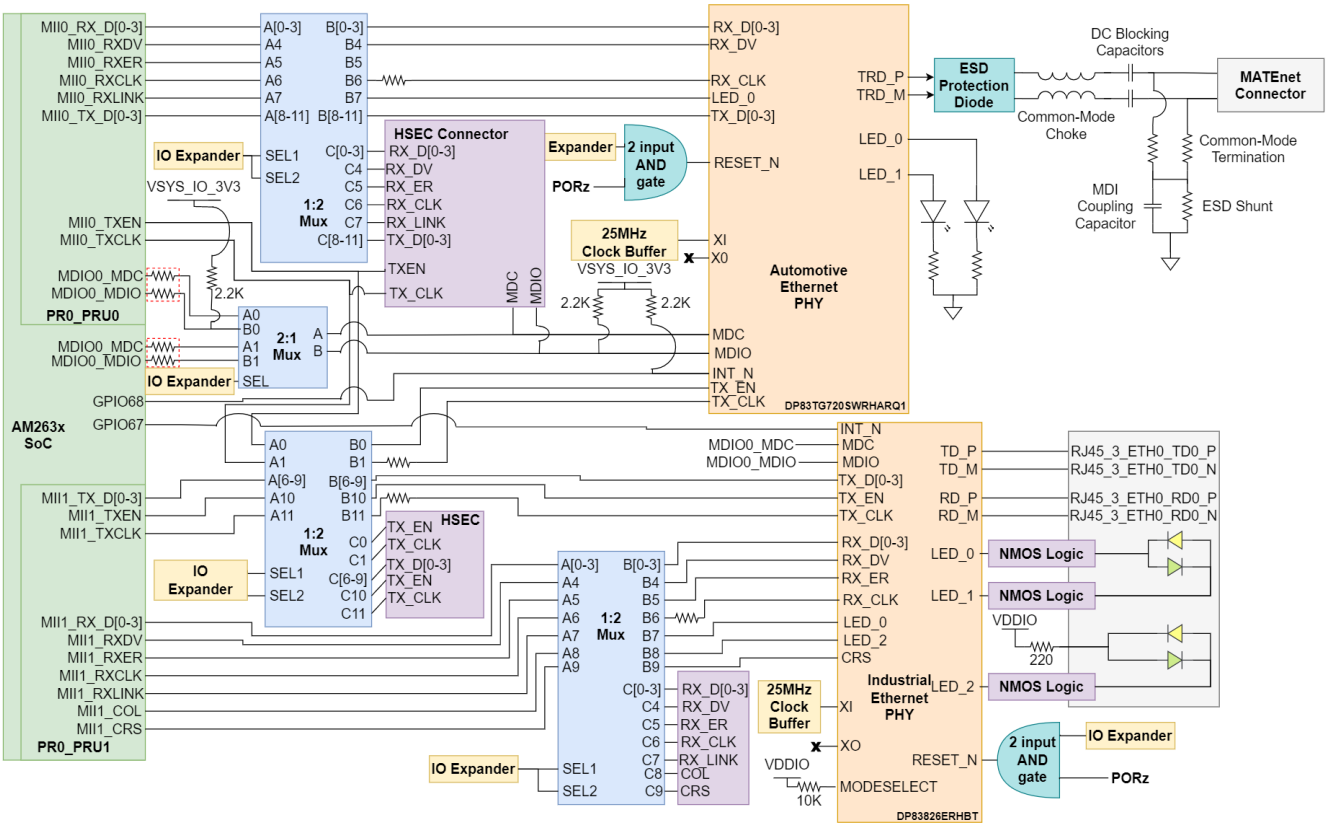



**Figure 2-20. PRU-ICSS Overview**

For the Automotive Ethernet PHY:

- The Ethernet PHY requires three separate power sources. VSYS_3V3A from the PMIC is filtered using two different ferrite beads to supply voltage to VDDIO and VDDA of the Ethernet PHY. There is a dedicated LDO for the 1.0V supply for the Ethernet PHY.
- The Ethernet PHY uses many functional pins as strap options to place the device into a specific mode of operation. Each functional pin has a default mode that is driven by an internal pull resistor.
- There is a 2:1 mux (TMUX154EDGSR) that controls the mapping of MDIO and MDC signals for the ethernet PHY's.

**Table 2-17. Gigabit Ethernet PHY MDIO/MDC MUX**

| SEL | Condition | Function |
|---|---|---|
| HIGH | AM263x SoC MDIO0 MDIO/MDC signals selected | A1/B1→A/B port |
| LOW | PRU MDIO/MDC signals selected | A0/B0→ A/B port |

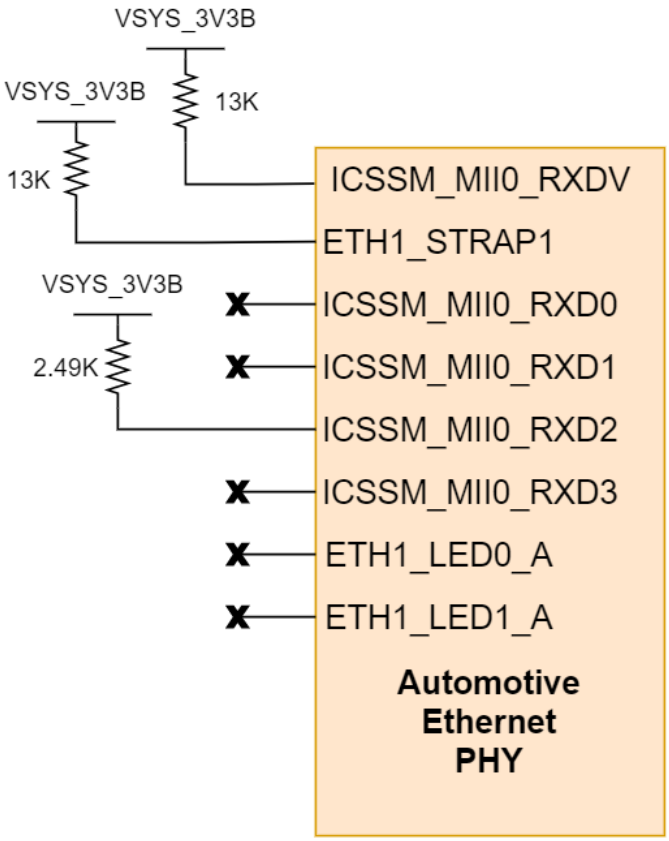



**Figure 2-21. PRU0 ICSS Automotive Ethernet PHY Strapping Resistors**

**Table 2-18. PRU0 ICSS Automotive Ethernet PHY Strapping Resistors**

| Functional Pin | Default Mode | Mode in CC | Function |
|---|---|---|---|
| RX_D0 | 0 | 0 | RGMII (Align Mode) |
| RX_D1 | 0 | 0 | |
| RX_D2 | 0 | 1 | |
| RX_CTRL | 0 | 1 | PHY Address: 0x000C |
| STRP_1 | 0 | 1 | |
| LED_0 | 0 | 0 | MS: Peripheral |
| LED_1 | 0 | 0 | AUTO: Autonomous |

For the Industrial Ethernet PHY transceiver:

- The Ethernet PHY requires two separate power sources. VSYS_3V3B from the PMIC is filtered by two separate ferrite beads to be used as the supply for VDDIO and VDDA3V3.
- The Ethernet PHY is set to ENHANCED mode by pulling the MODESELECT pin up to VSYS_3V3B.
  - ENHANCED mode allows the DP83826E to support real-time Ethernet applications in addition to standard Ethernet applications.
- The Ethernet PHY uses many functional pins as strap options to place the device into a specific mode of operation. Each functional pin has a default mode that is driven by an internal pull resistor

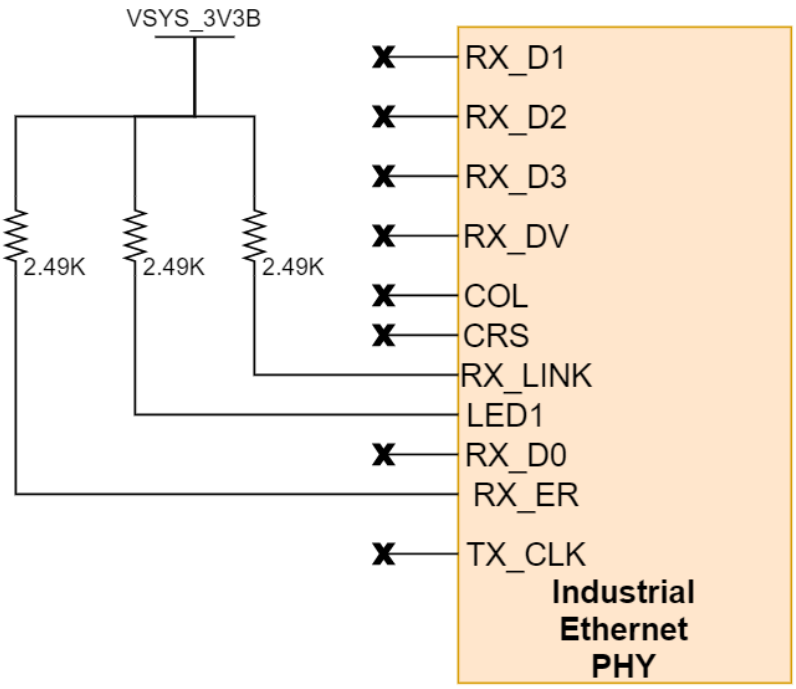



**Figure 2-22. PRU1 ICSS Industrial Ethernet PHY Strapping Resistors**

**Table 2-19. PRU1 ICSS Industrial Ethernet PHY Strapping Resistors**

| Functional Pin | Default Mode | Mode in CC | Function |
|---|---|---|---|
| RX_D0 | 1 | 1 | auto-negotiation enable |
| LED1 | 1 | 1 | odd nibble detection enable |
| RX_LINK | 0 | 1 | PHY address: 001 |
| CRS | 0 | 0 | |
| COL | 0 | 0 | |
| TX_CLK | 0 | 0 | RMII Controller Mode |
| RX_ER | 0 | 1 | LED1 on pin 31 |
| RX_D3 | 0 | 0 | fast link-drop disable |
| RX_D2 | 0 | 0 | MII MAC mode |
| RX_D1 | 0 | 0 | Auto MDIX enable |
| RX_DV | 0 | 0 | MDIX (applicable only when auto-MIDX is disabled) |

For both Ethernet PHYs:

- There are series termination resistors on the transmit and receive clock signals located near the AM263x SoC.
- The MDIO and Interrupt signals from the SoC to the PHY require 2.2KΩ pull up resistors to the I/O supply voltage for proper operation. The interrupt signal is driven by a GPIO signal that is mapped from the AM263x SoC.
- The reset signal for the Ethernet PHY is driven by a 2-input AND gate. The AND gate's inputs are a GPIO signal that is generated by the IO Expander and PORz.

- A 25 MHz clock is sourced from a four output clock buffer that has a 25 MHz oscillator as an input.
- There are three 1:2 muxes (TS3DDR3812RUAR) that control the mapping of ethernet signals from the SoC to either the Ethernet PHY's or the HSEC connector. The select logic for the three muxes is driven by two GPIO signals that are generated by the IO expander.

**Table 2-20. ICSS HSEC MUX**

| Select Signal | Logic Level | Condition | Function |
|---|---|---|---|
| ICSSM1_MUX_SEL | LOW | PRU0 signals mapped to Ethernet PHY | A[n] → B[n] |
| | HIGH | PRU0 signals mapped to HSEC | A[n] → C[n] |
| ICSSM2_MUX_SEL | LOW | PRU1 signals mapped to Ethernet PHY | A[n] → B[n] |
| | HIGH | PRU1 signals mapped to HSEC | A[n] → C[n] |

#### *2.12.2.3 LED Indication in RJ45 Connector*

The AM263x Control Card has one RJ45 network ports for the ICSSM port on PRU1 of the AM263x SoC. Each RJ45 connector contains two bi-color LEDs that are used to indicate link and activity.

- RJ45 Connector LED indication for the ICSSM PRU1 port:

**Table 2-21. ICSSM PRU1 RJ45 Connector LED indication**

| LED | Color | Indication |
|---|---|---|
| Right LED | Green | Ethernet PHY power established |
| | Yellow | 10BT speed link is up |
| Left LED | Green | Link OK |
| | Yellow | 1000BT speed link is up |

### 2.12.3 I2C

The AM263x Control Card uses three AM263x SoC inter-integrated circuit (I2C) ports to operate as a controller for various targets. TI recommends that all I2C data and clock lines are pulled up to the 3.3V IO voltage supply to enable communication.

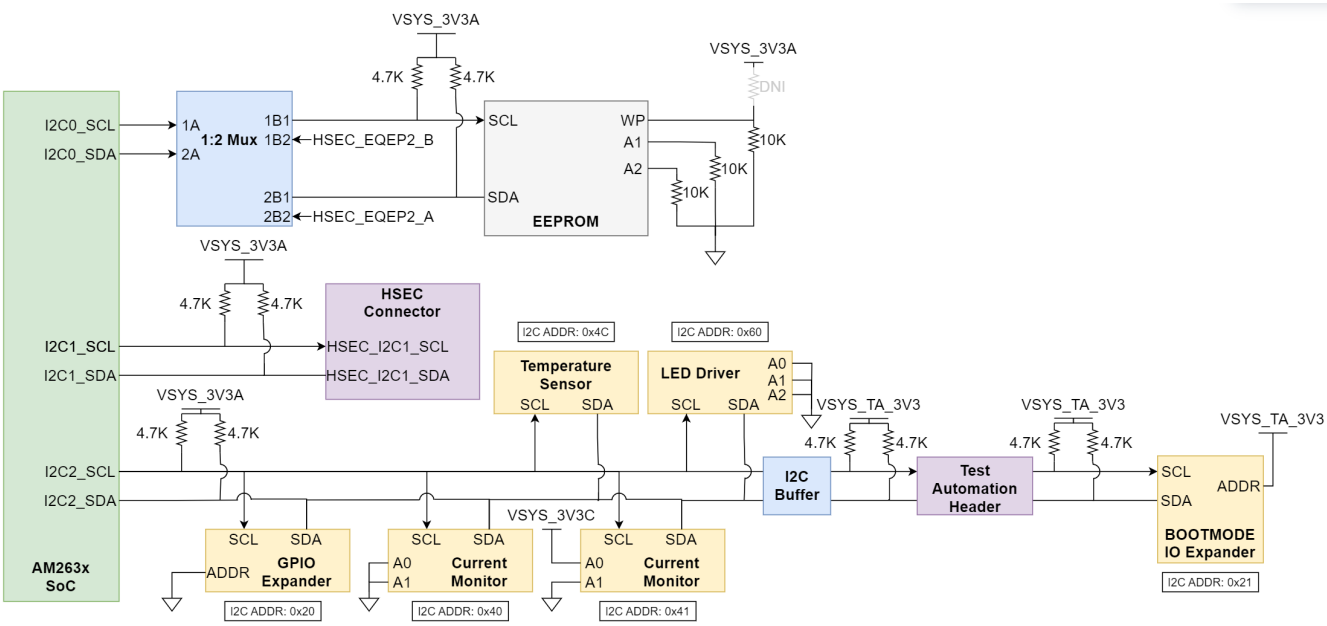



**Figure 2-23. I2C Instances Tree**

**Table 2-22. I2C Addressing**

| Target | I2C Instance | I2C Address Bit Description | Device Configuration | CC Config. | I2C Address |
|---|---|---|---|---|---|
| Board ID EEPROM | I2C0 | The first 4 bits of the device address are set to 1010, the next two are set by the A2 and A1 pins, the seventh bit, a16, is the most significant internal address bit | 0b10110[A2][A1][a16] A1/A2 are connected to ground | 0b1010000 | 0x50 |
| GPIO Expander | I2C2 | The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander | 0b010000[ADDR] ADDR pin connected to ground | 0b0100000 | 0x20 |
| BOOTMODE IO Expander | I2C2/ I2C1_TA | The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander | 0b010000[ADDR] ADDR pin connected to 3.3V IO supply | 0b0100001 | 0x21 |
| Current Monitor | I2C2 | The first three bits of the target address are 100, the following four bits are determined by what is hooked up to A1 and A0 | Refer to Address pin table from *Device Data Sheet*. | 0b1000000 | 0x40 |
| Current Monitor | I2C2 | The first three bits of the target address are 100, the following four bits are determined by what is hooked up to A1 and A0 | Refer to Address pin table from *Device Data Sheet*. | 0b1000001 | 0x41 |
| Temperature Sensor | I2C2 | Fixed value of 1001100 for part number TMP411Ax | N/A | 0b1001100 | 0x4C |
| LED Driver | I2C2 | The first four bits of the target address are 1100, the following three are determined by A2, A1, and A0 | 0b1100[A2][A1][A0] A2/A1/A0 all connected to ground | 0b1100000 | 0x60 |

**Note**

Underlined address bits are fixed based on the device addressing and cannot be configured.

### 2.12.4 Industrial Application LEDs

The AM263x Control Card has an LED driver (TPIC2810D) that is used for Industrial Communication LEDs. The driver is connected to eight green LEDs and has an I2C address of 0x60.

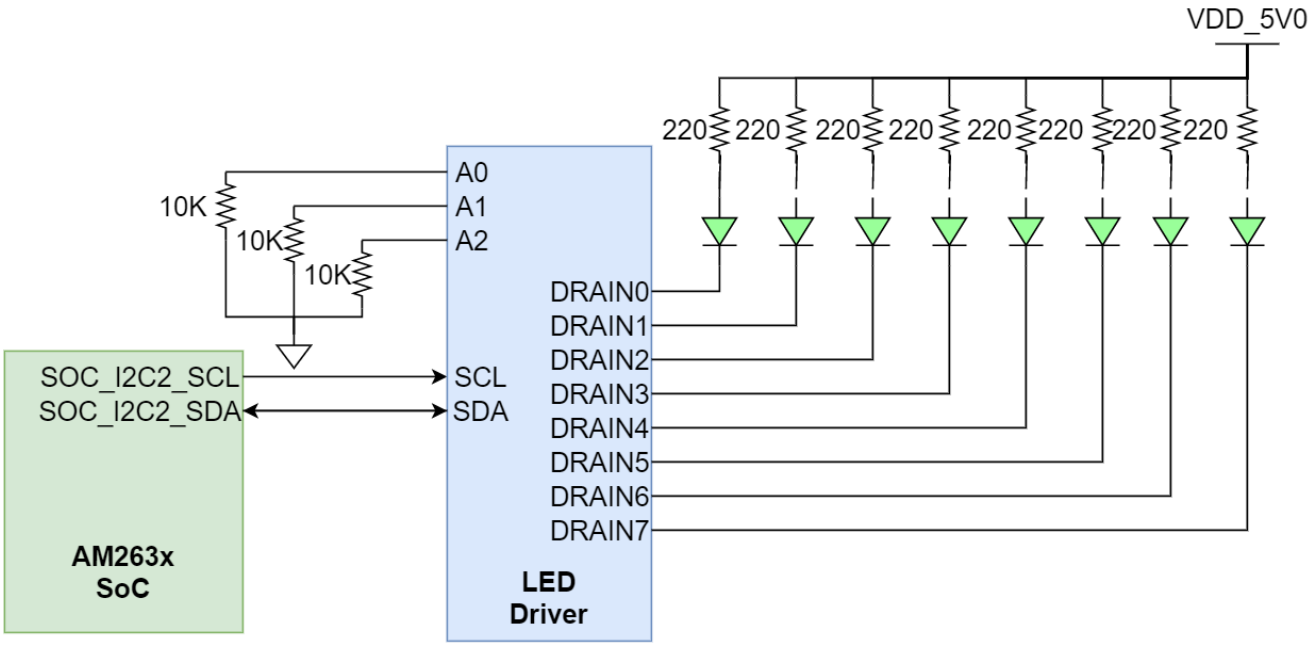



**Figure 2-24. Industrial Application LED Driver**

### 2.12.5 SPI

The AM263x Control Card maps two SPI instances (SPI0,SPI1) from the AM263x SoC to the HSEC 180 pin connector. Series termination resistors are placed near the SoC for each SPI clock signal.

There is 4-channel FET Switch that routes SPI1 between the PMIC and the HSEC Connector. This FET Switch has the select line driven by SPI1_MUX_SEL of the IO Expander. Additionally, there is an external pull-down resistor on the Select line, such that the PMIC routing for the SPI signals is in the default state.

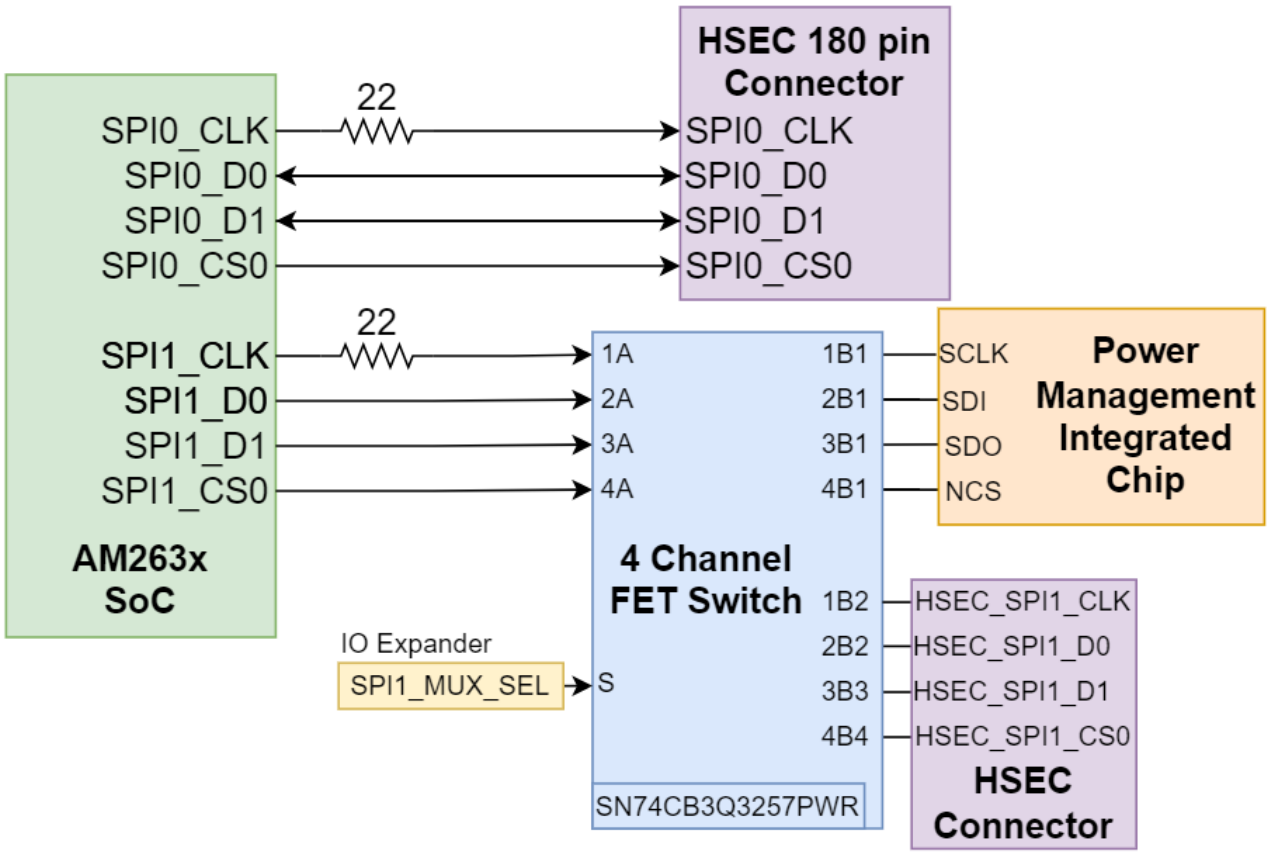



**Figure 2-25. SPI**

### 2.12.6 UART

The AM263x Control Card uses the XDS110 as a USB2.0 to UART bridge for terminal access. UART0 transmit and receive signals of the AM263x SoC are mapped to the XDS110 with a dual channel isolation buffer (ISO7221CDR) for translating from the 3.3 V IO voltage supply (VSYS_3V3C) to the 3.3 V XDS supply. The XDS110 is connected to a micro-B USB connector for the USB 2.0 signals. ESD protection is provided to the USB 2.0 signals by a transient voltage suppression device (TPD4E004DRYR). The micro-B USB connector's VBUS 5 V power is mapped to a low dropout regulator (TPS79601DRBR) to generate the 3.3 V XDS supply. A separate 3.3 V supply for the XDS110 allows for the emulator to maintain a connection when power to the Control Card is removed.

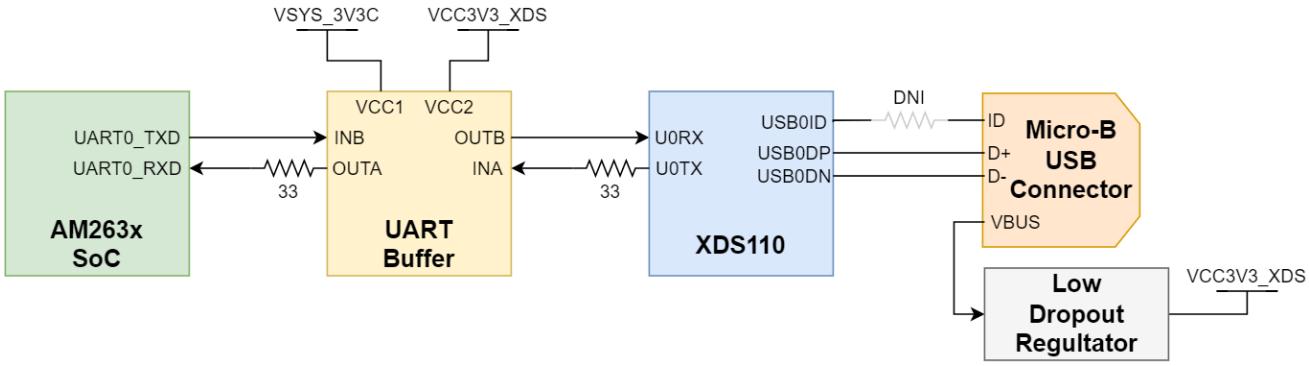



**Figure 2-26. UART-USB Bridge for Emulation**

The Control Card supports an additional UART1 instance that has the transmit and receive signals mapped from the AM263x SoC to the HSEC connector. To make use of UART1, the select line of a 1:2 mux must be high. The select line is driven by a GPIO signal (LIN_MUX_SEL) that is sourced from the IO expander.

**Table 2-23. UART Mux Select Logic**

| Select | Condition | Function |
|---|---|---|
| LOW | LIN Selected | A→B1 |
| HIGH | HSEC UART Selected | A→B2 |

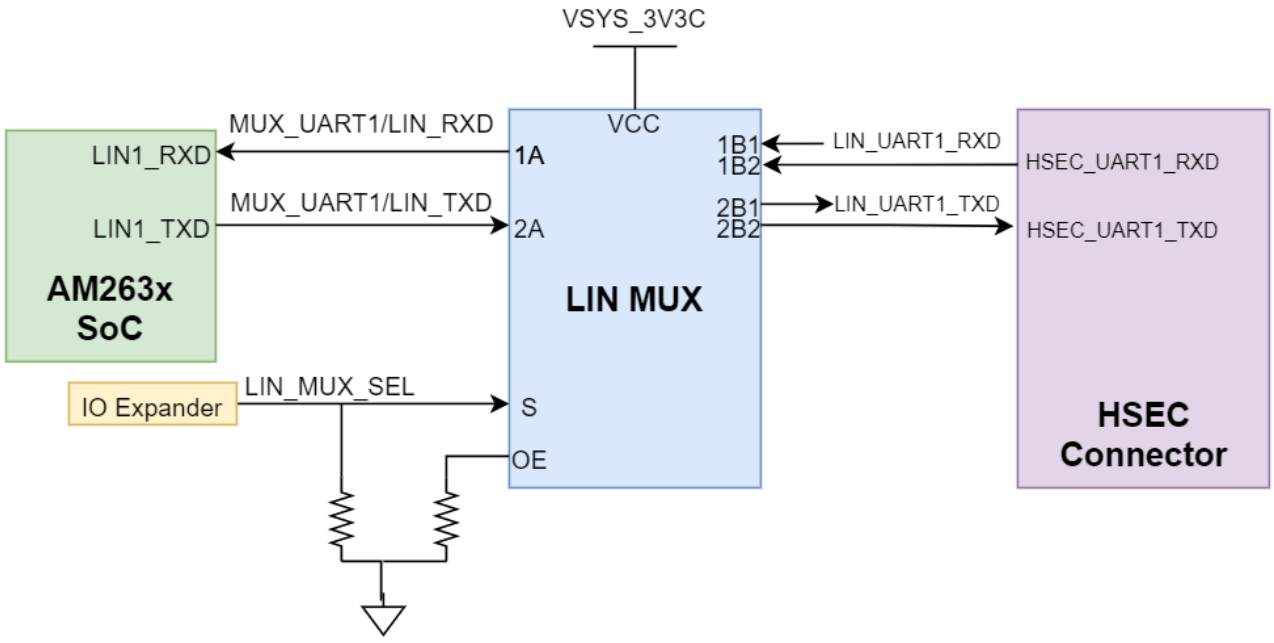



**Figure 2-27. UART 1:2 MUX to HSEC**

### 2.12.7 MCAN

The Control Card is equipped with a single MCAN transceiver (TCAN1024H-Q1) that is connected to the MCAN1 interface of the AM263x SoC. The MCAN0 interface of the AM263x SoC is mapped directly to the HSEC connector.

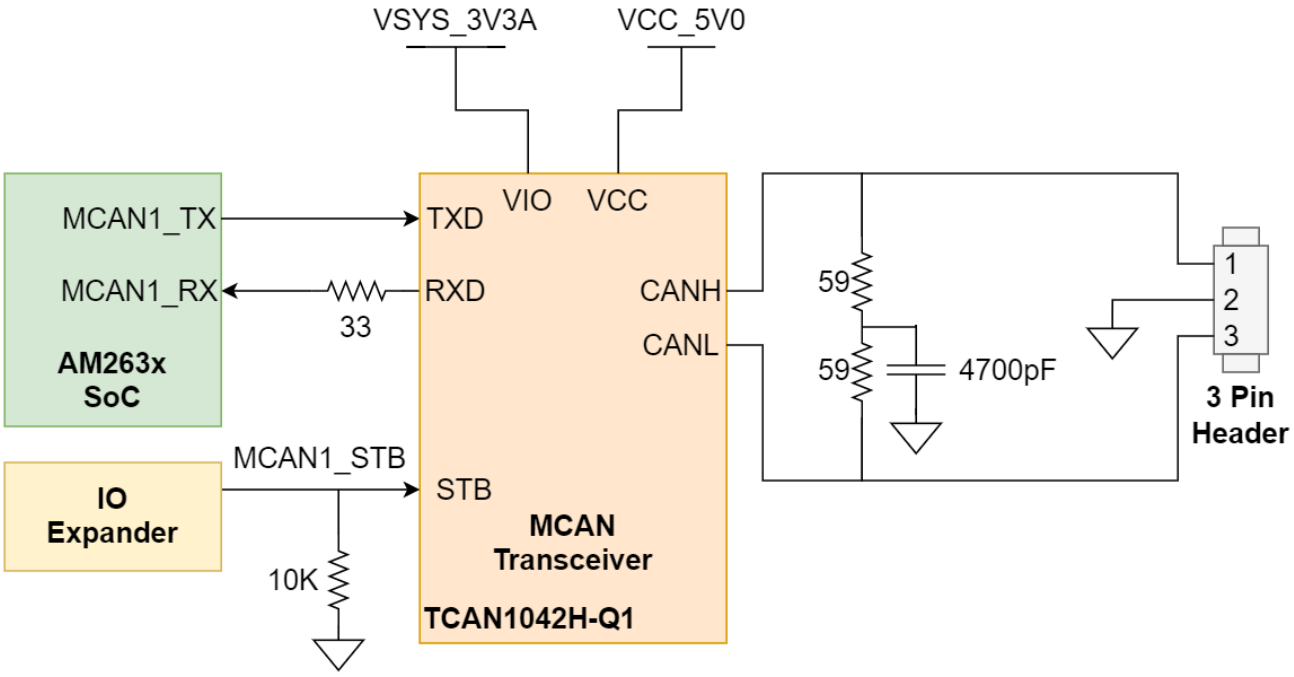



**Figure 2-28. MCAN Transceiver**

The MCAN transceiver has two power inputs, VIO is the transceiver I/O level shifting supply voltage and VCC is the transceiver 5 V supply voltage. The SoC CAN data transmit data input is mapped to TXD of the transceiver and the CAN receive data output of the transceiver is mapped to the MCAN RX signal of the SoC with a series termination resistor close to the transceiver.

The standby control signal is a GPIO signal sourced from the IO expander. The STB control input is active high and a pulldown resistor is used to have the transceiver operate in normal mode as opposed to the standby mode that is default due to a weak internal pull up.

The system has a 120 Ω split termination on the CANH and CANL signals to improve EMI performance. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

The low- and high-level CAN bus input output lines are terminated to a three pin header.

### 2.12.8 FSI

The AM263x Control Card supports a fast serial interface by terminating the SoC signals to a 10 pin header. The interface has two lines of data and a clock line for both the receive and transmit signals. The header is connected to the 3.3 V IO voltage supply (VSYS_3V3A).

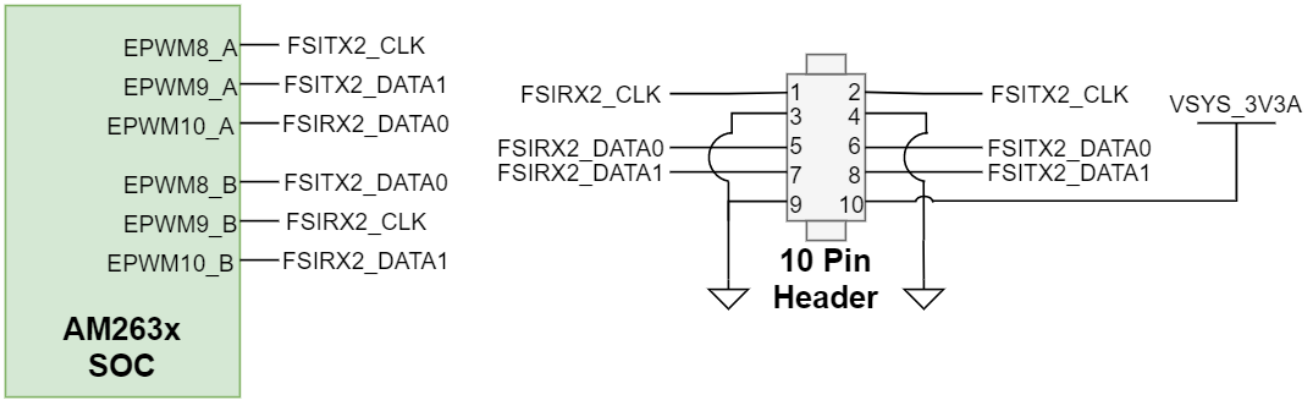



**Figure 2-29. FSI Header**

### 2.12.9 JTAG

The AM263x Control Card includes an XDS110 class on-board emulator. The control card also has the option to map the JTAG signals from the AM263x SoC to the HSEC connector.

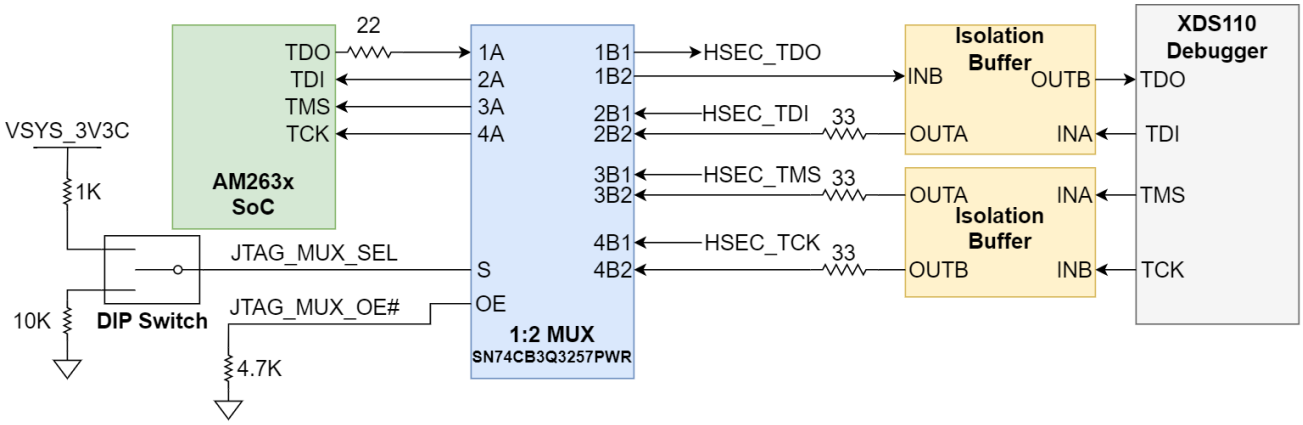



**Figure 2-30. JTAG**

A DIP switch is used to drive the select line of a 1:2 mux (SN74CB3Q3257PWR) that determines the path of the AM263x SoC JTAG signals. Figure 2-31 shows JTAG path selection for either switch position.

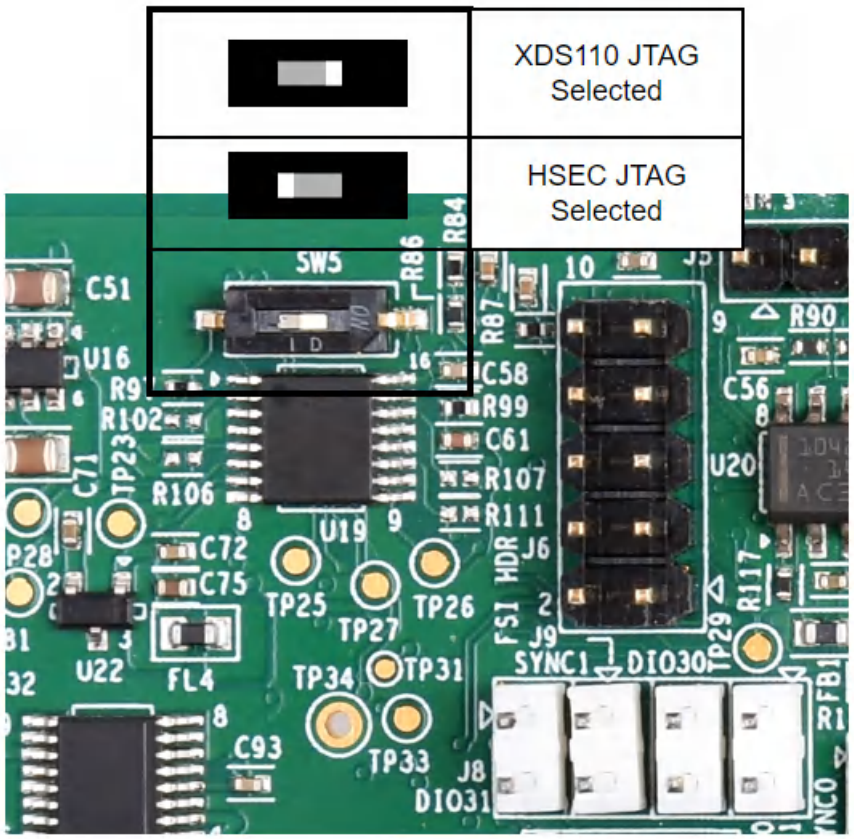



**Figure 2-31. JTAG Path Switch Position**

The Control Card includes all circuitry needed for XDS110 emulation. The emulator uses a USB 2.0 micro-B connector to interface the USB 2.0 signals that are created from the UART-USB bridge. The VBUS power from the connector is used to power the emulation circuit so that the connection to the emulator is not lost when power to the Control Card is removed.

The XDS110 controls two power status LED's. For more information refer to Section 2.3.2.

### 2.12.10 Test Automation Header

The AM263x Control Card supports a 40-pin test automation header that allows an external controller to manipulate basic operations such as power down, PORz, warm reset, and bootmode control.

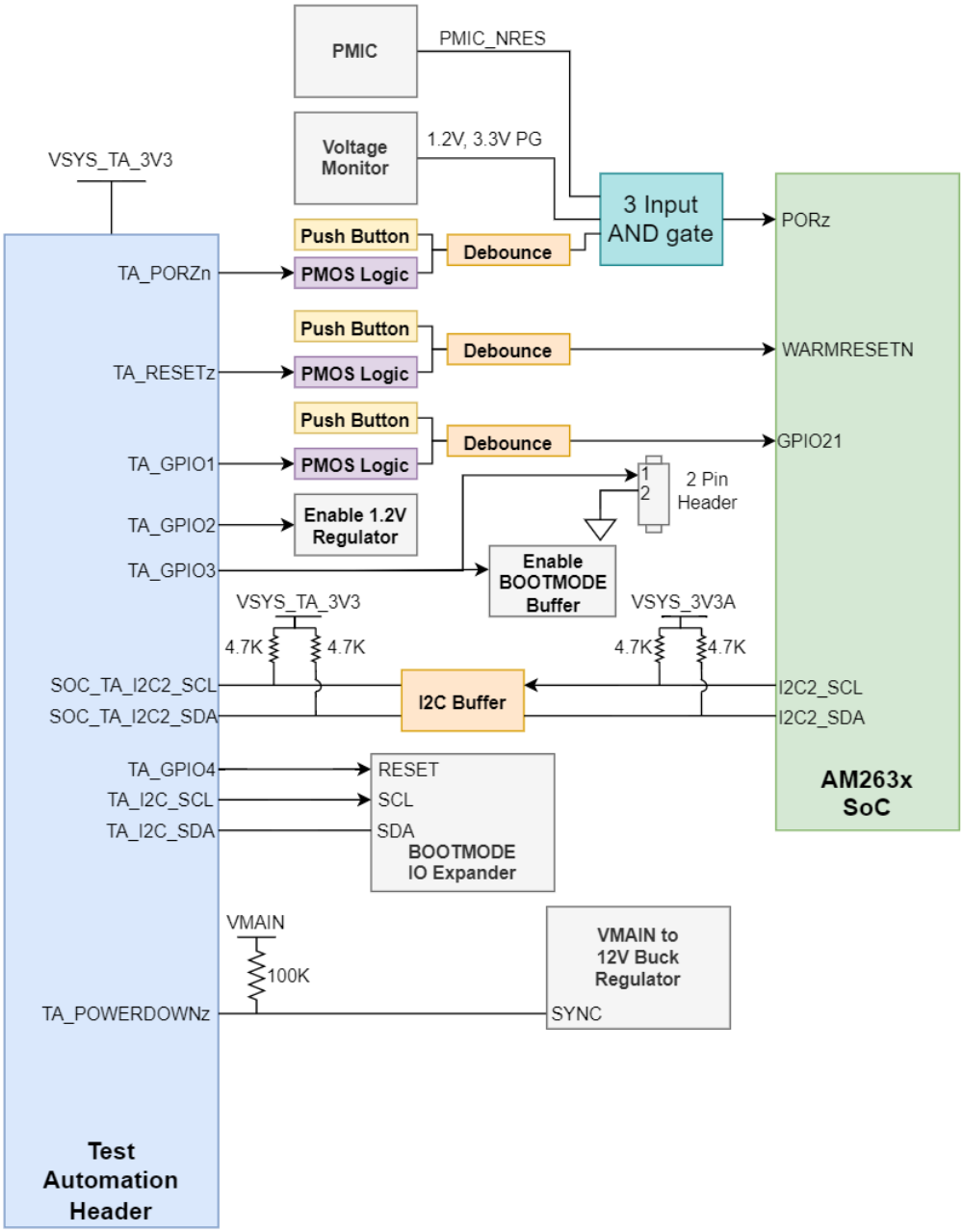



**Figure 2-32. Test Automation Header**

The Test Automation Circuit is powered by a dedicated 3.3 V power supply (VSYS_TA_3V3) that is generated by a 5 V to 3.3 V buck regulator (TPS62177DQCR).

The AM263x SoC I2C2 instance is connected to both the Test Automation Header and the bootmode IO expander (TCA6408ARGTR).

Test Automation Header GPIO Mapping details the Test Automation GPIO mapping:

**Table 2-24. Test Automation Header GPIO Mapping**

| Signal Name | Description | Direction |
|---|---|---|
| TA_POWERDOWN | When logic low, disables the 3.3 V buck regulator (TPS62913RPUR) that is used in the first stage of DC/DC conversion | Output |
| TA_PORZn | When logic low, connects the PORz signal to ground due to the PMOS V_GS being less than zero creating a power on reset to the MAIN domain | Output |
| TA_RESETz | When logic low, connects the WARMRESETn signal to ground due to the PMOS V_GS being less than zero creating a warm reset to the MAIN domain | Output |
| TA_GPIO1 | When logic low, connects the INTn signal to ground due to the PMOS V_GS being less than zero creating an interrupt to the SoC | Output |
| TA_GPIO2 | When logic low, disables the 1.2 V buck regulator (TPS62913RPUR) | Output |
| TA_GPIO3 | When logic low, disables the bootmode buffer output enable | Output |
| TA_GPIO4 | Reset signal for Bootmode IO Expander (TCA6408ARGTR) | Output |

### 2.12.11 LIN

The AM263x Control Card supports Local Interconnect Network communication through the use of a LIN transceiver (TLIN2029-Q1) that outputs the LIN Bus to the second pin of a 3 pin header.

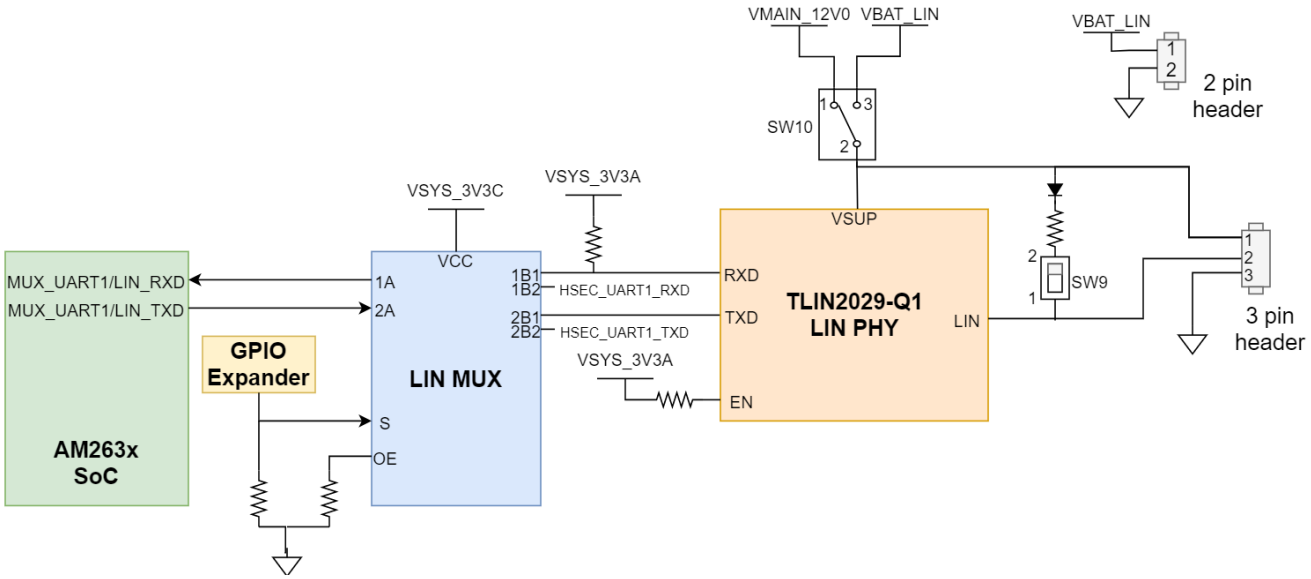



**Figure 2-33. LIN PHY**

The LIN transmit and receive signals are internally muxed on the AM263x with the UART1 transmit and receive signals. Because of the internal muxing, there is an external 1:2 mux (SN74CB3Q3257PWR) which has a select line that is driven by the GPIO Expander.

**Table 2-25. LIN MUX Select Logic**

| Select Logic | Condition | Function |
|---|---|---|
| LOW | LIN Selected | A→B1 |
| HIGH | HSEC UART Selected | A→B2 |

The AM263x SoC does not have an integrated pull up for the LIN RX signal, therefore, an external pull up resistor is needed to the processor I/O supply voltage is required.

The AM263x Control Card includes a double pole single throw switch (SW10) to control the voltage supply for the LIN Transceiver.

**Table 2-26. LIN Switch Logic**

| LIN Voltage Switch Position | Voltage Supply Selected |
|---|---|
| Pin 1-2 | VMAIN, 5 V supply output from either the USB-C connection or HSEC power connection. |
| Pin 2-3 | VBAT_LIN, external voltage supply from pin 1 of 2 pin header |

There is also a single pole throw switch (SW9) that drives the LIN Node application.

**Table 2-27. LIN Node Application Switch**

| LIN Node Application Switch Position | LIN Node Application |
|---|---|
| Pin 1 | Device node application |
| Pin 2 | Controller node application |

The Control Card pulls up the enable pin of the LIN transceiver for the transceiver to be in normal operational mode when the I/O Voltage supply is brought up.

### 2.12.12 MMC

The AM263x Control Card provides a micro SD card interface that is mapped to the MMC0 instance of the AM263x SoC.

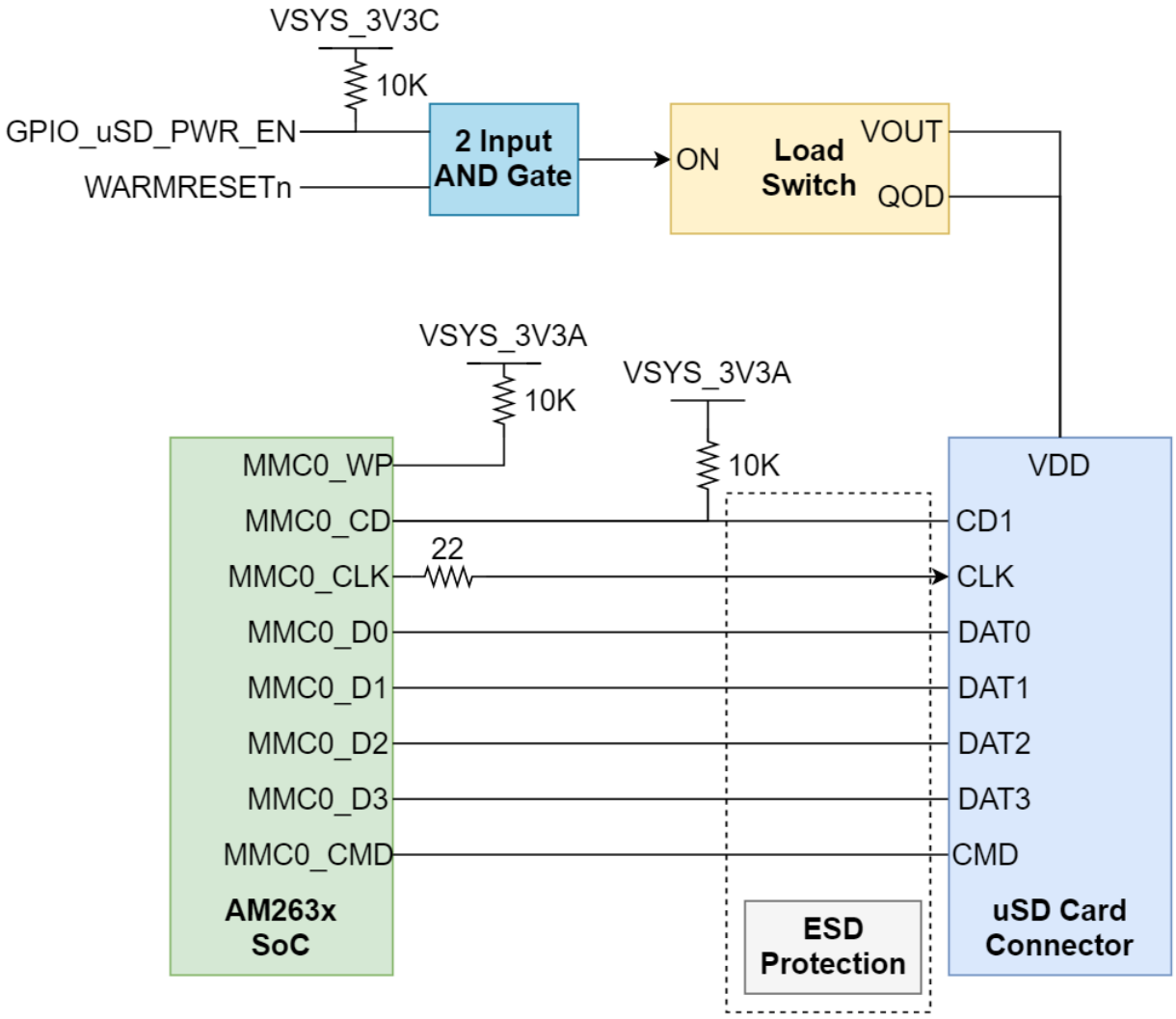



**Figure 2-34. Micro-SD Connector Interface**

A load switch (TPS22918DBVR) is used to power the micro SD card connector. The load switch is driven by the output of a 2-input AND gate between WARMRESETn and GPIO_uSD_PWR_EN to power cycle the card upon reset. The load switch uses quick output discharge (QOD) to make sure that the supply voltage reaches <10% of nominal value during reset.

Inline ESD protection is provided for the MMC signals in the form of a six channel transient voltage suppressor device (TPD6E001RSER).

The Write Protect (WP) and Card Detect (CD) signals of the SD card connector are pulled up to the 3.3 V IO voltage supply.

A series termination resistor is provided for the MMC clock signal.

### 2.12.13 ADC and DAC

The AM263x Control Card supports 24 ADC signal channels that are mapped for the AM263x SoC and terminated to the HSEC connector. All ADC signals are ESD protected (TPD4E001DBVR).

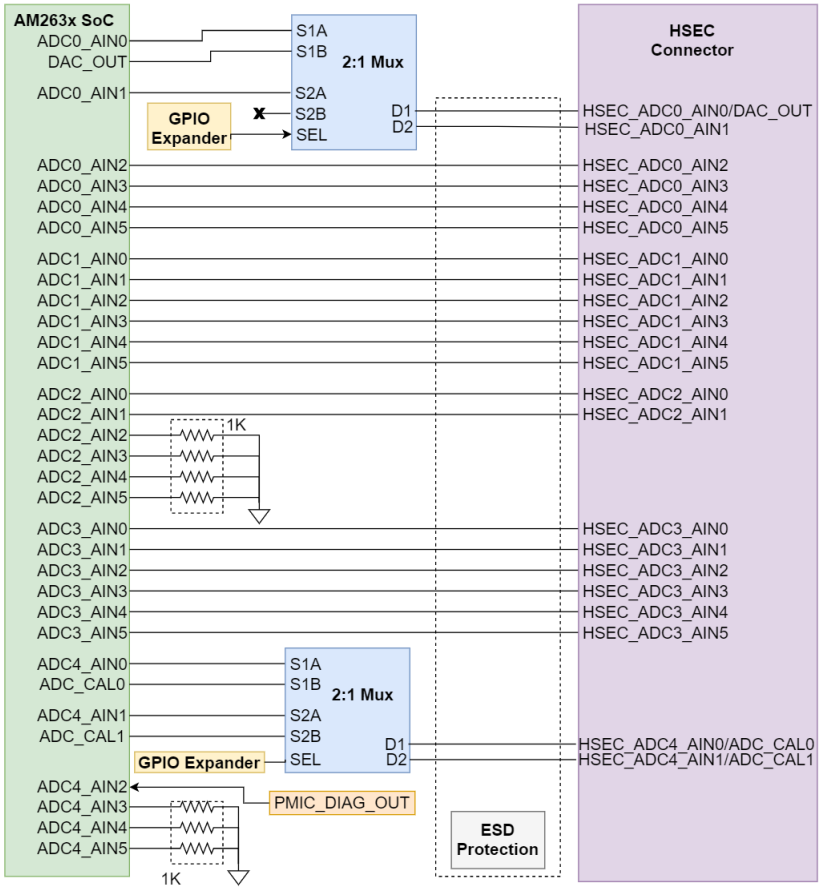



**Figure 2-35. ADC HSEC Connections**

There are two muxes (TMUX1136DQAR) that determine the pathing of ADC signals to and from the HSEC Connector.

**Table 2-28. ADC MUX Select Logic**

| MUX Select Signal | Condition | Function | Description |
|---|---|---|---|
| ADC1_MUX_SEL | SEL Signal HIGH | S1A → D1 | HSEC_ADC0_AIN0 selected |
| | | S2A → D2 | HSEC_ADC0_AIN1 selected |
| | SEL Signal LOW | S1B → D1 | HSEC_DAC_OUT selected |
| | | S2B → D2 | HSEC_DAC_OUT selected |
| ADC2_MUX_SEL | SEL Signal HIGH | S1A → D1 | HSEC_ADC4_AIN0 selected |
| | | S2A → D2 | HSEC_ADC4_AIN1 selected |
| | SEL Signal LOW | S1B → D1 | ADC_CAL0 selected |
| | | S2B → D2 | ADC_CAL1 selected |

There are three switches that are used to configure the reference voltages for the ADC and DAC.

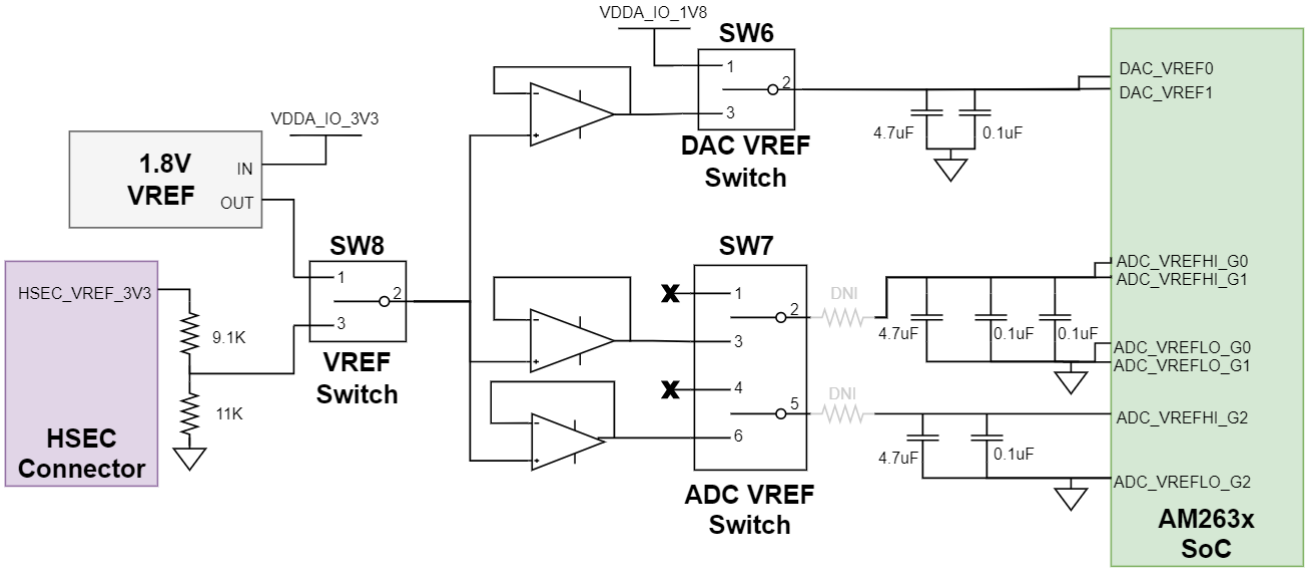



**Figure 2-36. ADC Switch Routing**

- The VREF Switch (SW8) is a single pole double throw switch that controls which 1.8 V reference is used for ADC and DAC.

**Table 2-29. VREF Switch**

| VREF Switch Position | Reference Selection |
|---|---|
| Pin 1-2 | On board 1.8 V Reference (REF3318AIDBZT) |
| Pin 2-3 | HSEC VREF |

- The DAC VREF Switch (SW6) is a single pole double throw switch that controls the input for the DAC VREF inputs of the AM263x SoC.

**Table 2-30. DAC VREF Switch**

| DAC VREF Switch Position | Reference Selection |
|---|---|
| Pin 1-2 | AM263x on-die LDO |
| Pin 2-3 | Output of VREF Switch |

- The ADC VREF Switch (SW7) contains two single pole double throw switches that control the input for the ADC VREF inputs of the AM263x SoC.

**Table 2-31. ADC VREF Switch**

| ADC VREF Switch Position | Reference Selection |
|---|---|
| Pin 1-2 | OPEN - Allow for reference to be AM263x on-die LDO reference |
| Pin 2-3 | Output of VREF Switch |
| Pin 4-5 | OPEN - Allow for reference to be AM263x on-die LDO reference |
| Pin 5-6 | Output of VREF Switch |

## 2.13 HSEC Pinout and Pinmux Mapping

Table 2-32 shows the pinout of the 180 High-Speed Edge Connector and all available pinmux options for each pin. Table 2-33 shows all AM263x balls and the available pinmux mode options for each ball.

**Table 2-32. HSEC Pinout**

| Pin # | Package Signal Name | Muxed Signal Options | | Muxed Signal Options | Signal Package Name | Pin # |
|---|---|---|---|---|---|---|
| 1 | NC | NC | | NC | NC | 2 |
| 3 | HSEC_TMS | TMS | | NC | NC | 4 |
| 5 | HSEC_TCK | TCK | | TDO | HSEC_TDO | 6 |
| 7 | GND | GND | | TDI | HSEC_TDI | 8 |
| 9 | HSEC_ADC0_AIN4/ DAC_OUT | HSEC_ADC0_AIN0/DAC_OUT | | GND | GND | 10 |
| 11 | HSEC_ADC0_AIN5/ DAC_OUT | HSEC_ADC0_AIN1/DAC_OUT | | ADC1_AIN0 | ADC1_AIN0 | 12 |
| 13 | GND | GND | | ADC1_AIN1 | ADC1_AIN1 | 14 |
| 15 | ADC0_AIN2 | ADC0_AIN2 | | GND | GND | 16 |
| 17 | ADC0_AIN3 | ADC0_AIN3 | | ADC1_AIN2 | ADC1_AIN2 | 18 |
| 19 | GND | GND | | ADC1_AIN3 | ADC1_AIN3 | 20 |
| 21 | ADC0_AIN4 | ADC0_AIN4 | | GND | GND | 22 |
| 23 | ADC0_AIN5 | ADC0_AIN5 | | ADC1_AIN4 | ADC1_AIN4 | 24 |
| 25 | ADC4_AIN0/ADC_CAL0 | ADC4_AIN0/ADC_CAL0 | | ADC1_AIN5 | ADC1_AIN5 | 26 |
| 27 | ADC4_AIN1/ADC_CAL1 | ADC4_AIN1/ADC_CAL1 | | ADC3_AIN0 | ADC3_AIN0 | 28 |
| 29 | GND | GND | | ADC3_AIN1 | ADC3_AIN1 | 30 |
| 31 | ADC2_AIN0 | ADC2_AIN0 | | GND | GND | 32 |
| 33 | ADC2_AIN1 | ADC2_AIN1 | | ADC3_AIN2 | ADC3_AIN2 | 34 |
| 35 | GND | GND | | ADC3_AIN3 | ADC3_AIN3 | 36 |
| 37 | ADC2_AIN2 | ADC2_AIN2 | | GND | GND | 38 |
| 39 | ADC2_AIN3 | ADC2_AIN3 | | ADC3_AIN4 | ADC3_AIN4 | 40 |
| 41 | NC | NC | | ADC3_AIN5 | ADC3_AIN5 | 42 |
| 43 | NC | NC | | NC | NC | 44 |
| 45 | HSEC_ADC-VREFHI | HSEC_ADC-VREFHI | | GND | GND | 46 |
| 47 | GND | GND | | HSEC_5V0 | HSEC_5V0 | 48 |
| 49 | EPWM0_A | EPWM0_A/GPIO43 | | EPWM2_A/GPIO47 | EPWM2_A | 50 |
| 51 | EPWM0_B | EPWM0_B/GPIO44 | | EPWM2_B/GPIO48 | EPWM2_B | 52 |
| 53 | EPWM1_A | EPWM1_A/GPIO45 | | EPWM3_A/GPIO49 | EPWM3_A | 54 |
| 55 | EPWM1_B | EPWM1_B/GPIO46 | | EPWM3_B/GPIO50 | EPWM3_B | 56 |
| 57 | EPWM4_A | EPWM4_A/GPIO51 | | EPWM6_A/FSIRX1_CLK/GPIO55 | EPWM6_A | 58 |
| 59 | EPWM4_B | EPWM4_B/FSITX1_CLK/GPIO52 | | EPWM6_B/FSIRX1_DATA0/GPIO56 | EPWM6_B | 60 |
| 61 | EPWM5_A | EPWM5_A/FSITX1_DATA0/GPIO53 | | EPWM7_A/FSIRX1_DATA1/GPIO57 | EPWM7_A | 62 |
| 63 | EPWM5_B | EPWM5_B/FSITX1_DATA1/GPIO54 | | EPWM7_B/GPIO58 | EPWM7_B | 64 |
| 65 | GND | GND | | NC | NC | 66 |
| 67 | SPI0_D0 | SPI0_D0/FSITX0_DATA0/GPIO13/SOP3 | | PR0_PRU1_GPO19/UART3_RXD/PR0_IEP0_EDC_SYNC_OUT0/TRC_CLK/ XBAROUT13/GPIO119/EQEP1_A | EQEP1_A | 68 |

**Table 2-32. HSEC Pinout (continued)**

| Pin # | Package Signal Name | Muxed Signal Options | | Muxed Signal Options | Signal Package Name | Pin # |
|---|---|---|---|---|---|---|
| 69 | SPI0_D1 | SPI0_D1/FSITX0_DATA1/GPIO14 | | PR0_PRU1_GPO18/UART3_TXD/PR0_IEP0_EDIO_DATA_IN_OUT31/TRC_CTL/ XBAROUT14/GPMC0_WAIT1/GPIO120/EQEP1_B | EQEP1_B | 70 |
| 71 | SPI0_CLK | SPI0_CLK/UART3_TXD/LIN3_TXD/FSITX0_CLK/GPIO12/SOP2 | | SDFM0_CLK0/CLKOUT1/GPIO122/EQEP1_STROBE | EQEP1_STROBE | 72 |
| 73 | SPI0_CS0 | SPI0_CS0/UART3_RXD/LIN3_RXD/GPIO11 | | EXT_REFCLK0/XBAROUT15/GPIO121/EQEP1_INDEX | EQEP1_INDEX | 74 |
| 75 | SPI1_D0 | SPI1_D0/UART5_TXD/XBAROUT3/FSIRX0_DATA0/GPIO17 | | LIN1_RXD/UART1_RXD/SPI2_CS0/XBAROUT5/GPIO19 | UART1_RXD | 76 |
| 77 | SPI1_D1 | SPI1_D1/UART5_RXD/XBAROUT4/FSIRX0_DATA1/GPIO18 | | LIN1_TXD/UART1_TXD/SPI2_CLK/XBAROUT6/GPIO20 | UART1_TXD | 78 |
| 79 | SPI1_CLK | SPI1_CLK/UART4_RXD/LIN4_RXD/XBAROUT2/FSIRX0_CLK/GPIO16 | | MCAN0_RX/SPI4_CS0/GPIO7 | MCAN0_RX | 80 |
| 81 | SPI1_CS0 | SPI1_CS0/UART4_TXD/LIN4_TXD/XBAROUT1/GPIO15 | | MCAN0_TX/SPI4_CLK/GPIO8 | MCAN0_TX | 82 |
| 83 | GND | GND | | HSEC_5V0 | HSEC_5V0 | 84 |
| 85 | I2C1_SDA | I2C1_SDA/SPI3_CLK/XBAROUT8/GPIO24 | | EPWM11_A/UART2_CTSn/GPMC0_CLKLB/GPIO65 | GPMC0_CLKB | 86 |
| 87 | I2C1_SCL | I2C1_SCL/SPI3_CS0/XBAROUT7/GPIO23 | | NC | NC | 88 |
| 89 | EPWM21_A | PR0_MDIO0_MDIO/EPWM21_A/GPMC0_CSn2/GPIO85 | | PR0_MDIO0_MDC/EPWM21_B/GPMC0_CSn3/GPIO86 | EPWM21_B | 90 |
| 91 | SDFM0_D0 | SDFM0_D0/PR0_ECAP0_APWM_OUT/GPIO123 | | I2C0_SDA/GPIO134/EQEP2_A/SDFM1_CLK2 | EQEP2_A | 92 |
| 93 | EQEP2_B | I2C0_SCL/GPIO135/EQEP2_B/SDFM1_CLK3 | | MCAN2_RX/UART2_RTSn/GPIO137/EQEP2_INDEX/SDFM1_D3 | EQEP2_INDEX | 94 |
| 95 | EQEP2_STROBE | MCAN2_TX/UART1_RTSn/GPIO136/EQEP2_STROBE/SDFM1_D2 | | NC | NC | 96 |
| 97 | GND | GND | | HSEC_5V0 | HSEC_5V0 | 98 |
| 99 | SDFM0_D1 | SDFM0_D1/PR0_PRU1_GPIO17/UART5_CTSn/ PR0_IEP0_EDIO_DATA_IN_OUT30/GPIO125 | | EQEP0_A/UART4_RTSn/SPI4_CLK/GPIO130/SDFM1_CLK0 | EQEP0_B | 100 |
| 101 | SDFM0_CLK1 | SDFM0_CLK1/PR0_PRU1_GPIO7/CPTS0_TS_SYNC/UART5_RTSn/ PR0_IEP0_EDC_SYNC_OUT1/I2C3_SDA/GPIO124 | | EQEP0_B/UART4_CTSn/SPI4_CS0/GPIO131/SDFM1_D0 | EQEP0_A | 102 |
| 103 | SDFM0_D2 | SDFM0_D2/UART5_RXD/GPIO127 | | EQEP0_STROBE/UART4_TXD/LIN4_TXD/SPI4_D0/GPIO132/SDFM1_CLK1 | EQEP0_STROBE | 104 |
| 105 | SDFM0_CLK2 | SDFM0_CLK2/UART5_TXD/I2C3_SCL/GPMC0_ADVn_ALE/GPIO126/ SDFM0_CLK2 | | EQEP0_INDEX/UART4_RXD/LIN4_RXD/SPI4_D1/GPIO133/SDFM1_D1 | EQEP0_INDEX | 106 |
| 107 | SDFM0_D3 | SDFM0_D3/MCAN3_RX/GPIO129 | | PR0_PRU0_GPO5/RMII2_RX_ER/MII2_RX_ER/EPWM22_A/GPMC0_DIR/ GPIO87 | MII0_RXER | 108 |
| 109 | SDFM0_CLK3 | SDFM0_CLK3/MCAN3_TX/UART5_RXD/GPIO128 | | PR0_PRU0_GPO9/PR0_UART0_CTSn/MII2_COL/EPWM22_B/GPMC0_CLK/ GPIO88 | MII0_CO | 110 |
| 111 | GND | GND | | HSEC_5V0 | HSEC_5V0 | 112 |
| 113 | NC | NC | | NC | NC | 114 |
| 115 | NC | NC | | NC | NC | 116 |
| 117 | NC | NC | | HSEC_5V0 | HSEC_5V0 | 118 |
| 119 | NC | NC | | PORz | PORz | 120 |
| | | | | | | |
| 121 | ICSS_MII0_CRS | PR0_PRU0_GPO10/RMII2_CRS_DV/PR0_UART0_RTSn/MII2_CRS/EPWM23_A/ GPMC0_WAIT0/GPIO89 | | PR0_PRU0_GPO8/EPWM23_B/GPMC0_WPn/GPIO90 | ICSS_MII0_RXLINK | 122 |
| 123 | ICSS_MII0_RXCLK | PR0_PRU0_GPO6/RMII2_REF_CLK/RGMII2_RXC/MII2_RXCLK/EPWM24_A/ GPMC0_CSn1/GPIO91 | | PR0_PRU0_GPO4/RGMII2_RX_CTL/MII2_RXDV/EPWM24_B/GPMC0_A0/ GPIO92 | ICSS_MII0_RXDV | 124 |
| 125 | ICSS_MII0_RXD0 | PR0_PRU0_GPO0/RMII2_RXD0/RGMII2_RD0/MII2_RXD0/EPWM25_A/ GPMC0_A1/GPIO93 | | PR0_PRU0_GPO1/RMII2_RXD1/RGMII2_RD1/MII2_RXD1/EPWM25_B/ GPMC0_A2/GPIO94 | ICSS_MII0_RXD1 | 126 |
| 127 | ICSS_MII0_RXD2 | PR0_PRU0_GPO2/RGMII2_RD2/MII2_RXD2/EPWM26_A/GPMC0_A3/GPIO95 | | PR0_PRU0_GPO3/RGMII2_RD3/MII2_RXD3/EPWM26_B/GPMC0_A4/GPIO96 | ICSS_MII0_RXD3 | 128 |
| 129 | ICSS_MII0_TXCLK | PR0_PRU0_GPO16/RGMII2_TXC/MII2_TXCLK/EPWM27_A/GPMC0_A5/GPIO97 | | PR0_PRU0_GPO15/RMII2_TX_EN/RGMII2_TX_CTL/MII2_TX_EN/EPWM27_B/ GPMC0_A6/GPIO98 | ICSS_MII0_TXEN | 130 |
| 131 | ICSS_MII0_TXD0 | PR0_PRU0_GPO11/RMII2_TXD0/RGMII2_TD0/MII2_TXD0/EPWM28_A/ GPMC0_A7/GPIO99 | | PR0_PRU0_GPO12/RMII2_TXD1/RGMII2_TD1/MII2_TXD1/EPWM28_B/ GPMC0_A8/GPIO100 | ICSS_MII0_TXD1 | 132 |
| 133 | ICSS_MII0_TXD2 | PR0_PRU0_GPO14/RGMII2_TD3/MII2_TXD3/EPWM29_B/GPMC0_A10/ GPIO102 | | PR0_PRU0_GPO14/RGMII2_TD3/MII2_TXD3/EPWM29_B/GPMC0_A10/ GPIO102 | ICSS_MII0_TXD3 | 134 |

**Table 2-32. HSEC Pinout (continued)**

| Pin # | Package Signal Name | Muxed Signal Options | | Muxed Signal Options | Signal Package Name | Pin # |
|---|---|---|---|---|---|---|
| 135 | GND | GND | | NC | NC | 136 |
| 137 | ICSS_MII1_RXER | PR0_PRU1_GPO5/TRC_DATA0/EPWM30_A/GPMC0_OEn_REn/GPIO103 | | PR0_PRU1_GPO9/PR0_UART0_RXD/TRC_DATA1/EPWM30_B/ GPMC0_BE0n_CLE/GPIO104 | ICSS_MII1_COL | 138 |
| 139 | ICSS_MII1_CRS | PR0_PRU1_GPO10/PR0_UART0_TXD/TRC_DATA2/EPWM31_A/GPMC0_BE1n/ GPIO105 | | PR0_PRU1_GPO8/TRC_DATA3/EPWM31_B/GPMC0_WEn/GPIO106 | ICSS_MII1_RXLINK | 140 |
| 141 | ICSS_MII1_RXCLK | PR0_PRU1_GPO6/FSITX2_CLK/TRC_DATA4/GPMC0_A11/GPIO107 | | PR0_PRU1_GPO4/FSITX2_DATA0/TRC_DATA5/GPMC0_A12/GPIO108 | ICSS_MII1_RXDV | 142 |
| 143 | ICSS_MII1_RXD0 | PR0_PRU1_GPO0/FSITX2_DATA1/TRC_DATA6/GPMC0_A13/GPIO109 | | PR0_PRU1_GPO1/FSIRX2_CLK/TRC_DATA7/GPMC0_A14/GPIO110 | ICSS_MII1_RXD1 | 144 |
| 145 | ICSS_MII1_RXD2 | PR0_PRU1_GPO2/FSIRX2_DATA0/TRC_DATA8/GPMC0_A15/GPIO111 | | PR0_PRU1_GPO3/FSIRX2_DATA1/TRC_DATA9/GPMC0_A16/GPIO112 | ICSS_MII1_RXD3 | 146 |
| 147 | ICSS_MII1_TXCLK | PR0_PRU1_GPO16/FSITX3_CLK/TRC_DATA10/GPMC0_A17/GPIO113 | | PR0_PRU1_GPO15/FSITX3_DATA0/TRC_DATA11/GPMC0_A18/GPIO114 | ICSS_MII1_TXEN | 148 |
| 149 | ICSS_MII1_TXD0 | PR0_PRU1_GPO11/FSITX3_DATA1/TRC_DATA12/GPMC0_A19/GPIO115 | | PR0_PRU1_GPO12/FSIRX3_CLK/TRC_DATA13/GPMC0_A20/GPIO116 | ICSS_MII1_TXD1 | 150 |
| 151 | ICSS_MII1_TXD2 | PR0_PRU1_GPO13/FSIRX3_DATA0/TRC_DATA14/XBAROUT11/GPMC0_A21/ GPIO117 | | PR0_PRU1_GPO14/FSIRX3_DATA1/TRC_DATA15/XBAROUT12/GPMC0_CSn0/ GPIO118 | ICSS_MII1_TXD3 | 152 |
| 153 | GPMC0_AD0 | EPWM13_A/UART1_RIn/GPMC0_AD0/GPIO69 | | EPWM13_B/UART1_DTRn/GPMC0_AD1/GPIO70 | GPMC0_AD1 | 154 |
| 155 | GPMC0_AD2 | EPWM14_A/UART1_DSRn/GPMC0_AD2/GPIO71 | | EPWM14_B/MII1_RX_ER/GPMC0_AD3/GPIO72 | GPMC0_AD3 | 156 |
| 157 | GND | GND | | HSEC_5V0 | HSEC_5V0 | 158 |
| 159 | GPMC0_AD4 | EPWM15_A/UART5_TXD/MII1_COL/GPMC0_AD4/GPIO73 | | EPWM15_B/UART5_RXD/MII1_CRS/GPMC0_AD5/GPIO74 | GPMC0_AD5 | 160 |
| 161 | GPMC0_AD6 | UART1_RXD/LIN1_RXD/EPWM16_A/GPMC0_AD6/GPIO75 | | UART1_TXD/LIN1_TXD/EPWM16_B/GPMC0_AD7/GPIO76 | GPMC0_AD7 | 162 |
| 163 | GPMC0_AD8 | MMC0_CLK/UART0_RXD/LIN0_RXD/EPWM17_A/GPMC0_AD8/GPIO77/ SDFM1_CLK0 | | MMC0_CMD/UART0_TXD/LIN0_TXD/EPWM17_B/GPMC0_AD9/GPIO78/ SDFM1_D0 | GPMC0_AD9 | 164 |
| 165 | GPMC0_AD10 | MMC0_D0/UART2_RXD/I2C1_SCL/EPWM18_A/GPMC0_AD10/GPIO79/ SDFM1_CLK1 | | MMC0_D1/EPWM18_B/GPMC0_AD11/GPIO80/SDFM1_D1 | GPMC0_AD11 | 166 |
| 167 | GPMC0_AD12 | MMC0_D2/UART2_TXD/I2C1_SDA/EPWM19_A/GPMC0_AD12/GPIO81/ SDFM1_CLK2 | | MMC0_D3/UART3_RTSn/EPWM19_B/GPMC0_AD13/GPIO82/SDFM1_D2 | GPMC0_AD13 | 168 |
| 169 | GPMC0_AD14 | MMC0_WP/UART0_RTSn/I2C2_SCL/EPWM20_A/GPMC0_AD14/GPIO83/ SDFM1_CLK3 | | MMC0_CD/UART0_CTSn/I2C2_SDA/EPWM20_B/GPMC0_AD15/GPIO84/ SDFM1_D3 | GPMC0_AD15 | 170 |
| 171 | NC | NC | | NC | NC | 172 |
| 173 | NC | NC | | NC | NC | 174 |
| 175 | NC | NC | | NC | NC | 176 |
| 177 | NC | NC | | NC | NC | 178 |
| 179 | GND | GND | | HSEC_5V0 | HSEC_5V0 | 180 |

**Table 2-33. Pinmux Mapping Table**

| Pin# | Pinlist | Mode0 | Mode1 | Mode2 | Mode3 | Mode4 | Mode5 | Mode6 | Mode7 | Mode8 | Mode9 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| U16 | **ADC_CAL0** | ADC_CAL0 | | | | | | | | | |
| T15 | **ADC_CAL1** | ADC_CAL1 | | | | | | | | | |
| V14 | **ADC_VREFHI_G0** | ADC_VREFHI_G0 | | | | | | | | | |
| V10 | **ADC_VREFHI_G1** | ADC_VREFHI_G1 | | | | | | | | | |
| V6 | **ADC_VREFHI_G2** | ADC_VREFHI_G2 | | | | | | | | | |
| V13 | **ADC_VREFLO_G0** | ADC_ VREFLOSRC0 | | | | | | | | | |
| V11 | **ADC_VREFLO_G1** | ADC_ VREFLO1 | | | | | | | | | |
| V7 | **ADC_VREFLO_G2** | ADC_ VREFLOSRC1 | | | | | | | | | |
| V15 | **ADC0_AIN0** | ADC0_AIN0 | | | | | | | | | |

**Table 2-33. Pinmux Mapping Table (continued)**

| Pin# | Pinlist | Mode0 | Mode1 | Mode2 | Mode3 | Mode4 | Mode5 | Mode6 | Mode7 | Mode8 | Mode9 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| U15 | **ADC0_AIN1** | ADC0_AIN1 | | | | | | | | | |
| T14 | **ADC0_AIN2** | ADC0_AIN2 | | | | | | | | | |
| U14 | **ADC0_AIN3** | ADC0_AIN3 | | | | | | | | | |
| U13 | **ADC0_AIN4** | ADC0_AIN4 | | | | | | | | | |
| R14 | **ADC0_AIN5** | ADC0_AIN5 | | | | | | | | | |
| T11 | **ADC1_AIN0** | ADC1_AIN0 | | | | | | | | | |
| U11 | **ADC1_AIN1** | ADC1_AIN1 | | | | | | | | | |
| T12 | **ADC1_AIN2** | ADC1_AIN2 | | | | | | | | | |
| V12 | **ADC1_AIN3** | ADC1_AIN3 | | | | | | | | | |
| U12 | **ADC1_AIN4** | ADC1_AIN4 | | | | | | | | | |
| R12 | **ADC1_AIN5** | ADC1_AIN5 | | | | | | | | | |
| R10 | **ADC2_AIN0** | ADC2_AIN0 | | | | | | | | | |
| T10 | **ADC2_AIN1** | ADC2_AIN1 | | | | | | | | | |
| U10 | **ADC2_AIN2** | ADC2_AIN2 | | | | | | | | | |
| T9 | **ADC2_AIN3** | ADC2_AIN3 | | | | | | | | | |
| V9 | **ADC2_AIN4** | ADC2_AIN4 | | | | | | | | | |
| T8 | **ADC2_AIN5** | ADC2_AIN5 | | | | | | | | | |
| U7 | **ADC3_AIN0** | ADC3_AIN0 | | | | | | | | | |
| U8 | **ADC3_AIN1** | ADC3_AIN1 | | | | | | | | | |
| T7 | **ADC3_AIN2** | ADC3_AIN2 | | | | | | | | | |
| R7 | **ADC3_AIN3** | ADC3_AIN3 | | | | | | | | | |
| V8 | **ADC3_AIN4** | ADC3_AIN4 | | | | | | | | | |
| U9 | **ADC3_AIN5** | ADC3_AIN5 | | | | | | | | | |
| U6 | **ADC4_AIN0** | ADC4_AIN0 | | | | | | | | | |
| V5 | **ADC4_AIN1** | ADC4_AIN1 | | | | | | | | | |
| V4 | **ADC4_AIN2** | ADC4_AIN2 | | | | | | | | | |
| U5 | **ADC4_AIN3** | ADC4_AIN3 | | | | | | | | | |
| V3 | **ADC4_AIN4** | ADC4_AIN4 | | | | | | | | | |
| U4 | **ADC4_AIN5** | ADC4_AIN5 | | | | | | | | | |
| U3 | **ATESTV0** | ATESTV0 | | | | | | | | | |
| V2 | **ATESTV1** | ATESTV1 | | | | | | | | | |
| M2 | **CLKOUT0** | CLKOUT0 | | | | | | | GPIO138 | | |
| T5 | **DAC_OUT** | DAC_OUT | | | | | | | | | |
| T13 | **DAC_VREF0** | DAC_VREF0 | | | | | | | | | |
| T6 | **DAC_VREF1** | DAC_VREF1 | | | | | | | | | |
| B2 | **EPWM0_A** | EPWM0_A | | | | | | | GPIO43 | | |
| B1 | **EPWM0_B** | EPWM0_B | | | | | | | GPIO44 | | |
| D3 | **EPWM1_A** | EPWM1_A | | | | | | | GPIO45 | | |
| D2 | **EPWM1_B** | EPWM1_B | | | | | | | GPIO46 | | |
| G4 | **EPWM10_A** | EPWM10_A | UART1_CTSn | | | | | FSIRX2_DATA0 | GPIO63 | | |
| J3 | **EPWM10_B** | EPWM10_B | UART2_RTSn | | | | | FSIRX2_DATA1 | GPIO64 | | |

**Table 2-33. Pinmux Mapping Table (continued)**

| Pin# | Pinlist | Mode0 | Mode1 | Mode2 | Mode3 | Mode4 | Mode5 | Mode6 | Mode7 | Mode8 | Mode9 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| H1 | **EPWM11_A** | EPWM11_A | UART2_CTSn | | | | | GPMC0_CLKLB | GPIO65 | | |
| J1 | **EPWM11_B** | EPWM11_B | UART3_RTSn | | | | | GPMC0_OEn_REn | GPIO66 | | |
| K2 | **EPWM12_A** | EPWM12_A | UART3_CTSn | SPI4_CS1 | | | | GPMC0_WEn | GPIO67 | | |
| J4 | **EPWM12_B** | EPWM12_B | UART1_DCDn | | | | | GPMC0_CSn0 | GPIO68 | | |
| K4 | **EPWM13_A** | EPWM13_A | UART1_RIn | | | | | GPMC0_AD0 | GPIO69 | | |
| K3 | **EPWM13_B** | EPWM13_B | UART1_DTRn | | | | | GPMC0_AD1 | GPIO70 | | |
| V17 | **EPWM14_A** | EPWM14_A | UART1_DSRn | | | | | GPMC0_AD2 | GPIO71 | | |
| T16 | **EPWM14_B** | EPWM14_B | | MII1_RX_ER | | | | GPMC0_AD3 | GPIO72 | | |
| P15 | **EPWM15_A** | EPWM15_A | UART5_TXD | MII1_COL | | | | GPMC0_AD4 | GPIO73 | | |
| R16 | **EPWM15_B** | EPWM15_B | UART5_RXD | MII1_CRS | | | | GPMC0_AD5 | GPIO74 | | |
| C2 | **EPWM2_A** | EPWM2_A | | | | | | | GPIO47 | | |
| C1 | **EPWM2_B** | EPWM2_B | | | | | | | GPIO48 | | |
| E2 | **EPWM3_A** | EPWM3_A | | | | | | | GPIO49 | | |
| E3 | **EPWM3_B** | EPWM3_B | | | | | | | GPIO50 | | |
| D1 | **EPWM4_A** | EPWM4_A | | | | | | | GPIO51 | | |
| E4 | **EPWM4_B** | EPWM4_B | | | | | | FSITX1_CLK | GPIO52 | | |
| F2 | **EPWM5_A** | EPWM5_A | | | | | | FSITX1_DATA0 | GPIO53 | | |
| G2 | **EPWM5_B** | EPWM5_B | | | | | | FSITX1_DATA1 | GPIO54 | | |
| E1 | **EPWM6_A** | EPWM6_A | | | | | | FSIRX1_CLK | GPIO55 | | |
| F3 | **EPWM6_B** | EPWM6_B | | | | | | FSIRX1_DATA0 | GPIO56 | | |
| F4 | **EPWM7_A** | EPWM7_A | | | | | | FSIRX1_DATA1 | GPIO57 | | |
| F1 | **EPWM7_B** | EPWM7_B | | | | | | | GPIO58 | | |
| G3 | **EPWM8_A** | EPWM8_A | UART4_TXD | I2C3_SDA | | | | FSITX2_CLK | GPIO59 | | |
| H2 | **EPWM8_B** | EPWM8_B | UART4_RXD | I2C3_SCL | | | | FSITX2_DATA0 | GPIO60 | | |
| G1 | **EPWM9_A** | EPWM9_A | | | | | | FSITX2_DATA1 | GPIO61 | | |
| J2 | **EPWM9_B** | EPWM9_B | UART1_RTSn | | | | | FSIRX2_CLK | GPIO62 | | |
| B14 | **EQEP0_A** | UART4_RTSn | | | SPI4_CLK | | | | GPIO130 | EQEP0_A | SDFM1_CLK0 |
| A14 | **EQEP0_B** | UART4_CTSn | | | SPI4_CS0 | | | | GPIO131 | EQEP0_B | SDFM1_D0 |
| D11 | **EQEP0_INDEX** | UART4_RXD | LIN4_RXD | | SPI4_D1 | | | | GPIO133 | EQEP0_INDEX | SDFM1_D1 |
| C12 | **EQEP0_STROBE** | UART4_TXD | LIN4_TXD | | SPI4_D0 | | | | GPIO132 | EQEP0_STROBE | SDFM1_CLK1 |
| P2 | **EXT_REFCLK0** | EXT_REFCLK0 | | | | | XBAROUT15 | | GPIO121 | | EQEP1_INDEX |
| A13 | **I2C0_SCL** | I2C0_SCL | | | | | | | GPIO135 | EQEP2_B | SDFM1_CLK3 |
| B13 | **I2C0_SDA** | I2C0_SDA | | | | | | | GPIO134 | EQEP2_A | SDFM1_CLK2 |
| D7 | **I2C1_SCL** | I2C1_SCL | | SPI3_CS0 | | | XBAROUT7 | | GPIO23 | | |
| C8 | **I2C1_SDA** | I2C1_SDA | | SPI3_CLK | | | XBAROUT8 | | GPIO24 | | |
| A9 | **LIN1_RXD** | LIN1_RXD | UART1_RXD | SPI2_CS0 | | | XBAROUT5 | | GPIO19 | | |
| B9 | **LIN1_TXD** | LIN1_TXD | UART1_TXD | SPI2_CLK | | | XBAROUT6 | | GPIO20 | | |
| B8 | **LIN2_RXD** | LIN2_RXD | UART2_RXD | SPI2_D0 | | | | | GPIO21 | | |
| A8 | **LIN2_TXD** | LIN2_TXD | UART2_TXD | SPI2_D1 | | | | | GPIO22 | | |
| M1 | **MCAN0_RX** | MCAN0_RX | SPI4_CS0 | | | | | | GPIO7 | | |
| L1 | **MCAN0_TX** | MCAN0_TX | SPI4_CLK | | | | | | GPIO8 | | |

**Table 2-33. Pinmux Mapping Table (continued)**

| Pin# | Pinlist | Mode0 | Mode1 | Mode2 | Mode3 | Mode4 | Mode5 | Mode6 | Mode7 | Mode8 | Mode9 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| L2 | **MCAN1_RX** | MCAN1_RX | SPI4_D0 | | | | | | GPIO9 | | |
| K1 | **MCAN1_TX** | MCAN1_TX | SPI4_D1 | | | | | | GPIO10 | | |
| A12 | **MCAN2_RX** | MCAN2_RX | UART2_RTSn | | | | | | GPIO137 | EQEP2_INDEX | SDFM1_D3 |
| B12 | **MCAN2_TX** | MCAN2_TX | UART1_RTSn | | | | | | GPIO136 | EQEP2_STROBE | SDFM1_D2 |
| M17 | **MDIO0_MDC** | MDIO0_MDC | | | | | | | GPIO42 | | |
| N16 | **MDIO0_MDIO** | MDIO0_MDIO | | | | | | | GPIO41 | | |
| A5 | **MMC0_CD** | MMC0_CD | UART0_CTSn | I2C2_SDA | | | EPWM20_B | GPMC0_AD15 | GPIO84 | SDFM1_D3 | |
| B6 | **MMC0_CLK** | MMC0_CLK | UART0_RXD | LIN0_RXD | | | EPWM17_A | GPMC0_AD8 | GPIO77 | SDFM1_CLK0 | |
| A4 | **MMC0_CMD** | MMC0_CMD | UART0_TXD | LIN0_TXD | | | EPWM17_B | GPMC0_AD9 | GPIO78 | SDFM1_D0 | |
| B5 | **MMC0_D0** | MMC0_D0 | UART2_RXD | I2C1_SCL | | | EPWM18_A | GPMC0_AD10 | GPIO79 | SDFM1_CLK1 | |
| B4 | **MMC0_D1** | MMC0_D1 | | | | | EPWM18_B | GPMC0_AD11 | GPIO80 | SDFM1_D1 | |
| A3 | **MMC0_D2** | MMC0_D2 | UART2_TXD | I2C1_SDA | | | EPWM19_A | GPMC0_AD12 | GPIO81 | SDFM1_CLK2 | |
| A2 | **MMC0_D3** | MMC0_D3 | UART3_RTSn | | | | EPWM19_B | GPMC0_AD13 | GPIO82 | SDFM1_D2 | |
| C6 | **MMC0_WP** | MMC0_WP | UART0_RTSn | I2C2_SCL | | | EPWM20_A | GPMC0_AD14 | GPIO83 | SDFM1_CLK3 | |
| R2 | **PORZ** | PORZ | | | | | | | | | |
| L18 | **PR0_MDIO0_MDC** | PR0_MDIO0_MDC | | | | | EPWM21_B | GPMC0_CSn3 | GPIO86 | | |
| L17 | **PR0_MDIO0_ MDIO** | PR0_MDIO0_ MDIO | | | | | EPWM21_A | GPMC0_CSn2 | GPIO85 | | |
| K17 | **PR0_PRU0_GPO0** | PR0_PRU0_ GPIO0 | | RMII2_RXD0 | RGMII2_RD0 | MII2_RXD0 | EPWM25_A | GPMC0_A1 | GPIO93 | | |
| K18 | **PR0_PRU0_GPO1** | PR0_PRU0_ GPIO1 | | RMII2_RXD1 | RGMII2_RD1 | MII2_RXD1 | EPWM25_B | GPMC0_A2 | GPIO94 | | |
| G18 | **PR0_PRU0_ GPO10** | PR0_PRU0_ GPIO10 | | RMII2_CRS_DV | PR0_UART0_RTSn | MII2_CRS | EPWM23_A | GPMC0_WAIT0 | GPIO89 | | |
| M16 | **PR0_PRU0_GPO11** | PR0_PRU0_ GPIO11 | | RMII2_TXD0 | RGMII2_TD0 | MII2_TXD0 | EPWM28_A | GPMC0_A7 | GPIO99 | | |
| M15 | **PR0_PRU0_ GPO12** | PR0_PRU0_ GPIO12 | | RMII2_TXD1 | RGMII2_TD1 | MII2_TXD1 | EPWM28_B | GPMC0_A8 | GPIO100 | | |
| H17 | **PR0_PRU0_ GPO13** | PR0_PRU0_ GPIO13 | | | RGMII2_TD2 | MII2_TXD2 | EPWM29_A | GPMC0_A9 | GPIO101 | | |
| H16 | **PR0_PRU0_ GPO14** | PR0_PRU0_ GPIO14 | | | RGMII2_TD3 | MII2_TXD3 | EPWM29_B | GPMC0_A10 | GPIO102 | | |
| L16 | **PR0_PRU0_ GPO15** | PR0_PRU0_ GPIO15 | | RMII2_TX_EN | RGMII2_TX_CTL | MII2_TX_EN | EPWM27_B | GPMC0_A6 | GPIO98 | | |
| H18 | **PR0_PRU0_ GPO16** | PR0_PRU0_ GPIO16 | | | RGMII2_TXC | MII2_TXCLK | EPWM27_A | GPMC0_A5 | GPIO97 | | |
| J18 | **PR0_PRU0_GPO2** | PR0_PRU0_ GPIO2 | | | RGMII2_RD2 | MII2_RXD2 | EPWM26_A | GPMC0_A3 | GPIO95 | | |
| J17 | **PR0_PRU0_GPO3** | PR0_PRU0_ GPIO3 | | | RGMII2_RD3 | MII2_RXD3 | EPWM26_B | GPMC0_A4 | GPIO96 | | |
| K16 | **PR0_PRU0_GPO4** | PR0_PRU0_ GPIO4 | | | RGMII2_RX_CTL | MII2_RXDV | EPWM24_B | GPMC0_A0 | GPIO92 | | |
| G17 | **PR0_PRU0_GPO5** | PR0_PRU0_ GPIO5 | | RMII2_RX_ER | | MII2_RX_ER | EPWM22_A | GPMC0_DIR | GPIO87 | | |
| K15 | **PR0_PRU0_GPO6** | PR0_PRU0_ GPIO6 | | RMII2_REF_CLK | RGMII2_RXC | MII2_RXCLK | EPWM24_A | GPMC0_CSn1 | GPIO91 | | |

**Table 2-33. Pinmux Mapping Table (continued)**

| Pin# | Pinlist | Mode0 | Mode1 | Mode2 | Mode3 | Mode4 | Mode5 | Mode6 | Mode7 | Mode8 | Mode9 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| G15 | **PR0_PRU0_GPO8** | PR0_PRU0_GPIO8 | | | | | EPWM23_B | GPMC0_WPn | GPIO90 | | |
| F17 | **PR0_PRU0_GPO9** | PR0_PRU0_GPIO9 | | | PR0_UART0_CTSn | MII2_COL | EPWM22_B | GPMC0_CLK | GPIO88 | | |
| F18 | **PR0_PRU1_GPO0** | PR0_PRU1_GPIO0 | | | FSITX2_DATA1 | TRC_DATA6 | | GPMC0_A13 | GPIO109 | | |
| G16 | **PR0_PRU1_GPO1** | PR0_PRU1_GPIO1 | | | FSIRX2_CLK | TRC_DATA7 | | GPMC0_A14 | GPIO110 | | |
| D17 | **PR0_PRU1_GPO10** | PR0_PRU1_GPIO10 | | | PR0_UART0_TXD | TRC_DATA2 | EPWM31_A | GPMC0_BE1n | GPIO105 | | |
| B18 | **PR0_PRU1_GPO11** | PR0_PRU1_GPIO11 | | | FSITX3_DATA1 | TRC_DATA12 | | GPMC0_A19 | GPIO115 | | |
| B17 | **PR0_PRU1_GPO12** | PR0_PRU1_GPIO12 | | | FSIRX3_CLK | TRC_DATA13 | | GPMC0_A20 | GPIO116 | | |
| D16 | **PR0_PRU1_GPO13** | PR0_PRU1_GPIO13 | | | FSIRX3_DATA0 | TRC_DATA14 | XBAROUT11 | GPMC0_A21 | GPIO117 | | |
| C17 | **PR0_PRU1_GPO14** | PR0_PRU1_GPIO14 | | | FSIRX3_DATA1 | TRC_DATA15 | XBAROUT12 | GPMC0_CSn0 | GPIO118 | | |
| A17 | **PR0_PRU1_GPO15** | PR0_PRU1_GPIO15 | | | FSITX3_DATA0 | TRC_DATA11 | | GPMC0_A18 | GPIO114 | | |
| C16 | **PR0_PRU1_GPO16** | PR0_PRU1_GPIO16 | | | FSITX3_CLK | TRC_DATA10 | | GPMC0_A17 | GPIO113 | | |
| C15 | **PR0_PRU1_GPO18** | PR0_PRU1_GPIO18 | | UART3_TXD | PR0_IEP0_EDIO_DATA_IN_OUT31 | TRC_CTL | XBAROUT14 | GPMC0_WAIT1 | GPIO120 | | EQEP1_B |
| D15 | **PR0_PRU1_GPO19** | PR0_PRU1_GPIO19 | | UART3_RXD | PR0_IEP0_EDC_SYNC_OUT0 | TRC_CLK | XBAROUT13 | | GPIO119 | | EQEP1_A |
| E17 | **PR0_PRU1_GPO2** | PR0_PRU1_GPIO2 | | | FSIRX2_DATA0 | TRC_DATA8 | | GPMC0_A15 | GPIO111 | | |
| E18 | **PR0_PRU1_GPO3** | PR0_PRU1_GPIO3 | | | FSIRX2_DATA1 | TRC_DATA9 | | GPMC0_A16 | GPIO112 | | |
| F16 | **PR0_PRU1_GPO4** | PR0_PRU1_GPIO4 | | | FSITX2_DATA0 | TRC_DATA5 | | GPMC0_A12 | GPIO108 | | |
| F15 | **PR0_PRU1_GPO5** | PR0_PRU1_GPIO5 | | | | TRC_DATA0 | EPWM30_A | GPMC0_OEn_REn | GPIO103 | | |
| E16 | **PR0_PRU1_GPO6** | PR0_PRU1_GPIO6 | | | FSITX2_CLK | TRC_DATA4 | | GPMC0_A11 | GPIO107 | | |
| D18 | **PR0_PRU1_GPO8** | PR0_PRU1_GPIO8 | | | | TRC_DATA3 | EPWM31_B | GPMC0_WEn | GPIO106 | | |
| C18 | **PR0_PRU1_GPO9** | PR0_PRU1_GPIO9 | | | PR0_UART0_RXD | TRC_DATA1 | EPWM30_B | GPMC0_BE0n_CLE | GPIO104 | | |
| N2 | **QSPI0_CLK** | QSPI0_CLK | | | | | | | GPIO2 | | |
| P1 | **QSPI0_CSN0** | QSPI0_CSn0 | | | | | | | GPIO0 | | |
| R3 | **QSPI0_CSN1** | QSPI0_CSn1 | | | | | XBAROUT0 | | GPIO1 | | |
| N1 | **QSPI0_D0** | QSPI0_D0 | | | | | | | GPIO3 | | |
| N4 | **QSPI0_D1** | QSPI0_D1 | | | | | | | GPIO4 | | |
| M4 | **QSPI0_D2** | QSPI0_D2 | | | | | | | GPIO5 | | |
| P3 | **QSPI0_D3** | QSPI0_D3 | | | | | | | GPIO6 | | |
| U17 | **RGMII1_RD0** | RGMII1_RD0 | RMII1_RXD0 | MII1_RXD0 | | | | FSITX0_DATA1 | GPIO31 | EQEP2_STROBE | |
| T17 | **RGMII1_RD1** | RGMII1_RD1 | RMII1_RXD1 | MII1_RXD1 | | | | FSIRX0_CLK | GPIO32 | EQEP2_INDEX | |

**Table 2-33. Pinmux Mapping Table (continued)**

| Pin# | Pinlist | Mode0 | Mode1 | Mode2 | Mode3 | Mode4 | Mode5 | Mode6 | Mode7 | Mode8 | Mode9 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| U18 | **RGMII1_RD2** | RGMII1_RD2 | | MII1_RXD2 | | | | FSIRX0_DATA0 | GPIO33 | EQEP0_A | |
| T18 | **RGMII1_RD3** | RGMII1_RD3 | | MII1_RXD3 | | | | FSIRX0_DATA1 | GPIO34 | EQEP0_B | |
| R18 | **RGMII1_RX_CTL** | RGMII1_RX_CTL | RMII1_RX_ER | MII1_RXDV | | | | FSITX0_DATA0 | GPIO30 | EQEP2_B | |
| R17 | **RGMII1_RXC** | RGMII1_RXC | RMII1_REF_CLK | MII1_RXCLK | | | | FSITX0_CLK | GPIO29 | EQEP2_A | |
| P16 | **RGMII1_TD0** | RGMII1_TD0 | RMII1_TXD0 | MII1_TXD0 | | | | FSITX1_DATA1 | GPIO37 | EQEP1_A | |
| P17 | **RGMII1_TD1** | RGMII1_TD1 | RMII1_TXD1 | MII1_TXD1 | | | | FSIRX1_CLK | GPIO38 | EQEP1_B | |
| P18 | **RGMII1_TD2** | RGMII1_TD2 | RMII1_CRS_DV | MII1_TXD2 | | | | FSIRX1_DATA0 | GPIO39 | EQEP1_STROBE | |
| N17 | **RGMII1_TD3** | RGMII1_TD3 | | MII1_TXD3 | | | | FSIRX1_DATA1 | GPIO40 | EQEP1_INDEX | |
| M18 | **RGMII1_TX_CTL** | RGMII1_TX_CTL | RMII1_TX_EN | MII1_TX_EN | | | | FSITX1_DATA0 | GPIO36 | EQEP0_STROBE | |
| N18 | **RGMII1_TXC** | RGMII1_TXC | | MII1_TXCLK | | | | FSITX1_CLK | GPIO35 | EQEP0_INDEX | |
| D4 | **SAFETY_ ERRORN** | SAFETY_ ERRORn | | | | | | | | | |
| B16 | **SDFM0_CLK0** | CLKOUT1 | | | | | | | GPIO122 | SDFM0_CLK0 | EQEP1_STROBE |
| A16 | **SDFM0_CLK1** | PR0_PRU1_ GPIO7 | CPTS0_TS_SYNC | UART5_RTSn | PR0_IEP0_EDC_S YNC_OUT1 | | I2C3_SDA | | GPIO124 | SDFM0_CLK1 | |
| B15 | **SDFM0_CLK2** | UART5_TXD | | | | | I2C3_SCL | GPMC0_ADVn_ALE | GPIO126 | SDFM0_CLK2 | |
| A15 | **SDFM0_CLK3** | MCAN3_TX | UART5_RXD | | | | | | GPIO128 | SDFM0_CLK3 | |
| D14 | **SDFM0_D0** | PR0_ECAP0_ APWM_OUT | | | | | | | GPIO123 | SDFM0_D0 | |
| D13 | **SDFM0_D1** | PR0_PRU1_ GPIO17 | | UART5_CTSn | PR0_IEP0_EDIO_D ATA_IN_OUT30 | | | | GPIO125 | SDFM0_D1 | |
| C13 | **SDFM0_D2** | UART5_RXD | | | | | | | GPIO127 | SDFM0_D2 | |
| C14 | **SDFM0_D3** | MCAN3_RX | | | | | | | GPIO129 | SDFM0_D3 | |
| A11 | **SPI0_CLK** | SPI0_CLK | UART3_TXD | LIN3_TXD | | | | FSITX0_CLK | GPIO12 | | |
| C11 | **SPI0_CS0** | SPI0_CS0 | UART3_RXD | LIN3_RXD | | | | | GPIO11 | | |
| C10 | **SPI0_D0** | SPI0_D0 | | | | | | FSITX0_DATA0 | GPIO13 | | |
| B11 | **SPI0_D1** | SPI0_D1 | | | | | | FSITX0_DATA1 | GPIO14 | | |
| A10 | **SPI1_CLK** | SPI1_CLK | UART4_RXD | LIN4_RXD | | | XBAROUT2 | FSIRX0_CLK | GPIO16 | | |
| C9 | **SPI1_CS0** | SPI1_CS0 | UART4_TXD | LIN4_TXD | | | XBAROUT1 | | GPIO15 | | |
| B10 | **SPI1_D0** | SPI1_D0 | UART5_TXD | | | | XBAROUT3 | FSIRX0_DATA0 | GPIO17 | | |
| D9 | **SPI1_D1** | SPI1_D1 | UART5_RXD | | | | XBAROUT4 | FSIRX0_DATA1 | GPIO18 | | |
| B3 | **TCK** | TCK | | | | | | | | | |
| C5 | **TDI** | TDI | | | | | | | | | |
| C4 | **TDO** | TDO | | | | | | | | | |
| U1 | **TEMPCAL** | TEMPCAL | | | | | | | | | |
| D5 | **TMS** | TMS | | | | | | | | | |
| B7 | **UART0_CTSN** | UART0_CTSn | I2C2_SDA | SPI3_D1 | MCAN3_RX | SPI0_CS1 | XBAROUT10 | | GPIO26 | | |
| C7 | **UART0_RTSN** | UART0_RTSn | I2C2_SCL | SPI3_D0 | MCAN3_TX | | XBAROUT9 | | GPIO25 | | |
| A7 | **UART0_RXD** | UART0_RXD | LIN0_RXD | | | | | | GPIO27 | | |
| A6 | **UART0_TXD** | UART0_TXD | LIN0_TXD | | | | | | GPIO28 | | |
| L3 | **UART1_RXD** | UART1_RXD | LIN1_RXD | | | | EPWM16_A | GPMC0_AD6 | GPIO75 | | |
| M3 | **UART1_TXD** | UART1_TXD | LIN1_TXD | | | | EPWM16_B | GPMC0_AD7 | GPIO76 | | |
| U2 | **VSYS_MON** | VSYS_MON | | | | | | | | | |

**Table 2-33. Pinmux Mapping Table (continued)**

| Pin# | Pinlist | Mode0 | Mode1 | Mode2 | Mode3 | Mode4 | Mode5 | Mode6 | Mode7 | Mode8 | Mode9 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C3 | **WARMRSTN** | WARMRSTn | | | | | | | | | |
| T1 | **XTAL_XI** | XTAL_XI | | | | | | | | | |
| R1 | **XTAL_XO** | XTAL_XO | | | | | | | | | |

# 3 Software

## 3.1 SDK Installation

The TMDSCNCD263-PMIC uses a one-time version of the SDK for the example CCS projects. The download for the one-time SDK can be found here: MCU-PLUS-SDK-AM263-PMIC. This SDK version has been validated and contains the examples from the original TMDSCNCD263 along with new drivers for the Automotive Ethernet interface and PMIC.

# 4 Hardware Design Files

**Note**

This User Guide is associated with the TMDSCNCD263-PMIC which is only released as the E1 revision. E2 schematic and layout files were generated to address some of the issues with the E1 design.

**Note**

If this design is being used as reference, please use the E2 version of the schematic and layout.

To download the zip file containing the design files for the E1 and E2 version of the EVM, click the following link.

# 5 Additional Information

## 5.1 Trademarks

Texas Instruments™, Sitara™, and E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

## 5.2 E1 Design Hardware Modifications

The following section describes the hardware modifications that were made to each E1 Control Card.

1. **TUSB320 CC Controller GPIO Mode**
   - The TUSB320 is intended to be used in the GPIO mode to negotiate whether the type-C CC pins represent a power source that is an excellent choice for the Control Card. For the TUSB320 to be GPIO mode, the ADDR pin needs to floating and therefore R170 was removed.
   - Modification 1:
     – Depopulate R170


**Figure 5-1. Modification 1**

2. **Bypass PMIC VSYS_3V3C Power**
   - The PMIC LDO output VSOUT2 is used to power the VSYS_3V3C power net. VSYS_3V3C is used to power loads for various peripheral circuits, many of which are required for AM263x reset and boot.

- The PMIC LDO output VSOUT2 is disabled by default and requires a SPI register write from the AM263x to enable after initial start-up.
- As a workaround, the VSYS_3V3C rail is shorted with the VSYS_3V3A PMIC output.
- Modification 2:
  - Lift pin U30.29 from PMIC to disconnect LDO output of PMIC
  - Short TP359 and TP362 using 22GA wire

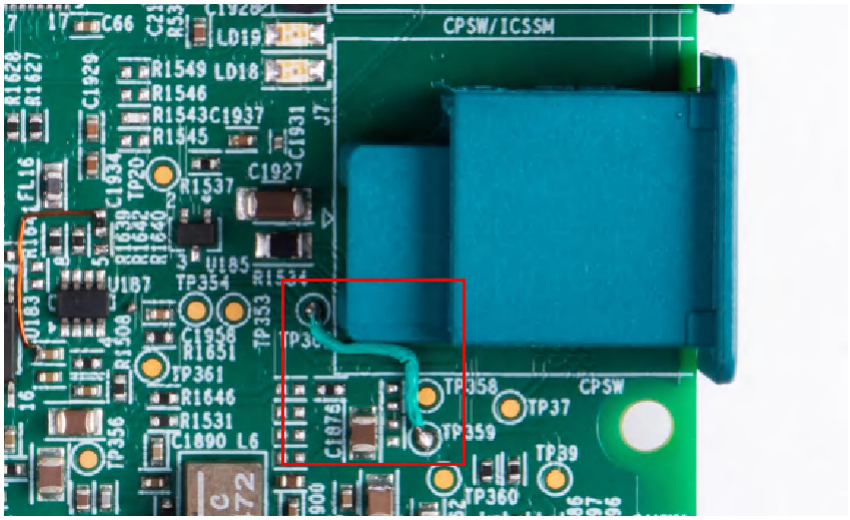



**Figure 5-2. Modification 2**

3. **TPS37042A30 Startup RESET Output Transients**
   - The TPS37042A3O power supervisor (U187) open-drain outputs RESET1# and RESET2# cause transient PORZ assertions during initial 3.3V (VSYS_3V3A) and 1.2V (VSYS_1V2) power-on.
   - These open-drain outputs are pulled to USB-C/HSEC supplied VMAIN 5.0V supply. That VMAIN supply showed noisy behavior during start-up and caused these open-drain I/O to provide a faulty PORZ. Changing U187 RESET1# and RESET2# output pull-up resistors to reference PMIC supplied VDD_5V0 creates a functional PORZ.
   - Modification 3:
     - Remove R1640
     - Install 10 kΩ pull-up resistor on the RESET# output pad of the R1640 resistor position
     - Attach the other 10 kΩ resistor pad to the VDD_5V0 power net

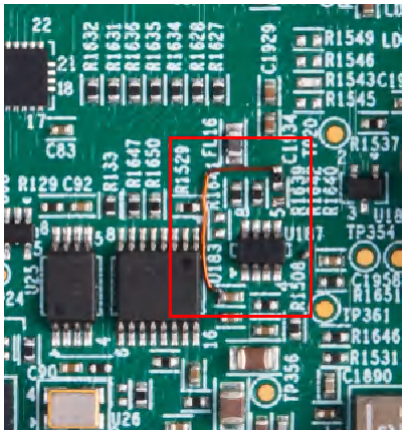



**Figure 5-3. Modification 3**

# 6 References

## 6.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- *AM2634 Sitara™ Microcontrollers*
- *AM263x Sitara™ Microcontrollers Data Sheet*
- *AM263x Sitara™ Microcontrollers Technical Reference Manual*
- *AM263x Sitara™ Microcontrollers Silicon Errata*
- *Texas Instruments Code Composer Studio*
- *Updating XDS110 Firmware*
  - To find the serial number, only follow steps 1 and 2 of updating XDS110 firmware

## 6.2 Other TI Components Used in This Design

This Control Card uses various other TI components for the functions. A consolidated list of these components with links to their TI product data sheets is shown below.

- *TPS22918 Load Switch*
- *TMP411 Temperature Sensor*
- *TCAN1042-Q1 CAN Transceiver*
- *XDS110 JTAG Debug Probe*
- *DP83869HM 10/100/1000 Ethernet Physical Layer Transceiver*
- *DP83826 10/100 Industrial Ethernet PHY*
- *TPS3711 Voltage Detector*
- *LMK1C110x LVCMOS Clock Buffer*
- *INA228 Current Monitor with I2C Interface*
- *TLIN2029-Q1 LIN Transceiver*
- *TCA6408 8-Bit I2C I/O Expander*
- *TPIC2810 8-Bit LED Driver with I2C Interface*
- *TCA6416 16-BIT I2C I/O Expander*
- *TUSB320LAI USB Type-C Configuration Channel Logic and Port Control*
- *TPS212x Power MUX*
- *TPS6291x Buck Converter*
- *TPS6217x Step-Down Converter*
- *TPS22918 Load Switch*
- *TPS62097 Step-Down Converter*
- *TPS389x Adjustable Voltage Monitor*

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   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

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   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

**WARNING**

**Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.**

**User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.**

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

**CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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