REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	03/31/2017	JAC
B	BETA	06/06/2017	JAC
B1	BETA	06/13/2017	JAC
C	PRODUCTION	09/08/2017	JAC

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== SH01 - TITLE PAGE
== SH02 - NOTES
== SH03 - ECN HISTORY
== SH04 - J6PLUS_NONVOL_MEM_SYS
== SH05 - J6PLUS_VOL_MEM
== SH06 - J6PLUS_CAM_DISPLAY_VIDEO
== SH07 - J6PLUS_CONVITY
== SH08 - J6PLUS_ANA_PWR
== SH09 - J6PLUS_DIG_PWR
== SH10 - J6PLUS_GND
== SH11 - BLANK 1
== SH12 - BLANK 2
== SH13 - DDR BANK1
== SH14 - DDR BANK2
== SH15 - MUX-SERIAL
== SH16 - MUX-GPMC
== SH17 - MUX-VIDEO/EMAC
== SH18 - IOEXPANDER/SDCARD
== SH19 - QSPI/NAND/BOOT/EEPR/TMP
== SH20 - EMMC/NORFLASH
== SH21 - FPD-LINK/LCD
== SH22 - HDMI-FPDLINK/USB HUB
== SH23 - HDMI
== SH24 - CAMERA/CSI2
== SH25 - JTAG/MLB/FTDI CONSOLE
== SH26 - PCIE/SATA
== SH27 - AIC3106
== SH28 - USB
== SH29 - ENET PORT0
== SH30 - ENET PORT1
== SH31 - COMQ8
== SH32 - STAGE1 BUCK
== SH33 - STAGE2 TPS65917
== SH34 - STAGE2 LP87565
== SH35 - STAGE2 TPS54116
== SH36 - MISC POWER/SWITCHES
== SH37 - INA/PWR ROUTER
== SH38 - DARA/TEST
== SH39 - EXPANSION/CAN
== SH40 - DDR3 TEST POINTS
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REVISION STATUS OF SHEETS

REV	A	C	C	C	C	B	B	C	C	A
SH	31	32	33	34	35	36	37	38	39	40
REV	C	C	A	A	A	A	A	A	B1	B1
SH	21	22	23	24	25	26	27	28	29	30
REV	A	A	A	A	C	A	A	A	A	A
SH	11	12	13	14	15	16	17	18	19	20
REV	C	B1	C	C	C	C	C	C	C	C
SH	1	2	3	4	5	6	7	8	9	10

NEXT ASSY | USED ON

APPLICATION

DWN	J.A.C.	DATE 03/16/2017
CHK	T.W.K.	DATE 03/16/2017
ENGR	J.A.C.	DATE 03/16/2017
ENGR-MGR	J.A.C.	DATE 03/16/2017
QA	C.M.D.	DATE 03/16/2017
MFG	J.A.C.	DATE 03/16/2017
RLSE	J.A.C.	DATE 03/16/2017

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD	
Page Contents:	TITLE PAGE	
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	Board/Function	Device	Device Function	VAYUH	J6Plus-A	J6Plus-B	7b	8b
1	CPU	U8	DS90UB921-Q1	NA	i2c1	i2c3	0x0C	0x18
2	CPU	U115	DS90UB949	NA	i2c1	i2c3	0x1A	0x26
3	CPU	U38	O917A14	i2c1	i2c1	i2c1	0x12	0x24
4	CPU	U50	AIC3106	i2c1	i2c1	i2c1	0x19	0x32
5	CPU	U30	PCF8575	i2c1	i2c1	i2c1	0x20	0x40
6	CPU	U21	PCF8575	i2c1	i2c1	i2c1	0x21	0x42
7	CPU	U110	PCF8575	i2c2	i2c1	i2c1	0x26	0x4C
8	CPU	U53	TMP102	i2c1	i2c1	i2c1	0x48	0x90
9	CPU	U139	24WC256	i2c1	i2c1	i2c1	0x50	0xa0
10	CPU	U38	O917A14 - Power	i2c1	i2c1	i2c1	0x58	0xB0
11	CPU	U38	O917A14 - Interfaces	i2c1	i2c1	i2c1	0x59	0xB2
12	CPU	U38	O917A14 - Trimming	i2c1	i2c1	i2c1	0x5A	0xB4
13	CPU	U38	O917A14 - OTP	i2c1	i2c1	i2c1	0x5B	0xB6
14	CPU	U40	LP87565	NA	i2c1	i2c1	0x60	0xC0
15	CPU	U110	CDCE813-Q1	NA	i2c1	i2c1	0x65	0xCA
16	CPU	P5	MLB	i2c1	i2c1	i2c1		
17	CPU	P9	COMQ	i2c1	i2c1	i2c1		
18	CPU	P7	HDMI	i2c2	i2c2	i2c2	0x50	0xa0
19	CPU	J8	IMAGER	i2c2	i2c3	i2c5	0x10	0x20
20	CPU	J8	IMAGER	i2c2	i2c3	i2c5	0x37	0x6E
21								
22	1080P LCD		EEPROM	i2c1	i2c1	i2c3	0x57	0xAE
23	1080P LCD		PCF8575	i2c1	i2c1	i2c3	0x27	0x4E
24	1080P LCD		TC358778	i2c1	i2c1	i2c3	0x0E	0x1C
25	1080P LCD		TOUCH	i2c1	i2c1	i2c3	0x38	0x70
26	1080P LCD		TLC59108IPW	i2c1	i2c1	i2c3	0x40	0x80
27								
28	HDMI LCD		TFP410(EP)	NA		i2c3	0x38	0x70
29	HDMI LCD		PCF8575	NA		i2c3	0x27	0x4E
30	HDMI LCD		EEPROM	NA		i2c3	0x57	0xAE
31	HDMI LCD		EEDID	NA		i2c3	0x50	0xa0
32								
33	VISION	APTINA		i2c2	i2c3	i2c5	0x10	0x20
34	VISION	FBD-LINK	GPIO Expander 3	i2c2	i2c3	i2c5	0x25	0x4A
35	VISION	FBD-LINK	GPIO Expander 2	i2c2	i2c3	i2c5	0x21	0x42
36	VISION	FBD-LINK	GPIO Expander 1	i2c2	i2c3	i2c5	0x27	0x4E
37	VISION	FBD-LINK	INFO EEPROM	i2c2	i2c3	i2c5	0x50	0xA0
38	VISION	FBD-LINK	De-Serializer 1	i2c2	i2c3	i2c5	0x60	0xC0
39	VISION	FBD-LINK	De-Serializer 5	i2c2	i2c3	i2c5	0x61	0xC2
40	VISION	FBD-LINK	De-Serializer 2	i2c2	i2c3	i2c5	0x64	0xC8
41	VISION	FBD-LINK	De-Serializer 3	i2c2	i2c3	i2c5	0x68	0xD0
42	VISION	FBD-LINK	De-Serializer 6	i2c2	i2c3	i2c5	0x69	0xD2
43	VISION	FBD-LINK	De-Serializer 4	i2c2	i2c3	i2c5	0x6C	0xD8
44	VISION	LI IMAGER		i2c2	i2c3	i2c5	0x10	0x20
45	VISION	OV IMAGER		i2c2	i2c3	i2c5	0x30	0x60
46	HDMI	ADV7611	BASE	i2c2	i2c3	i2c5	0x4C	0x98
47	HDMI	ADV7611	CEC	i2c2	i2c3	i2c5	0x40	0x80
48	HDMI	ADV7611	INFOFRAME	i2c2	i2c3	i2c5	0x3E	0x7C
49	HDMI	ADV7611	DPLL	i2c2	i2c3	i2c5	0x55	0xAA
50	HDMI	ADV7611	KSV	i2c2	i2c3	i2c5	0X56	0xAB
51	HDMI	ADV7611	EDID	i2c2	i2c3	i2c5	0x57	0xAC
52	HDMI	ADV7611	HDMI	i2c2	i2c3	i2c5	0x34	0x68
53	HDMI	ADV7611	CP	i2c2	i2c3	i2c5	0x22	0x44
54								
55	JAMR3	u21	24c256	i2c1	i2c1	i2c1	0x51	0xA2
56	JAMR3	U26	AIC3106	i2c2	i2c3	i2c5	0x18	0x30
57	JAMR3	U25	AIC3106	i2c2	i2c3	i2c5	0x19	0x32
58	JAMR3	U24	AIC3106	i2c2	i2c3	i2c5	0x1A	0x34
59	JAMR3	U5	DS90UH926Q	i2c2	i2c3	i2c5	0x2C	0X58
60	JAMR3	U10	TVP5158	i2c2	i2c3	i2c5	0x58	0xB0
61	JAMR3	J15		i2c3	i2c3	i2c3	???	
62	JAMR3	P5	APPLE AUTH	i2c3	i2c3	i2c3	0x10	0x20
63	JAMR3	P2		i2c3	i2c3	i2c3	???	
64	JAMR3	J17		i2c3	i2c3	i2c3	???	
65	JAMR3	U14	PCF8578	i2c4	i2c4	i2c4	0x22	0x44
66	JAMR3	U9	AFE8310	i2c4	i2c4	i2c4	0x48	0x90
67	JAMR3	U8	AFE8310	i2c4	i2c4	i2c4	0x49	0x92
68	JAMR3	U7	AFE8310	i2c4	i2c4	i2c4	0x4A	0x94
69	JAMR3	U6	AFE8310	i2c4	i2c4	i2c4	0x4B	0x96
70								
71								
72	AUO FPD		Display DS90UB924-Q1	NA	i2c1	i2c3	0x2C	
73	AUO FPD		Display PCF8575	NA	i2c1	i2c3	Alias-tbd	
74	AUO FPD		Display TLC59108IPW	NA	i2c1	i2c3	Alias-tbd	
75	AUO FPD		Display TLC59108IPW ALL CALL	NA	i2c1	i2c3	Alias-tbd	
76	AUO FPD		Display EEPROM	NA	i2c1	i2c3	Alias-tbd	
77	AUO FPD		Display Touch Controller	NA	i2c1	i2c3	Alias-tbd	
78	AUO FPD		RF430CL330H	NA	i2c1	i2c3	Alias-tbd	
79								
80								
81	ADAS FUSION		DS90UB960TRGCRQ1-U1	NA	i2c3	i2c5	0x30	0x60
82	ADAS FUSION		DS90UB960TRGCRQ1-U2	NA	i2c3	i2c5	0x3D	0x7A
83	ADAS FUSION		Alias IDs Camera/Radar???	NA	i2c3	i2c5		
84	ADAS FUSION		ID EEPROM	NA	i2c3	i2c5	0x50	0xA0
85								

86									Sense R
87	INA226-PM1	U86	VDD_MPU_AVS	NA	i2c2	i2c2	0x40	0x80	R249
88	INA226-PM1	U85	VDD_GPU_AVS	NA	i2c2	i2c2	0x41	0x82	R191
89	INA226-PM1	U84	VDD_DSPEVE_AVS	NA	i2c2	i2c2	0x42	0x84	R208
90	INA226-PM1	U83	VDD_CORE_AVS	NA	i2c2	i2c2	0x43	0x86	R189
91	INA226-PM1	U82	VDD_IVA_AVS	NA	i2c2	i2c2	0x44	0x88	R179
92	INA226-PM1	U81	VDDSHV_3V3	NA	i2c2	i2c2	0x45	0x8A	R514
93	INA226-PM1	U80	VDDR_MEM_1V35	NA	i2c2	i2c2	0x46	0x8C	R703
94	INA226-PM1	U79	VDDR_SOC_1V35	NA	i2c2	i2c2	0x47	0x8E	R642
95	INA226-PM1	U71	VIO_1V8	NA	i2c2	i2c2	0x48	0x90	R220
96	INA226-PM1	U70	VDDS_1V8	NA	i2c2	i2c2	0x49	0x92	R219
97	INA226-PM1	U69	VDD_SDIO_DV	NA	i2c2	i2c2	0x4A	0x94	R196
98	INA226-PM1	U68	VDDA_USB_3V3	NA	i2c2	i2c2	0x4B	0x96	R192
99	INA226-PM1	U67	VDDA_PLL_1V8	NA	i2c2	i2c2	0x4C	0x98	R204
100	INA226-PM1	U65	VDDA_PHY2_1V8	NA	i2c2	i2c2	0x4D	0x9A	R182
101	INA226-PM1	U66	VDDA_PHY1_1V8	NA	i2c2	i2c2	0x4E	0x9C	R183
102									
103	INA226-PM2	U90	VSYS_12V0	NA	i2c2	i2c2	0x40	0x80	R32
104	INA226-PM2	U89	VSYS_5V0	NA	i2c2	i2c2	0x41	0x82	R162
105	INA226-PM2	U88	VSYS_3V3	NA	i2c2	i2c2	0x42	0x84	R160
106	INA226-PM2	U87	VIO_3V3	NA	i2c2	i2c2	0x43	0x86	R513
107	INA226-PM2	U78	VPIN_B01_3V3	NA	i2c2	i2c2	0x44	0x88	R225
108	INA226-PM2	U77	VPIN_B23_3V3	NA	i2c2	i2c2	0x45	0x8A	R205
109	INA226-PM2	U76	VPIN_S12_3V3	NA	i2c2	i2c2	0x46	0x8C	R549
110	INA226-PM2	U75	VPIN_S3_3V3	NA	i2c2	i2c2	0x47	0x8E	R548
111	INA226-PM2	U74	VPIN_S4_3V3	NA	i2c2	i2c2	0x48	0x90	R533
112	INA226-PM2	U73	VPIN_S5_3V3	NA	i2c2	i2c2	0x49	0x92	R575
113	INA226-PM2	U72	VPIN_LDO_3V3	NA	i2c2	i2c2	0x4A	0x94	R537
114	INA226-PM2	U91	VPIN_LDO_5V0	NA	i2c2	i2c2	0x4B	0x96	R194

SCHEMATIC SIGNAL	GPIO	EXTERNAL	INTERNAL	T-POINT	NOTE
H_NMIN		PU-10K	PD		NU
H_WKUP_0	GPIO1_0	PU-10K	OFF	TP74	LP87xx INT
H_WKUP_1	GPIO1_1	PU-10K	OFF	TP69	PMIC INT
H_GP1[2]_TOUCH_EVT		PD-10K	OFF	TP73	TOUCH
H_GP1[3]/H_PCF8575_INT		PU-1K	OFF	TP72	EXP
H_ENET_INTSn	GPIO6_16		PU		ENET
H_GP6[17]			PD		EXP
H_GP6[20]			PD		EXP
H_GP6[28]			PD		MLB
H_GP2[27]			PU		EXP
H_GP5[17]			PD		EXP
H_POWERHOLD_CLK	GPIO3_30	PD-1K	PU	TP56	
H_MMC_PWR_ON	GPIO4_21	PU-1K	PD	TP57	
H_GP5[9]			PD		MLB
H_GP5[8]			PD		COM8
H_GP5[7]			PD		COM8
H_GP5[6]			PD		COM8
H_GP5[5]			PD		COM8
H_GP5[4]			PD		COM8
H_GP5[1]			PD		EXP
H_GP5[0]			PD		EXP/AUTOMATION
H_GP2[22]			PU	TP55	NU
CON_LCD_PWR_DN	GPIO3_1	PU-1K	PD		
HDMI_CT_HPD	GPIO7_30	PU-1K	PD		
HDMI_LS_OE	GPIO7_31	PU-1K	PD		

TEXAS INSTRUMENTS INCORPORATED

Title: DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents: NOTES		
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ECN Number	518450-E002			
Date Requested	9/8/2017			
Requester	Tony C.			
Approvals	Tony C.			
Assembly Number	518450-0001R			
Current Assembly Rev	B			
New Assembly Rev	C			
Implentation notes				

Item#	Init Date	Priority	Status	Description
1				ASSY, PWB, LOGIC Re B TO C
2				EEPROM Rev 1.1 to 1.2
DR-2				Sheet 33: Add in 3.3v/1.8V LDO for VDD_SDIO_DV support.
				ADD
				Q19 104958-0001R
				R753 101370-1001R
				R754 102145-1003R
				R755 102145-1003R
				U148 105156-0001R
DR-3				Sheet 22: Change U124 (TXS0108EPW) OE to pull high vs pull low to enable.
DR-4				Update SOC Symbol
ER-5				Sheet 4, 7, 15, 39 add "MCAN" to DCAN1 and DCAN2 signals. No logic changes.
				Change J20/J21 silkscreen to CAN1, CAN2.
ER-6				Sheet 18,19: Add 4 user GPIO switches with access from I/O expander, SW10 and Automation header.
				ADD
				R745 103158-1003R
				R746 103158-1003R
				R747 103158-1003R
				R748 103158-1003R
				R749 103158-1002R
				R750 103158-1002R
				R751 103158-1002R
				R752 103158-1002R
				SW10 101184-0004R
DR-7				Sheet 21: RJ3/RJ5 population change to enable I2C access to CDCE813.
				From 1-2 (101370-4702R, 4.7k) to 2-3 (101370-2200R, 22 ohm)
DR-8				MLB probe points, J4, J5, J6 spacing to match J6 Entry. Change footprint from 2mm to 2.54mm.
ER-9				Sheet 32, 34, 35: Add undervoltage circuit from J6 LCARD for better controlled shutdown.
				ADD
				C711 103885-1220R
				C712 101782-1153R
				C713 C0402-NOPOP
				D24 NO-POP
				Q18 104958-0001R
				RJ17 101370-0001R
				R742 102145-2744R
				R743 102145-1004R
				R744 102145-1004R
				U147 NO-POP
				R756 102145-2003R
				TP98 TP-30RD13-NO-POP
				Relabel TP96 PGD_STAGE1_3V3_5V0
				Label TP98 PGD_UV_DETECT
ER-10				Update SOC Symbol
DR-11				Evaluate SOC thermal and apply heatsink and fan if needed.
DR-12				Sheet 38: Add automation header note.
DR-13				Sheet 22: Add R-mux between VCC_1V1USB and H_USB2_DRV_VBUS to enable the USB HUB. H_USB2_DRV_VBUS Postion 2-3 default.
				Add
				RJ16, 102145-2003R
DR-14				Fusion power connector silkscreen outline and text needs to be corrected so it is not under the connector.
ER-15				Sheet 18: Update the micro SD card footprint to Molex 502774-0891. Current micro SD is giong EOL. No logic change but the footprints are slightly different.
				P14 From 103053-0001R To 105161-0001R
ER-16				Sheet 32: Add smt gnd TPs near center of the board on top and bottom.
				Add TP99, TP100 104178-0001R
ER-17				Sheet 33: Update PMIC OTP part# to O917A154TRGZRQ1/ PO917A154TRGZRQ1
				U38 From 105046-0001R-TI To105046-0002R-TI
				105046-0002R-TI O917A154TRGZRQ1/ PO917A154TRGZRQ1

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
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DRA77xP / DRA76xP / TDA2Px

Data Manual: SPRS993A_July_2017
Package: ACD, 23x23mm, 784 PBGA, 0.8mm Pitch
PCB Footprint: bga784_28x28_0p8mm
SCH Symbol: IC_J6Plus_ACD_23mm_784BGA_v1.0

SYSTEM

MEMORY–Nonvolatile

GPMC/GPIO
VDDSHV10

gpmc_a0/vin3a_d16/vout3_d16/vin4a_d0/usb4_ulpi_d7/vin4b_d0/i2c4_scl/uart5_rxd/gpio7_3/gpmc_a26/gpmc_a16
gpmc_a1/vin3a_d17/vout3_d17/vin4a_d1/usb4_ulpi_d6/vin4b_d1/i2c4_sda/uart5_txd/gpio7_4
gpmc_a2/vin3a_d18/vout3_d18/vin4a_d2/usb4_ulpi_d5/vin4b_d2/uart7_rxd/uart5_ctsn/gpio7_5
gpmc_a3/qspi1_cs2/vin3a_d19/vout3_d19/vin4a_d3/usb4_ulpi_d4/vin4b_d3/uart7_txd/uart5_rtsn/gpio7_6
gpmc_a4/qspi1_cs3/vin3a_d20/vout3_d20/vin4a_d4/usb4_ulpi_d3/vin4b_d4/i2c5_scl/uart6_rxd/gpio1_26
gpmc_a5/vin3a_d21/vout3_d21/vin4a_d5/usb4_ulpi_d2/vin4b_d5/i2c5_sda/uart6_txd/gpio1_27
gpmc_a6/vin3a_d22/vout3_d22/vin4a_d6/usb4_ulpi_d1/vin4b_d6/uart8_rxd/uart6_ctsn/gpio1_28
gpmc_a7/vin3a_d23/vout3_d23/vin4a_d7/usb4_ulpi_d0/vin4b_d7/uart8_txd/uart6_rtsn/gpio1_29
gpmc_a8/vin3a_hsync0/vout3_hsync/usb4_ulpi_nxt/vin4b_hsync1/timer12/spi4_sclk/gpio1_30
gpmc_a9/vin3a_vsync0/vout3_vsync/usb4_ulpi_dir/vin4b_vsync1/timer11/spi4_d1/gpio1_31
gpmc_a10/vin3a_de0/vout3_de/usb4_ulpi_stp/vin4b_clk1/timer10/spi4_d0/gpio2_0
gpmc_a11/vin3a_fld0/vout3_fld/vin4a_fld0/usb4_ulpi_clk/vin4b_de1/timer9/spi4_cs0/gpio2_1
gpmc_a12/vin4a_clk0/gpmc_a0/vin4b_fld1/timer8/spi4_cs1/dma_evt1/gpio2_2
gpmc_a13/qspi1_rtclk/vin4a_hsync0/timer7/spi4_cs2/dma_evt2/gpio2_3
gpmc_a14/qspi1_d3/vin4a_vsync0/timer6/spi4_cs3/gpio2_4
gpmc_a15/qspi1_d2/vin4a_d8/timer5/gpio2_5
gpmc_a16/qspi1_d0/vin4a_d9/gpio2_6
gpmc_a17/qspi1_d1/vin4a_d10/gpio2_7
gpmc_a18/qspi1_sclk/vin4a_d11/gpio2_8

GPMC/MMC2
VDDSHV11

gpmc_a19/mmc2_dat4/gpmc_a13/vin4a_d12/vin3b_d0/gpio2_9
gpmc_a20/mmc2_dat5/gpmc_a14/vin4a_d13/vin3b_d1/gpio2_10
gpmc_a21/mmc2_dat6/gpmc_a15/vin4a_d14/vin3b_d2/gpio2_11
gpmc_a22/mmc2_dat7/gpmc_a16/vin4a_d15/vin3b_d3/gpio2_12
gpmc_a23/mmc2_clk/gpmc_a17/vin4a_fld0/vin3b_d4/gpio2_13
gpmc_a24/mmc2_dat0/gpmc_a18/vin4a_d8/vin3b_d5/gpio2_14
gpmc_a25/mmc2_dat1/gpmc_a19/vin4a_d9/vin3b_d6/gpio2_15
gpmc_a26/mmc2_dat2/gpmc_a20/vin4a_d10/vin3b_d7/gpio2_16
gpmc_a27/mmc2_dat3/gpmc_a21/vin4a_d11/vin3b_hsync1/gpio2_17

GPMC/GPIO
VDDSHV10

gpmc_ad0/vin3a_d0/vout3_d0/gpio1_6/sysboot0
gpmc_ad1/vin3a_d1/vout3_d1/gpio1_7/sysboot1
gpmc_ad2/vin3a_d2/vout3_d2/gpio1_8/sysboot2
gpmc_ad3/vin3a_d3/vout3_d3/gpio1_9/sysboot3
gpmc_ad4/vin3a_d4/vout3_d4/gpio1_10/sysboot4
gpmc_ad5/vin3a_d5/vout3_d5/gpio1_11/sysboot5
gpmc_ad6/vin3a_d6/vout3_d6/gpio1_12/sysboot6
gpmc_ad7/vin3a_d7/vout3_d7/gpio1_13/sysboot7
gpmc_ad8/vin3a_d8/vout3_d8/gpio7_18/sysboot8
gpmc_ad9/vin3a_d9/vout3_d9/gpio7_19/sysboot9
gpmc_ad10/vin3a_d10/vout3_d10/gpio7_28/sysboot10
gpmc_ad11/vin3a_d11/vout3_d11/gpio7_29/sysboot11
gpmc_ad12/vin3a_d12/vout3_d12/gpio1_18/sysboot12
gpmc_ad13/vin3a_d13/vout3_d13/gpio1_19/sysboot13
gpmc_ad14/vin3a_d14/vout3_d14/gpio1_20/sysboot14
gpmc_ad15/vin3a_d15/vout3_d15/gpio1_21/sysboot15

gpmc_advn_ale/gpmc_cs6/clkout2/gpmc_wait1/vin4a_vsync0/gpmc_a2/gpmc_a23/timer3/i2c3_sda/dma_evt2/gpio2_23(gpmc_a19)
gpmc_ben0/gpmc_cs4/vin1b_hsync1/vin3b_de1/timer2/dma_evt3/gpio2_26(gpmc_a21)
gpmc_ben1/gpmc_cs5/vin1b_de1/vin3b_clk1/gpmc_a3/vin3b_fld1/timer1/dma_evt4/gpio2_27(gpmc_a22)
gpmc_cs0/gpio2_19
gpmc_cs1/mmc2_cmd/gpmc_a22/vin4a_de0/vin3b_vsync1/gpio2_18
gpmc_cs2/qspi1_cs0/gpio2_20(gpmc_a23/gpmc_a13)
gpmc_cs3/qspi1_cs1/vin3a_clk0/vout3_clk/gpmc_a1/gpio2_21(gpmc_a24/gpmc_a14)
gpmc_oen_ren/gpio2_24
gpmc_wait0/gpio2_28(gpmc_a25/gpmc_a15)
gpmc_wen/gpio2_25
gpmc_clk/gpmc_cs7/clkout1/gpmc_wait1/vin4a_hsync0/vin4a_de0/vin3b_clk1/timer4/i2c3_scl/dma_evt1/gpio2_22(gpmc_a20)

MMC1
VDDSHV8

mmc1_clk/gpio6_21
mmc1_cmd/gpio6_22
mmc1_sdcd/uart6_rxd/i2c4_sda/gpio6_27
mmc1_sdwp/uart6_txd/i2c4_scl/gpio6_28
mmc1_dat0/gpio6_23
mmc1_dat1/gpio6_24
mmc1_dat2/gpio6_25
mmc1_dat3/gpio6_26

MMC3/GPIO
VDDSHV7

mmc3_clk/usb3_ulpi_d5/vin2b_d7/ehrpwm2_tripzone_input/pr2_mii1_txd3/xx/gpio6_29
mmc3_cmd/spi3_sclk/usb3_ulpi_d4/vin2b_d6/eCAP2_in_PWM2_out/pr2_mii1_txd2/xx/gpio6_30
mmc3_dat0/spi3_d1/uart5_rxd/usb3_ulpi_d3/vin2b_d5/eQEP3A_in/pr2_mii1_txd1/xx/gpio6_31
mmc3_dat1/spi3_d0/uart5_txd/usb3_ulpi_d2/vin2b_d4/eQEP3B_in/pr2_mii1_txd0/xx/gpio7_0
mmc3_dat2/spi3_cs0/uart5_ctsn/usb3_ulpi_d1/vin2b_d3/eQEP3_index/pr2_mii_mr1_clk/xx/gpio7_1
mmc3_dat3/spi3_cs1/uart5_rtsn/usb3_ulpi_d0/vin2b_d2/eQEP3_strobe/pr2_mii1_rxdv/xx/gpio7_2
mmc3_dat4/spi4_sclk/uart10_rxd/usb3_ulpi_nxt/vin2b_d1/ehrpwm3A/pr2_mii1_rxd3/xx/gpio1_22
mmc3_dat5/spi4_d1/uart10_txd/usb3_ulpi_dir/vin2b_d0/ehrpwm3B/pr2_mii1_rxd2/xx/gpio1_23
mmc3_dat6/spi4_d0/uart10_ctsn/usb3_ulpi_stp/vin2b_de1/ehrpwm3_tripzone_input/pr2_mii1_rxd1/xx/gpio1_24
mmc3_dat7/spi4_cs0/uart10_rtsn/usb3_ulpi_clk/vin2b_clk1/eCAP3_in_PWM3_out/pr2_mii1_rxd0/xx/gpio1_25

gpio6_10/mdio_mclk/i2c3_sda/usb3_ulpi_d7/vin2b_hsync1/ehrpwm2A/pr2_mii_mt1_clk/xx/gpio6_10
gpio6_11/mdio_d/i2c3_scl/usb3_ulpi_d6/vin2b_vsync1/ehrpwm2B/pr2_mii1_txen/xx/gpio6_11

SATA
VDDA_SATA

sata1_rxp0
sata1_rxn0
sata1_txp0
sata1_txn0

CONTROL
VDDSHV3

nmin
porz
resetn
rstoutn

RTC
VDDSHV5

wakeup0/dcan1_rx/gpio1_0
wakeup1/dcan2_rx/gpio1_1
wakeup2/sys_nirq2/gpio1_2
wakeup3/sys_nirq1/gpio1_3

GPIO
VDDSHV3

gpio6_14/mcasp1_axr8/dcan2(mcan)_tx/uart10_rxd/vout2_hsync/vin4a_hsync0/i2c3_sda/timer1/gpio6_14
gpio6_15/mcasp1_axr9/dcan2(mcan)_rx/uart10_txd/vout2_vsync/vin4a_vsync0/i2c3_scl/timer2/gpio6_15
gpio6_16/mcasp1_axr10/vout2_fld/vin4a_fld0/clkout1/timer3/gpio6_16

CLOCKS
VDDA_OSC

xi_osc0
xo_osc0
vssa_osc0
xi_osc1
xo_osc1
vssa_osc1

VDDSHV3

xref_clk0/mcasp2_axr8/mcasp1_axr4/mcasp1_ahclkx/mcasp5_ahclkx/atl_clk0/hdq0/clkout2/timer13/pr2_mii1_col/xx/gpio6_17
xref_clk1/mcasp2_axr9/mcasp1_axr5/mcasp2_ahclkx/mcasp6_ahclkx/atl_clk1/timer14/pr2_mii1_crs/xx/gpio6_18
xref_clk2/mcasp2_axr10/mcasp1_axr6/mcasp3_ahclkx/mcasp7_ahclkx/atl_clk2/vout2_clk/vin4a_clk0/timer15/gpio6_19
xref_clk3/mcasp2_axr11/mcasp1_axr7/mcasp4_ahclkx/mcasp8_ahclkx/atl_clk3/vout2_de/hdq0/vin4a_de0/clkout3/timer16/gpio6_20

I2C
VDDSHV3

i2c1_scl
i2c1_sda
i2c2_scl/hdmi1_ddc_sda
i2c2_sda/hdmi1_ddc_scl

Debug
VDDSHV3

emu0/gpio8_30
emu1/gpio8_31
rtck/gpio8_29
tclk
tdi/gpio8_27
tdo/gpio8_28
tms
trstn

Si Test

iforce
vsense
atestv
vpp

These 3 "No Connects" are Silicon test signals that do not need to be routed, aka "Captured Signals".

U42A

H_NMIN 4
H_PORz 34
H_RESETn 34
H_RSTOUTn 19,20,24,25,26,27,33,34,38
H_WKUP_0 4,34
H_WKUP_1 4,33
H_GP1[2]_TOUCH_EVT 4,21,39
H_GP1[3] 4,18,39
H_I2C3_SDA_DCAN2_MCAN_TX 15
H_I2C3_SCL_DCAN2_MCAN_RX 15
H_ENET_INTSn 29
XI_OSC0 4
XI_OSC1 4
H_GP6[17] 39
H_XREF_CLK1 15
H_XREF_CLK2 25
H_AIC3106_MCLK 27
H_GP6[20] 39
H_I2C1_SCL 18,19,25,27,31,33,34,39
H_I2C1_SDA 18,19,25,27,31,33,34,39
H_I2C2_SCL 15
H_I2C2_SDA 15
H_EMU0 25
H_EMU1 25
H_RTCK 25
H_TCK 25
H_TDI 25
H_TDO 25
H_TMS 25
H_TRSTn 25

VIO_3V3
R618 2.2K
R626 2.2K

R234 0 XI_OSC0 4
AB16 H_XI_OSC0 C474 NP-18pF
Y5 NP-20MHz
AB14 H_XO_OSC0 C457 NP-18pF
AB15 VSSA_OSC0 R233 0

R247 0 XI_OSC1 4
AC19 H_XI_OSC1 C517 NP-18pF
Y7 NP-22.5792MHz
AB18 H_XO_OSC1 C518 NP-18pF
AC18 VSSA_OSC1 R243 0

R596 0 H_XREF_CLK1
R613 NP H_XREF_CLK2
R252 0 H_AIC3106_MCLK

R593 22 H_EMU0
R611 22 H_EMU1

R599 22 H_RTCK
R598 22 H_TDO

AQSPI PATH IS THE FAST PATH WITH MAX TRACE LENGTH OF 2.75 INCHES.

AQSPI1_RTCLK	R173 0 / R172 NP	H_GPMC_A13	4	
AQSPI1_D[3]	R187 0 / R186 NP	H_GPMC_A14	4	
AQSPI1_D[2]	R181 0 / R180 NP	H_GPMC_A15	4	
AQSPI1_D[0]	R170 0 / R169 NP	H_GPMC_A16	4	SPI_D[0] - I/O
AQSPI1_D[1]	R175 0 / R174 NP	H_GPMC_A17	4	
AQSPI1_SCLK	R185 0 / R184 NP	H_GPMC_A18	4	
AQSPI1_CS[0]	R171 0	H_GPMC_CS2	4	

VIO_3V3
R257 NP
TP73 H_GP1[2]_TOUCH_EVT 4,21,39
R259 10K

VIO_3V3
R269 10K
R266 NP
H_NMIN 4

VIO_3V3
R712 10K
TP74
H_WKUP_0 4,34

VIO_3V3
R242 10K
TP69
H_WKUP_1 4,33

TP72
H_GP1[3] 4,18,39
H_PCF8575_INT 18,39
R253 NP

NP-6.8pF C480
TP89
Y6 25MHz-8pF
C479 NP-6.8pF
U125 CDCEL925
VCTR VDD VDDOUT2 VDDOUT1 XIN/CLK XOUT S0 S1/SDA S2/SCL GND1 GND2
Y1 Y2 Y3 Y4 Y5
TP66 TP68 TP67
VDD_CDCEL925
C458 0.1uF C164 0.22uF C159 1uF C165 2.2uF
L19 220Ohm
VDA_PLL_APM 33,37
XIN_PDIV1_25MHz R584 22 XI_PHY0 29
XIN_PDIV2_25MHz R581 22 XI_PHY1 30
PLL1_PDIV3_20MHz XI_OSC0 4
PLL2_PDIV5_22p5792MHz XI_OSC1 4

COMMON CLOCK SOURCE FOR CPU AND ENET PHYS.

VPP
C405 0.1uF
1.8V
U37 TPS73101DBVR
OUT IN GND FB EN
R552 23.2K
47K R551
R550 10K
VPP_EN 18

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents:	J6PLUS_NONVOL_MEM_SYS		
Size: C	DOC NO: 518451	REV: C	
Date: Monday, November 13, 2017	Sheet 4 of 40		

J6Plus SYM-B

U42B

DRA77xP / DRA76xP / TDA2Px

Data Manual: SPRS993A_July_2017
Package: ACD, 23x23mm, 784 PBGA, 0.8mm Pitch
PCB Footprint: bga784_28x28_0p8mm
SCH Symbol: IC_J6Plus_ACD_23mm_784BGA_v1.0

VOLATILE MEMORY

EMIF1

VDDS_DDR1

13	H_DDR1_A0	AE22	ddr1_a0
13	H_DDR1_A1	AD20	ddr1_a1
13	H_DDR1_A2	AE21	ddr1_a2
13	H_DDR1_A3	AD22	ddr1_a3
13	H_DDR1_A4	AE23	ddr1_a4
13	H_DDR1_A5	AH22	ddr1_a5
13	H_DDR1_A6	AD24	ddr1_a6
13	H_DDR1_A7	AC22	ddr1_a7
13	H_DDR1_A8	AG23	ddr1_a8
13	H_DDR1_A9	AF24	ddr1_a9
13	H_DDR1_A10	AD21	ddr1_a10
13	H_DDR1_A11	AE24	ddr1_a11
13	H_DDR1_A12	AG21	ddr1_a12
13	H_DDR1_A13	AF21	ddr1_a13
13	H_DDR1_A14	AC23	ddr1_a14
13	H_DDR1_A15	AG20	ddr1_a15
13	H_DDR1_BA0	AE20	ddr1_ba0
13	H_DDR1_BA1	AC21	ddr1_ba1
13	H_DDR1_BA2	AH21	ddr1_ba2
13	H_DDR1_ODT0	AF22	ddr1_odt0
13	H_DDR1_CASN	AG19	ddr1_casn
13	H_DDR1_RASN	AH20	ddr1_rasn
13	H_DDR1_CKE	AH23	ddr1_cke
13	H_DDR1_CLK_P	AG24	ddr1_ck
13	H_DDR1_CLK_N	AH24	ddr1_nck
13	H_DDR1_CSN0	AD23	ddr1_csn0
13,35	H_DDR1_RST	AF23	ddr1_rst
13	H_DDR1_WEN	AG22	ddr1_wen
13	H_DDR1_DQM0	AG26	ddr1_dqm0
13	H_DDR1_DQS0_P	AH25	ddr1_dqs0
13	H_DDR1_DQS0_N	AG25	ddr1_dqsn0
13	H_DDR1_D0	AE26	ddr1_d0
13	H_DDR1_D1	AE27	ddr1_d1
13	H_DDR1_D2	AF28	ddr1_d2
13	H_DDR1_D3	AH26	ddr1_d3
13	H_DDR1_D4	AF25	ddr1_d4
13	H_DDR1_D5	AG27	ddr1_d5
13	H_DDR1_D6	AF27	ddr1_d6
13	H_DDR1_D7	AF26	ddr1_d7
13	H_DDR1_DQM1	AC24	ddr1_dqm1
13	H_DDR1_DQS1_P	AC27	ddr1_dqs1
13	H_DDR1_DQS1_N	AC28	ddr1_dqsn1
13	H_DDR1_D8	AB24	ddr1_d8
13	H_DDR1_D9	AD27	ddr1_d9
13	H_DDR1_D10	AE28	ddr1_d10
13	H_DDR1_D11	AD28	ddr1_d11
13	H_DDR1_D12	AD26	ddr1_d12
13	H_DDR1_D13	AE25	ddr1_d13
13	H_DDR1_D14	AD25	ddr1_d14
13	H_DDR1_D15	AC26	ddr1_d15
13	H_DDR1_DQM2	AB26	ddr1_dqm2
13	H_DDR1_DQS2_P	AB27	ddr1_dqs2
13	H_DDR1_DQS2_N	AB28	ddr1_dqsn2
13	H_DDR1_D16	AA25	ddr1_d16
13	H_DDR1_D17	AB25	ddr1_d17
13	H_DDR1_D18	AA26	ddr1_d18
13	H_DDR1_D19	AA28	ddr1_d19
13	H_DDR1_D20	AA27	ddr1_d20
13	H_DDR1_D21	AA24	ddr1_d21
13	H_DDR1_D22	AC25	ddr1_d22
13	H_DDR1_D23	Y26	ddr1_d23
13	H_DDR1_DQM3	Y27	ddr1_dqm3
13	H_DDR1_DQS3_P	W28	ddr1_dqs3
13	H_DDR1_DQS3_N	W27	ddr1_dqsn3
13	H_DDR1_D24	W26	ddr1_d24
13	H_DDR1_D25	AB23	ddr1_d25
13	H_DDR1_D26	V24	ddr1_d26
13	H_DDR1_D27	Y24	ddr1_d27
13	H_DDR1_D28	W25	ddr1_d28
13	H_DDR1_D29	Y25	ddr1_d29
13	H_DDR1_D30	W24	ddr1_d30
13	H_DDR1_D31	Y28	ddr1_d31
		AB22	ddr1_vref0

0 R292

VDDR_SOC_VREFSTL

C180 0.1uF

ECC

VDDS_DDR1

13	H_DDR1_ECC_DQM	T27	ddr1_dqm_ecc
13	H_DDR1_ECC_DQS_P	U27	ddr1_dqs_ecc
13	H_DDR1_ECC_DQS_N	U28	ddr1_dqsn_ecc
13	H_DDR1_ECC_D0	U25	ddr1_ecc_d0
13	H_DDR1_ECC_D1	U26	ddr1_ecc_d1
13	H_DDR1_ECC_D2	V25	ddr1_ecc_d2
13	H_DDR1_ECC_D3	V26	ddr1_ecc_d3
13	H_DDR1_ECC_D4	V27	ddr1_ecc_d4
13	H_DDR1_ECC_D5	T28	ddr1_ecc_d5
13	H_DDR1_ECC_D6	T26	ddr1_ecc_d6
13	H_DDR1_ECC_D7	V28	ddr1_ecc_d7

EMIF2

VDDS_DDR2

ddr2_a0	P25	H_DDR2_A0	14,40
ddr2_a1	P26	H_DDR2_A1	14,40
ddr2_a2	P28	H_DDR2_A2	14,40
ddr2_a3	P27	H_DDR2_A3	14,40
ddr2_a4	P24	H_DDR2_A4	14,40
ddr2_a5	P23	H_DDR2_A5	14,40
ddr2_a6	N26	H_DDR2_A6	14,40
ddr2_a7	M25	H_DDR2_A7	14,40
ddr2_a8	N28	H_DDR2_A8	14,40
ddr2_a9	M27	H_DDR2_A9	14,40
ddr2_a10	L25	H_DDR2_A10	14,40
ddr2_a11	N27	H_DDR2_A11	14,40
ddr2_a12	M28	H_DDR2_A12	14,40
ddr2_a13	R24	H_DDR2_A13	14,40
ddr2_a14	N24	H_DDR2_A14	14,40
ddr2_a15	R23	H_DDR2_A15	14,40
ddr2_ba0	L24	H_DDR2_BA0	14,40
ddr2_ba1	U24	H_DDR2_BA1	14,40
ddr2_ba2	M24	H_DDR2_BA2	14,40
ddr2_odt0	K25	H_DDR2_ODT0	14,40
ddr2_casn	T25	H_DDR2_CASN	14,40
ddr2_rasn	R26	H_DDR2_RASN	14,40
ddr2_cke	R25	H_DDR2_CKE	14,40
ddr2_ck	R28	H_DDR2_CLK_P	14,40
ddr2_nck	R27	H_DDR2_CLK_N	14,40
ddr2_csn0	M26	H_DDR2_CSN0	14,40
ddr2_rst	N25	H_DDR2_RST	14,35
ddr2_wen	T24	H_DDR2_WEN	14,40
ddr2_dqm0	C27	H_DDR2_DQM0	14
ddr2_dqs0	D28	H_DDR2_DQS0_P	14
ddr2_dqsn0	D27	H_DDR2_DQS0_N	14
ddr2_d0	C28	H_DDR2_D0	14
ddr2_d1	A26	H_DDR2_D1	14
ddr2_d2	E24	H_DDR2_D2	14
ddr2_d3	D25	H_DDR2_D3	14
ddr2_d4	D26	H_DDR2_D4	14
ddr2_d5	B27	H_DDR2_D5	14
ddr2_d6	B26	H_DDR2_D6	14
ddr2_d7	C26	H_DDR2_D7	14
ddr2_dqm1	E27	H_DDR2_DQM1	14
ddr2_dqs1	F27	H_DDR2_DQS1_P	14
ddr2_dqsn1	F28	H_DDR2_DQS1_N	14
ddr2_d8	F26	H_DDR2_D8	14
ddr2_d9	E25	H_DDR2_D9	14
ddr2_d10	E26	H_DDR2_D10	14
ddr2_d11	G27	H_DDR2_D11	14
ddr2_d12	E28	H_DDR2_D12	14
ddr2_d13	G26	H_DDR2_D13	14
ddr2_d14	G28	H_DDR2_D14	14
ddr2_d15	F25	H_DDR2_D15	14
ddr2_dqm2	G23	H_DDR2_DQM2	14
ddr2_dqs2	J27	H_DDR2_DQS2_P	14
ddr2_dqsn2	J28	H_DDR2_DQS2_N	14
ddr2_d16	G25	H_DDR2_D16	14
ddr2_d17	G24	H_DDR2_D17	14
ddr2_d18	F23	H_DDR2_D18	14
ddr2_d19	F24	H_DDR2_D19	14
ddr2_d20	H28	H_DDR2_D20	14
ddr2_d21	H25	H_DDR2_D21	14
ddr2_d22	H27	H_DDR2_D22	14
ddr2_d23	H26	H_DDR2_D23	14
ddr2_dqm3	J26	H_DDR2_DQM3	14
ddr2_dqs3	L28	H_DDR2_DQS3_P	14
ddr2_dqsn3	L27	H_DDR2_DQS3_N	14
ddr2_d24	K27	H_DDR2_D24	14
ddr2_d25	K26	H_DDR2_D25	14
ddr2_d26	J25	H_DDR2_D26	14
ddr2_d27	K28	H_DDR2_D27	14
ddr2_d28	H24	H_DDR2_D28	14
ddr2_d29	J24	H_DDR2_D29	14
ddr2_d30	K24	H_DDR2_D30	14
ddr2_d31	L26	H_DDR2_D31	14
ddr2_vref0	M22		

N25 R698 0 T24

VDDR_SOC_VREFSTL

C216 0.1uF

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD	
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U42F

DIFF-PAIR-100-OHM

CAMERA

CSI2

VDDA_CSI2

24	H_CSI2_0_DX0	AD17	csi2_0_dx0
24	H_CSI2_0_DY0	AD18	csi2_0_dy0
24	H_CSI2_0_DX1	AF16	csi2_0_dx1
24	H_CSI2_0_DY1	AF17	csi2_0_dy1
24	H_CSI2_0_DX2	AF19	csi2_0_dx2
24	H_CSI2_0_DY2	AF20	csi2_0_dy2
24	H_CSI2_0_DX3	AE15	csi2_0_dx3
24	H_CSI2_0_DY3	AE16	csi2_0_dy3
24	H_CSI2_0_DX4	AE19	csi2_0_dx4
24	H_CSI2_0_DY4	AE18	csi2_0_dy4
24	H_CSI2_1_DX0	AC13	csi2_1_dx0
24	H_CSI2_1_DY0	AC14	csi2_1_dy0
24	H_CSI2_1_DX1	AD15	csi2_1_dx1
24	H_CSI2_1_DY1	AD14	csi2_1_dy1
24	H_CSI2_1_DX2	AC16	csi2_1_dx2
24	H_CSI2_1_DY2	AC17	csi2_1_dy2

DRA77xP / DRA76xP / TDA2Px

Data Manual: SPRS993A_July_2017
Package: ACD, 23x23mm, 784 PBGA, 0.8mm Pitch
PCB Footprint: bga784_28x28_0p8mm
SCH Symbol: IC_J6Plus_ACD_23mm_784BGA_v1.0

DISPLAY

HDMI

VDDA_HDMI

DIFF-PAIR-100-OHM

AG14	hdmi1_clockx	H_HDMI_CLKX	23
AH15	hdmi1_clocky	H_HDMI_CLKY	23
AG15	hdmi1_data0x	H_HDMI_DX0	23
AH16	hdmi1_data0y	H_HDMI_DY0	23
AG17	hdmi1_data1x	H_HDMI_DX1	23
AH18	hdmi1_data1y	H_HDMI_DY1	23
AG18	hdmi1_data2x	H_HDMI_DX2	23
AH19	hdmi1_data2y	H_HDMI_DY2	23

VIDEO INPUT

VIP1

VDDSHV6

39	H_VIN1_D0	AE9	vin1a_d0/vout3_d7/vout3_d23/uart8_rxd/ehrpwm1A/gpio3_4
39	H_VIN1_D1	AF10	vin1a_d1/vout3_d6/vout3_d22/uart8_txd/ehrpwm1B/gpio3_5
39	H_VIN1_D2	AE7	vin1a_d2/vout3_d5/vout3_d21/uart8_ctsn/ehrpwm1_tripzone_input/gpio3_6
39	H_VIN1_D3	AE8	vin1a_d3/vout3_d4/vout3_d20/uart8_rtsn/eCAP1_in_PWM1_out/xx/gpio3_7
39	H_VIN1_D4	AE6	vin1a_d4/vout3_d3/vout3_d19/ehrpwm1_synci/xx/gpio3_8
39	H_VIN1_D5	AF7	vin1a_d5/vout3_d2/vout3_d18/ehrpwm1_synco/xx/gpio3_9
39	H_VIN1_D6	AF8	vin1a_d6/vout3_d1/vout3_d17/eQEP2A_in/xx/gpio3_10
39	H_VIN1_D7	AF6	vin1a_d7/vout3_d0/vout3_d16/eQEP2B_in/xx/gpio3_11
39	H_VIN1_D8	AF4	vin1a_d8/vin1b_d7/vout3_d15/kbd_row2/eQEP2_index/xx/gpio3_12
39	H_VIN1_D9	AF2	vin1a_d9/vin1b_d6/vout3_d14/kbd_row3/eQEP2_strobe/xx/gpio3_13
39	H_VIN1_D10	AF3	vin1a_d10/vin1b_d5/vout3_d13/kbd_row4/pr1_edc_latch0_in/xx/gpio3_14
39	H_VIN1_D11	AF5	vin1a_d11/vin1b_d4/vout3_d12/gpmc_a23/kbd_row5/pr1_edc_latch1_in/xx/gpio3_15
39	H_VIN1_D12	AE5	vin1a_d12/vin1b_d3/usb3_ulpi_d7/vout3_d11/gpmc_a24/kbd_row6/pr1_edc_sync0_out/xx/gpio3_16
39	H_VIN1_D13	AF1	vin1a_d13/vin1b_d2/usb3_ulpi_d6/vout3_d10/gpmc_a25/kbd_row7/pr1_edc_sync1_out/xx/gpio3_17
39	H_VIN1_D14	AD6	vin1a_d14/vin1b_d1/usb3_ulpi_d5/vout3_d9/gpmc_a26/kbd_row8/pr1_edio_latch_in/xx/gpio3_18
39	H_VIN1_D15	AE3	vin1a_d15/vin1b_d0/usb3_ulpi_d4/vout3_d8/gpmc_a27/kbd_col0/pr1_edio_sof/xx/gpio3_19
39	H_VIN1_D16	AE4	vin1a_d16/vin1b_d7/usb3_ulpi_d3/vout3_d7/vin3a_d0/kbd_col1/pr1_edio_data_in0/pr1_edio_data_out0/xx/gpio3_20
39	H_VIN1_D17	AE1	vin1a_d17/vin1b_d6/usb3_ulpi_d2/vout3_d6/vin3a_d1/kbd_col2/pr1_edio_data_in1/pr1_edio_data_out1/xx/gpio3_21
39	H_VIN1_D18	AD5	vin1a_d18/vin1b_d5/usb3_ulpi_d1/vout3_d5/vin3a_d2/kbd_col3/pr1_edio_data_in2/pr1_edio_data_out2/xx/gpio3_22
39	H_VIN1_D19	AD3	vin1a_d19/vin1b_d4/usb3_ulpi_d0/vout3_d4/vin3a_d3/kbd_col4/pr1_edio_data_in3/pr1_edio_data_out3/xx/gpio3_23
39	H_VIN1_D20	AD4	vin1a_d20/vin1b_d3/usb3_ulpi_nxt/vout3_d3/vin3a_d4/kbd_col5/pr1_edio_data_in4/pr1_edio_data_out4/xx/gpio3_24
39	H_VIN1_D21	AE2	vin1a_d21/vin1b_d2/usb3_ulpi_dir/vout3_d2/vin3a_d5/kbd_col6/pr1_edio_data_in5/pr1_edio_data_out5/xx/gpio3_25
39	H_VIN1_D22	AD1	vin1a_d22/vin1b_d1/usb3_ulpi_stp/vout3_d1/vin3a_d6/kbd_col7/pr1_edio_data_in6/pr1_edio_data_out6/xx/gpio3_26
39	H_VIN1_D23	AD2	vin1a_d23/vin1b_d0/usb3_ulpi_clk/vout3_d0/vin3a_d7/kbd_col8/pr1_edio_data_in7/pr1_edio_data_out7/xx/gpio3_27
39	H_VIN1A_CLK	AD8	vin1a_clk0/vout3_d16/vout3_fld/gpio2_30
39	H_VIN1B_CLK	AC8	vin1b_clk1/vin3a_clk0/gpio2_31
39	H_VIN1_VSYNC	AD7	vin1a_vsync0/vin1b_de1/vout3_vsync/uart7_rtsn/timer13/spi3_cs0/eQEP1_strobe/gpio3_3
39	H_VIN1_HSYNC	AC10	vin1a_hsync0/vin1b_fld1/vout3_hsync/uart7_ctsn/timer14/spi3_d0/eQEP1_index/gpio3_2
21	CON_LCD_PWR_DN	AD9	vin1a_fld0/vin1b_vsync1/vout3_clk/uart7_txd/timer15/spi3_d1/kbd_row1/eQEP1B_in/gpio3_1
39	H_VIN1_DE	AC9	vin1a_de0/vin1b_hsync1/vout3_d17/vout3_de/uart7_rxd/timer16/spi3_sclk/kbd_row0/eQEP1A_in/gpio3_0

VIP2

VDDSHV1

17	H_VIN2_D0	F2	vin2a_d0/vout2_d23/emu10/uart9_ctsn/spi4_d0/kbd_row4/ehrpwm1B/pr1_uart0_rxd/xx/gpio4_1
17	H_VIN2_D1	E3	vin2a_d1/vout2_d22/emu11/uart9_rtsn/spi4_cs0/kbd_row5/ehrpwm1_tripzone_input/pr1_uart0_txd/xx/gpio4_2
17	H_VIN2_D2	E1	vin2a_d2/vout2_d21/emu12/uart10_rxd/kbd_row6/eCAP1_in_PWM1_out/pr1_ecap0_ecap_capin_apwm_o/xx/gpio4_3
17	H_VIN2_D3	E2	vin2a_d3/vout2_d20/emu13/uart10_txd/kbd_col0/ehrpwm1_synci/pr1_edc_latch0_in/xx/gpio4_4
17	H_VIN2_D4	D2	vin2a_d4/vout2_d19/emu14/uart10_ctsn/kbd_col1/ehrpwm1_synco/pr1_edc_sync0_out/xx/gpio4_5
17	H_VIN2_D5	F3	vin2a_d5/vout2_d18/emu15/uart10_rtsn/kbd_col2/eQEP2A_in/pr1_edio_sof/xx/gpio4_6
17	H_VIN2_D6	D1	vin2a_d6/vout2_d17/emu16/mii1_rxd1/kbd_col3/eQEP2B_in/pr1_mii_mt1_clk/xx/gpio4_7
17	H_VIN2_D7	E4	vin2a_d7/vout2_d16/emu17/mii1_rxd2/kbd_col4/eQEP2_index/pr1_mii1_txen/xx/gpio4_8
17	H_VIN2_D8	G3	vin2a_d8/vout2_d15/emu18/mii1_rxd3/kbd_col5/eQEP2_strobe/pr1_mii1_txd3/xx/gpio4_9(gpmc_a26)
17	H_VIN2_D9	C5	vin2a_d9/vout2_d14/emu19/mii1_rxd0/kbd_col6/ehrpwm2A/pr1_mii1_txd2/xx/gpio4_10(gpmc_a25)
17	H_VIN2_D10	D3	vin2a_d10/mdio_mclk/vout2_d13/kbd_col7/ehrpwm2B/pr1_mdio_mdclk/xx/gpio4_11(gpmc_a24)
17	H_VIN2_D11	F4	vin2a_d11/mdio_d/vout2_d12/kbd_row7/ehrpwm2_tripzone_input/pr1_mdio_data/xx/gpio4_12(gpmc_a23)
17	H_VIN2_D12	R556 0 E6	vin2a_d12/rgmii1_txc/vout2_d11/mii1_rxclk/kbd_col8/eCAP2_in_PWM2_out/pr1_mii1_txd1/xx/gpio4_13
17	H_VIN2_D13	R176 0 C1	vin2a_d13/rgmii1_txctl/vout2_d10/mii1_rxdv/kbd_row8/eQEP3A_in/pr1_mii1_txd0/xx/gpio4_14
17	H_VIN2_D14	R178 0 C2	vin2a_d14/rgmii1_txd3/vout2_d9/mii1_txclk/eQEP3B_in/pr1_mii_mr1_clk/xx/gpio4_15
17	H_VIN2_D15	R554 0 C3	vin2a_d15/rgmii1_txd2/vout2_d8/mii1_txd0/eQEP3_index/pr1_mii1_rxdv/xx/gpio4_16
17	H_VIN2_D16	R177 0 B2	vin2a_d16/vin2b_d7/rgmii1_txd1/vout2_d7/vin3a_d8/mii1_txd1/eQEP3_strobe/pr1_mii1_rxd3/xx/gpio4_24
17	H_VIN2_D17	R558 0 B5	vin2a_d17/vin2b_d6/rgmii1_txd0/vout2_d6/vin3a_d9/mii1_txd2/ehrpwm3A/pr1_mii1_rxd2/xx/gpio4_25
17	H_VIN2_D18	D4	vin2a_d18/vin2b_d5/rgmii1_rxc/vout2_d5/vin3a_d10/mii1_txd3/ehrpwm3B/pr1_mii1_rxd1/xx/gpio4_26
17	H_VIN2_D19	A3	vin2a_d19/vin2b_d4/rgmii1_rxctl/vout2_d4/vin3a_d11/mii1_txer/ehrpwm3_tripzone_input/pr1_mii1_rxd0/xx/gpio4_27
17	H_VIN2_D20	B3	vin2a_d20/vin2b_d3/rgmii1_rxd3/vout2_d3/vin3a_de0/vin3a_d12/mii1_rxer/eCAP3_in_PWM3_out/pr1_mii1_rxer/xx/gpio4_28
17	H_VIN2_D21	B4	vin2a_d21/vin2b_d2/rgmii1_rxd2/vout2_d2/vin3a_fld0/vin3a_d13/mii1_col/pr1_mii1_rxlink/xx/gpio4_29
17	H_VIN2_D22	C4	vin2a_d22/vin2b_d1/rgmii1_rxd1/vout2_d1/vin3a_hsync0/vin3a_d14/mii1_crs/pr1_mii1_col/xx/gpio4_30
17	H_VIN2_D23	A4	vin2a_d23/vin2b_d0/rgmii1_rxd0/vout2_d0/vin3a_vsync0/vin3a_d15/mii1_txen/pr1_mii1_crs/xx/gpio4_31
17	H_VIN2_CLK	F1	vin2a_clk0/vout2_fld/emu5/kbd_row0/eQEP1A_in/xx/gpio3_28(gpmc_a27/gpmc_a17)
17	H_VIN2_VSYNC	E5	vin2a_vsync0/vin2b_vsync1/vout2_vsync/emu9/uart9_txd/spi4_d1/kbd_row3/ehrpwm1A/pr1_uart0_rts_n/xx/gpio4_0
17	H_VIN2_HSYNC	G1	vin2a_hsync0/vin2b_hsync1/vout2_hsync/emu8/uart9_rxd/spi4_sclk/kbd_row2/eQEP1_strobe/pr1_uart0_cts_n/xx/gpio3_31(gpmc_a27)
17	H_VIN2_DE	D5	vin2a_fld0/vin2b_clk1/vout2_clk/emu7/eQEP1_index/xx/gpio3_30(gpmc_a27/gpmc_a18)
		G2	vin2a_de0/vin2a_fld0/vin2b_fld1/vin2b_de1/vout2_de/emu6/kbd_row1/eQEP1B_in/xx/gpio3_29

TP56 1

35 H_POWERHOLD_CLK 0 R571

VIDEO OUTPUT

VOP1

VDDSHV2

F9	22	R567	H_LCD_B0 21
E10	22	R198	H_LCD_B1 21
D9	0	R206	H_LCD_B2 21,25
C6	22	R201	H_LCD_B3 21,25
E9	22	R568	H_LCD_B4 21,25
F8	22	R562	H_LCD_B5 21,25
F7	22	R565	H_LCD_B6 21,25
E7	22	R553	H_LCD_B7 21,25
E8	22	R555	H_LCD_G0 21
D8	22	R564	H_LCD_G1 21
D6	22	R561	H_LCD_G2 21,25
D7	22	R557	H_LCD_G3 21,25
A5	22	R200	H_LCD_G4 21,25
B6	22	R559	H_LCD_G5 21,25
C8	22	R560	H_LCD_G6 21,25
C7	22	R563	H_LCD_G7 21,25
B7	22	R203	H_LCD_R0 21
B8	22	R195	H_LCD_R1 21
A6	22	R199	H_LCD_R2 21,25
A7	22	R202	H_LCD_R3 21,25
C9	22	R566	H_LCD_R4 21,25
A8	22	R197	H_LCD_R5 21,25
B9	22	R212	H_LCD_R6 21,25
A9	22	R207	H_LCD_R7 21,25
D11	0	R574	H_LCD_PCLK 21
D10	22	R570	H_LCD_VS 21
A10	22	R577	H_LCD_HS 21
B10			
C10	22	R210	H_LCD_DE 21

22 OHM OK FOR LCD AS IT IS NOT GOING THROUGH MUXES, EXCEPT FOR THE CLOCK PINS

LCD_B2 = EMU2 TRACE CLOCK

vout1_d0/uart5_rxd/vin4a_d16/vin3a_d16/spi3_cs2/pr1_uart0_cts_n/xx/gpio8_0
vout1_d1/uart5_txd/vin4a_d17/vin3a_d17/pr1_uart0_rts_n/xx/gpio8_1
vout1_d2/emu2/vin4a_d18/vin3a_d18/obs0/obs16/obs_irq1/pr1_uart0_rxd/xx/gpio8_2
vout1_d3/emu5/vin4a_d19/vin3a_d19/obs1/obs17/obs_dmarq1/pr1_uart0_txd/xx/gpio8_3
vout1_d4/emu6/vin4a_d20/vin3a_d20/obs2/obs18/pr1_ecap0_ecap_capin_apwm_o/xx/gpio8_4
vout1_d5/emu7/vin4a_d21/vin3a_d21/obs3/obs19/pr2_edc_latch0_in/xx/gpio8_5
vout1_d6/emu8/vin4a_d22/vin3a_d22/obs4/obs20/pr2_edc_latch1_in/xx/gpio8_6
vout1_d7/emu9/vin4a_d23/vin3a_d23/pr2_edc_sync0_out/xx/gpio8_7
vout1_d8/uart6_rxd/vin4a_d8/vin3a_d8/pr2_edc_sync1_out/xx/gpio8_8
vout1_d9/uart6_txd/vin4a_d9/vin3a_d9/pr2_edio_latch_in/xx/gpio8_9
vout1_d10/emu3/vin4a_d10/vin3a_d10/obs5/obs21/obs_irq2/pr2_edio_sof/xx/gpio8_10
vout1_d11/emu10/vin4a_d11/vin3a_d11/obs6/obs22/obs_dmarq2/pr2_uart0_cts_n/xx/gpio8_11
vout1_d12/emu11/vin4a_d12/vin3a_d12/obs7/obs23/pr2_uart0_rts_n/xx/gpio8_12
vout1_d13/emu12/vin4a_d13/vin3a_d13/obs8/obs24/pr2_uart0_rxd/xx/gpio8_13
vout1_d14/emu13/vin4a_d14/vin3a_d14/obs9/obs25/pr2_uart0_txd/xx/gpio8_14
vout1_d15/emu14/vin4a_d15/vin3a_d15/obs10/obs26/pr2_ecap0_ecap_capin_apwm_o/xx/gpio8_15
vout1_d16/uart7_rxd/vin4a_d0/vin3a_d0/pr2_edio_data_in0/pr2_edio_data_out0/xx/gpio8_16
vout1_d17/uart7_txd/vin4a_d1/vin3a_d1/pr2_edio_data_in1/pr2_edio_data_out1/xx/gpio8_17
vout1_d18/emu4/vin4a_d2/vin3a_d2/obs11/obs27/pr2_edio_data_in2/pr2_edio_data_out2/xx/gpio8_18
vout1_d19/emu15/vin4a_d3/vin3a_d3/obs12/obs28/pr2_edio_data_in3/pr2_edio_data_out3/xx/gpio8_19
vout1_d20/emu16/vin4a_d4/vin3a_d4/obs13/obs29/pr2_edio_data_in4/pr2_edio_data_out4/xx/gpio8_20
vout1_d21/emu17/vin4a_d5/vin3a_d5/obs14/obs30/pr2_edio_data_in5/pr2_edio_data_out5/xx/gpio8_21
vout1_d22/emu18/vin4a_d6/vin3a_d6/obs15/obs31/pr2_edio_data_in6/pr2_edio_data_out6/xx/gpio8_22
vout1_d23/emu19/vin4a_d7/vin3a_d7/spi3_cs3/pr2_edio_data_in7/pr2_edio_data_out7/xx/gpio8_23

vout1_clk/vin4a_fld0/vin3a_fld0/spi3_cs0/gpio4_19
vout1_vsync/vin4a_vsync0/vin3a_vsync0/spi3_sclk/xx/gpio4_23
vout1_hsync/vin4a_hsync0/vin3a_hsync0/spi3_d0/gpio4_22
vout1_fld/vin4a_clk0/vin3a_clk0/spi3_cs1/gpio4_21
vout1_de/vin4a_de0/vin3a_de0/spi3_d1/gpio4_20

1 TP57

H_MMC_PWR_ON 18

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J6Plus SYM-E

CONNECTIVITY

PCIe

DIFF-PAIR-100-OHM

26	H_PCIE_RXP0	AH12	pcie_rxp0
26	H_PCIE_RXN0	AG11	pcie_rxn0
26	H_PCIE_TXP0	AH13	pcie_txp0
26	H_PCIE_TXN0	AG12	pcie_txn0
26	H_PCIE_RXP1	AH9	pcie_rxp1
26	H_PCIE_RXN1	AG8	pcie_rxn1
26	H_PCIE_TXP1	AH10	pcie_txp1
26	H_PCIE_TXN1	AG9	pcie_txn1
26	H_LJCB_CLKP	AE13	ljcb_clkp
26	H_LJCB_CLKN	AF14	ljcb_clkn

VDDA_PCIE0 / VDDA_PCIE1 / VDDA_PCIE

USB

28	H_USB1_DP	AF11	usb1_dp
28	H_USB1_DN	AE10	usb1_dm
28	H_USB1_DRV_VBUS	AD12	usb1_drvvbus/timer16/gpio6_12
22	H_USB2_DP	AE12	usb2_dp
22	H_USB2_DN	AF13	usb2_dm
22	H_USB2_DRV_VBUS	AC11	usb2_drvvbus/timer15/gpio6_13
28	H_USB3_RXP	AH4	usb_rxp0
28	H_USB3_RXN	AG3	usb_rxn0
28	H_USB3_TXP	AH3	usb_txp0
28	H_USB3_TXN	AG2	usb_txn0

VDDA33V_USB1 / VDDSHV6 / VDDA33V_USB2 / VDDSHV6 / VDDA_USB1

USB-DIFF-PAIR-90-OHM

17	H_RGMII0_TXC	R526 0	T6	rgmii0_txc/uart3_ctsn/rmii1_rxd1/mii0_rxd3/vin2a_d3/vin4b_d3/usb4_ulpi_clk/spi3_d0/spi4_cs2/pr1_mii0_rxd3/xx/gpio5_20
17	H_RGMII0_TXCTL	R524 0	U5	rgmii0_txctl/uart3_rtsn/rmii1_rxd0/mii0_rxd2/vin2a_d4/vin4b_d4/usb4_ulpi_stp/spi3_cs0/spi4_cs3/pr1_mii0_rxd2/xx/gpio5_21
17	H_RGMII0_TXD0	R529 0	T5	rgmii0_txd0/rmii0_rxd0/mii0_rxd0/vin2a_d10/usb4_ulpi_d1/spi4_cs0/uart4_rtsn/pr1_mii0_rxd0/xx/gpio5_25
17	H_RGMII0_TXD1	R530 0	U6	rgmii0_txd1/rmii0_rxd1/mii0_rxd1/vin2a_vsync0/vin4b_vsync1/usb4_ulpi_d0/spi4_d0/uart4_ctsn/pr1_mii0_rxd1/xx/gpio5_24
17	H_RGMII0_TXD2	R531 0	T3	rgmii0_txd2/rmii0_rxer/mii0_rxer/vin2a_hsync0/vin4b_hsync1/usb4_ulpi_nxt/spi4_d1/uart4_txd/pr1_mii0_rxer/xx/gpio5_23
17	H_RGMII0_TXD3	R532 0	T4	rgmii0_txd3/rmii0_crs/mii0_crs/vin2a_de0/vin4b_de1/usb4_ulpi_dir/spi4_sclk/uart4_rxd/pr1_mii0_crs/xx/gpio5_22
17	H_RGMII0_RXC		U4	rgmii0_rxc/rmii1_txen/mii0_txclk/vin2a_d5/vin4b_d5/usb4_ulpi_d2/pr1_mii_mt0_clk/xx/gpio5_26
17	H_RGMII0_RXCTL		V4	rgmii0_rxctl/rmii1_txd1/mii0_txd3/vin2a_d6/vin4b_d6/usb4_ulpi_d3/pr1_mii0_txd3/xx/gpio5_27
17	H_RGMII0_RXD0		W1	rgmii0_rxd0/rmii0_txd0/mii0_txd0/vin2a_fld0/vin4b_fld1/usb4_ulpi_d7/pr1_mii0_txd0/xx/gpio5_31
17	H_RGMII0_RXD1		Y2	rgmii0_rxd1/rmii0_txd1/mii0_txd1/vin2a_d9/usb4_ulpi_d6/pr1_mii0_txd1/xx/gpio5_30
17	H_RGMII0_RXD2		V3	rgmii0_rxd2/rmii0_txen/mii0_txen/vin2a_d8/usb4_ulpi_d5/pr1_mii0_txen/xx/gpio5_29
17	H_RGMII0_RXD3		W2	rgmii0_rxd3/rmii1_txd0/mii0_txd2/vin2a_d7/vin4b_d7/usb4_ulpi_d4/pr1_mii0_txd2/xx/gpio5_28
39	H_GP5[17]		U2	RMII_MHZ_50_CLK/vin2a_d11/xx/gpio5_17
17	H_MDIO_D		U3	mdio_d/uart3_ctsn/mii0_txer/vin2a_d0/vin4b_d0/pr1_mii0_rxlink/xx/gpio5_16
17	H_MDIO_MCLK		V1	mdio_mclk/uart3_rtsn/mii0_col/vin2a_clk0/vin4b_clk1/pr1_mii0_col/xx/gpio5_15

DRA77xP / DRA76xP / TDA2Px

Data Manual: SPRS993A_July_2017
Package: ACD, 23x23mm, 784 PBGA, 0.8mm Pitch
PCB Footprint: bga784_28x28_0p8mm
SCH Symbol: IC_J6Plus_ACD_23mm_784BGA_v1.0

ETHERNET

VDDSHV9

7,25	H_MLBP_CLKP	AB1	mlbp_clk_p
7,25	H_MLBP_CLKN	AB2	mlbp_clk_n
7,25	H_MLBP_DP	AA1	mlbp_dat_p
7,25	H_MLBP_DN	AA2	mlbp_dat_n
7,25	H_MLBP_SIGP	AC1	mlbp_sig_p
7,25	H_MLBP_SIGN	AC2	mlbp_sig_n

MLBP

VDDS_MLBP

DIFF-PAIR-100-OHM

UART

VDDSHV4

25	H_UART1_TXD	C21	uart1_txd/mmc4_sdwp/gpio7_23
25	H_UART1_RXD	F22	uart1_rxd/mmc4_sdcd/gpio7_22
31	H_MMC4_CMD	E23	uart1_rtsn/uart9_txd/mmc4_cmd/gpio7_25
31	H_MMC4_CLK	F21	uart1_ctsn/uart9_rxd/mmc4_clk/gpio7_24
31	H_MMC4_DAT1	E22	uart2_txd/uart3_rtsn/uart3_sd/mmc4_dat1/uart2_txd/uart1_dsrn/gpio7_27
31	H_MMC4_DAT0	D22	uart2_rxd/uart3_ctsn/uart3_rctx/mmc4_dat0/uart2_rxd/uart1_dcdn/gpio7_26
31	H_MMC4_DAT3	C22	uart2_rtsn/uart3_txd/uart3_irtx/mmc4_dat3/uart10_txd/uart1_rin/gpio1_17
31	H_MMC4_DAT2	F20	uart2_ctsn/uart3_irrx/mmc4_dat2/uart10_rxd/uart1_dtrn/gpio1_16
25	H_UART3_TXD_BOOT	Y1	uart3_txd/rmii1_rxer/mii0_rxclk/vin2a_d2/vin4b_d2/spi3_d1/spi4_cs1/pr1_mii_mr0_clk/xx/gpio5_19
25	H_UART3_RXD_BOOT	V2	uart3_rxd/rmii1_crs/mii0_rxdv/vin2a_d1/vin4b_d1/spi3_sclk/pr1_mii0_rxdv/xx/gpio5_18
17	H_UART3_TXD		
17	H_UART3_RXD		

NP R157 / NP R158

VDDSHV9

MCASP

VDDSHV3

U42E

A13			mcasp1_aclkr/mcasp7_axr2/vout2_d0/vin4a_d0/i2c4_sda/gpio5_0
B13	R580 0	H_GP5[0] 38,39	mcasp1_aclkx/i2c3_sda/pr2_mdio_mdclk/xx/gpio7_31
C13	R582 0	HDMI_LS_OE 23	mcasp1_fsx/i2c3_scl/pr2_mdio_data/gpio7_30
F14		HDMI_CT_HPD 23	mcasp1_fsr/mcasp7_axr3/vout2_d1/vin4a_d1/i2c4_scl/gpio5_1
F10		H_GP5[1] 39	mcasp1_axr0/uart6_rxd/i2c5_sda/pr2_mii0_rxer/xx/gpio5_2
F11		H_I2C5_SDA 15	mcasp1_axr1/uart6_txd/i2c5_scl/pr2_mii_mt0_clk/xx/gpio5_3
E13		H_I2C5_SCL 15	mcasp1_axr2/mcasp6_axr2/uart6_ctsn/vout2_d2/vin4a_d2/gpio5_4
E11		H_GP5[4] 31	mcasp1_axr3/mcasp6_axr3/uart6_rtsn/vout2_d3/vin4a_d3/gpio5_5
E12		H_GP5[5] 31	mcasp1_axr4/mcasp4_axr2/vout2_d4/vin4a_d4/gpio5_6
D13		H_GP5[6] 31	mcasp1_axr5/mcasp4_axr3/vout2_d5/vin4a_d5/gpio5_7
C11		H_GP5[7] 31	mcasp1_axr6/mcasp5_axr2/vout2_d6/vin4a_d6/gpio5_8
D12		H_GP5[8] 31	mcasp1_axr7/mcasp5_axr3/vout2_d7/vin4a_d7/timer4/gpio5_9
B11		H_GP5[9] 25	mcasp1_axr8/mcasp6_axr0/spi3_sclk/timer5/pr2_mii0_txen/xx/gpio5_10
A11		H_MCA6_AXR0 15	mcasp1_axr9/mcasp6_axr1/spi3_d1/timer6/pr2_mii0_txd3/xx/gpio5_11
C12	R209 0	H_MCA6_AXR1 15	mcasp1_axr10/mcasp6_aclkx/mcasp6_aclkr/spi3_d0/timer7/pr2_mii0_txd2/xx/gpio5_12
A12	R213 0	H_MCA6_CLKX 15	mcasp1_axr11/mcasp6_fsx/mcasp6_fsr/spi3_cs0/timer8/pr2_mii0_txd1/xx/gpio4_17
D14		H_MCA6_FSX 15	mcasp1_axr12/mcasp7_axr0/spi3_cs1/timer9/pr2_mii0_txd0/xx/gpio4_18
B12		H_MCA7_AXR0 15	mcasp1_axr13/mcasp7_axr1/timer10/pr2_mii_mr0_clk/xx/gpio6_4
F12	R583 0	H_MCA7_AXR1 15	mcasp1_axr14/mcasp7_aclkx/mcasp7_aclkr/timer11/pr2_mii0_rxdv/xx/gpio6_5
E14	R218 0	H_MCA7_CLKX 15	mcasp1_axr15/mcasp7_fsx/mcasp7_fsr/timer12/pr2_mii0_rxd3/xx/gpio6_6
E15		H_MCA7_FSX 15	
A18	R231 0	TP65 1	mcasp2_aclkr/mcasp8_axr2/vout2_d8/vin4a_d8
A17	R224 0	H_MCA2_ACLKX 15	mcasp2_aclkx/pr2_mii0_rxd2/xx
A19		H_MCA2_AFSX 15	mcasp2_fsx/pr2_mii0_rxd1/xx
B14		TP75 1	mcasp2_fsr/mcasp8_axr3/vout2_d9/vin4a_d9
A14		H_MCA2_AXR0 15	mcasp2_axr0/vout2_d10/vin4a_d10
C14		H_MCA2_AXR1 15	mcasp2_axr1/vout2_d11/vin4a_d11
A15		H_MCA2_AXR2 15	mcasp2_axr2/mcasp3_axr2/vin6a_d5/pr2_mii0_rxd0/xx/gpio6_8
D15		H_MCA2_AXR3 15	mcasp2_axr3/mcasp3_axr3/vin6a_d4/pr2_mii0_rxlink/xx/gpio6_9
B15		H_MCA2_AXR4 15	mcasp2_axr4/mcasp8_axr0/vout2_d12/vin4a_d12/gpio1_4
B16		H_MCA2_AXR5 15	mcasp2_axr5/mcasp8_axr1/vout2_d13/vin4a_d13/gpio6_7
A16		H_MCA2_AXR6 15	mcasp2_axr6/mcasp8_aclkx/mcasp8_aclkr/vout2_d14/vin4a_d14/gpio2_29
		H_MCA2_AXR7 15	mcasp2_axr7/mcasp8_fsx/mcasp8_fsr/vout2_d15/vin4a_d15/gpio1_5
B17	R221 0	H_MCA3_ACLKX 15	mcasp3_aclkx/mcasp3_aclkr/mcasp2_axr12/uart7_rxd/pr2_mii0_crs/xx/gpio5_13
F13	R214 0	H_MCA3_AFSX 15	mcasp3_fsx/mcasp3_fsr/mcasp2_axr13/uart7_txd/pr2_mii0_col/xx/gpio5_14
B18	R228 0	H_MCA3_AXR0 15	mcasp3_axr0/mcasp2_axr14/uart7_ctsn/uart5_rxd/pr2_mii1_rxer/xx
C16	R586 0	H_MCA3_AXR1 15	mcasp3_axr1/mcasp2_axr15/uart7_rtsn/uart5_txd/pr2_mii1_rxlink/xx
C17		H_VIN[5]A_D[15] 39	mcasp4_aclkx/mcasp4_aclkr/spi3_sclk/uart8_rxd/i2c4_sda/vout2_d16/vin4a_d16
A20		H_VIN[5]A_D[14] 39	mcasp4_fsx/mcasp4_fsr/spi3_d1/uart8_txd/i2c4_scl/vout2_d17/vin4a_d17
D16		H_VIN[5]A_D[13] 39	mcasp4_axr0/spi3_d0/uart8_ctsn/uart4_rxd/vout2_d18/vin4a_d18
D17		H_VIN[5]A_D[12] 39	mcasp4_axr1/spi3_cs0/uart8_rtsn/uart4_txd/vout2_d19/vin4a_d19/xx
AA3		R535 NP	mcasp5_aclkx/mcasp5_aclkr/spi4_sclk/uart9_rxd/i2c5_sda/mlb_clk/vout2_d20/vin4a_d20/xx
AB6		R539 0 H_MLBP_CLK 25	mcasp5_fsx/mcasp5_fsr/spi4_d1/uart9_txd/i2c5_scl/vout2_d21/vin4a_d21/xx
AB3		R542 0 H_VIN[5]A_D[11] 39	mcasp5_axr0/spi4_d0/uart9_ctsn/uart3_rxd/mlb_sig/vout2_d22/vin4a_d22/pr2_mdio_mdclk/xx
AA4		R540 NP H_VIN[5]A_D[10] 39	mcasp5_axr1/spi4_cs0/uart9_rtsn/uart3_txd/mlb_dat/vout2_d23/vin4a_d23/pr2_mdio_data/xx
		R536 0 H_MLBP_SIG 25	
		R190 NP H_VIN[5]A_D[9] 39	
		R543 0 H_MLBP_DAT 25	
		H_VIN[5]A_D[8] 39	

SPI

VDDSHV3

A23	R245 0 R607 0	H_CAM_SPI[1]_CS[0]n 24	spi1_cs0/gpio7_10
A21		H_SPI[1]_CS[0]n 39	spi1_cs1/sata1_led/spi2_cs1/gpio7_11
B20		H_SPI[1]_CS[1]n 39	spi1_cs2/uart4_rxd/mmc3_sdcd/spi2_cs2/dcan2_tx/mdio_mclk/hdmi1_hpd/gpio7_12
B19		H_SPI1_CS2n 23	spi1_cs3/uart4_txd/mmc3_sdwp/spi2_cs3/dcan2_rx/mdio_d/hdmi1_cec/gpio7_13
B24		H_SPI1_CS3n 23	spi1_d0/gpio7_9
C15		R235 0	spi1_d1/gpio7_8
A24		R603 0 H_CAM_SPI[1]_MOSI 24	spi1_sclk/gpio7_7
		R578 0 H_SPI[1]_MOSI 39	
		R216 0 H_SPI[1]_MISO 39	
		H_CAM_SPI[1]_MISO 24	
		H_SPI1_SCLK 7	
B23		H_SPI2_CS0n 15	spi2_cs0/uart3_rtsn/uart5_txd/gpio7_17
E16		H_SPI2_MOSI 15	spi2_d0/uart3_ctsn/uart5_rxd/gpio7_16
B21		H_SPI2_MISO 15	spi2_d1/uart3_txd/gpio7_15
A25	R255 0	H_SPI2_SCLK 15	spi2_sclk/uart3_rxd/gpio7_14

DCAN (MCAN)

VDDSHV3

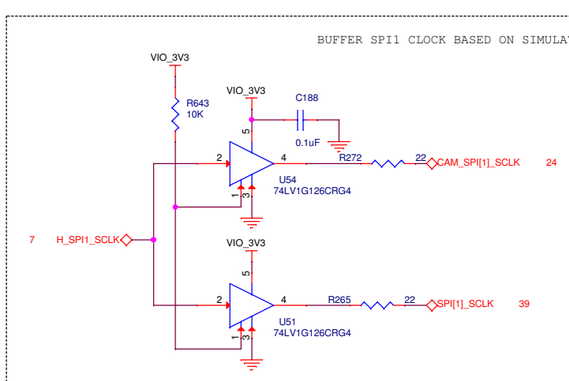
E19		H_DCAN1_MCAN_TX 39	dcan1(mcan)_tx/uart8_rxd/mmc2_sdcd/hdmi1_hpd/gpio1_14
D19		H_DCAN1_MCAN_RX 39	dcan1(mcan)_rx/uart8_txd/mmc2_sdwp/sata1_led/hdmi1_cec/gpio1_15

PLACE 100 OHM RESISTORS AT CPU

R167 100	H_MLBP_CLKP	7,25
	H_MLBP_CLKN	7,25
R166 100	H_MLBP_DP	7,25
	H_MLBP_DN	7,25
R165 100	H_MLBP_SIGP	7,25
	H_MLBP_SIGN	7,25

DIFF-PAIR-100-OHM

BUFFER SPI1 CLOCK BASED ON SIMULATIONS



TEXAS INSTRUMENTS INCORPORATED	
Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD
Page Contents:	J6PLUS_CONVITY
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J6Plus SYM-C

DRA77xP / DRA76xP / TDA2Px

Data Manual: SPRS993A_July_2017
Package: ACD, 23x23mm, 784 PBGA, 0.8mm Pitch
PCB Footprint: bga784_28x28_0p8mm
SCH Symbol: IC_J6Plus_ACD_23mm_784BGA_v1.0

POWER

ANALOG SUPPLIES

INTERNAL LDOs

U42C

VDA_PLL_1V8
E7 — 0.47uF 3T-0805 10V 0.3A
C450 1uF 10V X7S 0402
C431 0.1uF 16V X7R 0402
VDA_ABEPERMPU_F1V8 → N9 vdda_abe_per_1, P16 vdda_abe_per_2, P18 vdda_mpu

E8 — 0.47uF 3T-0805 10V 0.3A
C469 1uF 10V X7S 0402
C461 0.1uF 16V X7R 0402
VDA_DDRGCOREVID_F1V8 → N19 vdda_ddr, R15 vdda_gmac_core, R14 vdda_video

E9 — 0.47uF 3T-0805 10V 0.3A
C496 1uF 10V X7S 0402
C483 0.1uF 16V X7R 0402
VDA_DBGDSPEVE_F1V8 → N13 vdda_debug, J13 vdda_dsp_eve

E10 — 0.47uF 3T-0805 10V 0.3A
C521 1uF 10V X7S 0402
C508 0.1uF 16V X7R 0402
VDA_GPUIVA_F1V8 → W15 vdda_gpu, P20 vdda_iva

E12 — 0.47uF 3T-0805 10V 0.3A
C526 1uF 10V X7S 0402
C519 0.1uF 16V X7R 0402
VDA_OSC_F1V8 → AA15 vdda_osc

VDA_PHY1_1V8
E5 — 0.47uF 3T-0805 10V 0.3A
C388 1uF 10V X7S 0402
C389 0.1uF 16V X7R 0402
VDA_CSI_F1V8 → W17 vdda_csi

VDA_PHY2_1V8
E6 — 0.47uF 3T-0805 10V 0.3A
C386 1uF 10V X7S 0402
C387 0.47uF 10V X7S 0402
VDA_HDMI_F1V8 → AA17 vdda_hdmi

VDA_PHY1_1V8
E4 — 0.47uF 3T-0805 10V 0.3A
C370 1uF 10V X7S 0402
C371 0.1uF 16V X7R 0402
VDA_PCIE_F1V8 → Y12 vdda_pcie, Y14 vdda_pcie0, AB12 vdda_pcie1

VDA_PHY2_1V8
E2 — 0.47uF 3T-0805 10V 0.3A
C364 1uF 10V X7S 0402
C363 0.1uF 16V X7R 0402
VDA_SATA_F1V8 → AA13 vdda_sata

VDA_PHY2_1V8
E3 — 0.47uF 3T-0805 10V 0.3A
C367 1uF 10V X7S 0402
C368 0.1uF 16V X7R 0402
VDA_USB_F1V8 → Y10 vdda_usb_1, AA9 vdda_usb_2, AA11 vdda_usb_3

VDA_USB_3V3
C147 10uF 10V X7R 0805
C378 1uF 10V X7S 0402
C445 0.1uF 16V X7R 0402
AD11 vdda33v_usb1, AB10 vdda33v_usb2

cap_vbbldo_dspeve → J11 VCAP_VBBLDO_DSPEVE
cap_vbbldo_gpu → U13 VCAP_VBBLDO_GPU
cap_vbbldo_iva → R19 VCAP_VBBLDO_IVA
cap_vbbldo_mpu → J19 VCAP_VBBLDO_MPU
C494 1uF 10V X7S 0402, C486 1uF 10V X7S 0402, C449 1uF 10V X7S 0402, C443 1uF 10V X7S 0402

cap_vddram_core1 → H11 VCAP_VDDRAM_CORE1
cap_vddram_core2 → J17 VCAP_VDDRAM_CORE2
cap_vddram_core3 → U15 VCAP_VDDRAM_CORE3
cap_vddram_core4 → R17 VCAP_VDDRAM_CORE4
cap_vddram_core5 → Y16 VCAP_VDDRAM_CORE5
C475 1uF 10V X7S 0402, C473 1uF 10V X7S 0402, C465 1uF 10V X7S 0402, C478 1uF 10V X7S 0402, C451 1uF 10V X7S 0402

cap_vddram_dspeve1 → G10 VCAP_VDDRAM_DSPEVE1
cap_vddram_dspeve2 → H10 VCAP_VDDRAM_DSPEVE2
cap_vddram_gpu → T16 VCAP_VDDRAM_GPU
C477 1uF 10V X7S 0402, C442 1uF 10V X7S 0402, C437 1uF 10V X7S 0402

cap_vddram_iva → R20 VCAP_VDDRAM_IVA
cap_vddram_mpu1 → J16 VCAP_VDDRAM_MPU1
cap_vddram_mpu2 → J21 VCAP_VDDRAM_MPU2
C510 1uF 10V X7S 0402, C481 1uF 10V X7S 0402, C500 1uF 10V X7S 0402

TEXAS INSTRUMENTS INCORPORATED

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Route the feedback connections as 4-8mil trace widths
for remote sensing voltages only (not current carrying)
and connected as close as possible to SoC power balls
or Dcaps located very close to power ball (point of load).

POWER

DIGITAL SUPPLIES

DRA77xP / DRA76xP / TDA2Px

Data Manual: SPRS993A_July_2017
Package: ACD, 23x23mm, 784 PBGA, 0.8mm Pitch
PCB Footprint: bga784_28x28_0p8mm
SCH Symbol:
IC_J6Plus_ACD_23mm_784BGA_v1.0

J6Plus SYM-D

U42D

VDD_MPU_AVS: C174 10uF 10V X7R 0805; C173 10uF 10V X7R 0805; C503 1uF 4V X7S 0508; C505 1uF 4V X7S 0508; C484 1uF 4V X7S 0508; C485 1uF 4V X7S 0508; C504 1uF 4V X7S 0508; C482 0.47uF 10V X7S 0402; C491 0.47uF 10V X7S 0402; C499 0.47uF 10V X7S 0402; C492 0.47uF 10V X7S 0402; C463 0.1uF 16V X7R 0402; C472 0.1uF 16V X7R 0402

K16 vdd_mpu_1
K18 vdd_mpu_2
K20 vdd_mpu_3
L15 vdd_mpu_4
L17 vdd_mpu_5
L19 vdd_mpu_6
M16 vdd_mpu_7
M18 vdd_mpu_8
M20 vdd_mpu_9

VDD_DSPEVE_AVS: C163 10uF 10V X7R 0805; C162 10uF 10V X7R 0805; C440 1uF 4V X7S 0508; C455 1uF 4V X7S 0508; C428 1uF 4V X7S 0508; C456 1uF 4V X7S 0508; C439 1uF 4V X7S 0508; C446 0.47uF 10V X7S 0402; C452 0.47uF 10V X7S 0402; C438 0.47uF 10V X7S 0402; C433 0.47uF 10V X7S 0402; C464 0.1uF 16V X7R 0402; C444 0.1uF 16V X7R 0402

K10 vdd_dspeve_1
K12 vdd_dspeve_2
L9 vdd_dspeve_3
L11 vdd_dspeve_4
L13 vdd_dspeve_5
M10 vdd_dspeve_6
M12 vdd_dspeve_7
M14 vdd_dspeve_8

VDD_CORE_AVS: C141 10uF 10V X7R 0805; C372 1uF 4V X7S 0508; C373 1uF 4V X7S 0508; C384 1uF 4V X7S 0508; C383 1uF 4V X7S 0508; C498 0.47uF 10V X7S 0402; C435 0.47uF 10V X7S 0402; C447 0.47uF 10V X7S 0402; C459 0.47uF 10V X7S 0402; C462 0.47uF 10V X7S 0402

J9 vdd_1
J15 vdd_2
K14 vdd_3
N11 vdd_4
N15 vdd_5
N17 vdd_6
P10 vdd_7
P12 vdd_8
P14 vdd_9
P21 vdd_10
R9 vdd_11
R11 vdd_12
R13 vdd_13
T10 vdd_14
T12 vdd_15
T14 vdd_16
U9 vdd_17
U11 vdd_18
U17 vdd_19
V16 vdd_20
V20 vdd_21
W19 vdd_22
Y18 vdd_23
Y20 vdd_24

VDD_GPU_AVS: C140 10uF 10V X7R 0805; C382 1uF 4V X7S 0508; C374 1uF 4V X7S 0508; C369 1uF 4V X7S 0508; C396 0.47uF 10V X7S 0402; C448 0.47uF 10V X7S 0402; C466 0.47uF 10V X7S 0402; C441 0.47uF 10V X7S 0402; C400 0.1uF 16V X7R 0402; C434 0.1uF 16V X7R 0402

V10 vdd_gpu_1
V12 vdd_gpu_2
V14 vdd_gpu_3
W9 vdd_gpu_4
W11 vdd_gpu_5
W13 vdd_gpu_6

VDD_IVA_AVS: C172 10uF 10V X7R 0805; C497 1uF 4V X7S 0508; C516 1uF 4V X7S 0508; C489 0.47uF 10V X7S 0402; C495 0.47uF 10V X7S 0402; C511 0.1uF 16V X7R 0402; C502 0.1uF 16V X7R 0402

T18 vdd_iva_1
U19 vdd_iva_2
V18 vdd_iva_3

VDDR_SOC_1V35: C197 10uF 10V X7R 0805; C551 1uF 4V X7S 0508; C536 0.47uF 10V X7S 0402; C512 0.47uF 10V X7S 0402; C506 0.47uF 10V X7S 0402; C535 0.47uF 10V X7S 0402; C501 0.47uF 10V X7S 0402; C509 0.47uF 10V X7S 0402; C538 0.47uF 10V X7S 0402; C513 0.47uF 10V X7S 0402

T22 vdds_ddr1_1
U23 vdds_ddr1_2
V22 vdds_ddr1_3
W21 vdds_ddr1_4
W23 vdds_ddr1_5
Y22 vdds_ddr1_6
AA21 vdds_ddr1_7
AA23 vdds_ddr1_8

VDDR_SOC_1V35: C193 10uF 10V X7R 0805; C189 1uF 4V X7S 0508; C181 0.47uF 10V X7S 0402; C182 0.47uF 10V X7S 0402; C186 0.47uF 10V X7S 0402; C187 0.47uF 10V X7S 0402; C534 0.47uF 10V X7S 0402; C533 0.47uF 10V X7S 0402; C539 0.47uF 10V X7S 0402; C537 0.47uF 10V X7S 0402

J23 vdds_ddr2_1
K22 vdds_ddr2_2
L21 vdds_ddr2_3
L23 vdds_ddr2_4
N21 vdds_ddr2_5
N23 vdds_ddr2_6
P22 vdds_ddr2_7

U21 vdds18v_ddr1_1
AA19 vdds18v_ddr1_2
H22 vdds18v_ddr2_1
R21 vdds18v_ddr2_2

VDDS_1V8: C155 10uF 10V X7R 0805; C411 1uF 4V X7S 0508; C426 0.47uF 10V X7S 0402; C391 0.47uF 10V X7S 0402; C487 0.47uF 10V X7S 0402; C392 0.1uF 16V X7R 0402; C436 0.1uF 16V X7R 0402; C493 0.1uF 16V X7R 0402; C393 0.1uF 16V X7R 0402; C395 0.1uF 16V X7R 0402; C394 0.1uF 16V X7R 0402; C150 0.1uF 16V X7R 0402

H14 vdds18v_1
H20 vdds18v_2
M8 vdds18v_3
T20 vdds18v_4
AB8 vdds18v_5

R7 vdds_mlbp_1
T8 vdds_mlbp_2

VDDSHV_3V3: C425 0.47uF 10V X7S 0402; C421 0.47uF 10V X7S 0402; C149 4.7uF 16V X7R 0805; C145 10uF 10V X7R 0805

vddshv1_1 G7
vddshv1_2 G9
VIN2A

C427 0.1uF 16V X7R 0402; C399 0.1uF 16V X7R 0402

vddshv2_1 G11
vddshv2_2 G13
vddshv2_3 H12
VOUT1

DCAN(MCAN)
GPIO6_14-16
I2C1, I2C2
McASP_1-4
SPI_1-2
SoC Cntls
JTAG, EMU

vddshv3_1 G15
vddshv3_2 G17
vddshv3_3 G19
vddshv3_4 H16
vddshv3_5 H18

C398 0.1uF 16V X7R 0402; C151 0.1uF 16V X7R 0402

vddshv4_1 G21
UART_1-2

C460 0.1uF 16V X7R 0402

Removed VDDSHV5 for J6Plus since RTC is not supported

vddshv5_1 AA14
RTC IO
WAKEUP_0-3

VIN1A
USB_1-2_DRVBUS/GPIO

vddshv6_1 W7
vddshv6_2 Y8
vddshv6_3 AA7

C397 0.1uF 16V X7R 0402; C152 0.1uF 16V X7R 0402

vddshv7_1 V8
GPIO6_10-11
McASP_5
MMC3

VDD_SDIO_DV

vddshv8_1 U7
MMC1(SDIO)

C401 0.1uF 16V X7R 0402

vddshv9_1 N7
vddshv9_2 P8
MDIO
RGMII
UART_3

C422 0.1uF 16V X7R 0402; C476 0.1uF 16V X7R 0402; C432 0.1uF 16V X7R 0402

vddshv10_1 J7
vddshv10_2 K8
vddshv10_3 L7
GPIO/GPMC_A0-18
GPIO/GPMC_AD0-15
GPIO/GPMC_CNTLS

VDDSHV11

vddshv11_1 H8
MMC2/GPMC_A19-27, _CS1

C424 0.1uF 16V X7R 0402

To be connected to VDDS_1V8 if NOR Boot functionality is not required on J6Plus.

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J6Plus SYM-G

U42G

DRA77xP / DRA76xP / TDA2Px

Data Manual: SPRS993A_July_2017
Package: ACD, 23x23mm, 784 PBGA, 0.8mm Pitch
PCB Footprint: bga784_28x28_0p8mm
SCH Symbol: IC_J6Plus_ACD_23mm_784BGA_v1.0

A1	vss_1	vss_79	T19
A2	vss_2	vss_80	T21
A28	vss_3	vss_81	T23
B1	vss_4	vss_82	U8
G8	vss_5	vss_83	U10
G12	vss_6	vss_84	U12
G16	vss_7	vss_85	U14
G18	vss_8	vss_86	U16
G20	vss_9	vss_87	U18
G22	vss_10	vss_88	U20
H7	vss_11	vss_89	U22
H9	vss_12	vss_90	V7
H13	vss_13	vss_91	V9
H15	vss_14	vss_92	V11
H17	vss_15	vss_93	V13
H19	vss_16	vss_94	V15
H21	vss_17	vss_95	V17
H23	vss_18	vss_96	V19
J8	vss_19	vss_97	V21
J10	vss_20	vss_98	V23
J12	vss_21	vss_99	W8
J14	vss_22	vss_100	W10
J18	vss_23	vss_101	W12
J20	vss_24	vss_102	W14
J22	vss_25	vss_103	W16
K7	vss_26	vss_104	W18
K9	vss_27	vss_105	W20
K11	vss_28	vss_106	W22
K13	vss_29	vss_107	Y7
K15	vss_30	vss_108	Y9
K17	vss_31	vss_109	Y11
K19	vss_32	vss_110	Y13
K21	vss_33	vss_111	Y15
K23	vss_34	vss_112	Y17
L8	vss_35	vss_113	Y19
L10	vss_36	vss_114	Y21
L12	vss_37	vss_115	Y23
L14	vss_38	vss_116	AA8
L16	vss_39	vss_117	AA10
L18	vss_40	vss_118	AA12
L20	vss_41	vss_119	AA16
L22	vss_42	vss_120	AA18
M7	vss_43	vss_121	AA20
M9	vss_44	vss_122	AA22
M11	vss_45	vss_123	AB9
M13	vss_46	vss_124	AB11
M15	vss_47	vss_125	AB13
M17	vss_48	vss_126	AB17
M19	vss_49	vss_127	AC12
M21	vss_50	vss_128	AC15
M23	vss_51	vss_129	AD10
N8	vss_52	vss_130	AD13
N10	vss_53	vss_131	AD16
N12	vss_54	vss_132	AD19
N14	vss_55	vss_133	AE11
N16	vss_56	vss_134	AE14
N18	vss_57	vss_135	AE17
N20	vss_58	vss_136	AF9
N22	vss_59	vss_137	AF12
P7	vss_60	vss_138	AF15
P9	vss_61	vss_139	AF18
P11	vss_62	vss_140	AG1
P13	vss_63	vss_141	AG4
P15	vss_64	vss_142	AG7
P17	vss_65	vss_143	AG10
P19	vss_66	vss_144	AG13
R8	vss_67	vss_145	AG16
R10	vss_68	vss_146	AG28
R12	vss_69	vss_147	AH1
R16	vss_70	vss_148	AH2
R18	vss_71	vss_149	AH5
R22	vss_72	vss_150	AH8
T7	vss_73	vss_151	AH11
T9	vss_74	vss_152	AH14
T11	vss_75	vss_153	AH17
T13	vss_76	vss_154	AH27
T15	vss_77	vss_155	AH28
T17	vss_78		

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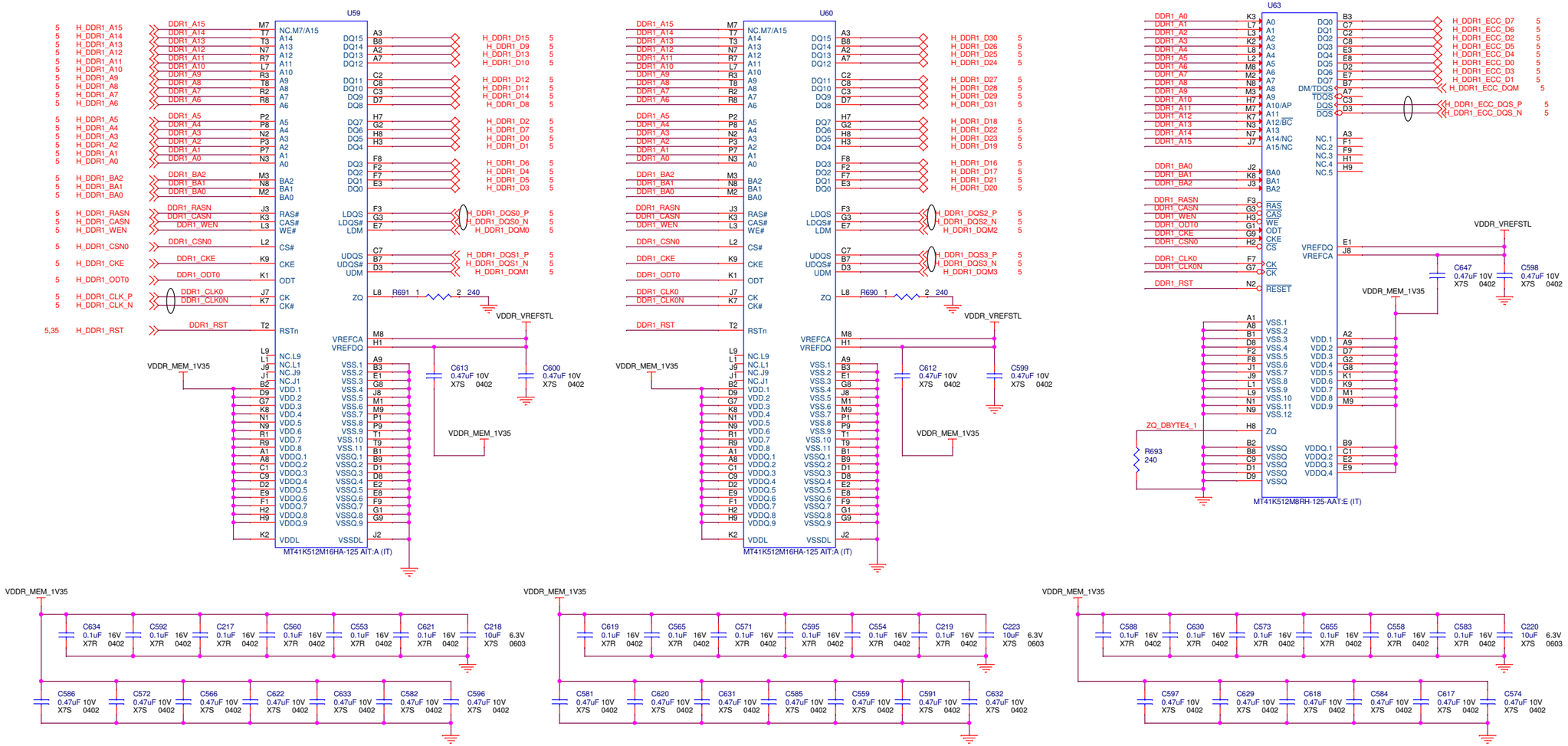

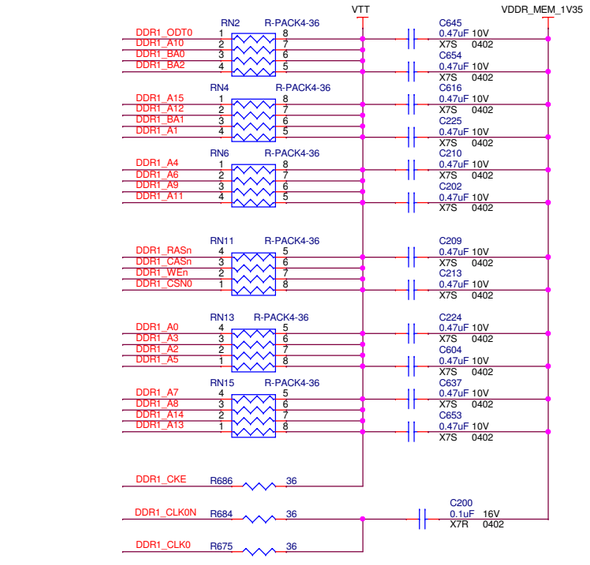

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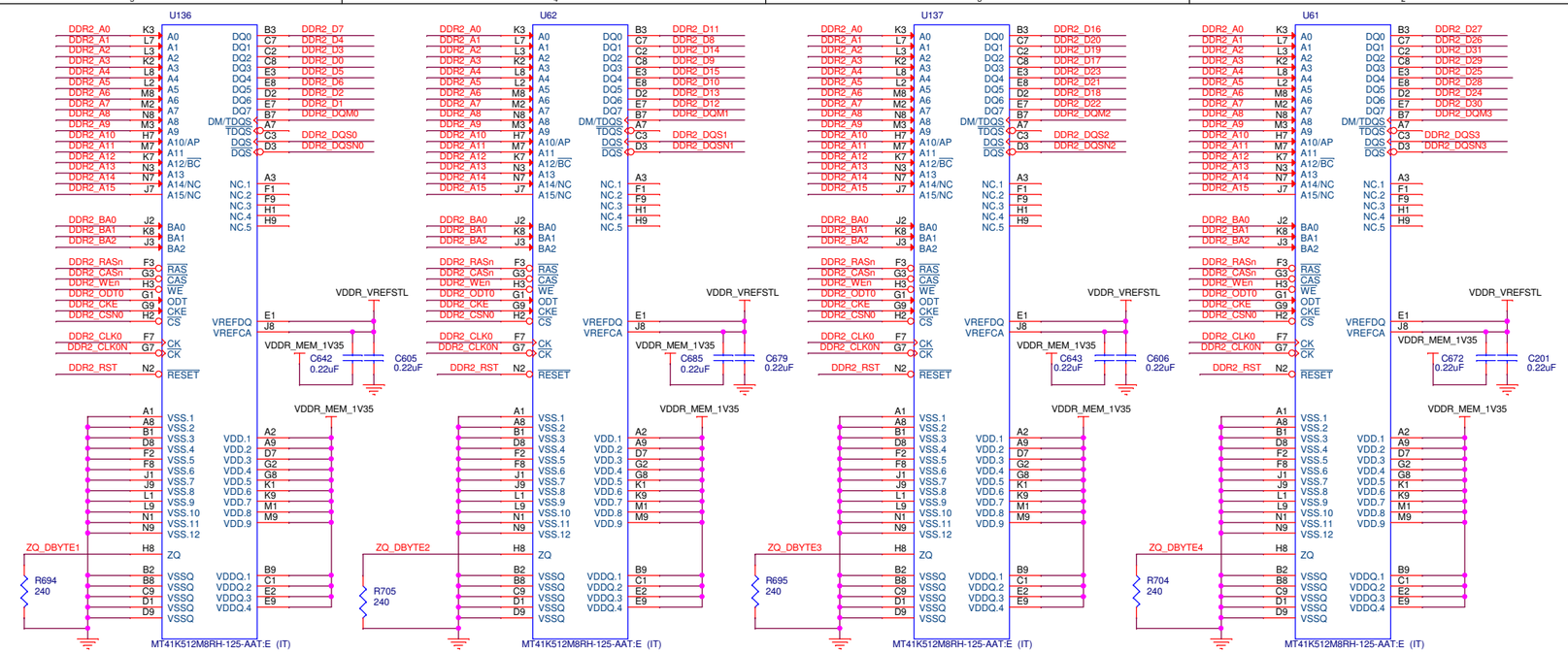
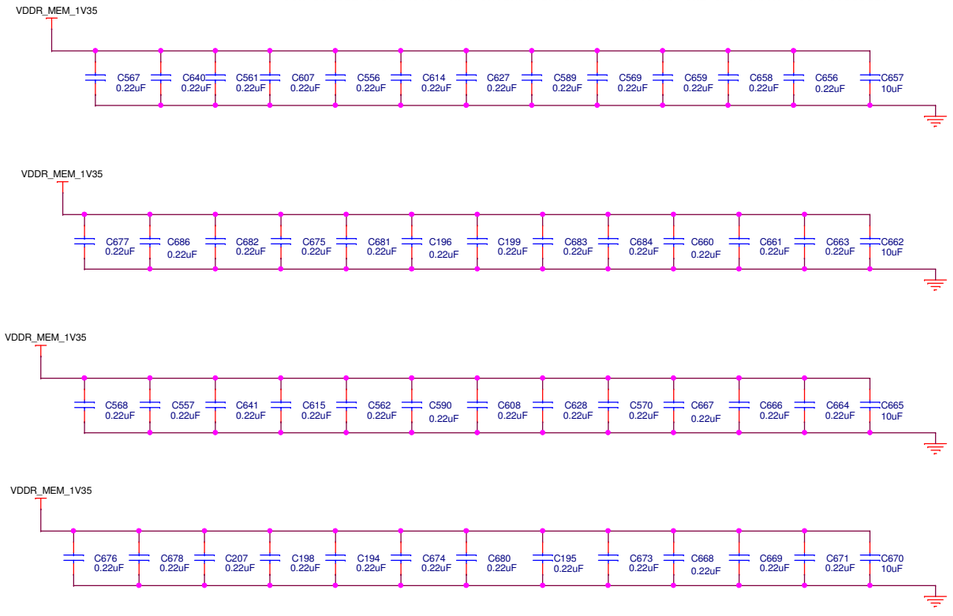
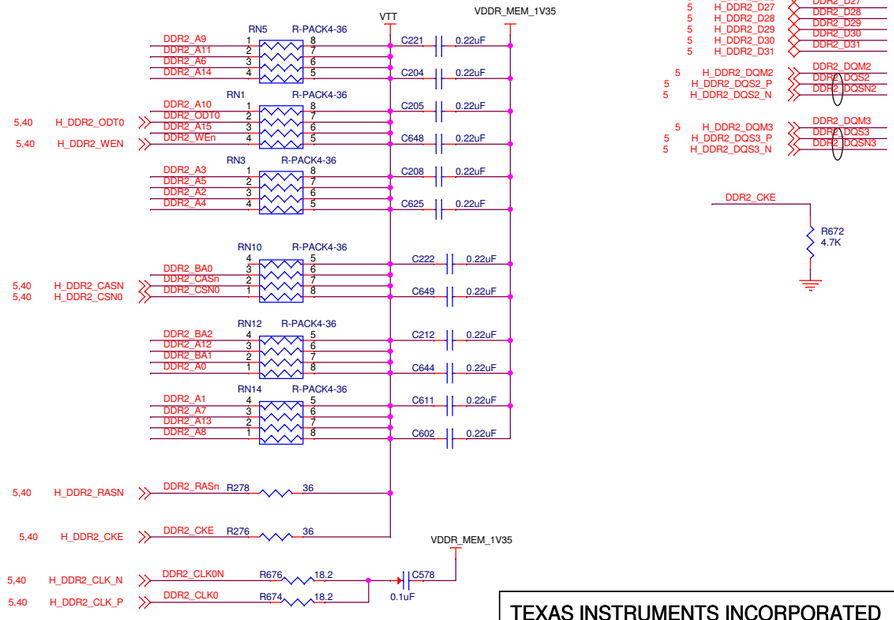


DELTA VAYU H, CHANGE OF CAPS TO 0201 AUTOMOTIVE IS TBD.
WITH DOUBLE SIDE MOUNT AND INTERPOSER SUPPORT 0402 IN THE DDR ARRAY NOT POSSIBLE.





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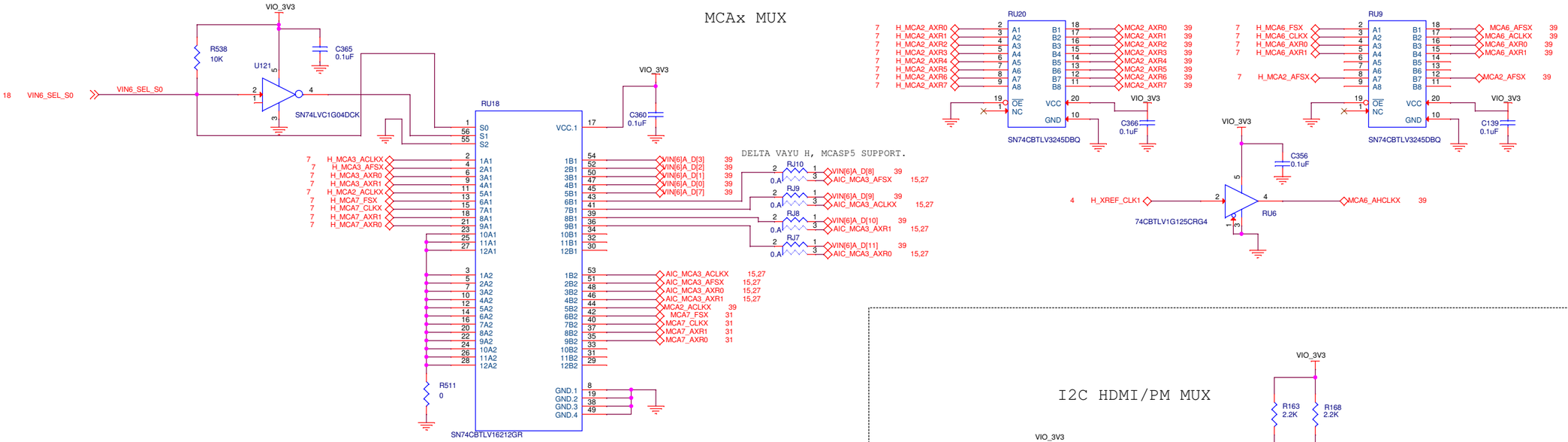
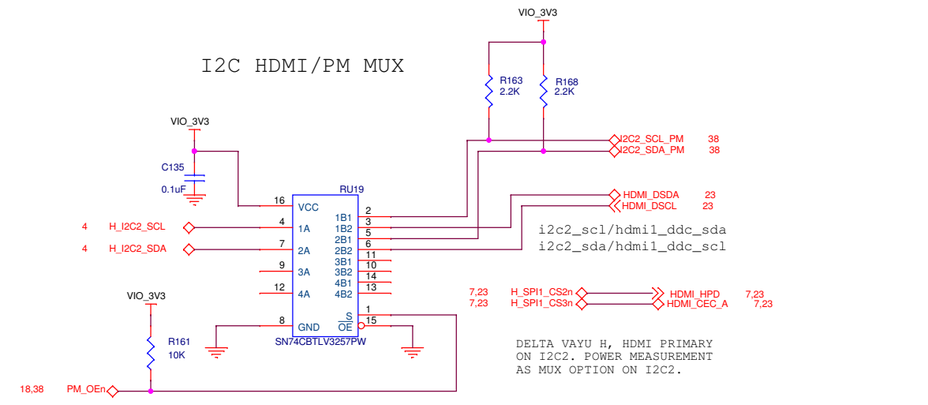
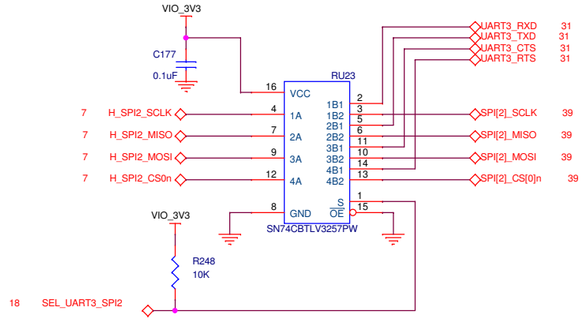
MCAx MUX



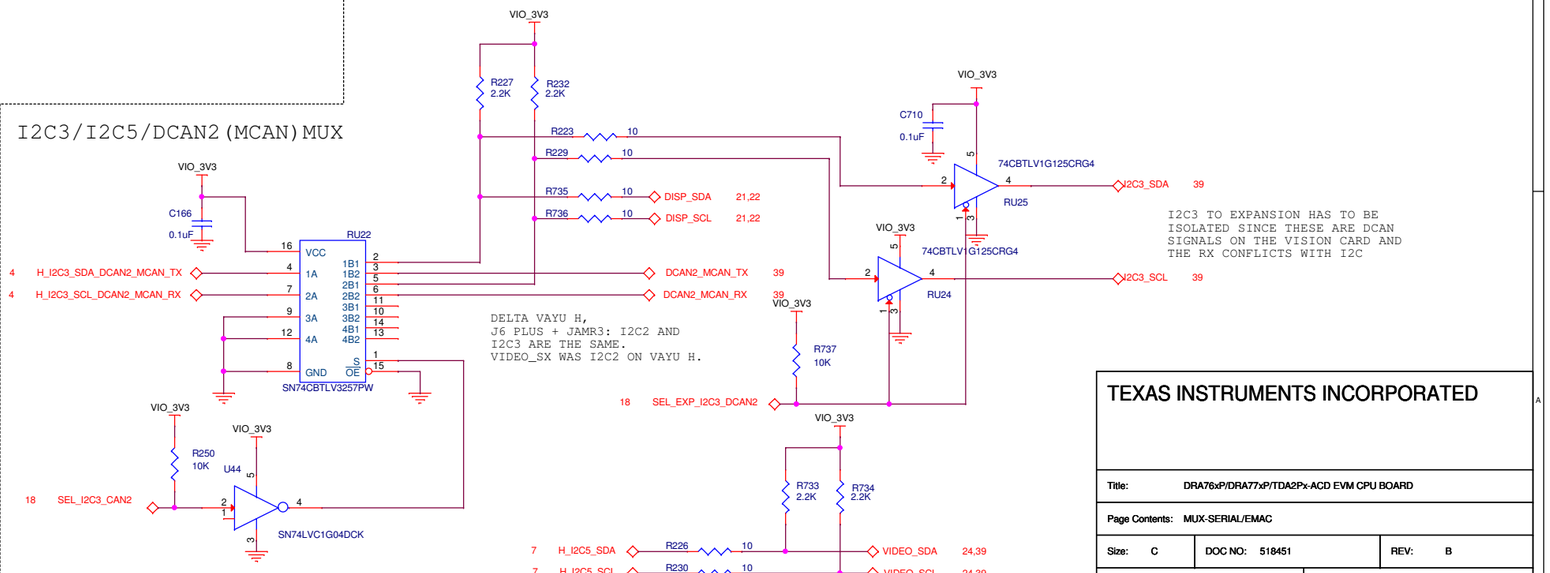
I2C HDMI/PM MUX



UART3/SPI2 MUX



I2C3/I2C5/DCAN2(MCAN)MUX



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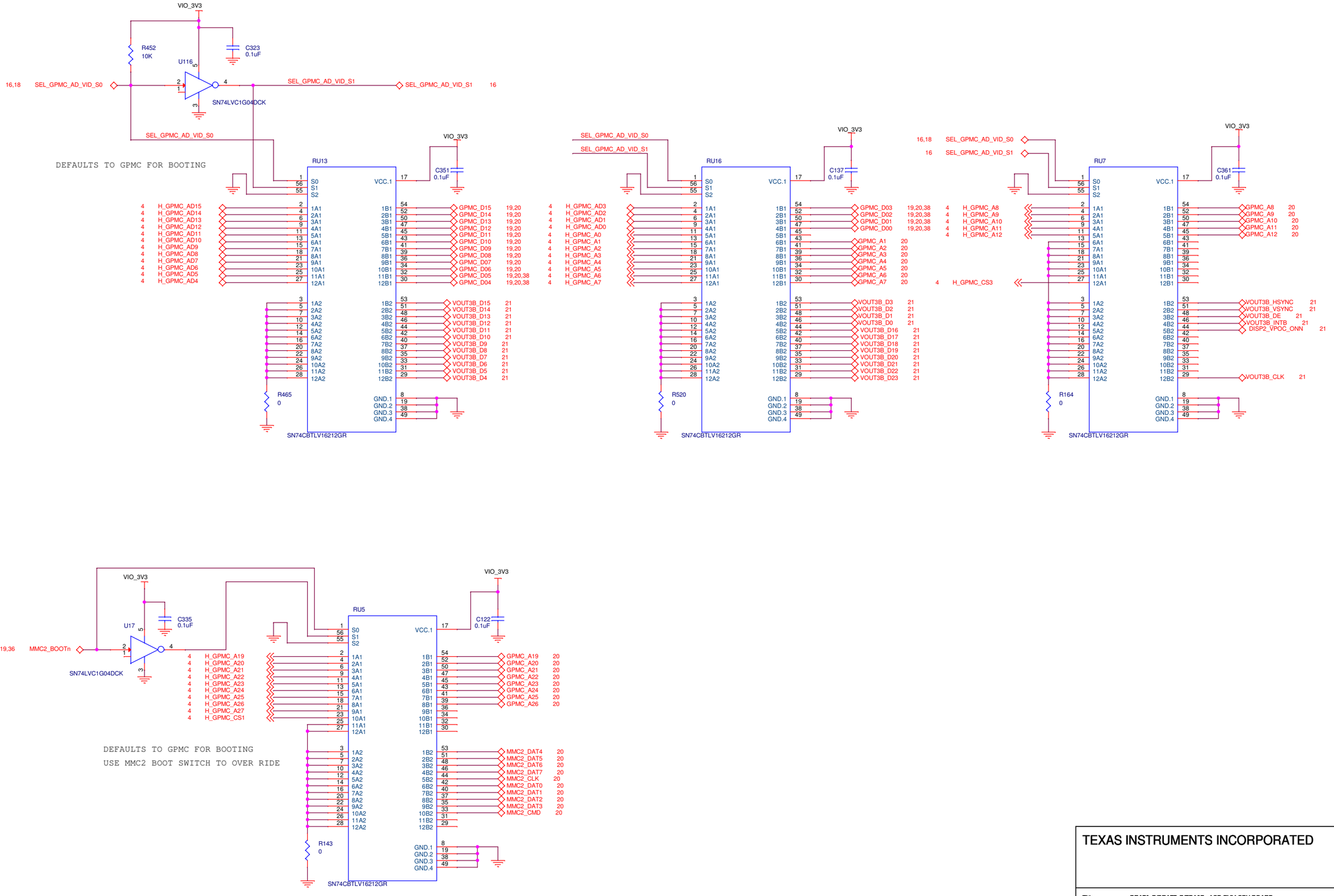

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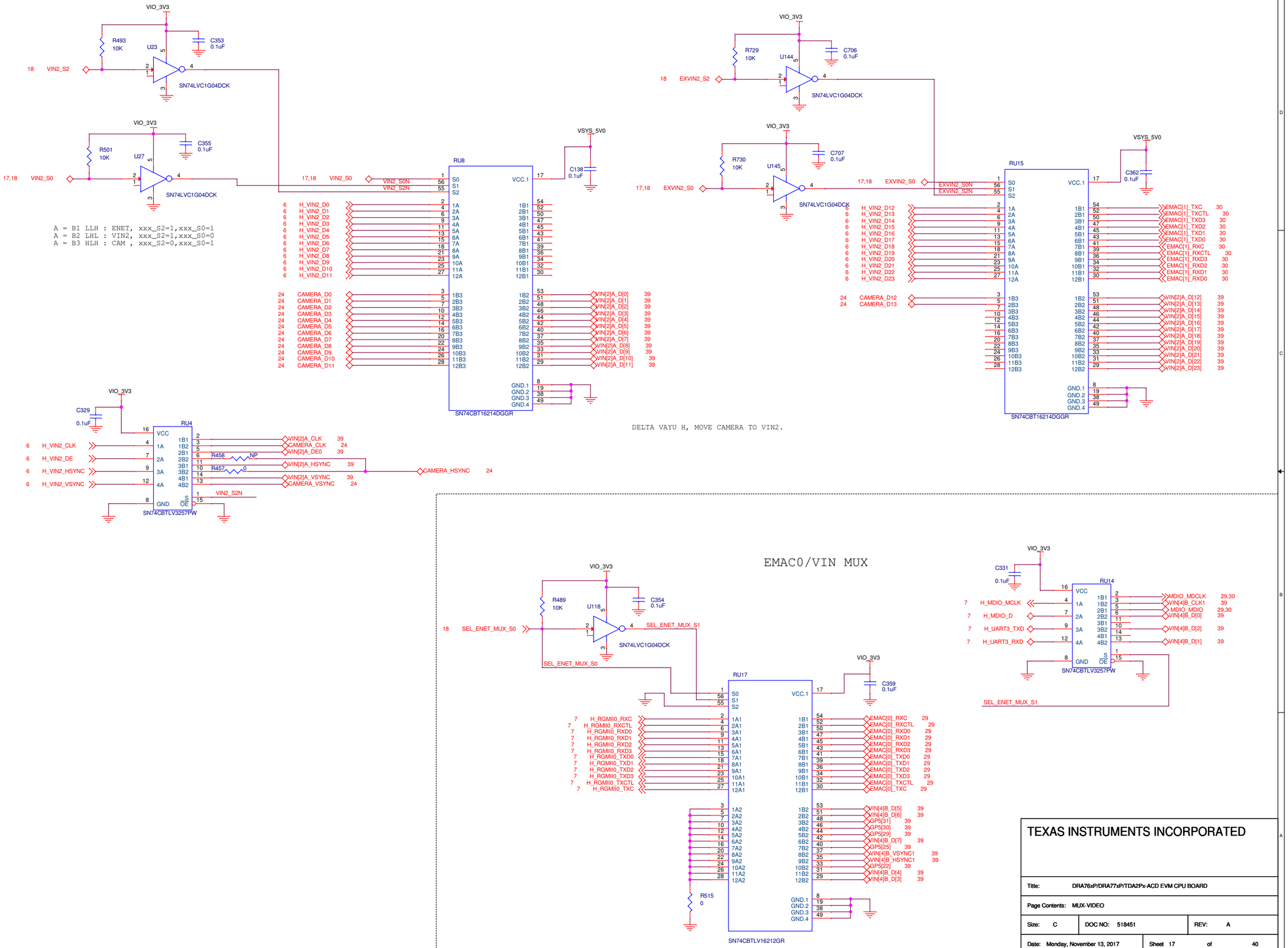
VIO_3V3
R493 10K
C353 0.1uF
U23
18 VIN2_S2
SN74LVC1G04DCK
R501 10K
C355 0.1uF
U27
17,18 VIN2_S0
A = B1 LLH : ENET, xxx_S2=1,xxx_S0=1
A = B2 LHL : VIN2, xxx_S2=1,xxx_S0=0
A = B3 HLH : CAM , xxx_S2=0,xxx_S0=1
RU8
VSYS_5V0
C138 0.1uF
VCC.1
S0
S1
S2
6 H_VIN2_D0
6 H_VIN2_D1
6 H_VIN2_D2
6 H_VIN2_D3
6 H_VIN2_D4
6 H_VIN2_D5
6 H_VIN2_D6
6 H_VIN2_D7
6 H_VIN2_D8
6 H_VIN2_D9
6 H_VIN2_D10
6 H_VIN2_D11
24 CAMERA_D0
24 CAMERA_D1
24 CAMERA_D2
24 CAMERA_D3
24 CAMERA_D4
24 CAMERA_D5
24 CAMERA_D6
24 CAMERA_D7
24 CAMERA_D8
24 CAMERA_D9
24 CAMERA_D10
24 CAMERA_D11
VIN[2]A_D[0] 39
VIN[2]A_D[1] 39
VIN[2]A_D[2] 39
VIN[2]A_D[3] 39
VIN[2]A_D[4] 39
VIN[2]A_D[5] 39
VIN[2]A_D[6] 39
VIN[2]A_D[7] 39
VIN[2]A_D[8] 39
VIN[2]A_D[9] 39
VIN[2]A_D[10] 39
VIN[2]A_D[11] 39
GND.1
GND.2
GND.3
GND.4
SN74CBT16214DGGR
R729 10K
C706 0.1uF
U144
18 EXVIN2_S2
R730 10K
C707 0.1uF
U145
17,18 EXVIN2_S0
RU15
C362 0.1uF
EXVIN2_S0N
EXVIN2_S2N
6 H_VIN2_D12
6 H_VIN2_D13
6 H_VIN2_D14
6 H_VIN2_D15
6 H_VIN2_D16
6 H_VIN2_D17
6 H_VIN2_D18
6 H_VIN2_D19
6 H_VIN2_D20
6 H_VIN2_D21
6 H_VIN2_D22
6 H_VIN2_D23
24 CAMERA_D12
24 CAMERA_D13
EMAC[1]_TXC 30
EMAC[1]_TXCTL 30
EMAC[1]_TXD3 30
EMAC[1]_TXD2 30
EMAC[1]_TXD1 30
EMAC[1]_TXD0 30
EMAC[1]_RXC 30
EMAC[1]_RXCTL 30
EMAC[1]_RXD3 30
EMAC[1]_RXD2 30
EMAC[1]_RXD1 30
EMAC[1]_RXD0 30
VIN[2]A_D[12] 39
VIN[2]A_D[13] 39
VIN[2]A_D[14] 39
VIN[2]A_D[15] 39
VIN[2]A_D[16] 39
VIN[2]A_D[17] 39
VIN[2]A_D[18] 39
VIN[2]A_D[19] 39
VIN[2]A_D[20] 39
VIN[2]A_D[21] 39
VIN[2]A_D[22] 39
VIN[2]A_D[23] 39
C329 0.1uF
RU4
6 H_VIN2_CLK
6 H_VIN2_DE
6 H_VIN2_HSYNC
6 H_VIN2_VSYNC
VIN[2]A_CLK 39
CAMERA_CLK 24
VIN[2]A_DE0 39
R458 NP
R457 0
VIN[2]A_HSYNC 39
VIN[2]A_VSYNC 39
CAMERA_VSYNC 24
CAMERA_HSYNC 24
VIN2_S2N
SN74CBTLV3257PW
DELTA VAYU H, MOVE CAMERA TO VIN2.
EMAC0/VIN MUX
R489 10K
C354 0.1uF
U118
18 SEL_ENET_MUX_S0
SEL_ENET_MUX_S1
RU17
C359 0.1uF
7 H_RGMII0_RXC
7 H_RGMII0_RXCTL
7 H_RGMII0_RXD0
7 H_RGMII0_RXD1
7 H_RGMII0_RXD2
7 H_RGMII0_RXD3
7 H_RGMII0_TXD0
7 H_RGMII0_TXD1
7 H_RGMII0_TXD2
7 H_RGMII0_TXD3
7 H_RGMII0_TXCTL
7 H_RGMII0_TXC
EMAC[0]_RXC 29
EMAC[0]_RXCTL 29
EMAC[0]_RXD0 29
EMAC[0]_RXD1 29
EMAC[0]_RXD2 29
EMAC[0]_RXD3 29
EMAC[0]_TXD0 29
EMAC[0]_TXD1 29
EMAC[0]_TXD2 29
EMAC[0]_TXD3 29
EMAC[0]_TXCTL 29
EMAC[0]_TXC 29
VIN[4]B_D[5] 39
VIN[4]B_D[6] 39
GP5[31] 39
GP5[30] 39
GP5[29] 39
VIN[4]B_D[7] 39
GP5[25] 39
VIN[4]B_VSYNC1 39
VIN[4]B_HSYNC1 39
GP5[22] 39
VIN[4]B_D[4] 39
VIN[4]B_D[3] 39
R515 0
SN74CBTLV16212GR
C331 0.1uF
RU14
7 H_MDIO_MCLK
7 H_MDIO_D
7 H_UART3_TXD
7 H_UART3_RXD
MDIO_MDCLK 29,30
VIN[4]B_CLK1 39
MDIO_MDIO 29,30
VIN[4]B_D[0] 39
VIN[4]B_D[2] 39
VIN[4]B_D[1] 39
SEL_ENET_MUX_S1
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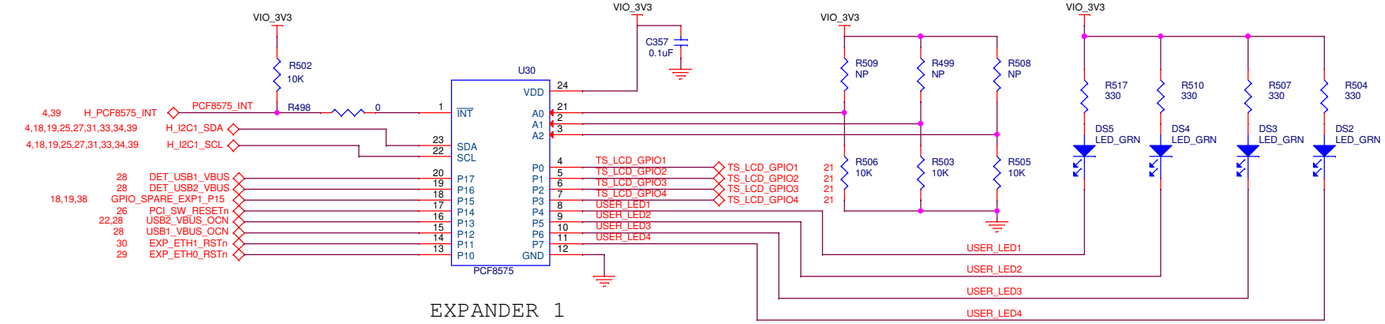
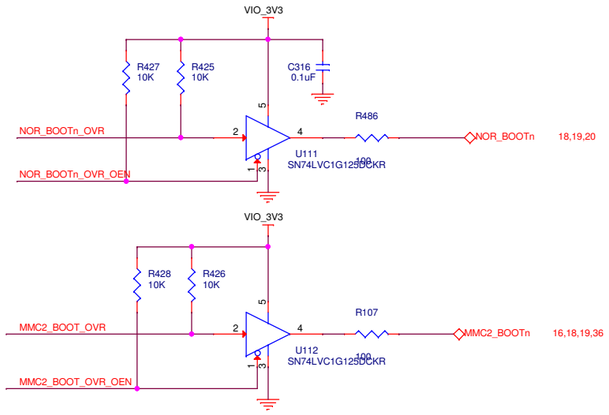
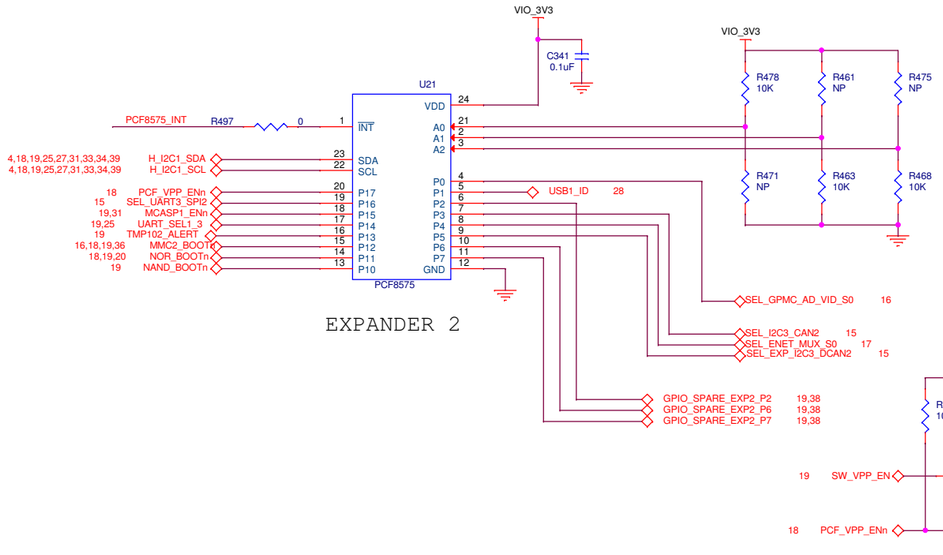
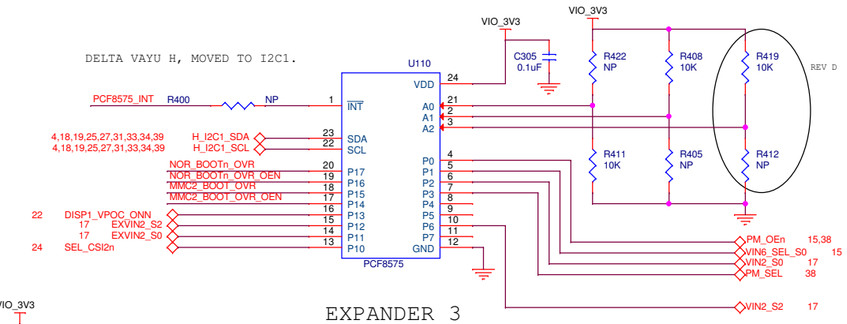
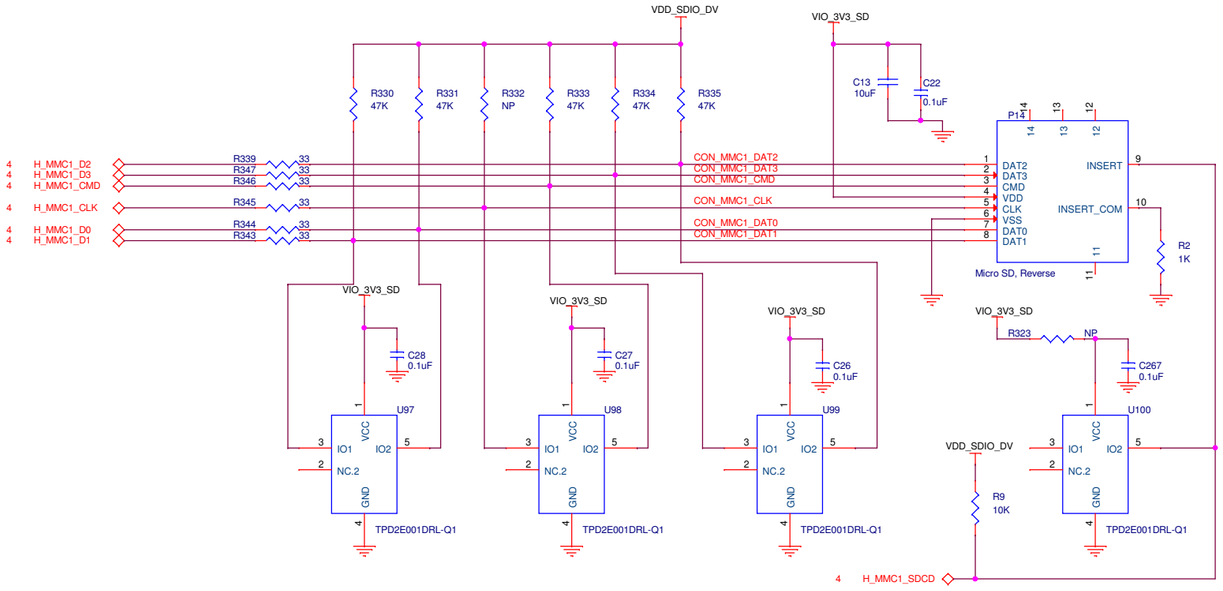


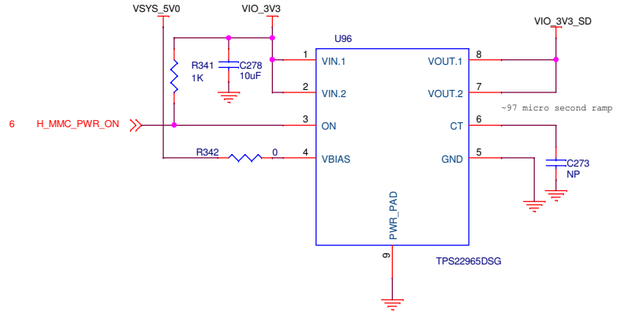






SD CARD





TEXAS INSTRUMENTS INCORPORATED			
Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents:	IOEXPANDER/SDCARD		
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QSPI

DELTA VAYU H, QSPI ACTIVE MUX PATH REMOVED.

4 AQSPI1_RTCLK
4 AQSPI1_SCLK
R145 10
R146 10
R_QSPI1_SCLK

VIO_3V3
R152 10K

4 AQSPI1_D[3]
R151 0
R_QSPI1_D[3]

VIO_3V3
C123 0.1uF

4,20,24,25,26,27,33,34,38 H_RSTOUTn

VIO_3V3
R136 10K

4 AQSPI1_CS[0]
R135 0
R_QSPI1_CS[0]

4 AQSPI1_D[1]
R133 0
R_QSPI1_D[1]

U20

1	HOLD/IO3	SCLK	16
2	VCC	SI/IO0	15
3	RESET/RFU	VIO/RFU	14
4	DNU.4	NC.13	13
5	DNU.5	DNU.12	12
6	RFU.6	DNU.11	11
7	CS	VSS	10
8	SO/IO1	WP/IO2	9

S25FL256SAGMFV001

R_QSPI1_D[0] 0 R144 AQSPI1_D[0] 4

VIO_3V3
C120 0.1uF

R_QSPI1_D[2] R131 0 AQSPI1_D[2] 4

VIO_3V3
R130 10K

ROUTE THE FOLLOWING SIGNALS AS A GROUP WITH A NET LENGTH LESS THEN 2.75 INCHES AND 60ps OF SKEW. PLACE THE DUAL RESISTOR CLOSE TOGETHER NEAR THE PIN OF THE FLASH.

AQSPI1_SCLK
AQSPI1_RTCLK
AQSPI1_CS[0]
AQSPI1_D[0]
AQSPI1_D[1]
AQSPI1_D[2]
AQSPI1_D[3]

CONFIG EEPROM

VIO_3V3
C646 0.1uF

U139

8	VCC	A0	1
7	WP	A1	2
6	SCL	NC	3
5	SDA	VSS	4

24WC256

19 I2C_EEPROM_WP
4,18,19,25,27,31,33,34,39 H_I2C1_SCL
4,18,19,25,27,31,33,34,39 H_I2C1_SDA

R678 NP
R680 NP
R682 NP
R679 NP
R681 0
R683 0

TEMP SENSOR

VIO_3V3
C531 0.1uF

U53

5	V+	ALERT	3
1	SCL		
6	SDA	ADD0	4
2	GND		

TMP102AIDRLT

TMP102_ALERT 18

4,18,19,25,27,31,33,34,39 H_I2C1_SCL
4,18,19,25,27,31,33,34,39 H_I2C1_SDA

VIO_3V3
R641 NP
R630 0

BOOT SWITCHES

SW3

16,19,20,38	GPMC_D00	1	16	1K R70
16,19,20,38	GPMC_D01	2	15	1K R71
16,19,20,38	GPMC_D02	3	14	1K R72
16,19,20,38	GPMC_D03	4	13	1K R73
16,19,20,38	GPMC_D04	5	12	1K R74
16,19,20,38	GPMC_D05	6	11	1K R75
16,19,20	GPMC_D06	7	10	1K R76
16,19,20	GPMC_D07	8	9	1K R77

TDA08H0SB1R

VIO_3V3
R120 10K
R119 10K
R118 10K
R117 10K
R116 10K
R115 10K
R114 10K
R113 10K

SW4

16,19,20	GPMC_D08	1	16	1K R78
16,19,20	GPMC_D09	2	15	1K R79
16,19,20	GPMC_D10	3	14	1K R80
16,19,20	GPMC_D11	4	13	1K R81
16,19,20	GPMC_D12	5	12	1K R82
16,19,20	GPMC_D13	6	11	1K R83
16,19,20	GPMC_D14	7	10	1K R84
16,19,20	GPMC_D15	8	9	1K R85

TDA08H0SB1R

VIO_3V3
R128 10K
R127 10K
R126 10K
R125 10K
R124 10K
R123 10K
R122 10K
R121 10K

USER CONFIG SWITCH

VIO_3V3
R702 10K
R134 10K
R137 10K
R135 10K
R474 10K
R482 10K
R460 10K
R147 10K
R153 10K

SW6

18,19	NAND_BOOTn	20	1	1K R495
18,20	NOR_BOOTn	19	2	1K R490
16,18,36	MMC2_BOOTn	18	3	1K R485
24	SEL_VCC_CSI2_IO	17	4	1K R481
18,25	UART_SEL1_3	16	5	1K R477
18,31	MCASP1_ENn	15	6	1K R469
18	SW_VPP_EN	14	7	1K R464
26	PCI_RESET_SEL	13	8	1K R462
19	GPMC_WPN	12	9	1K R459
19	I2C_EEPROM_WP	11	10	1K R455

DIP_SWITCH-10

VIO_3V3
R745 10K
R746 10K
R747 10K
R748 10K

SW10

18,38	GPIO_SPARE_EXP2_P2	8	1	1K R752
18,38	GPIO_SPARE_EXP2_P6	7	2	1K R751
18,38	GPIO_SPARE_EXP2_P7	6	3	1K R750
18,38	GPIO_SPARE_EXP1_P15	5	4	1K R749

TDA04H0SB1R

CONTROL VIA SWITCH, EXPANDER, AND AUTOMATION HEADER.

NAND FLASH

VIO_3V3
C66 0.01uF
C69 0.01uF
C67 0.01uF

VIO_3V3
R52 10K
R35 10K
R188 NP
R34 0
C49 0.1uF

4,20 H_GPMC_CS0
4 H_GPMC_WAIT0
4,20 H_GPMC_OEn_REn

RU3
74CBTLV1G125RG4

18,19 NAND_BOOTn

U12

	NC-1	GND4	48	GPMC_D15	GPMC_D15 16,19,20
	NC-2	I/O15	47	GPMC_D14	GPMC_D14 16,19,20
	NC-3	I/O14	46	GPMC_D13	GPMC_D13 16,19,20
	NC-4	I/O13	45	GPMC_D07	GPMC_D07 16,19,20
	NC-5	I/O7	44	GPMC_D08	GPMC_D08 16,19,20
	NC-6	I/O6	43	GPMC_D05	GPMC_D05 16,19,20,38
	R/B	I/O5	42	GPMC_D04	GPMC_D04 16,19,20,38
	RE	I/O4	41	GPMC_D12	GPMC_D12 16,19,20
	CE	I/O12	40		
	NC-7	VCC4	39		
	NC-8	23-NC	38		
	VCC	VCC3	37		
	GND1	GND3	36		
	NC-9	22-NC	35		
	NC-10	VCC2	34		
4 H_GPMC_BEN0	CLE	I/O11	33	GPMC_D11	GPMC_D11 16,19,20
4 H_GPMC_ADVn_ALE	ALE	I/O3	32	GPMC_D03	GPMC_D03 16,19,20,38
4,20 H_GPMC_WEn	WE	I/O2	31	GPMC_D02	GPMC_D02 16,19,20,38
19 GPMC_WPN	WP	I/O1	30	GPMC_D01	GPMC_D01 16,19,20,38
	NC-11	I/O0	29	GPMC_D00	GPMC_D00 16,19,20,38
	NC-12	I/O10	28	GPMC_D10	GPMC_D10 16,19,20
	NC-13	I/O9	27	GPMC_D09	GPMC_D09 16,19,20
	NC-14	I/O8	26	GPMC_D08	GPMC_D08 16,19,20
	NC-15	GND2	25		

MT29F4G16ABADAWP:D

TEXAS INSTRUMENTS INCORPORATED

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Page Contents:	QSPI/NAND/BOOT/EEPR/TMP		
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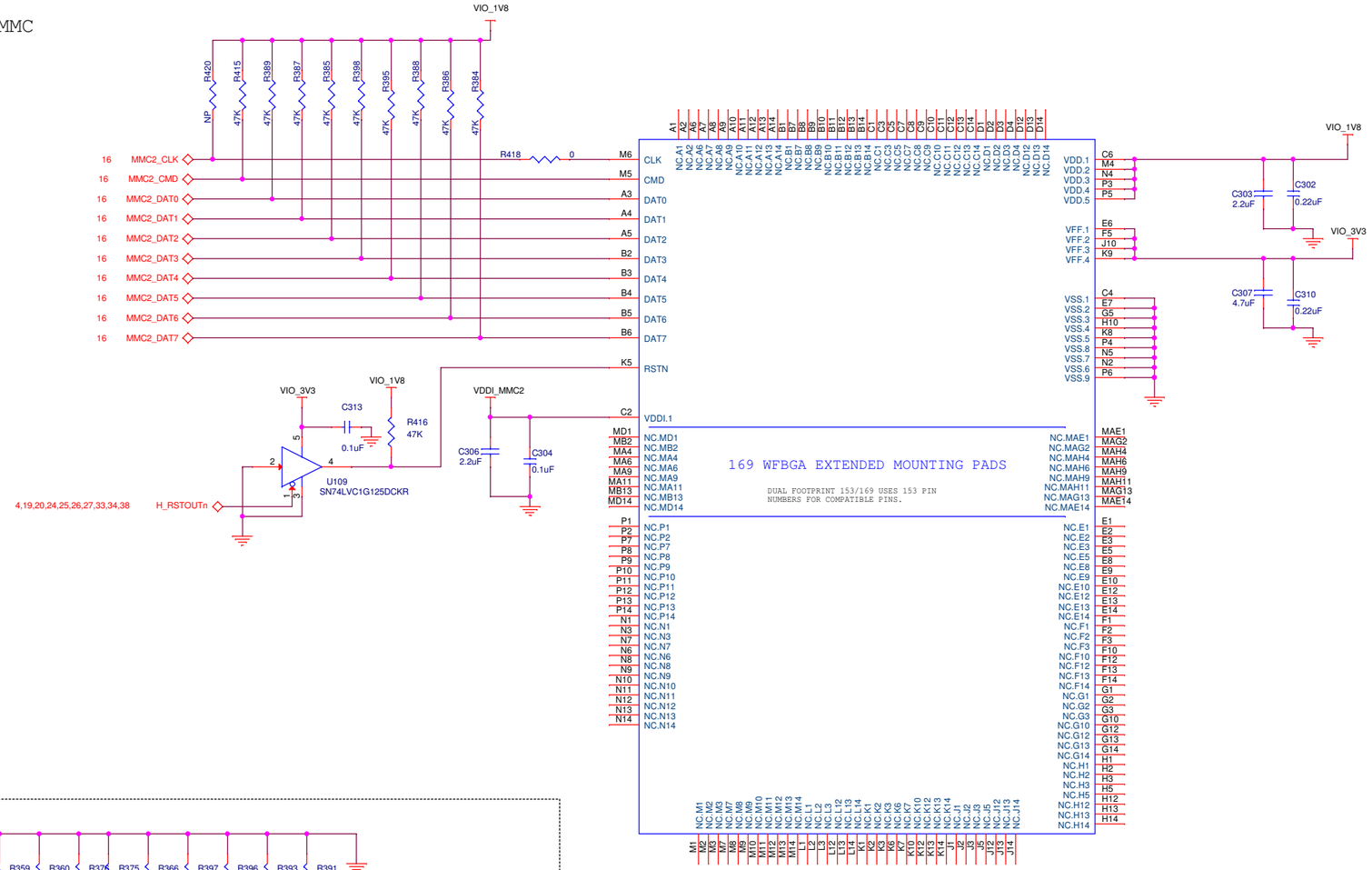
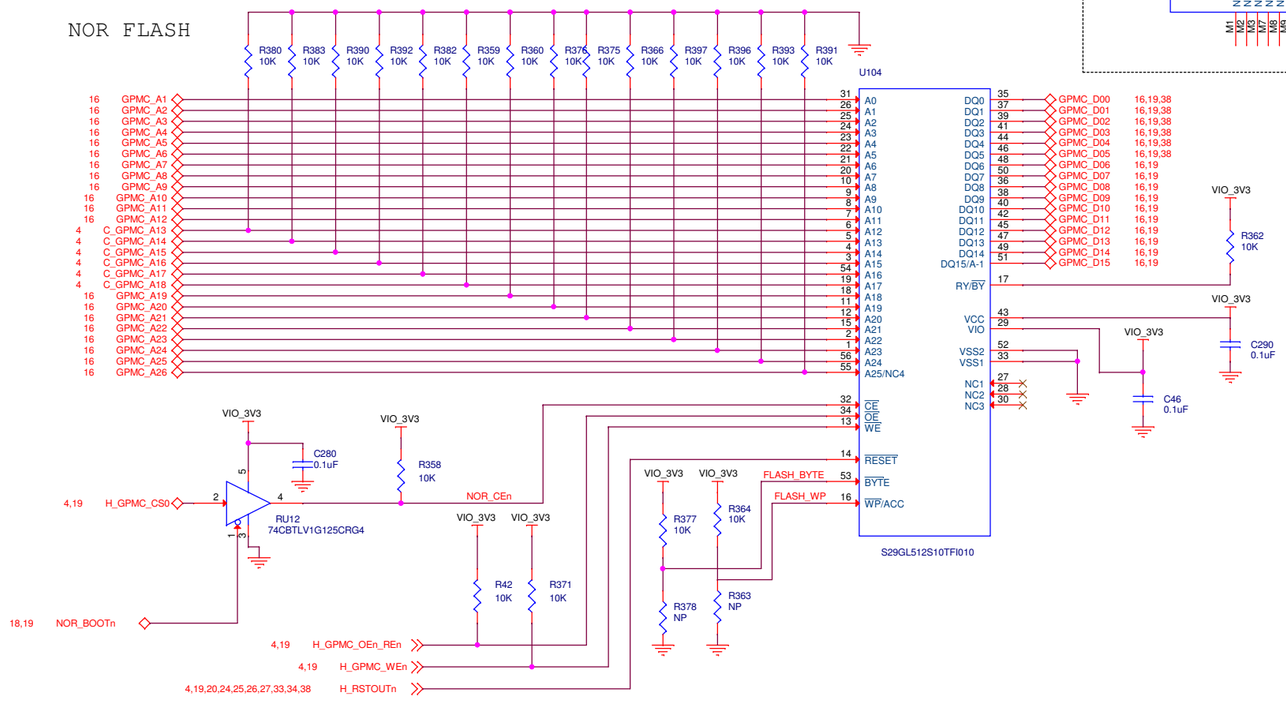
eMMC



DELTA VAYU H, QSPI ACTIVE MUX PATH REMOVED.

NOR FLASH



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FPD-LINK DISPLAY/TOUCH

	ECU HOST	ECU SLAVE(DISPLAY)
1	TPA+	DISPLAY GROUND
2	DISPLAY POWER	TPA-
3	TPA-	DISPLAY POWER
4	DISPLAY GROUND	TPA+

U8 — DS90UB921-Q1

I2C ADDR 0x0C(0x18)

DIFF-PAIR-100-OHM

D4S20G-400A5-C BLUE

DISPLAY POWER

Rcl = (Vcl,th * Kcl)/Iout

Rcl = (1.233*2000)/1.3

LCD/TOUCH INTERFACE

QSH-030-01 — J19

FPD-LINK CLOCK CLEANER

U11 — CDCE813QPWRQ1

I2C ADDR 0x65(0xCA)

RJ4 CLOCK CLEANER BYPASS OPTION

TEXAS INSTRUMENTS INCORPORATED	
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Page Contents:	FPD-LINK/LCD
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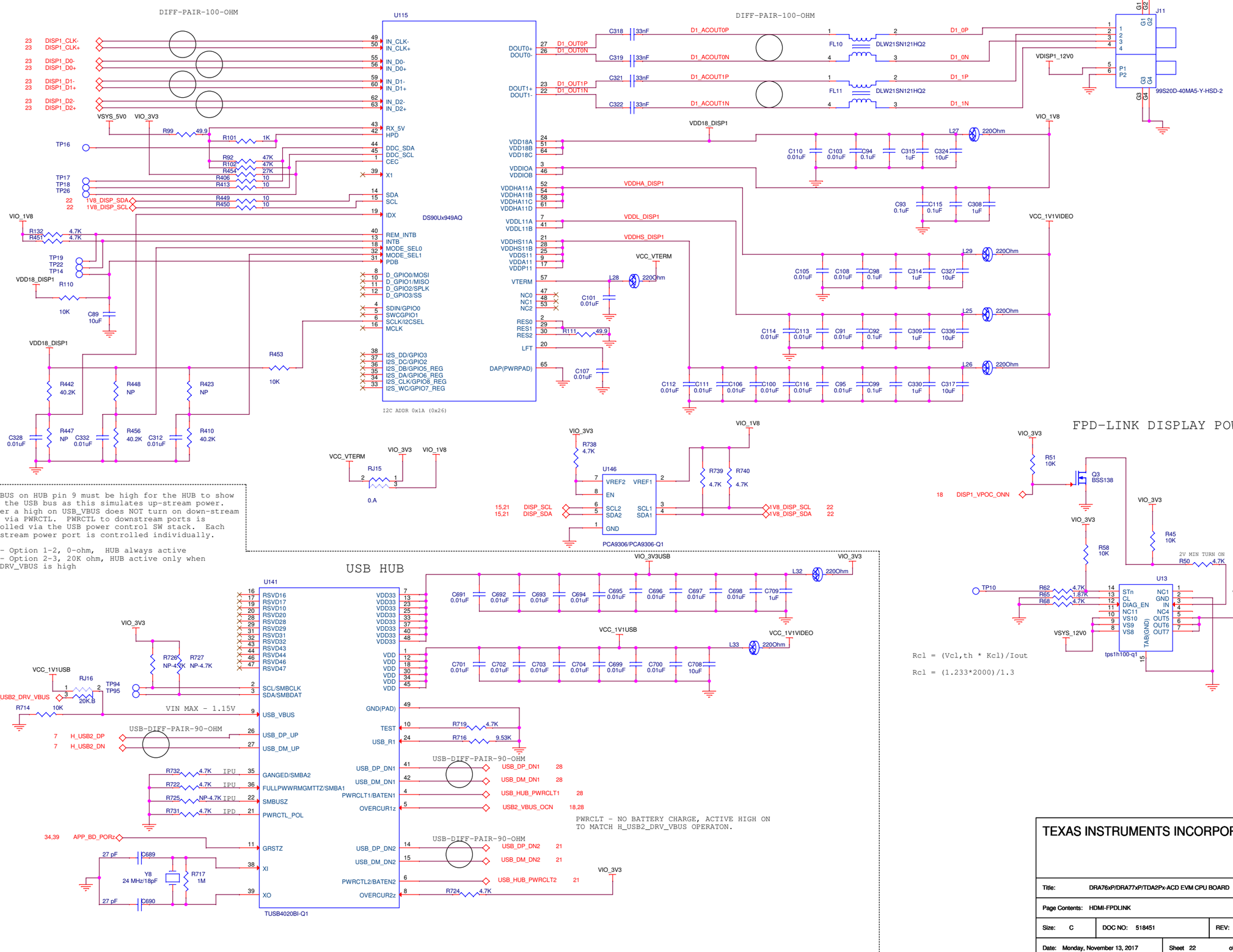
HDMI TO FPD-LINK DISPLAY



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD			
Page Contents: HDMI-FPDLINK			
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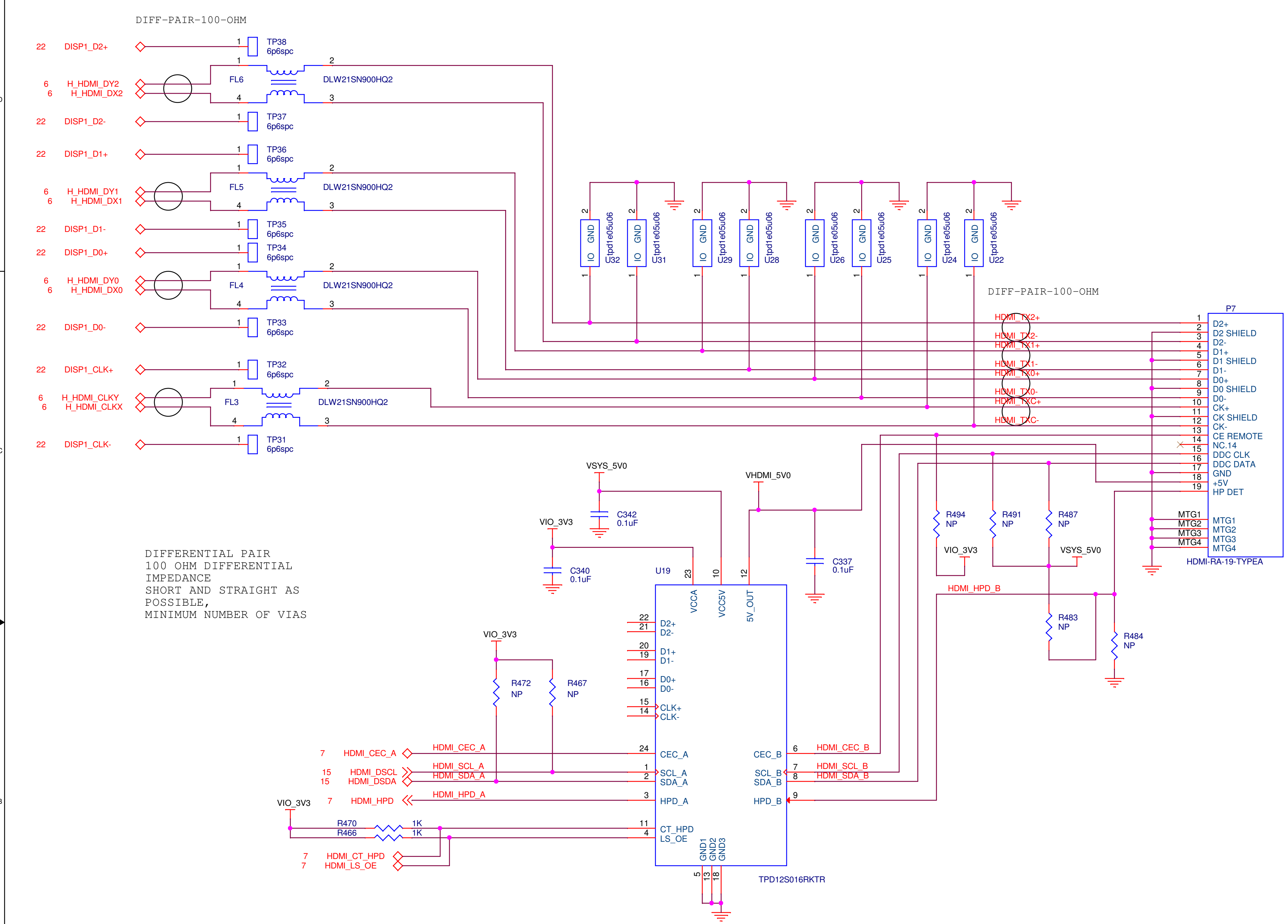

TEXAS INSTRUMENTS INCORPORATED

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Page Contents:	HDMI		
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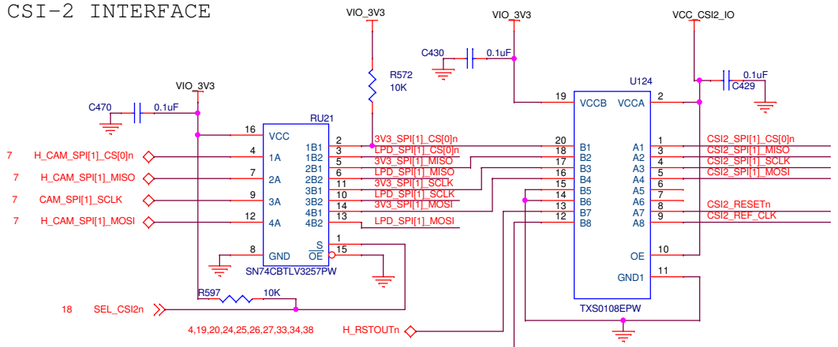
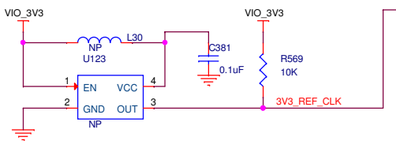
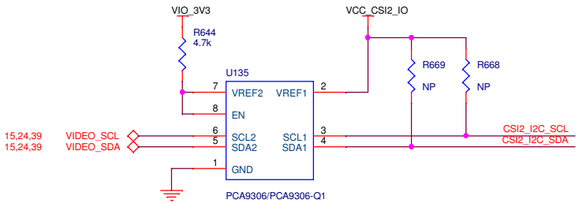
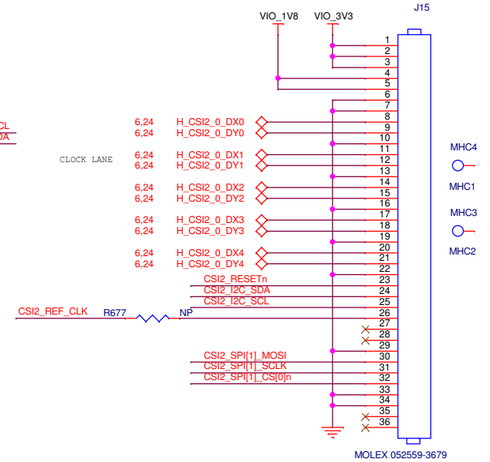
CSI-2 INTERFACE

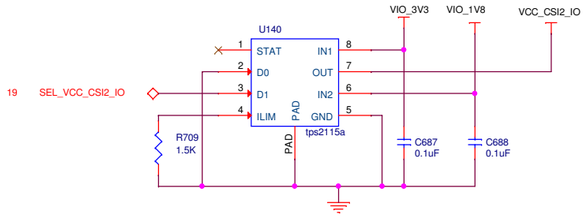


(SINGLE NET NODE)







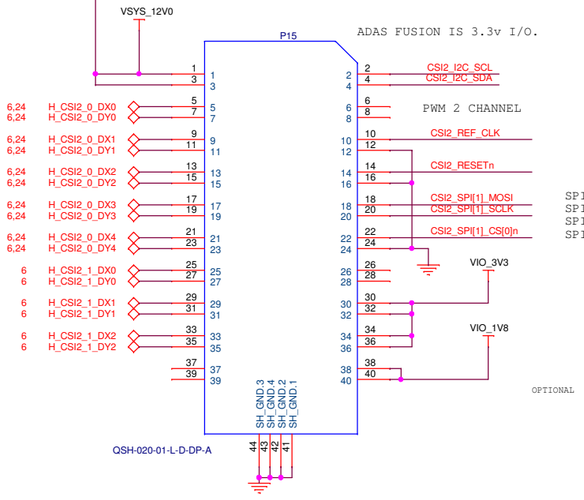


D1=1, IN1 VIO_3V3
D1=0, IN2 VIO_1V8

SWITCHES DEFAULT AS PULLUPS. SWITCH CLOSED TO PULL DOWN.

THE SWITCH SHOULD ONLY BE CHANGED WHILE EVM IS POWERED DOWN.

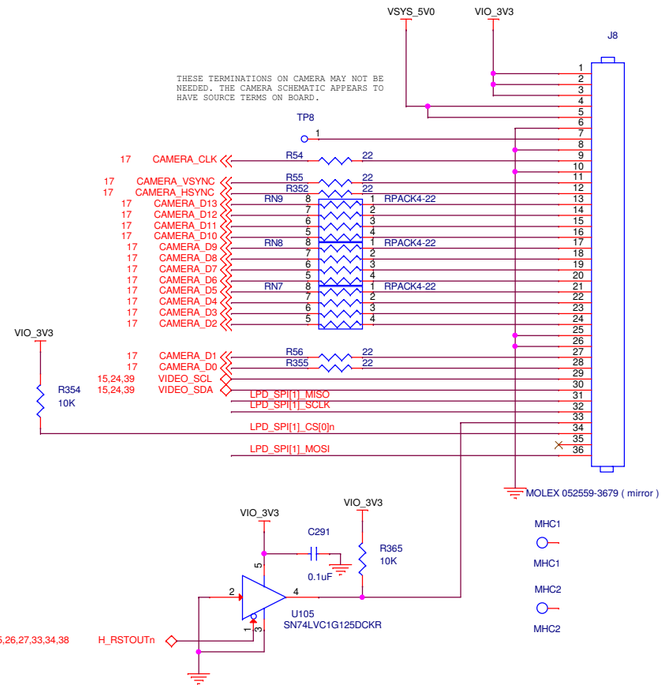
Phoenix Contact
12Amp



OPTIONAL

SPI1_CS0n - GPIO7_10
SPI1_SCLK - GPIO7_7 (OUTPUT ONLY)
SPI1_MOSI - GPIO7_9
SPI1_MISO - GPIO7_8

LEOPARD IMAGING INTERFACE



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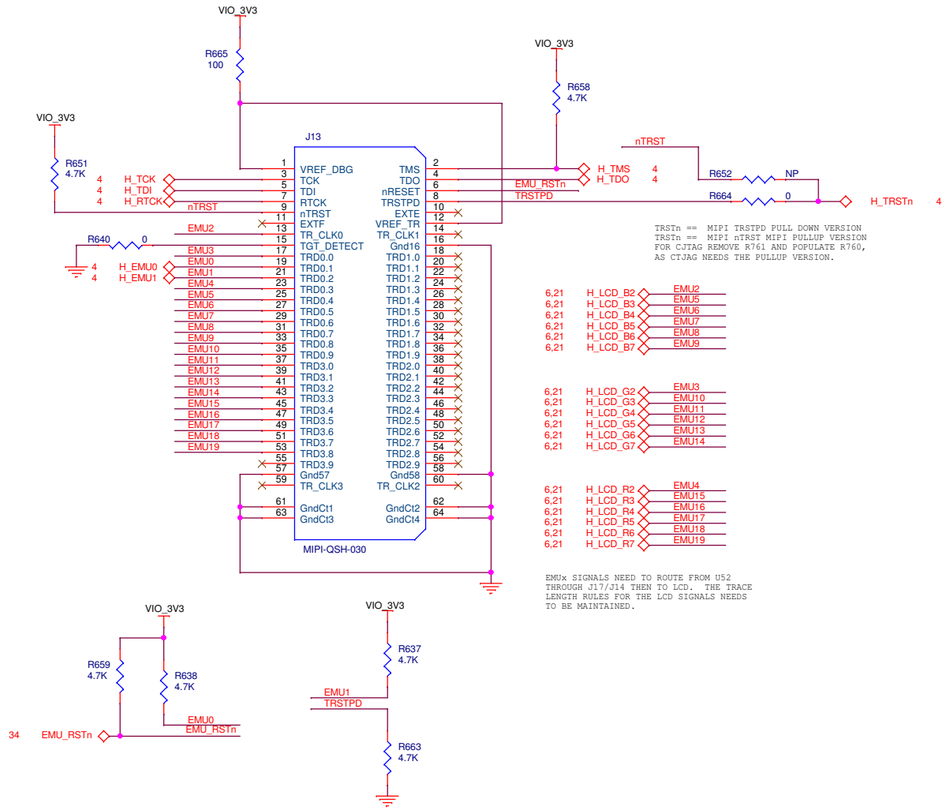
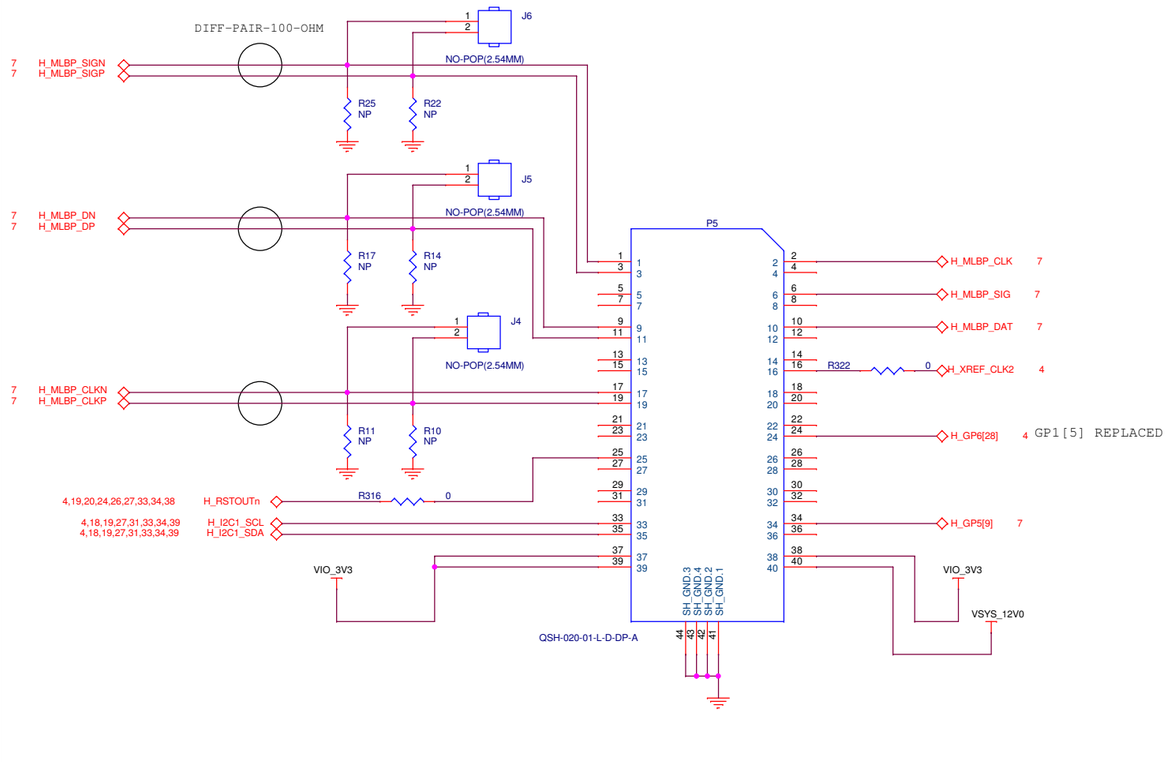
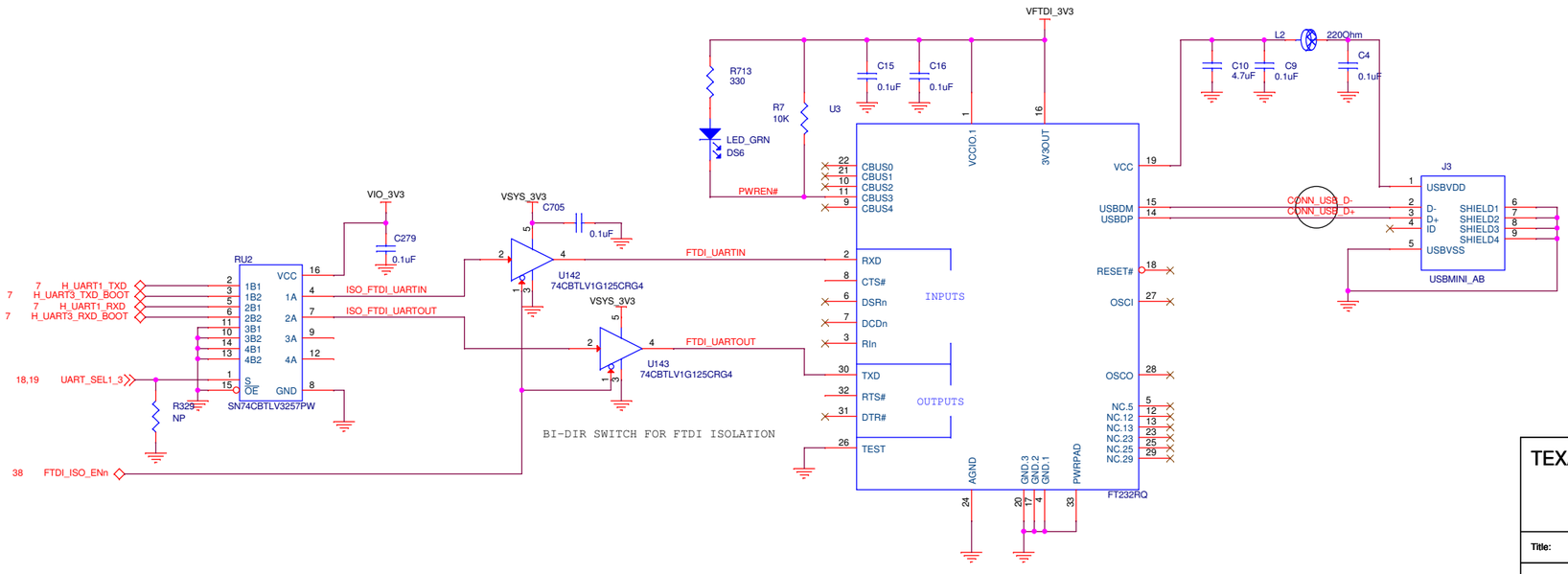
JTAG HEADER



MLB HEADER



FTDI USB/UART CONSOLE WITH ISOLATION



TEXAS INSTRUMENTS INCORPORATED

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VSYS_12V0 R16 10K R13 1K C264 0.1uF
U5 SENSE1 VDD CT RESET MR GND TPS3808G09DBVRG4
VSYS_5V0 C262 0.1uF
VIO_3V3 R319 10K
Reset Threshold 0.84 Volts

VIO_3V3 R19 1.5K R18 1K C276 0.1uF
U6 SENSE1 VDD CT RESET MR GND TPS3808G09DBVRG4
VSYS_5V0 C272 0.1uF
Reset Threshold 0.84 Volts

VIO_3V3 R328 10K C274 0.1uF
U7 74LVC1G08DCK
18 PCI_SW_RESETn
19 PCI_RESET_SEL
VIO_3V3 C263 0.1uF R317 10K
RU1 74CBTLV1G125CRG4

VIO_3V3 C259 0.1uF R12 10K
U4 74LV1G126CRG4
PCI_PORz 34

DIFF-PAIR-100-OHM
7 H_PCIE_TXP0 C82 0.1uF CON.PCIE_TXP0 26
7 H_PCIE_TXN0 C84 0.1uF CON.PCIE_TXN0 26
7 H_PCIE_RXN0 R90 0 CON.PCIE_RXN0 26
7 H_PCIE_RXP0 R89 0 CON.PCIE_RXP0 26
7 H_PCIE_TXP1 C85 0.1uF CON.PCIE_TXP1 26
7 H_PCIE_TXN1 C86 0.1uF CON.PCIE_TXN1 26
7 H_PCIE_RXN1 R94 0 CON.PCIE_RXN1 26
7 H_PCIE_RXP1 R93 0 CON.PCIE_RXP1 26
AC COUPLING CAP
PLACE BY CONNECTOR

VSYS_12V0 VSYS_3V3 VIO_3V3
P6
B1 +12V.1 B2 +12V.2 B3 +12V.3 B4 GND.1 B5 SMCLK B6 SMDAT B7 GND.2 B8 +3.3V.1 B9 TRSTn B10 3.3VAUX B11 WAKEn
PRSNT1 A1 +12V.4 A2 +12V.5 A3 GND.12 A4 TCK A5 TDI A6 TDO A7 TMS A8 +3.3V.2 A9 +3.3V.3 A10 PERSTn A11
KEY
B12 RSVD.1 B13 GND.3 B14 PETp0 B15 PETn0 B16 GND.4 PRSNT2 B17 GND.5 B18 PETp1 B19 PETn1 B20 GND.6 B21 PETp2 B22 PETn2 B23 GND.7 B24 GND.8 B25 PETp3 B26 PETn3 B27 GND.9 B28 GND.10 B29 RSVD.2 B30 PRSNT2.2 B31 GND.11 B32
GND.13 A12 REFCLK+ A13 REFCLK- A14 GND.14 A15 PERp0 A16 PERn0 A17 GND.15 A18 RSVD.3 A19 GND.16 A20 PERp1 A21 PERn1 A22 GND.17 A23 GND.18 A24 PERp2 A25 PERn2 A26 GND.19 A27 GND.20 A28 PERp3 A29 PERn3 A30 GND.21 A31 RSVD.4 A32
PCIe 4X Connector
R404 10K
R372 10K
R370 10K
R369 10K
26 CON.PCIE_TXP0 CON.PCIE_TXP0
26 CON.PCIE_TXN0 CON.PCIE_TXN0
R381 NP
26 CON.PCIE_TXP1
26 CON.PCIE_TXN1
DIFF-PAIR-100-OHM
REFCLKp REFCLKn
CON.PCIE_RXP0 CON.PCIE_RXN0
CON.PCIE_RXP0 26
CON.PCIE_RXN0 26
CON.PCIE_RXP1 26
CON.PCIE_RXN1 26
R57 100
0.1uF C43 PCI_CONN_REFP PCI_CONN_REFP 26
0.1uF C44 PCI_CONN_REFN PCI_CONN_REFN 26
DIFF-PAIR-100-OHM

SATA
AC COUPLING CAP
PLACE BY CONNECTOR
J12
Pin # Function
1 Ground
2 A+ (Transmit)
3 A- (Transmit)
4 Ground
5 B- (Receive)
6 B+ (Receive)
7 Ground
- coding notch
A 7-pin Serial ATA data cable
MH1 MH9 SATA HEADER 7
DIFF-PAIR-100-OHM
CON.SATA_TXP0 C134 10nF H_SATA_TXP0 4
CON.SATA_TXN0 C133 10nF H_SATA_TXN0 4
CON.SATA_RXN0 C132 10nF H_SATA_RXN0 4
CON.SATA_RXP0 C130 10nF H_SATA_RXP0 4
DIFF-PAIR-100-OHM

VDDA_CDCM9102 VIO_3V3
L7 220Ohm
VDDA_CDCM9102
C34 10uF C283 0.01uF C281 1000pF C282 0.1uF
VDD_CDCM9102
C288 0.1uF C286 0.1uF C287 10uF C285 0.1uF
E1 0.47uF
VIO_3V3
R27 10K R28 10K
LVDS OUTPUT
OSCOUT PIN = OFF
U10
VDD5 VDD4 VDD3 VDD6 VDD1_OUT0 VDD2_OUT1 OUT1P OUT1N OUT0P OUT0N XIN REG_CAP2 REG_CAP1 OSCOUT
OS1 OS0 0E RSTn GND.2 GND.1 PWR_PAD
NC.8 NC.13 NC.15 NC.24 NC.25 NC.26 NC.27 NC.28 NC.29 NC.30 NC.31 NC.32
CDCM9102RHBR
VDDA_CDCM9102 R25 NP R26 0
R349 10K
CE = '1' = OUTCLOCK
R340 NP
4,19,20,24,25,27,33,34,38 H_RSTOUTn
DIFF-PAIR-100-OHM
SERDES_IN_REFP SERDES_IN_REFN
SERDES_IN_REFP 26 SERDES_IN_REFN 26
PCI_CONN_REFP PCI_CONN_REFN
PCI_CONN_REFP 26 PCI_CONN_REFN 26
C48 10uF C41 10uF
TP11 TP
C55 NP
Y1 25.0000MHz
R48 0

DIFF-PAIR-100-OHM
26 SERDES_IN_REFN
26 SERDES_IN_REFP
C53 0.1uF C52 0.1uF
R211 100
DIFF-PAIR-100-OHM
H_LJCB_CLKN 7
H_LJCB_CLKP 7
R573 NP R576 NP

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents:	PCIE		
Size: C	DOC NO: 518451	REV: A	
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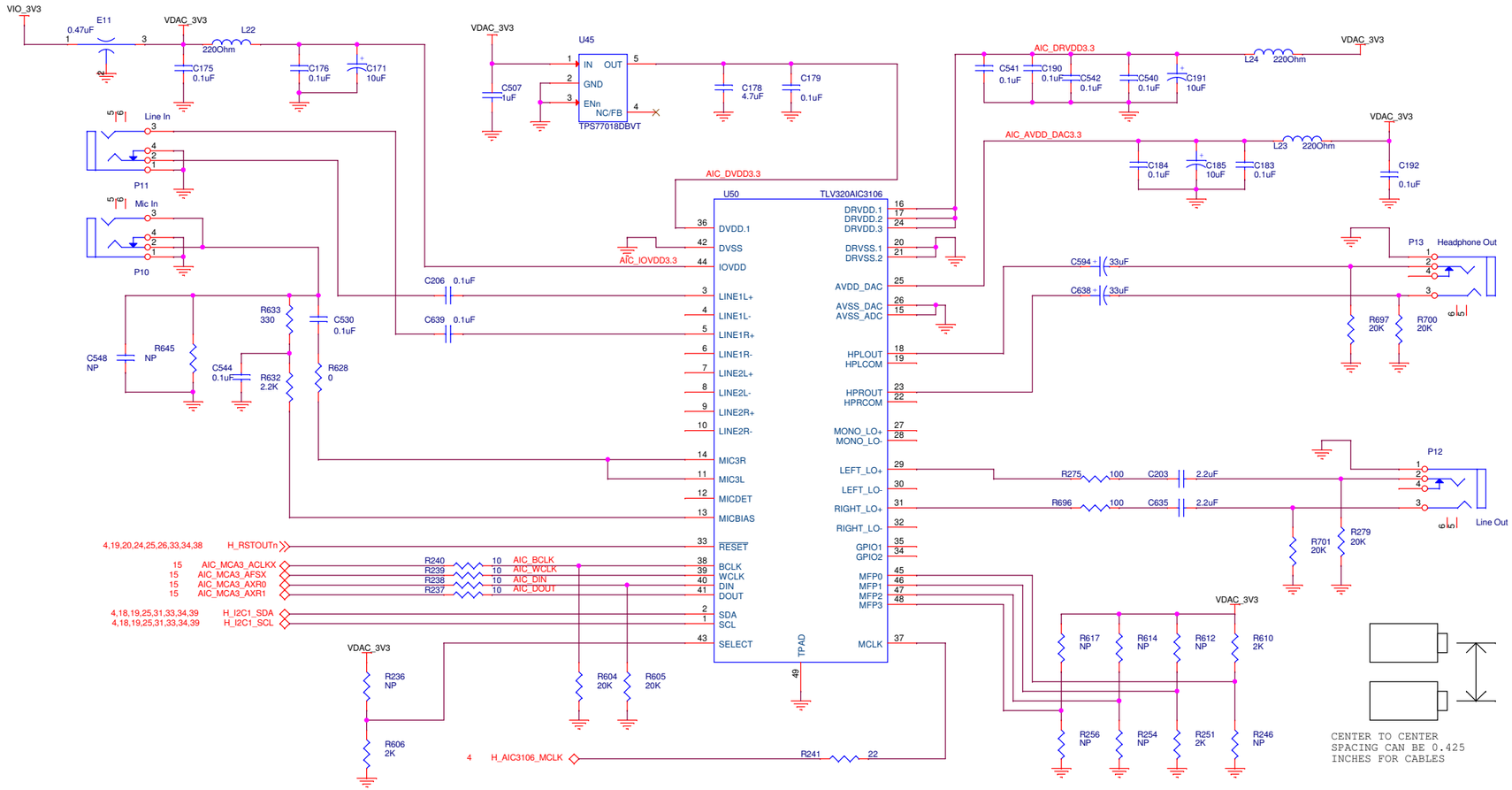

TEXAS INSTRUMENTS INCORPORATED			
Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents:	AIC3106		
Size: C	DOC NO: 518451		REV: A
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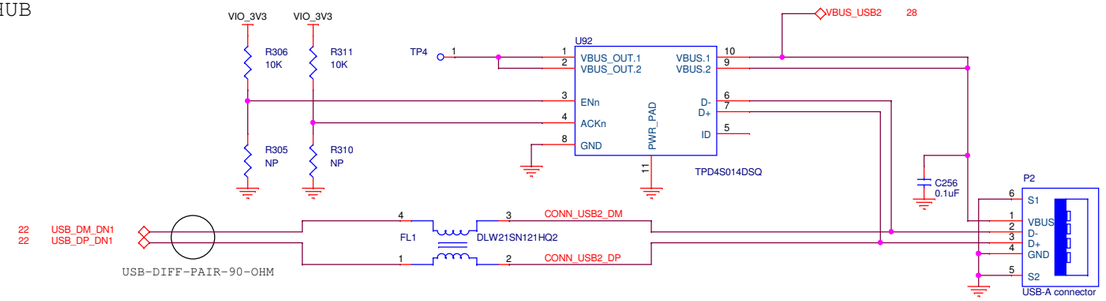
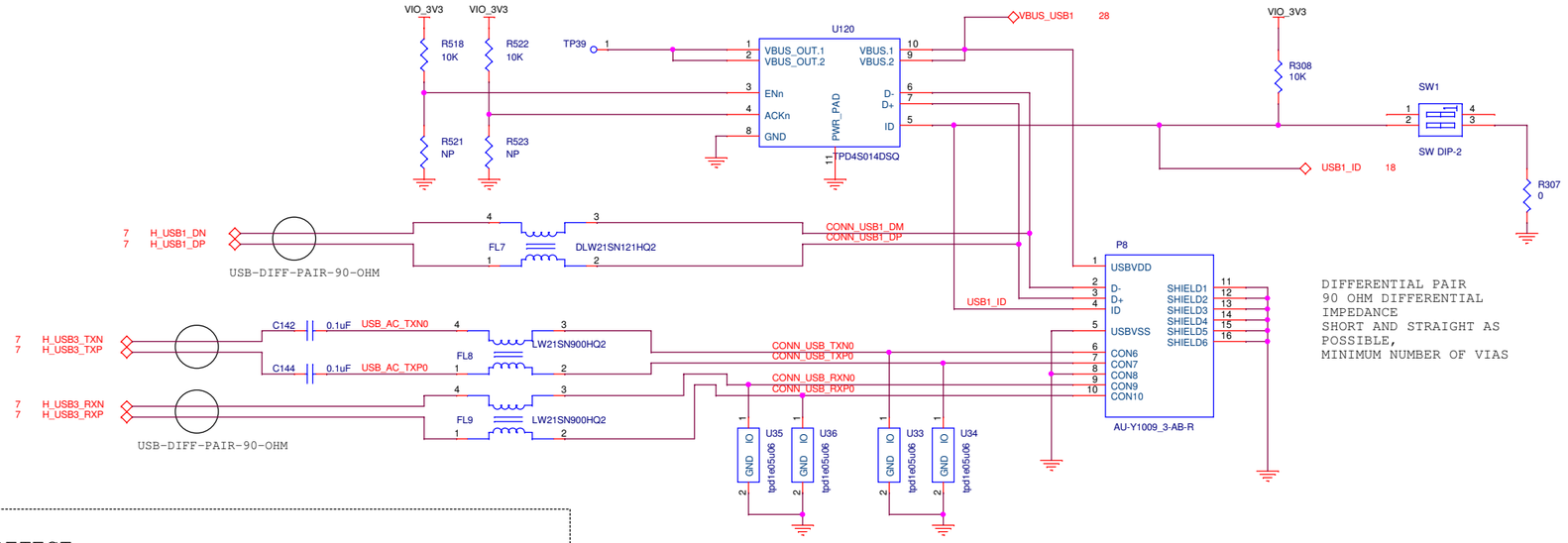
USB HS HOST PORT BEHIND HUB

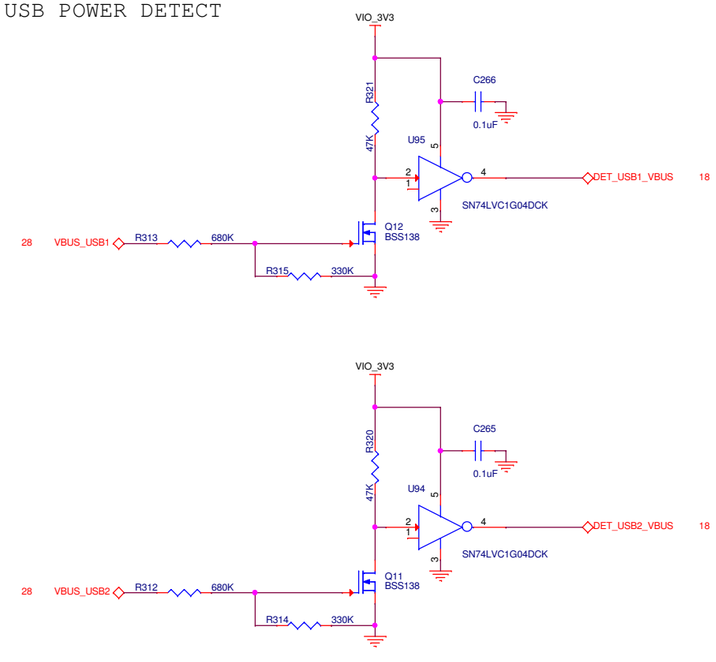


USB HS/SS OTG PORT

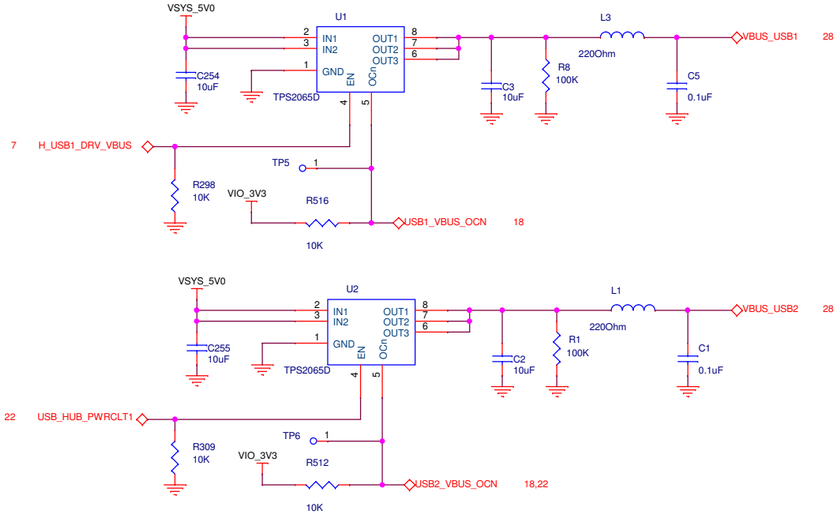


DIFFERENTIAL PAIR
90 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

USB POWER DETECT



USB POWER SWITCH



TEXAS INSTRUMENTS INCORPORATED			
Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents:	USB		
Size: C	DOC NO: 518451		REV: B
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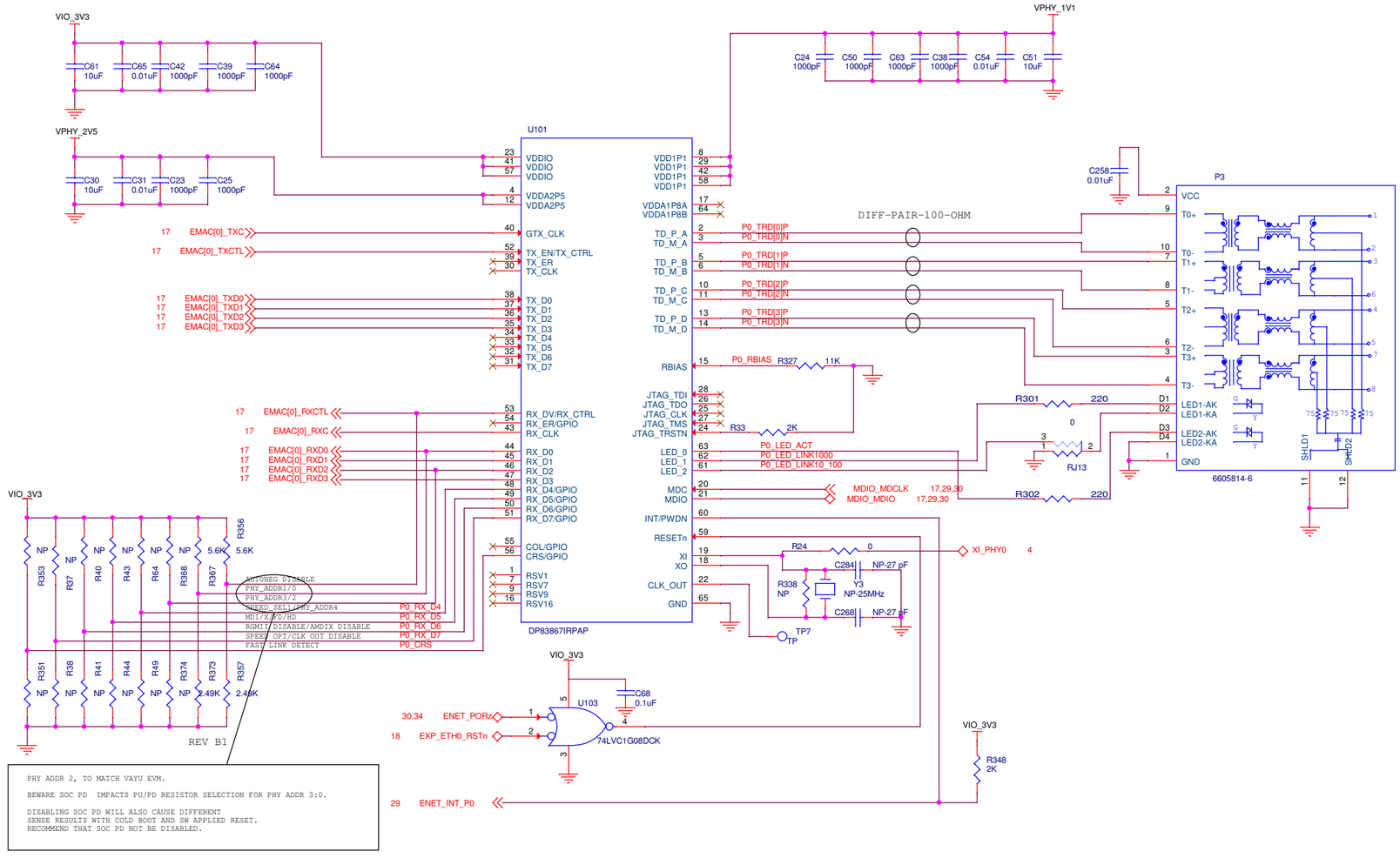

TEXAS INSTRUMENTS INCORPORATED

Title: DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents: ENET PORT0		
Size: C	DOC NO: 518451	REV: B1
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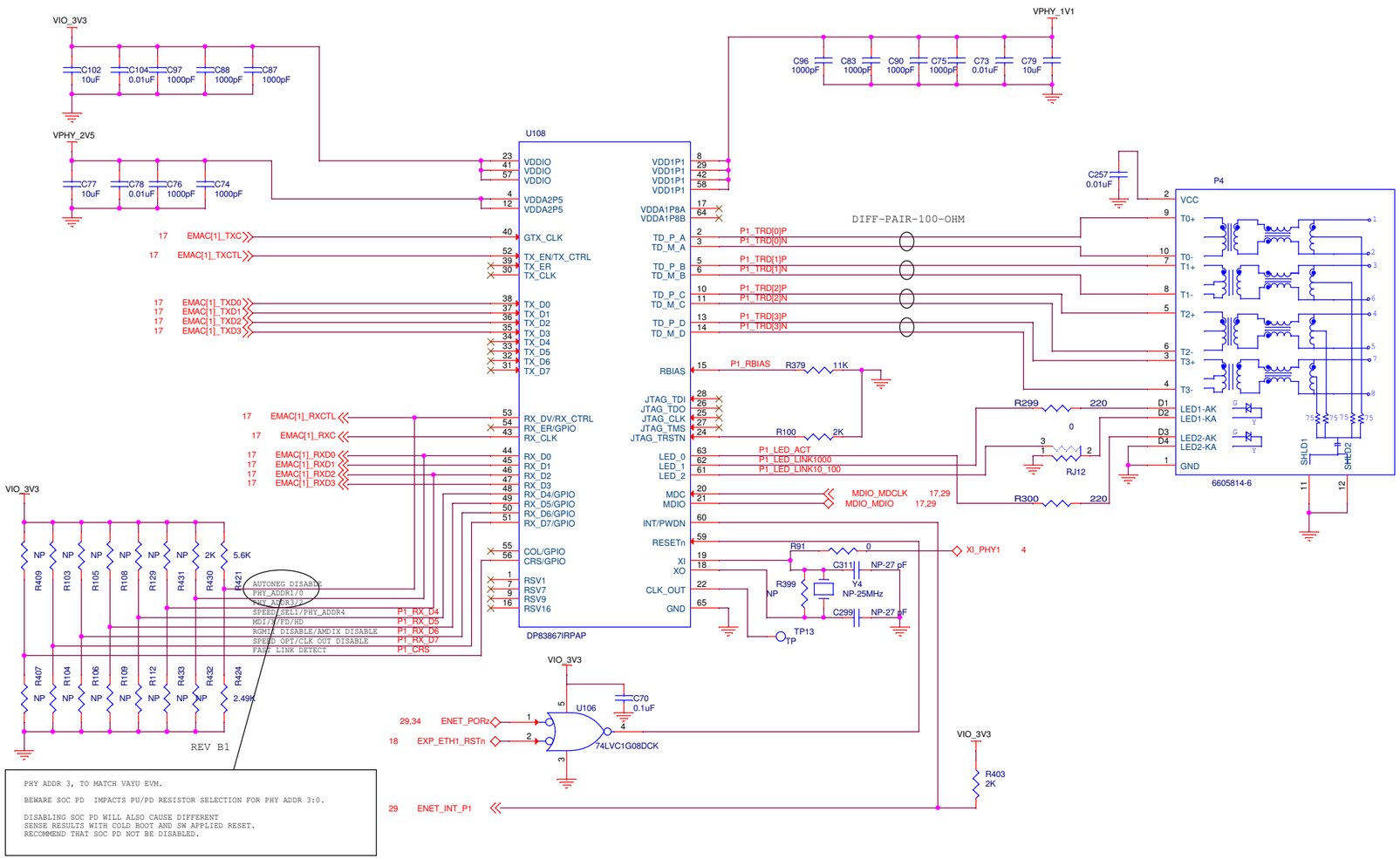

TEXAS INSTRUMENTS INCORPORATED

Title: DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents: ENET PORT1		
Size: C	DOC NO: 518451	REV: B1
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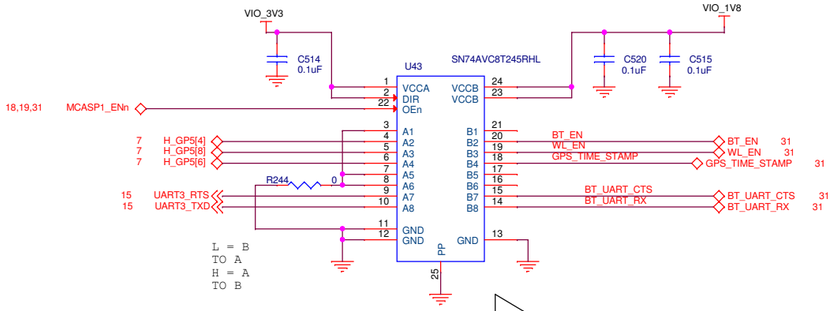
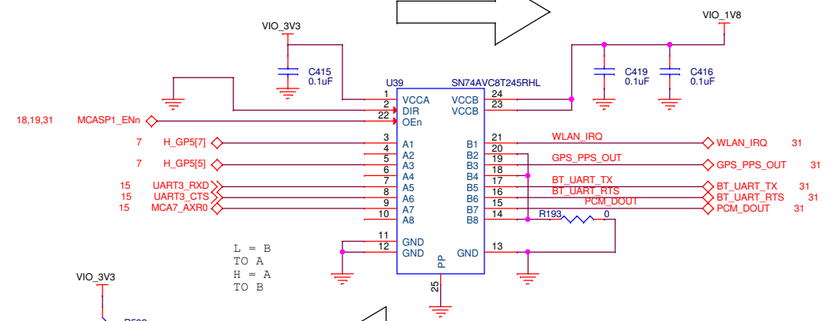
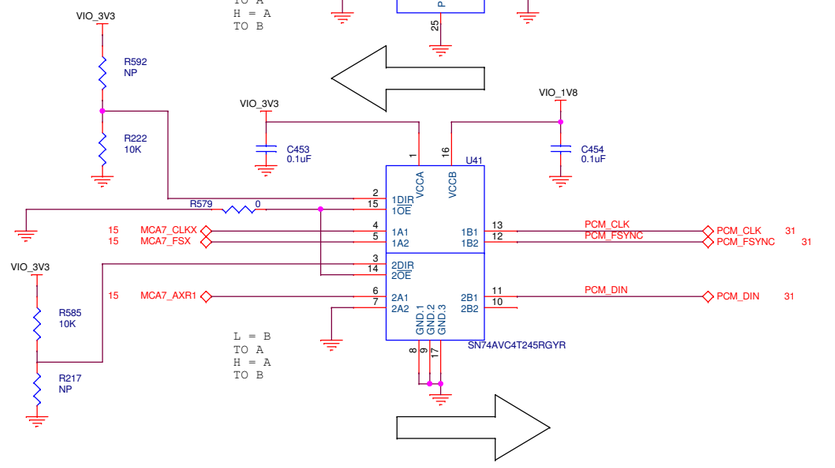
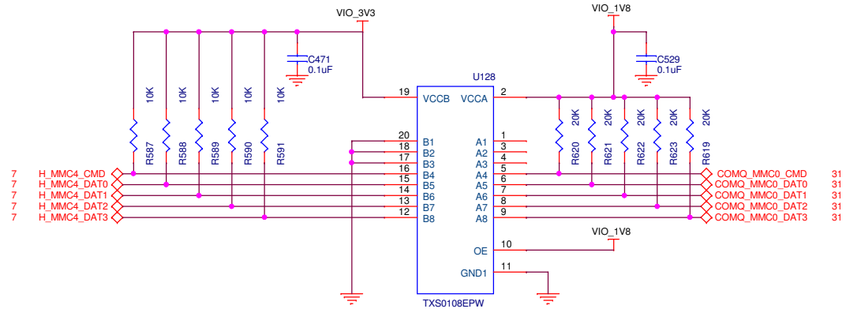
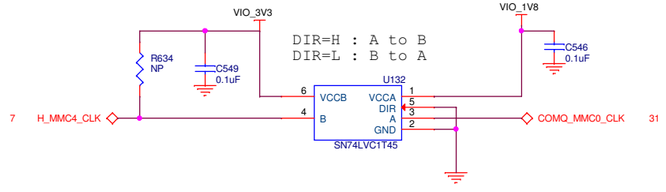
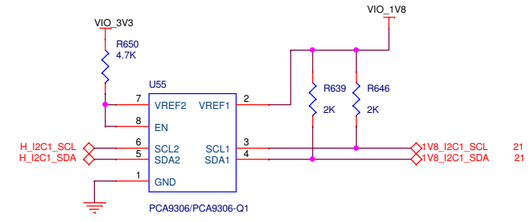




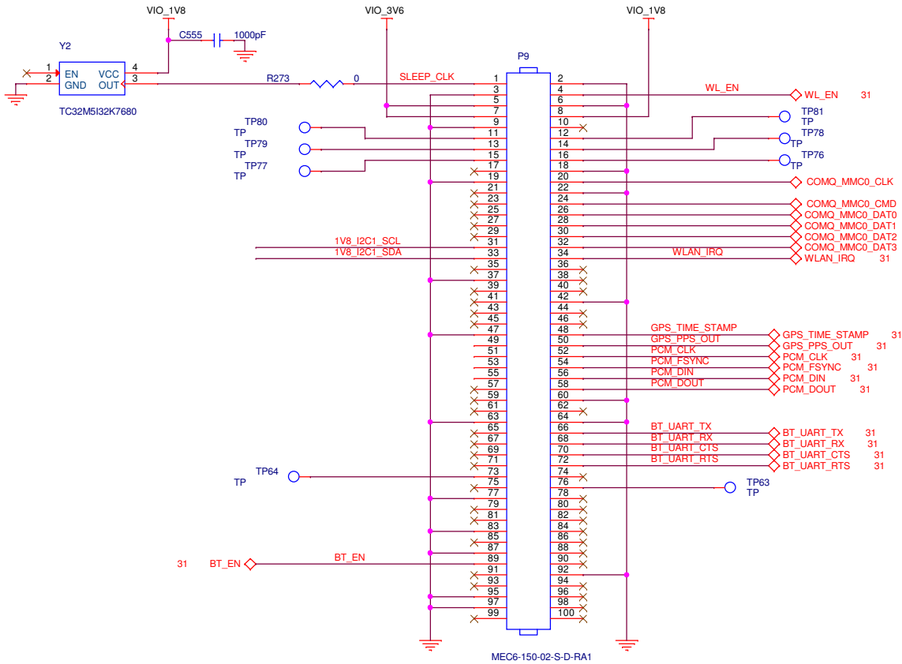


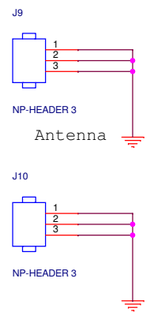






DELTA VAYU H, VCCB SIDE OF
BUFFER TIED DIRECTLY TO VIO_1V8.
COM8 INTERFACE IS ALWAYS 1.8V.





TEXAS INSTRUMENTS INCORPORATED

Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents:	COMQ8		
Size: C	DOC NO: 518451	REV: B	
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VBATT
9.5V-13.5V
8Amps
J2
PJ-063BH
MTG1
MTG2
VIN_CONN
F1
8A_QuickBlow
D3
SMCJ30A-13-F
SMCJ14A-13-F
D2
C37
0.22uF
50V
C47
2.2uF
25V
U9
VCAPL
GT PULL DWN
NC3
ANODE
CATHODE
VCAPH
GATE DRV
NC5
LM74610
CSD18501Q5A
Q2
REVERSE BATTERY PROTECTION
VLIM_12V0
VSYS_12V0_APM
VSYS_12V0
R32
0.01
05081W
SUD50P04-08
Q1
R23
4.7K
C40
4.7uF
25V
R36
1.5K
Q4
BSS138
32,38
PB_ON
C58
1uF
50V
C60
0.1uF
50V
C59
0.1uF
50V
C57
1uF
50V
C62
4.7uF
50V
R297
1K
DS1
LED_GRN
PB_ON - POWER ON BY DEFAULT. PB_ON LOW TURNS OFF VSYS_12V0 TO EVM AND EXPANSION CARDS.
P-FET POWER SWITCH WITH IN-RUSH LIMIT.
PB_ON CAN BE PULLED LOW FROM THE TEST AUTOMATION HEADER VIA A FET.
VLIM_12V0
R39
84.5K
D1
NP
R31
61.9K
R150
0
VSYS_12V0
R492
NP
EN_TPS43351
32
32,38
PB_ON
~5.07V
SW2
PB_SW
J7
NP
R350
1K
R21
61.9K
C35
0.22uF
BIAS THE ENABLES, AND DEBOUNCE THE PUSH BUTTON.
VIN_CONN
VSYS_12V0
TP9
TP
C72
100uF
25V
TPS43351QDAPRQ1
U18
GC2
VIN
VBAT
EXTSUP
VREG
SYNC
RT
SSA
ENA
ENB
SSB
DLYAB
CBA
GA1
PHA
GA2
SA1
SA2
FBA
COMPA
PGA
CBB
GB1
PHB
GB2
SB1
SB2
FBB
COMPB
PGB
NC.2
NC.3
NC.18
NC.36
AGND.1
AGND.2
PWR PAD
PGNDA
PGNDB
R441
1.5K
R445
NP
R446
0
C325
4.7uF
Fsw = 400KHZ
R479
0
C343
0.01uF
32
EN_TPS43351
C345
0.01uF
C352
1000pF
C334
0.22uF
GA1
R402
0
PHA
GA2
R417
0
C339
0.01uF
C333
0.22uF
GB1
R401
0
PHB
GB2
R414
0
C338
0.01uF
C348
2700pF
R480
15K
C350
56pf
C349
2000pF
R476
20K
C344
39pf
VSYS_3V3
TP96
R728
20K
PGD_STAGE1_3V3_5V0
35
Q7
CSD18501Q5A
Q9
CSD18501Q5A
Q8
CSD18501Q5A
Q10
CSD18501Q5A
VSYS_12V0
C301
22uF
25V
L10
2.2uH (7443330220)
R138
0.005
R87
10
C80
330pF
VSYS_12V0
C300
22uF
25V
L11
8.2uH(744771008)
R141
0.015
R88
10
C81
330pF
10 Volts
Less than ESR 35m-ohm
C126
100uF
10V
C109
100uF
10V
C117
100uF
10V
C119
100uF
10V
C127
100uF
10V
10TPB100ML
10 Volts
Less than ESR 35m-ohm
C136
47uF
16V
C131
47uF
16V
C125
NP
C128
100pF
C129
100pF
VSYS_3V3_APM
VSYS_3V3
R160
0.01
05081W
R154
49.9
R148
49.9K
R149
16K
VSYS_3V3 - 10Amps
VSYS_5V0_APM
VSYS_5V0
R162
0.01
05081W
R159
49.9
R156
84.5K
R155
16K
VSYS_5V0 - 5Amps
TP3
SMT-TP
TP83
SMT-TP
TP86
SMT-TP
TP93
SMT-TP
TP92
SMT-TP
TP84
SMT-TP
TP1
SMT-TP
TP87
SMT-TP
TP99
SMT-TP
TP100
SMT-TP
DISTRIBUTE ON BOARD, ONE GND TESTPOINT BY MLB CONNECTOR
TP12
TP
TP85
TP
TP91
TP
TP2
TP
VSYS_12V0
J1
NP
OPTIONAL FAN CONNECTOR

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents:	STAGE1 BUCK		
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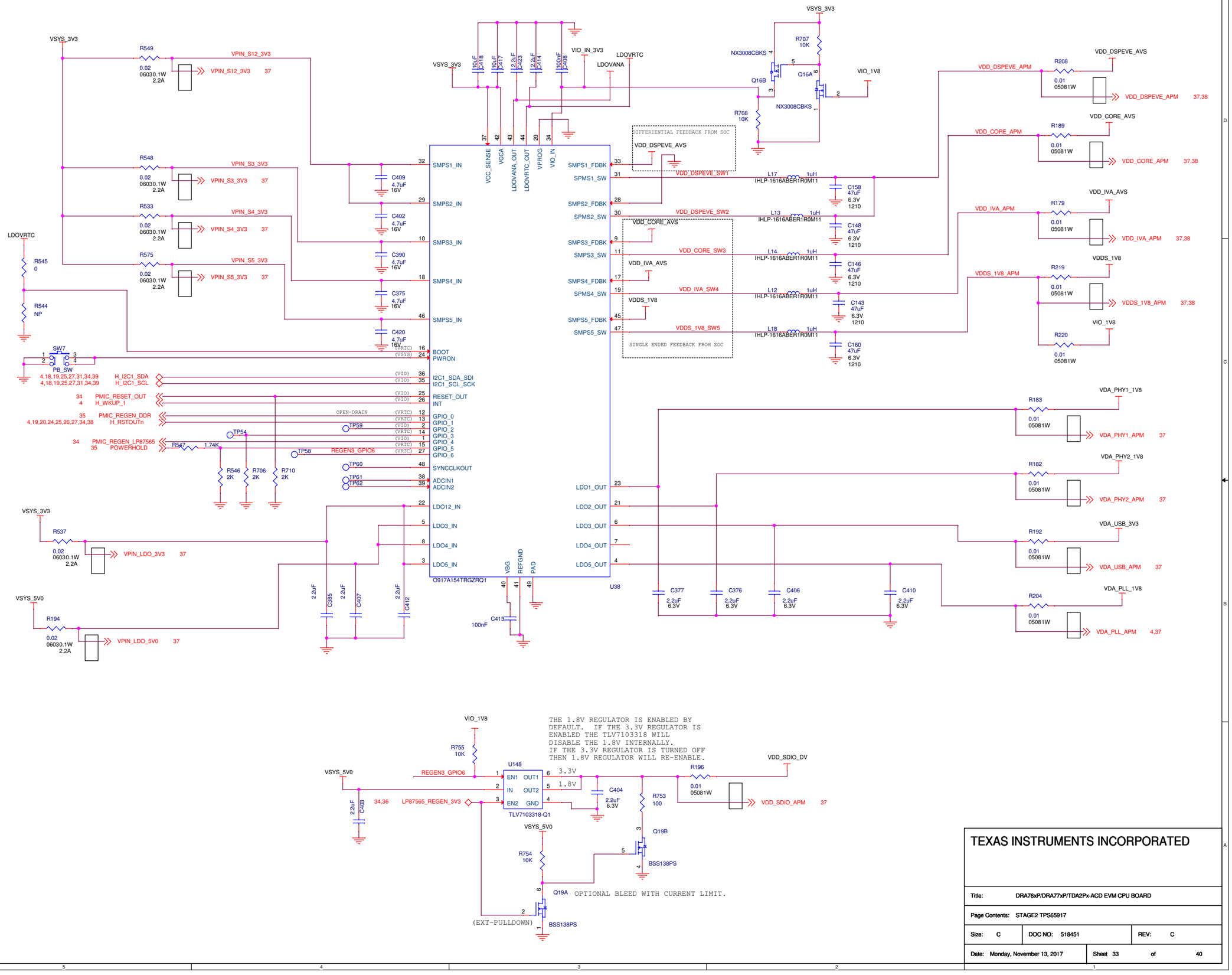

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD	
Page Contents:	STAGE2 TPS65917	
Size: C	DOC NO: 518451	REV: C
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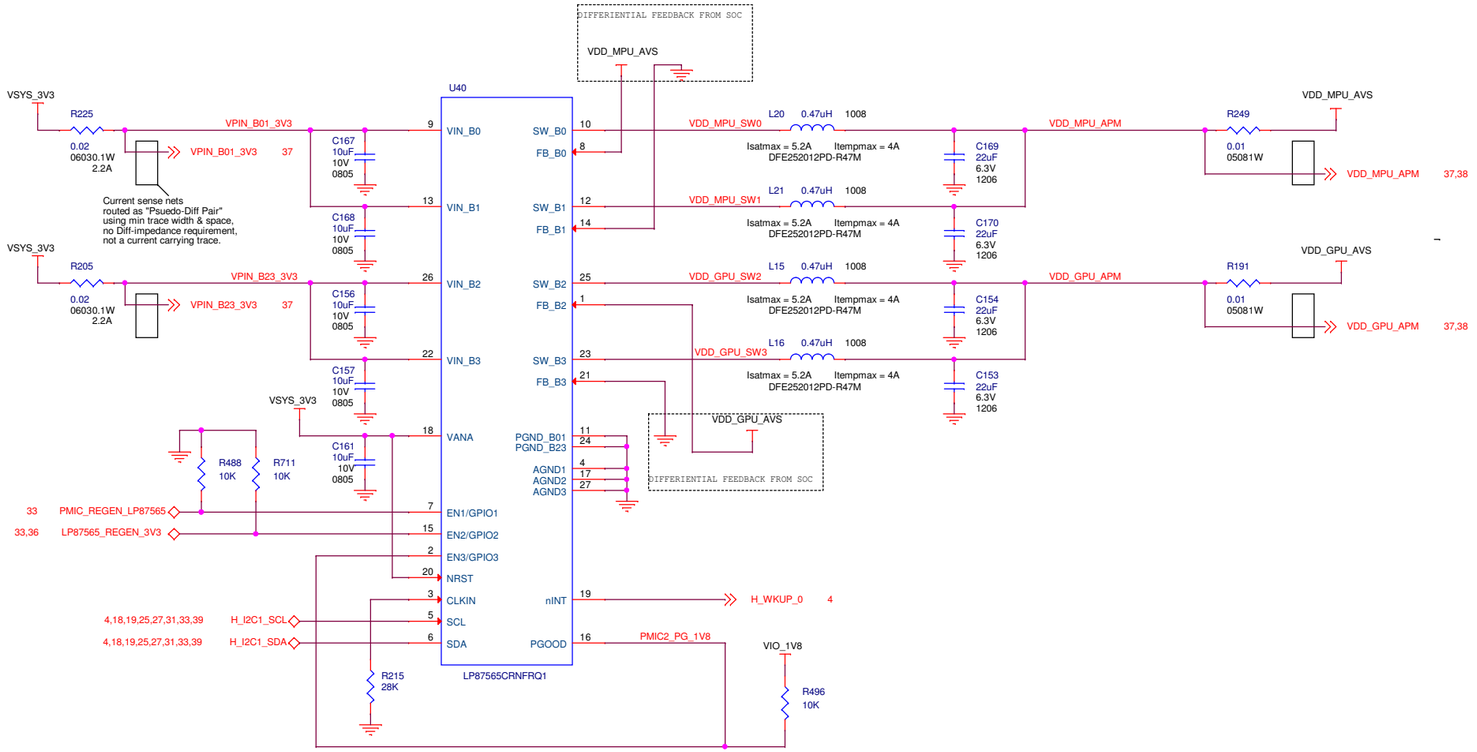

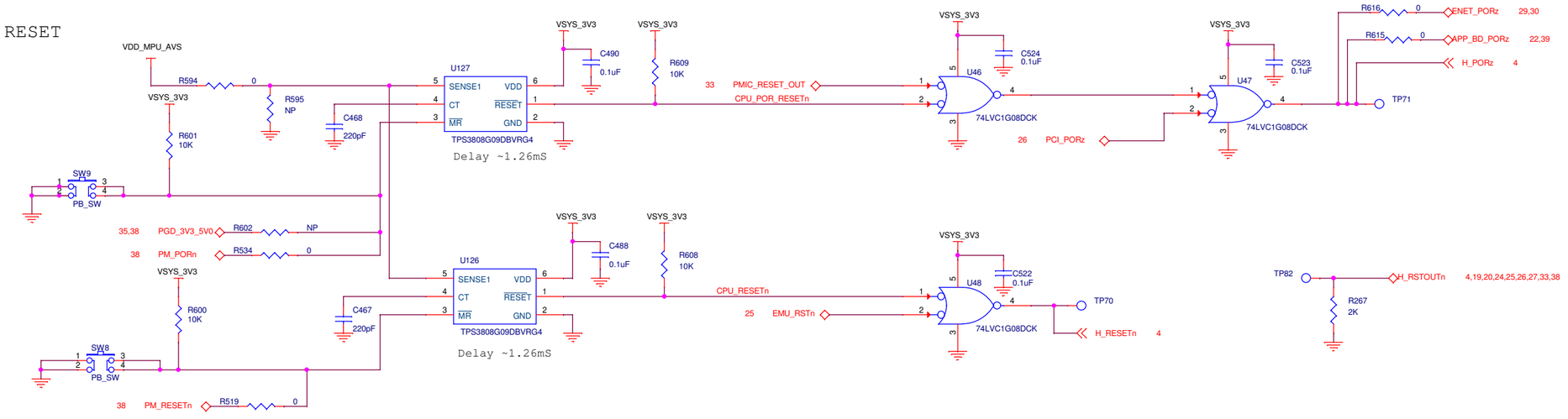

TEXAS INSTRUMENTS INCORPORATED

Title: DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents: STAGE2 LP87565		
Size: C	DOC NO: 518451	REV: C
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VDDR_MEM_1V35
R281 10K
R296 NP H_DDR1_RST 5,13
R699 NP H_DDR2_RST 5,14
TP90
VSYS_3V3
C636 10uF 10V 0805
C626 0.1uF
VSYS_3V3
C603 1uF
VTT_AGND
C575 10uF 0805
U138
C610 0.1uF
L31 0.47uH
Isatmax = 5.2A Itempmax = 4A
IHLP1616BZERR47M11
VDDR_APM
C650 47uF 6.3V 1210
C651 47uF 6.3V 1210
C652 47uF 6.3V 1210
R703 0.01 05081W
VDDR_MEM_1V35
VDDR_APM 37,38
VIO_IN_3V3
R667 10K
VSYS_3V3
R284 NP-10K
33 PMIC_REGEN_DDR
R285 0
AVIN
PVIN1
PVIN2
LDOIN
ENSW
ENLDO
PGOOD
ILIM
SS/TRK
COMP
FB
RT/SYNC
BOOT
SW1
SW2
SW3
VDDQSNS
VTT
VTTSNS
VTTREF
AGND
PGND1
PGND2
VTTGND
PAD
VPO_DDR_SW
TPS54116QRTWTQ1
C563 10uF 0805
C580 10uF 0805
VPO_DDR_VTT
R671 0.01 05081W
VTT
R283 100K
C211 3300pF
R286 28K
C214 24pF
C215 220pF
R291 28K
VTT_AGND
VDDR_SOC_VREFSTL
C587 0.22uF
VTT_AGND
C601 75pF
R692 20K
R688 16K
VTT_AGND
VDDR_APM
R280 NP-1K
VDDR_SOC_VREFSTL
R282 0
VDDR_VREFSTL
R277 NP-1K
VTT_AGND SINGLE POINT CONNECTION AT PIN 14 AND POWER PAD.
0 R653
U134
VDDR_APM
VIN.1
VIN.2
1.2 volt input
VSYS_5V0
ON
VBIAS
VOUT.1
VOUT.2
CT
GND
PWR_PAD
NP-TPS22965DSG
R642 0.01 05081W
VDDR_SOC_1V35
VDDR_SOC_APM 37,38
C545 220pF
POPULATIONS FOR SUSPEND TO RAM

	DEFAULT	SUSPEND TO RAM
R653	POP	NO-POP
U134	NO-POP	POP
R285	POP	NO-POP
R284	NO-POP	POP
R282	POP	NO-POP
R277	NO-POP	POP
R280	NO-POP	POP

UNDERVOLTAGE DETECT - 2 OPTIONS

SELECT STAGE1 BUCK POWER GOOD OR INDEPENDENT UNDER VOLTAGE DETECTION CIRCUIT TO ENABLE STAGE2 BUCKS.

VSYS_12V0
C711 0.22uF 50V
R742 274K
100K R744
C712 150pF
R743 100K
Q18B
Q18A
BSS138PS
BSS138PS
Vth .9v-1.5v, typ-1.2V
Vt ~ 4.48V
PGD_UV_DETECT
OPTION 1: LOW COST
32 PGD_STAGE1_3V3_5V0
RJ17 0.A
PGD_3V3_5V0 34,38
VSYS_3V3
TP98
R756 20K
OPTION 2: PRECISE SENSE
VSYS_3V3
C713 NP-0.1uF
NP-TPS3803-01-Q1
VDD RESETn GND SENSE NC
U147
Vth 1.226V
Vt ~ 4.58V
NP-6.2V D24

POWER HOLD

VSYS_3V3
C320 0.1uF
R429 10K
R444 1K
U114
SENSE1 VDD
CT RESET
MR GND
TPS3808G33DBVRG4
SW5
PB_SW
6 H_POWERHOLD_CLK
U113
CLK VCC
D PRE
QN CLR
GND Q
SN74LVC2G74DCT
R443 1K
VSYS_3V3
C326 0.1uF
U16
74LVC1G08DCK
POWERHOLD 33

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents:	STAGE2 TPS54116		
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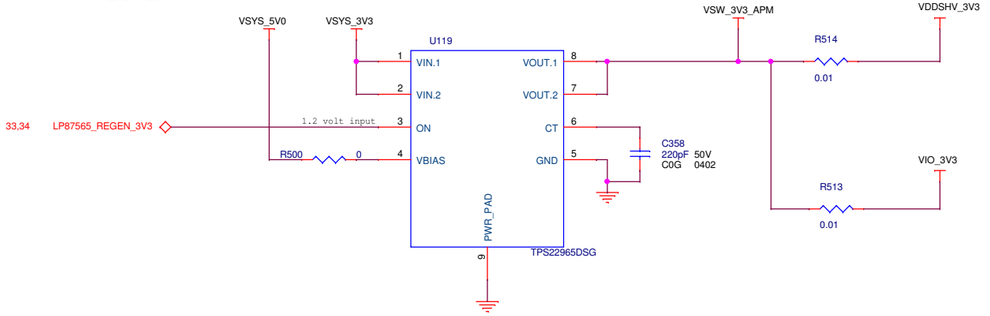
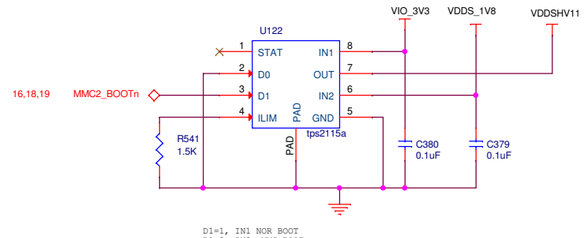
3V3 SWITCH



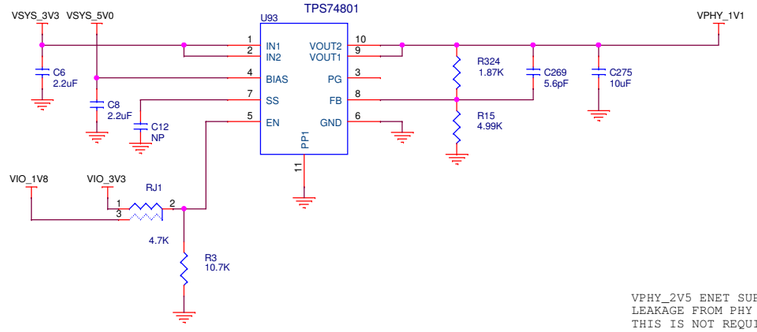
VDDSHV11 3.3V/1.8V MUX



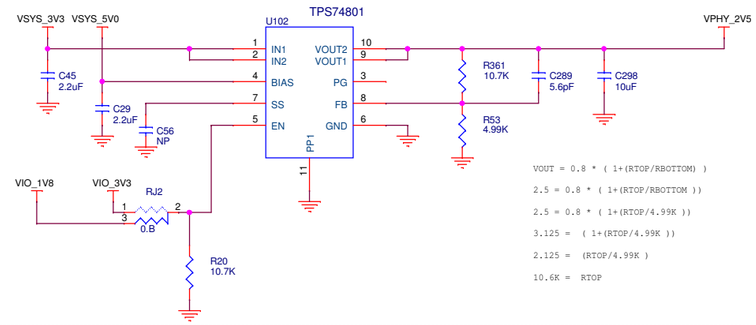
D1=1, IN1 NOR BOOT
D1=0, IN2 eMMC BOOT

BOOT SWITCHES DEFAULT AS PULLUPS. SWITCH
CLOSED IS PULL DOWN TO SELECT FUNCTION.

ETHERNET 2.5V/1.1V



VPHY_2V5 ENET SUPPLY TURNS ON WITH VIO_1V8 TO PREVENT
LEAKAGE FROM PHY CLK IN TO VPHY_2V5. RAIL.
THIS IS NOT REQUIRED IF USING A CRYSTAL ON THE ENET PHY.



VOUT = 0.8 * (1+(RTOP/RBOTTOM))

2.5 = 0.8 * (1+(RTOP/RBOTTOM))

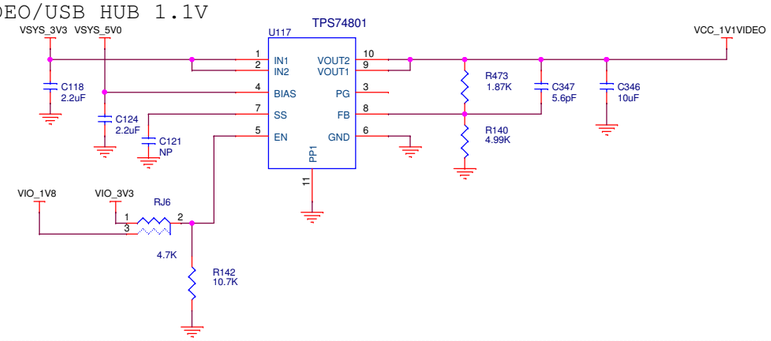
2.5 = 0.8 * (1+(RTOP/4.99K))

3.125 = (1+(RTOP/4.99K))

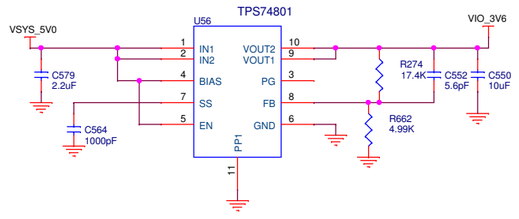
2.125 = (RTOP/4.99K)

10.6K = RTOP

VIDEO/USB HUB 1.1V



COMQ8 3.6V



TEXAS INSTRUMENTS INCORPORATED

Title: DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
Page Contents: MISC POWER/SWITCHES		
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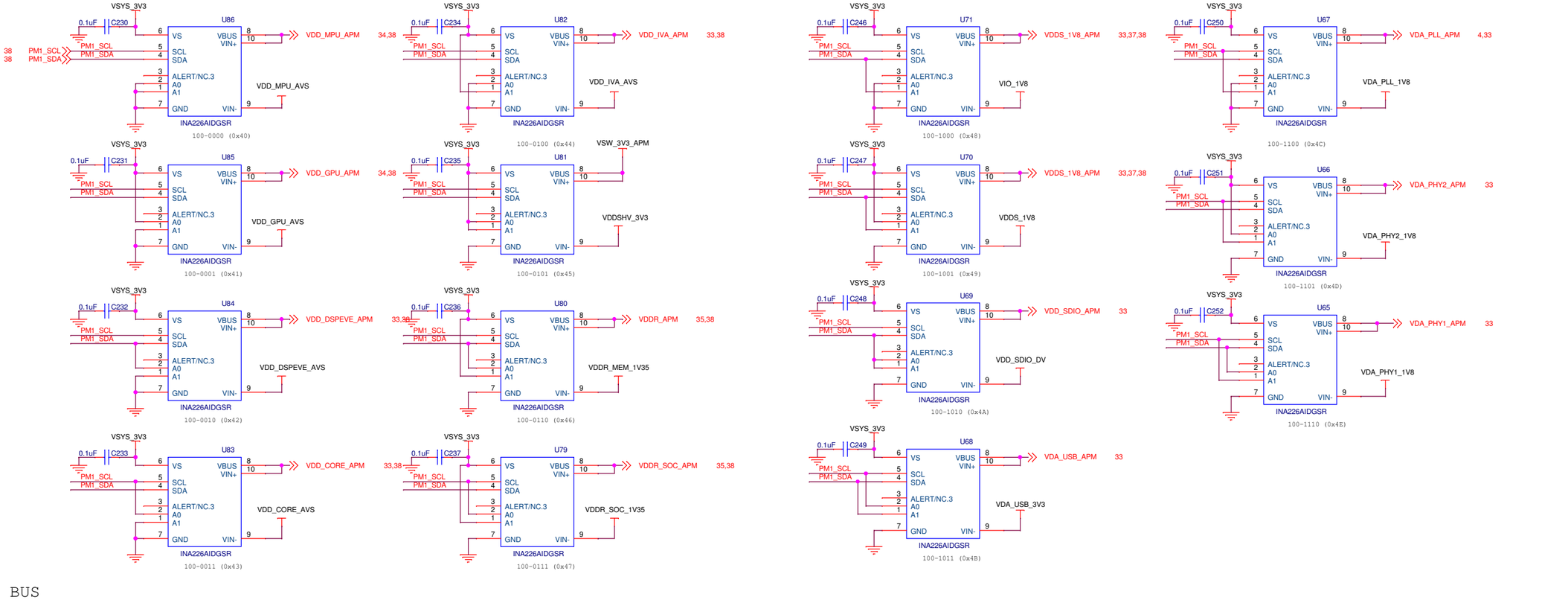
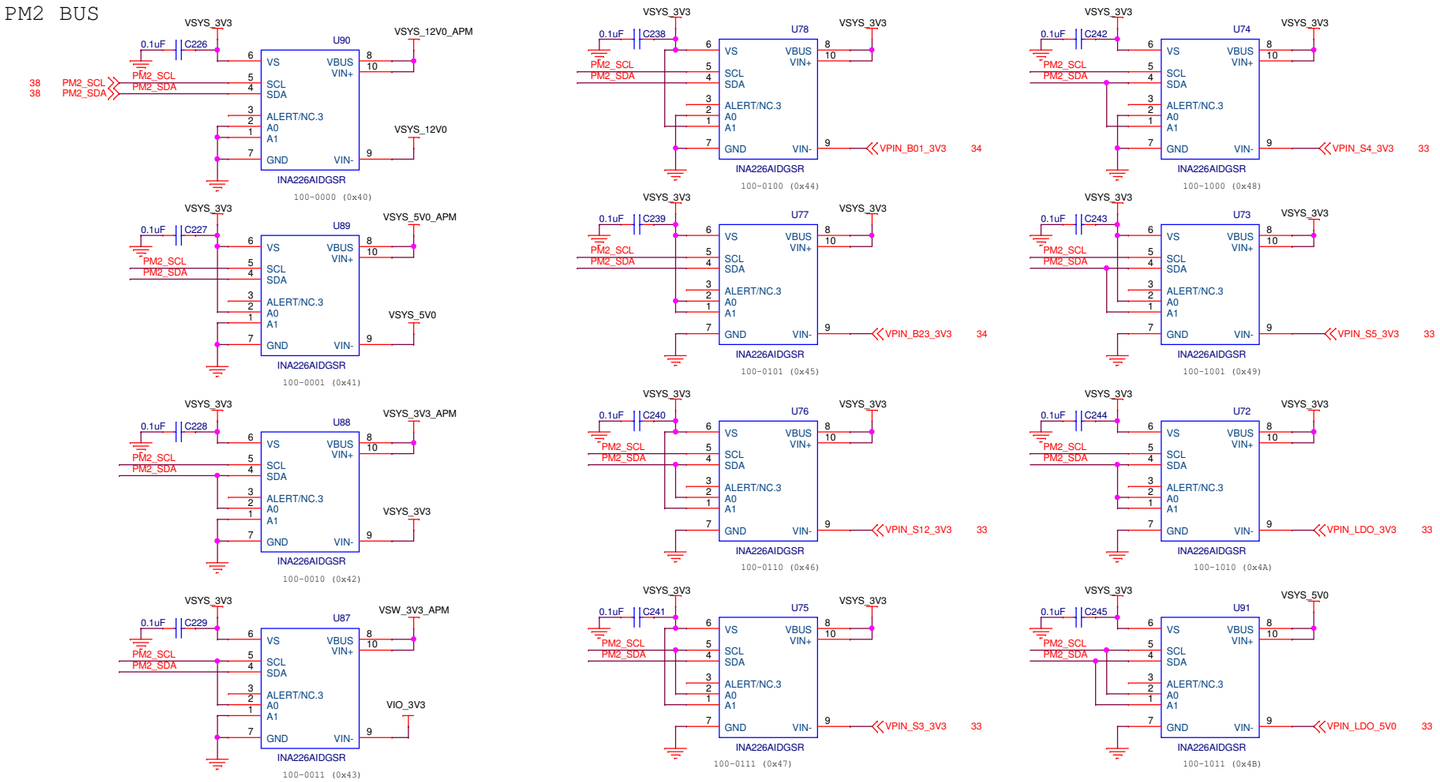
PM1 BUS



PM2 BUS



TEXAS INSTRUMENTS INCORPORATED			
Title:	DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD		
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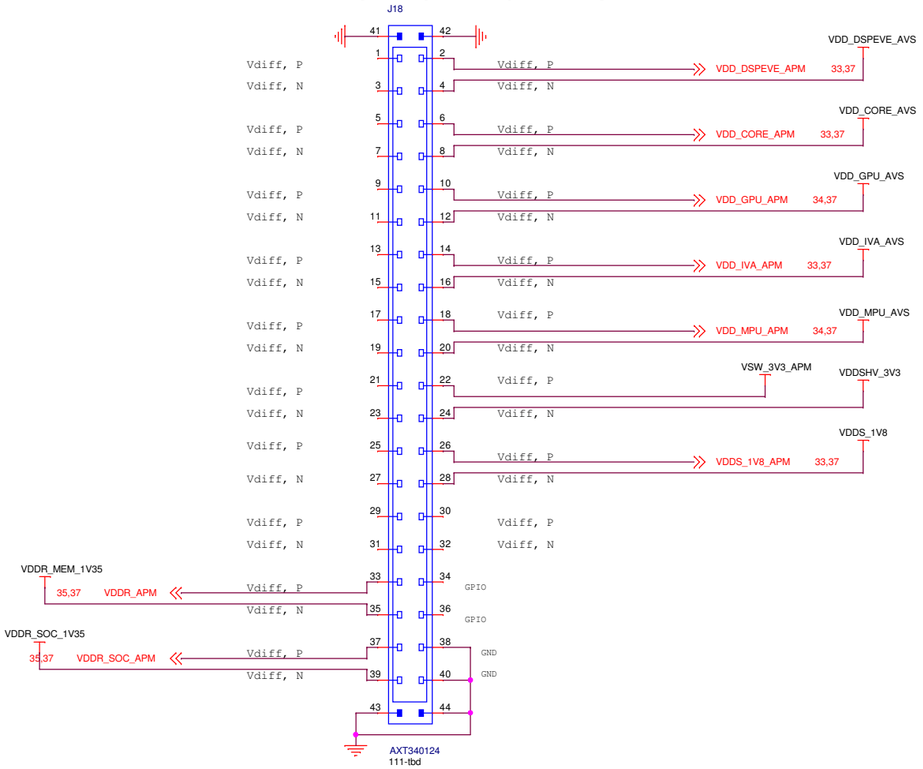
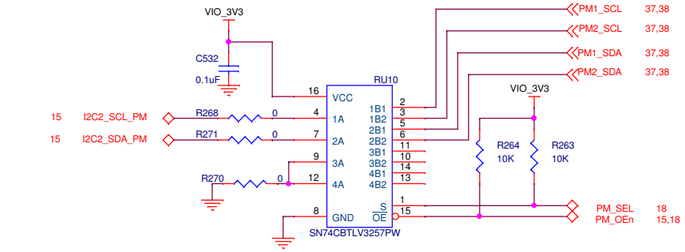
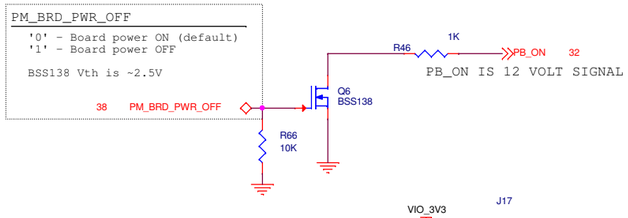
DARA Bd Interface Connector

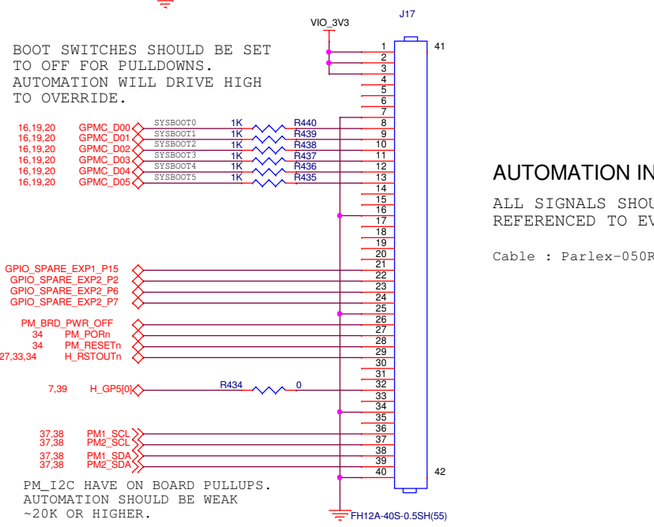
DARA Bd can be interfaced to conduct more in-depth
power measurements.

All Vdiff signal pairs (P & N) shown should be routed as
pseudo-Diff Pair segments using min trace widths since
these are low voltage sensing nets, not power delivery nets.







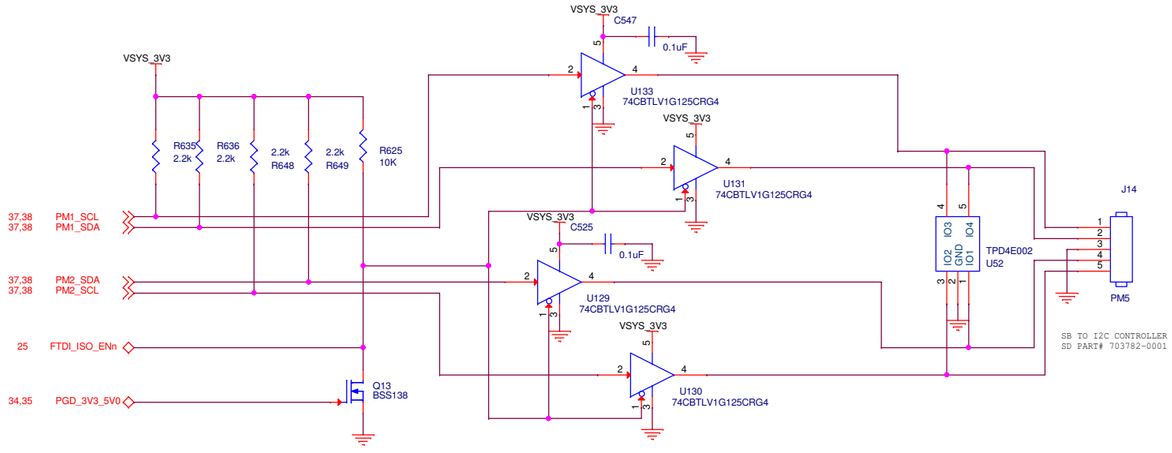


AUTOMATION INTERFACE

ALL SIGNALS SHOULD BE
REFERENCED TO EVM_3V3

Cable : Parlex-050R40-76B, .5mm 3"

EXTERNAL POWER MEASUREMENT WITH ISOLATION



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA76xP/DRA77xP/TDA2Px-ACD EVM CPU BOARD			
Page Contents: DARA/TEST			
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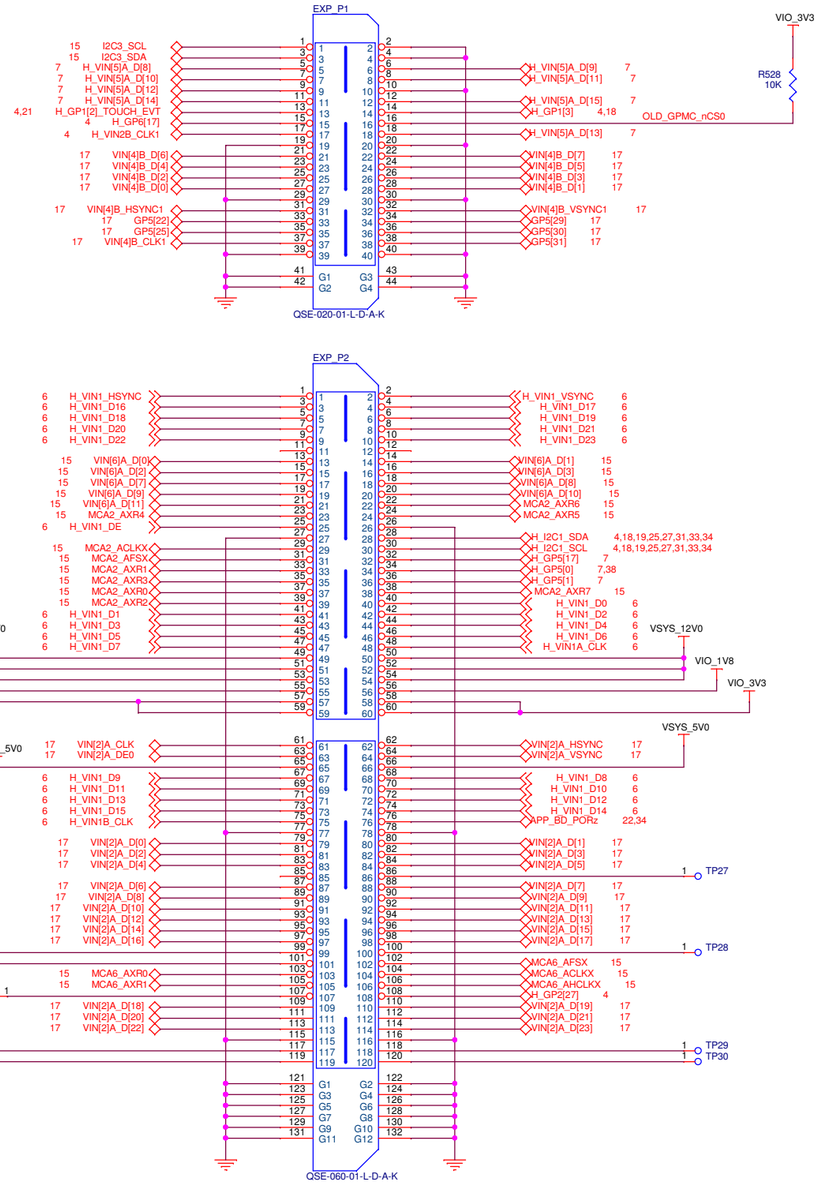
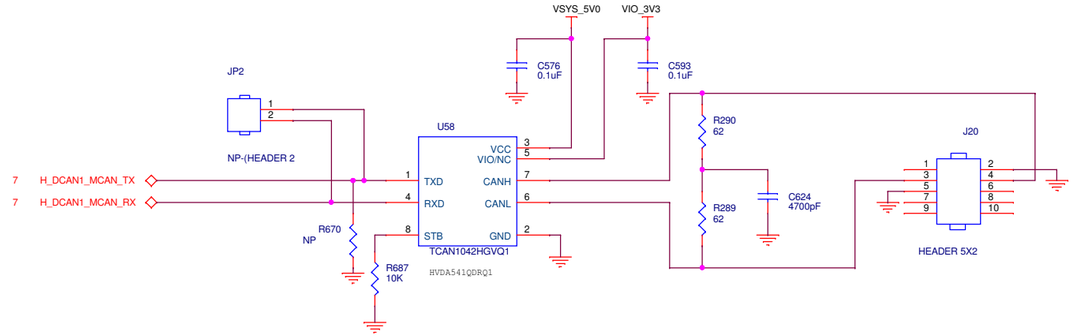
EXPANSION CARD CONNECTORS

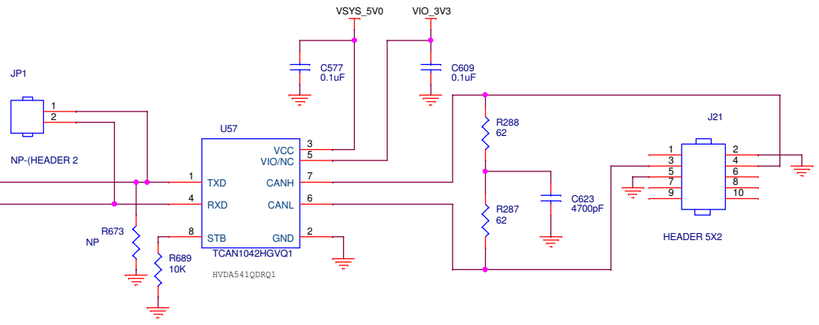


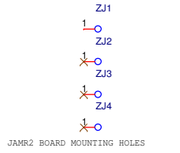
DCAN1/MCAN



DELTA VAYU H, ADD DCAN2/MCAN, DELETE VDDSHV5 WAKEUP SUPPORT.

DCAN2/MCAN





TEXAS INSTRUMENTS INCORPORATED

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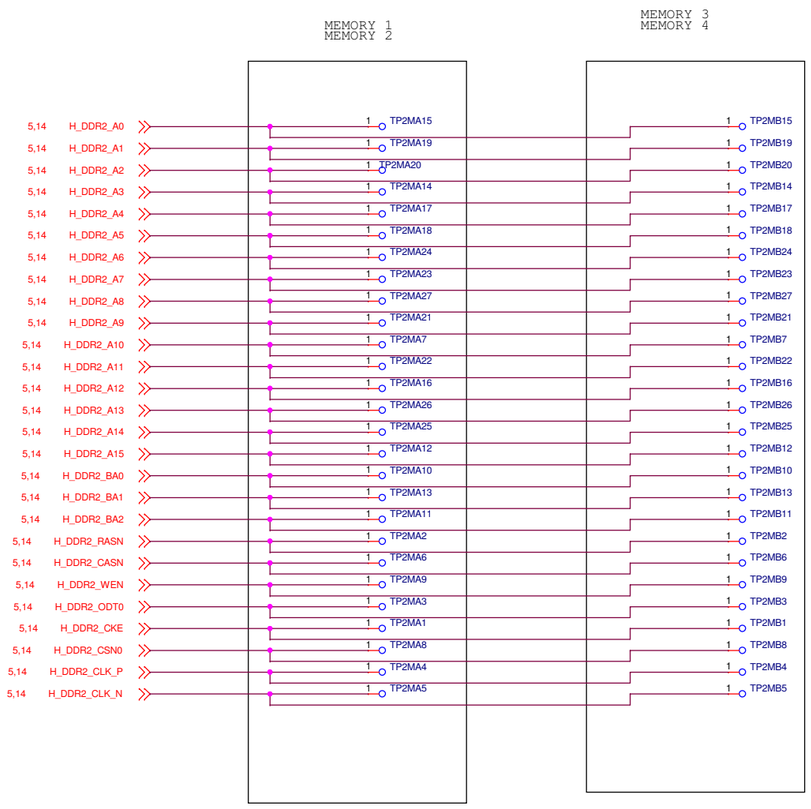
This section is an outline of vias labeled as Testpoints in the schematic. This allows us to determine pwb line lengths for memory to memory and CPU to memory it is purely a visibility tool no actual "component" is used the vias are just replaced with a via that is labeled a test point



ADAS FUSION MOUNTING AND CABLING

OPTION 1:

QTH-020-01-L-D-DP-A	**VISION REV A**
QSH-020-01-L-D-DP-A	**J6 ECO**

OPTION 2:

QSH-020-01-L-D-DP-A	**J6 PLUS**
QTH-020-01-L-D-DP-A	**VISION REV B**

OPTION 3:

QTH-020-01-L-D-DP-A	**VISION REV B**
QSH-020-01-L-D-DP-A	**J6 ECO**

SAMTEC CABLE: HQDP-020-04.00-SBL-TBR-1

NOTE THAT CABLE LENGHT GREATER THE 4 INCHES IS REQUIRED FOR J6 ECO.

TEXAS INSTRUMENTS INCORPORATED

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