Application Note

AM623, AM625, AM625SIP, AM620-Q1, AM625-Q1 Processor Family Schematic Design Guidelines and Schematic Review Checklist

ABSTRACT

The application note includes schematic design guidelines, implementation recommendations, and schematic review checklist for board designers using the AM623, AM625, AM625SIP, AM620-Q1 and AM625-Q1 processor family. This application note discusses the processor configurations, processor peripherals and the interface to attached (external) devices. Schematic review checklist at the end of each section, provides a comprehensive list of review points for each of the peripheral and guidelines section for board designers to verify the custom board.

Additionally, links are provided to processor product pages, processor related collaterals, FAQs related to processor and processor peripherals published on E2E, and some of the commonly referenced documents. The board designers can reference to the links during custom board design to minimize design errors, optimize the design efforts and optimize the timeline.

Table of Contents

Trademarks

1 Introduction

1.1 Application Note Usage Guidelines

The application note (*Schematic Design Guidelines and Schematic Review Checklist*) provides custom board design guidelines that can be used by board designers during custom board schematic design and schematic review checklist at the end of each section that can be used by board designers to review the custom board schematics.

1.1.1 Custom Board Design - Implementation References

The application note provides schematic design guidelines and schematic review checklist that can be used during custom board hardware design using the selected processor and peripherals (on-board or add-on) including memory, power, interface and other functional blocks.

Processor references to the selected processor and the attached device references to the external (on-board or add-on) peripherals that are interfaced to the processor based on the end equipment being designed and the application use case.

1.1.2 Processor Family Specific Application Note

The application note is for the AM62x family of processors covering AM623, AM625, AM625SIP, AM620-Q1, and AM625-Q1 processor families covers the custom board schematic design guidelines and schematic review checklist. The document is specific to AM62x family of processors and makes this easy-to-use for the chosen family of processors.

1.1.3 Schematic Design Guidelines

The application note provides schematic design guidelines for all the peripherals supported by AM62x processor family. Board designers can follow schematic design guidelines during the custom board schematic design. Along with the guidelines, links to FAQs have been added for use during custom board schematic design.

Schematic design guidelines can help board designers reduce the design efforts and minimize design errors that can affect functionality and performance.

1.1.4 Schematic Review Checklist

Schematic review checklist at the end of each section has been newly added to the application note. All the relevant peripheral or power sections in the application note includes checklist categorized as General, Schematic Review, and Additional. Board designers can use the checklist to do a self-review of the custom board design schematic to minimize possible errors that can cause functional or performance issues resulting in increased custom board.

Refer below FAQ for information on available checklists and format:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Schematics review checklists

1.1.5 FAQ Reference for Application Note Usage Guidelines

[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design - Custom Board Schematics Self Review

1.2 Family Wise List of Processors

The application note applies to all the processors listed in the listed below. All relevant documents are available on the product pages on TI.com. Follow the processor page link below to access the product page.

1.2.1 AM62x Processor Family

See the *Ordering and Quality* section for information on supported OPNs on the following product pages:

- *AM623*
- *AM625*
- *AM625SIP*
- *AM620-Q1*
- *AM625-Q1*

2 Related Collaterals

2.1 Links to Commonly Available and Applicable Collaterals

There are a number of documents relevant to the selected processor available on the processor-specific product page on TI.com. Before starting the custom board design, reading all the documents by the board designers is strongly recommended.

The below links summarize the collaterals that can be referred to when starting the custom board design.

[FAQ] AM625 Custom board hardware design – Collaterals to Get started

[FAQ] AM623 Custom board hardware design – Collaterals to Get started

[FAQ] AM625SIP Custom board hardware design – Collaterals to Get started

[FAQ] AM625-Q1 / AM620-Q1 Custom board hardware design – Collaterals to Get started

2.2 Hardware Design Considerations for Custom Board Design

Before start of the custom board design, the recommendation is to read through and take note of the recommendations in the processor-specific *Hardware Design Considerations for Custom Board Design* user's guide linked below:

Hardware Design Considerations for Custom Board Design Using AM623, AM625, AM625SIP, AM620-Q1, AM625-Q1 Family of Processors

3 Processor Selection

3.1 Data Sheet Use Case and Version Referenced

Processor-specific data sheet includes pin attributes (pin-to-function mapping), signal descriptions, pin connectivity requirements, electrical characteristics, timing and switching characteristics, and timing diagrams

for all the applicable processor peripherals and recommended operating conditions, power sequencing for all the processor supply rails.

List of data sheets with revision number referenced during the document update:

AM623 / AM625 / AM620-Q1 / AM625-Q1

SPRSP58B – JUNE 2022 – REVISED JUNE 2023

AM625SIP

SPRSP98A – NOVEMBER 2023 – REVISED JUNE 2024

For more information, refer to *[FAQ] AM625 / AM623 / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Current Data sheet revision, updates and usage notes*.

3.2 Processor Selection (OPN Orderable Part Number)

To get an overview of the processor architecture and for selecting the processor (base production part number), features, package (ALW / AMC / AMK) and speed grade, see the *Functional Block Diagram* and *Device Comparison* sections of the processor-specific data sheet.

Refer to *Device Comparison* section, *Device and Documentation Support* section of the processor-specific data sheet to choose the required processor OPN.

The recommendation is to update the selected processor ordering part number in the schematics with the chosen OPN.

3.3 Peripheral Instance Naming Convention

For peripherals naming and instances, the processor-specific TRM tends to be *generic* and the processor-specific data sheet is *specific*.

In the data sheet, a suffix number is assigned, even when there is a single peripheral instance. Documents that reference the peripheral name do not need to change from processor to processor.

The suffix starts with *0*. For the common platform Ethernet switch 3-port gigabit (CPSW3G) port names, port *0* is the internal (communications port programming interface (CPPI) host) port of the switch.

3.4 Unused Peripherals

Peripherals that have a dedicated function have connectivity requirements when not used. Refer to the *Pin Connectivity Requirements* section of processor-specific data sheet for connecting unused peripherals. The connectivity requirements include recommendations to connect the power supplies and the interface signals.

Peripherals (processor IOs) that have alternate functions, when not used can be left unconnected when there are no connectivity requirements specified. The pad configurations can be the reset state configuration.

For more information, refer *[FAQ] AM625 / AM623 / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Data sheet Pin Attributes and Pin connectivity related queries*

3.5 Processor Ordering and Quality

For information related to ordering and quality for the selected processor family, see the links below:

AM623-Ordering and quality

AM625-Ordering and quality

AM625SIP-Ordering and quality

AM620-Q1-Ordering and quality

AM625-Q1-Ordering and quality

3.6 Processor Selection Checklist

General

During the custom board schematic design process, review and verify the following collaterals and information:

1. Device selection (selected processor OPN (Orderable part number) based on the required features)
2. Pin attributes (Ball names, Signal names and the contents of each column including power) and pin mapping as per the data sheet
3. Pin connectivity requirements (for used and unused, peripherals)
4. Connection recommendations for RSVD (reserved) pins
5. Debug provision on-board for probing (OBSCLK and CLKOUT)
6. Errata related to the supported boot modes and the peripherals of interest
7. Recommended operating conditions, power-up and power-down sequencing for core, memory interface, analog and IO supplies
8. Electrical characteristics and timing information for selected peripherals
9. Application notes, Implementation recommendations, and Layout guidelines for selected peripherals

4 Power Architecture

For an overview, see the TI *Power management* page.

Additionally, *WEBENCH® circuit designer tool* provides a visual interface that creates customized power supply and active filter circuits.

4.1 Generating Supply Rails

The required supply rails for the selected processor are generated using integrated or discrete power architecture. Use of integrated power architecture (PMIC) simplifies design of processor-specific power architecture (power supplies). The PMIC generates commonly used supply rails to power the processor and the attached devices. Manages power-up sequencing, power-down sequencing, and supply slew rate control, and meet the processor-specific power requirements. Along with the PMIC, use additional DC/DC converters and LDOs to generate additional on-board supplies, based on the use case.

Discrete power architecture provides flexibility in design and component selection. Board designer is responsible for power device selection that sources the required current, provides the required output voltages, supports the required load transient response, controls supply slew rate, and supply sequencing.

Processor power supply rails have slew rate requirements specified. Follow the section *Power Supply Slew Rate Requirement* of processor-specific data sheet for all the generated or switched supply rails.

The recommended family of devices and related collaterals for generating the on-board supplies using different power architectures are summarized in the next sections.

4.1.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

4.1.1.1 Power Management IC (PMIC)

PMIC that can be used for integrated power architecture includes TPS65219. Space, performance, and the bill of materials (BOM) optimized power architecture are designed to power the processor and the attached devices.

The TPS65219 PMIC provides a number of output voltage (supply rails based on processor core, input voltage and memory) configurations (versions, fixed output, NVM programmed). Choose the required PMIC configuration (version) based on the design requirement. To choose the required configuration (version), see the TPS65219 product page. The *Schematic and Layout Checklist* is available for use during the custom board design.

For application note and operational details, reference the links below:

Powering the AM62x with the TPS65219 PMIC

Powering the AM625SIP with the TPS65219 PMIC

Additionally, refer to *[FAQ] AM625 / AM623 / AM625SIP / AM620-Q1 / AM625-Q1 Design Recommendations / Custom board hardware design – common queries for PMIC TPS65219*

Refer to the TPS65219 (OPNs - Example *TPS6521901 Technical Reference Manual*) for additional information.

Depending on the application and board design architecture, PMIC OPNs can be selected. Each of the OPN has a specific NVM configuration. For OPN NVM configuration TRM and the full register map, device data sheet refer TPS65219 product page.

Additionally refer Advantages of using TPS65219 PMIC to power AM62x processor family.

Advantages of Using TPS65219 PMIC to Power AM62 Processor Versus a Discrete Power Design

Refer FAQ related to residual voltage and detection:

[FAQ] AM625 / AM623 / AM62A / AM62D-Q1 / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to Residual Voltage and Detection

4.1.1.1.1 PMIC Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. PMIC selection (orderable device) based on the input supply, core voltage, IO voltage and DDR voltage configuration
3. PMIC checklist for addition of required input and output capacitors including values, feedback configuration, and pin connections
4. Voltage rating of the selected capacitors considering derating (> twice the worst-case applied voltage is a commonly used guideline)
5. Configuration of the recommended PMIC control and IO signals
6. Naming of the supply rails (indicate configured output voltage level)
7. Matching of the PMIC voltage levels with the supply requirements for the processor and attached devices
8. Net name matches (same name) for processor and attached devices IO supplies

Schematic Review

Follow the below list for the custom schematic design:

1. Compare the custom PMIC implementation with the SK schematic implementation for capacitors and values, IOs connections, and DC/DC output feedback connection
2. Processor to PMIC and PMIC to processor IO interface connections
3. Connection of the required control signals for processor IO supply sequencing (load switch EN for processor and attached device IO supply output voltage slew rate control)
4. Processor and PMIC I2C interface used versus recommend, considering the use case
5. SD card IO voltage control configuration pin connection (3.3V during processor or board reset and switched to 1.8V), verify the VSEL_SD connection based on SD card interface use case
6. PMIC nRSTOUT slew (pullup value) when connected directly to processor MCU_PORz input (recommend using a discrete push-pull output buffer)
7. Connection of interrupt, MODE/RESET, and EN/PB/VSENSE signals and connection of the required pulls for the PMIC IOs
8. Configuration of other discrete DC/DC supplies and LDOs used along with the PMIC
9. VPP supply (eFuse programming) external LDO implementation, output control and addition of bulk and decoupling capacitors considering load current transient and provision for isolation resistor for testing the VPP enable timing

Additional

1. In case power architecture is based on TI PMIC, obtain a review of the implementation done with the PMIC business unit or product line.

2. A 0Ω resistor or jumper is recommended at the output of the supply rails for isolation or current measurement for the initial board build.
3. Since the PMIC performs a warm reset, connecting the RESETSTATz output from the processor to the MODE/RESET input of PMIC can be optional. Adding a 0Ω resistor and make a DNI is recommended. An internal pull is enabled.
4. Show the PMIC input bulk capacitors connection for DC/DC inputs and VSYS separately and near to each of the pin separately for ease of placement and routing.
5. Reviewed and followed the FAQ related to residual voltage.

4.1.1.1.2 Additional References

For more information, see the following sections in the processor-specific data sheet.

- Device Connection and Layout Fundamentals
- Power Supply
- Power Supply Designs

4.1.1.2 Discrete Power

Use a discrete power architecture to generate the processor and the attached devices supply rails. Discrete power architecture is based on DC/DC converters and LDOs. Implement the power sequence using the power good output and discrete logic.

For more information on the device selection and power architecture implementation, see the *Discrete Power Solution for AM62x* application note.

When custom discrete power architecture is used, take note of the MCU_PORz (L->H) hold time (delay) (for oscillator start-up) requirements after all the supplies ramp specified in the data sheet.

MCU_PORz active (low) during power-up until the supplies are valid (using external crystal circuit) plus minimum delay of 9.5ms or MCU_PORz active (low) at power-up until the supplies are valid and external clock is stable (when using external LVCMOS clock source).

4.1.1.2.1 DC/DC Converter

Consider DC/DC converters such as the TPS62826 or LM61460-Q1 devices.

For an overview of the DC/DC converters available, see the *AC/DC & DC/DC converters (integrated FET)* page.

Additionally, refer below:

Quick Reference Guide To TI Buck Switching DC/DC Application Note

Power Supply Design training resources - Video library

4.1.1.2.2 LDO

Consider LDO devices such as TPS74518, TLV7103318, TLV75518.

For an overview of the LDOs available, see the TI *Linear and low-dropout (LDO) regulators* page.

Additionally, refer below:

Low Dropout Regulators Quick Reference Guide

Linear Regulator Design Guide For LDOs

A Topical Index of TI LDO Application Notes

4.1.1.2.3 Discrete Power Checklist

General

Review and verify the following for the custom schematic design:

1. Above section, including relevant application notes
2. The configured output voltage and the required current rating for all the supply rails
3. Output voltage feedback connection and feedback divider resistors tolerance

4. Selected discrete DC/DC architecture supports active discharge
5. DC/DC output supplies slew rate meets the processor requirements and sequencing of all the supply rails as per the processor requirement
6. MCU_PORz input (PG output) slew rate (connect through discrete push-pull output buffer) and L to H delay (MCU_PORz input low hold time) implementation after all the supplies ramp
7. Voltage rating of the selected capacitors considering derating (> twice the worst-case applied voltage is a commonly used guideline)
8. Device selection including output voltage level and current rating, active discharge capability, residual voltage detection (Allow to power-up only when the supply voltages are < 0.3V after power-down)
9. Implementation of SD card interface IO supply supporting UHS-I speed and eFuse programming VPP supply
10. Naming of the supply rails (indicate configured output voltage level)
11. Matching of the PMIC voltage levels with the supply requirements for the processor and attached devices
12. Net name matches (same name) for processor and attached devices IO supplies

Schematic Review

Follow the below list for the custom schematic design:

1. The resistor divider value including tolerance connected to the feedback input to generate the required output supply voltage matches with the calculated value
2. PG outputs have the required pullup and connects to the other DC/DC or LDO EN for supply sequencing
3. DC/DC or LDO output supply rails slew rate
4. MCU_PORz input low hold time after supplies ramp, in case the DC/DC PG output connects directly to the processor MCU_PORz input

Additional

1. In case power architecture is based on TI power, obtain a review of the implementation done with the relevant business unit or product line
2. A 0Ω resistor or jumper is recommended at the output of the supply rails for isolation or current measurement for the initial board build

4.2 Power Control and Circuit Protection

4.2.1 Load Switch (Power Switching)

Load switches are used to control (turn on and off) power to a specific peripheral or sub-system powered by the same supply rail, instead of using multiple DC/DC converters or LDOs to generate the supply. In some applications, there is a recommended power-up and power-down sequence that must be followed. Load switches simplifies the implementation of power sequencing to meet the power-up and power-down sequence requirements. The load switch enable is controlled by the PMIC or DC/DC converter PG to meet the processor power sequencing requirements.

Consider load switches such as TPS22965, TPS22918, TPS22902, and TPS22946.

For an overview of the load switches available, see the TI *load switches* page.

4.2.1.1 Load Switch Checklist

General

Review and verify the following for the custom schematic design:

1. Above section, including relevant application notes and FAQ links
2. Load switch current rating
3. Sequencing of the load switch enable (PMIC GPIO or DC/DC PG)
4. Output voltage slew rate configuration
5. Voltage rating of the selected capacitors considering derating (> twice the applied voltage is a commonly used guideline)

Schematic review

Follow the below list for the custom schematic design:

1. Input and output capacitor values and voltage rating
2. Output voltage slew rate is configured (capacitor value selection) per the processor IO supply slew rate requirements

4.2.2 eFuse IC (Power Switching and Protection)

eFuse power switching and protection ICs are integrated power path protection devices that are used to limit circuit current and voltages to a safe level during fault conditions. eFuses offer many benefits to the design and include protection features that are often difficult to implement with discrete components. For an overview of the eFuses available, see the TI *eFuses and hot swap controllers* page.

5 General Recommendations

The below general recommendations section contains the recommendations and guidelines for board designers to be familiar while designing the custom board.

5.1 Processor Performance Evaluation Module (SK - Starter Kit)

Processor (hardware) performance evaluation modules and platforms (SKs) are not reference designs, the modules and platforms do not represent a proper or complete board or system implementation. In many cases, the SKs are partially or completely designed and released for fabrication before the processor design is complete. The time line is so that a hardware platform is available when the first silicon arrives. New processor requirements come up during processor bring-up and bench validation. All the new requirements are not accounted for in the hardware evaluation platform. Therefore, TI expects board designers to carefully review and follow all requirements defined in the processor-specific data sheet, silicon errata, and TRM when designing the custom board.

Processor (hardware) performance evaluation platforms are not designed to be comprehensive of any board or system specific requirements, such as EMI or EMC purposes (reduce radiated emissions), noise susceptibility, thermal management, and so forth.

See the following FAQ for design update notes that board designers can refer along with the SK schematics:

[FAQ] AM625 / AM623 / AM62A Common design Errors / Recommendations for Custom board hardware design – SK Schematics Design Update Note.

5.1.1 Evaluation Module Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. SK referenced matches the selected processor family
3. Processor package on the referenced SK board matches with the processor selected for custom board design
4. The SK schematic revision referenced includes D-Notes, R-Notes, and CAD Notes

5.2 Processor-Specific SK Versus Data Sheet

In case of any discrepancy between the processor-specific SK and the data sheet during evaluation or the custom board design, follow the data sheet. Despite the best efforts by the board designer, the SK can contain errors that still function but are not completely aligned with the data sheet specifications.

5.2.1 Notes About Component Selection

Selection of SK components is not always optimized. Review the BOM and optimize the component selection based on the data sheet recommendations, application requirements, and board circuit design.

Design calculations, design review, and performing board level tests and measurements as required is recommended before finalizing the components value and ratings (such as voltage and power).

5.2.1.1 Series Resistor

The recommended values for the series resistors are a starting point for board designers. Verify the values on the board and adjust accordingly (step function that occurs on the pin is not near the mid-supply).

5.2.1.2 Parallel Pull Resistor

Provide provision for adding parallel pulls to the processor IOs. Parallel pull polarity and the values depend on the specific peripheral connectivity recommendations, recommendations for improved processor performance, and relevant interface or standards requirements.

Processor-specific SK pull values can be used as a starting point and board designer can select the appropriate pull values based on the recommendations for the processor and attached device, or specific board design implementation.

When traces are connected to the processor IO pads and is not being actively driven, a parallel pull is recommended. Pull polarity is design use case dependent. During reset, processor IO buffers are off and the IOs are in a high impedance state, effectively serving as an antenna that picks up noise. Without any termination, the IOs are high impedance. High impedance makes this easy for noise to couple energy on the floating signal trace and develop a potential that can exceed the recommended operating conditions, which creates an electrical over-stress (EOS) on the IOs. Electrostatic discharge (ESD) protection circuits inside the processor are designed to protect the device from handling before being installed on a PCB assembly.

5.2.1.3 Drive Strength Configuration

TI currently does not support configuring any other drive strength besides the nominal (default) value for SDIO and LVCMOS buffers, as the nominal value is the only configuration at which chip-level STA (Static Timing Analysis) is closed. The nominal value corresponds to a 40Ω for SDIO and 60Ω for LVCMOS. The IBIS model has been updated to contain only drive strengths where the timing is closed internally.

Refer below FAQ for information related to drive strength configuration support:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - I/O Drive Strength Configuration for SDIO and LVCMOS

5.2.1.4 Data Sheet Recommendations

The board designers are responsible for implementing whatever precautions are necessary or required to establish that the custom board design does not violate the requirements specified in the processor-specific data sheet. Example processor requirements include I2C Open-Drain and Fail-Safe (I2C OD FS) Electrical Characteristics - Input Slew Rate.

When data sheet recommendations are not available, use recommendations provided in the following checklist or implementation in the SK schematic as a starting point.

5.2.1.5 Processor IOs - External ESD Protection

An external ESD protection is recommended to any of the processor IOs connected directly to an external connector or exposed to external inputs, because internal ESD protection circuit were not designed to handle the board level ESD requirements. For an overview of the ESD protection devices, see the TI *ESD protection* page.

5.2.1.6 Peripheral Clock Output Series Resistors

Series resistor on the clock output near to the processor clock output pin is required to resolve issues with signal distortion at the source of the clock since the clock output is also used for retiming. For MMCx and OSPI interface an unbonded pad is used (internal),so series resistor is not a requirement. In some cases, a low value series resistor is added for signal integrity purpose. The recommendation is to have the series resistor as a place holder just in case the resistor is needed for improving signal integrity.

5.2.1.7 Component Selection Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes
2. Selection of resistor values, tolerance, size and wattage
3. Only specific resistors need 1% tolerance (refer to the processor or attached device data sheet, SK schematics, or EVMs)
4. Standard tolerance resistors can be used for other use cases, example: pullup, pulldown or series resistor
5. Compare the pull values on the custom board with the SK schematics
6. Voltage rating of the capacitors used to include derating (> twice the applied voltage is a commonly used guideline)
7. Voltage rating of capacitors considering DC bias effect (to be within the recommended value)
8. Package selection (application and use case dependent, consider voltage and temperature range)
9. Selection of compatible attached devices (DDR and flash memory, EPHY)
10. Recommended memory size, selection of required memory size (DDR) and providing provision for expanding the memory as required
11. Reviewed the FAQ related to passive components value, tolerance and voltage rating

Reference the below FAQ as a starting point for information on key components used on the EVMs and SKs, component values and tolerances:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design - Starter kit / EVM variants (versions) and Key components list

[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

5.2.2 Additional Information Regarding Reuse of SK Design

5.2.2.1 Updated SK Schematic With Design, Review and CAD Notes Added

During custom board design, designers frequently reuse the SK design files and edit the design file. Alternatively, designers reuse common implementations, including processor, memory and communication interfaces. The SK is expected to have additional functions, so designers optimize the SK implementation to fit board design requirements. While optimizing the SK schematics, errors are introduced into the custom design that cause functional, performance or reliability problems. When optimizing, designers have queries regarding the SK implementation, resulting in design errors. Many of the optimization and design errors are common across designs. Based on the multiple board designers inputs and data sheet pin connectivity recommendations, comprehensive Design Notes (D-Note), Review Notes (R-Note) and CAD Notes (CAD-Note) are added near each section of the SK schematic for designers to review and follow to minimize errors. As part of the design downloads, additional files are included to support evaluation.

The list of documents that can be download on TI.com for each of the SK is listed in the below product overview document.

5.2.2.1.1 AM625 / AM623

SK-AM62B-P1 Design Package Content Overview Product Overview

SK-AM62B Design Package Folder and Files List Product Overview

5.2.2.1.2 AM625-Q1 / AM620-Q1

SK-AM62-LP Design Package Content Overview Product Overview

5.2.2.1.3 AM625SIP

SK-AM62-SIP Design Package Folder and Files List Product Overview

5.2.2.2 SK Design Files Reuse

Based on the design approach followed during the custom board design and project schedule, the SK design files can be reused as a starting point to make the required updates. The recommendation is to verify the SK implementation and component selection.

The following link summarize the considerations board designers are required to be familiar with when reusing TI SK design files.

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design - Reusing TI SK (EVM) design files

5.2.2.2.1 Reuse of SK Design Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Latest version of the selected or required SK design is referenced
3. D-Notes and R-Notes are considered
4. Resetting of component DNIs configuration when saved as a different project or the schematic pages or circuit sections are rearranged
5. The change in connections including off-page connections when the schematics design is translated to an alternate CAD tool

5.3 Before Beginning the Design

5.3.1 Documentation

During the custom board design cycle, the recommendation is to refer to or use the latest version of the documentation, examples include the processor-specific data sheet, silicon errata, TRM, and other commonly referenced design collaterals. Verify the processor-specific product page for the latest available documents or addition of new documents.

Tips for documentation search: Search the documentation for words such as: *recommended*, *require*, *do not*, *note*, *pin connectivity*, and so forth. Important criteria for the processor typically contain one or more words.

Tips to get updated information: On a TI.com processor product page, there is a *Notifications* button. Registering at the button enables automatic notification of processor documentation changes.

5.3.2 Processor Pin Attributes (Pinout) Verification

Verify the following pin attributes

- Processor pin label corresponds to the correct pin numbers listed in the *Pin Attributes* section of the processor-specific data sheet. Maintain the data sheet names in the symbol and change the function (net) names per the application use case.
- Supply voltages that are connected to the processor power pins are within the *Recommended Operating Conditions*.
- All the processor pins (grouped into functions and having separate symbol blocks) including reserved pins are include in the schematics to minimize tool related and functional errors.
- Most of the processor IOs TX (Output) and RX (Input) buffers and pulls are turned off during reset. External pull resistors are recommended to hold inputs of any attached device in a valid logic state until software initializes the IOs when a TP or trace is connected and IOs are not being actively driven. Use of pull resistor depends on the attached device IO capabilities.
- For improved performance of custom board, recommendations include implementing external monitoring of voltage, current, or temperature.

Refer below FAQ for queries related to processor data sheet pin attributes.

[FAQ] AM625 / AM623 / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to SOC data sheet Pin Attributes

5.3.3 Device Comparison, IOSET and Voltage Conflict

Refer to the note regarding shared IO pins in the *Device Comparison* section of the processor-specific data sheet. IOSETs are a grouping of signals specific to an interface that are timed as a set. The processor is timing closed using IOSETs. Any interface that has IOSETs must select all interface signals from the same IOSET. Some interface signals can be shared over multiple IOSETs. The valid pin combinations are detailed in the SysConfig-PinMux tool.

Refer below FAQ for information on Voltage conflict and IOSET:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to SysConfig-PinMux IOSET and Voltage Conflict

5.3.4 RSVD Reserved Pins (Signals)

Pins named RSVD are Reserved. Leave the RSVD pins unconnected (no TP connected) as recommended in the data sheet.

Recommendations are to not connect any PCB trace or test points to RSVD pins.

For more information, see the *[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Connection recommendations for RSVD pins*.

5.3.5 Note on PADCONFIG Registers

Many of the processor IOs support multiplexing of functions. The IO function is chosen from multiple functions. The list of functions available for each pad is enumerated in the *SIGNAL NAME* column in the *Pin Attributes* table of the processor-specific data sheet.

The required function is selected through the MUXMODE field of the associated pad configuration register. The PADCFG_CTRL0_CFG0_PADCONFIG0 to PADCFG_CTRL0_CFG0_PADCONFIG150 registers control the signal multiplexing of IOs in the processor Main Domain and MCU_PADCFG_CTRL0_CFG0_PADCONFIG0 to MCU_PADCFG_CTRL0_CFG0_PADCONFIG33 registers control the signal multiplexing of IOs in the processor MCU Domain.

The *Pad Configuration PADCONFIG Registers* table in the *Pad Configuration Registers* section of the processor-specific TRM summarizes the Bit Field Reset Values for all the PADCONFIG registers. Follow the notes listed at the end of the table while configuring the PADCONFIG registers. Never set the RXACTIVE bit without a valid logic state sourced to the pin that is associated with the respective PADCONFIG register. A floating input can damage the processor or affect reliability.

5.3.6 Processor IO (Signal) Isolation for Fail-Safe Operation

In case the processor and the attached devices or an additional host are powered by different power sources, signal isolation is recommended because most of the processor IOs are not fail-safe. The recommendations are to route the signals through a FET bus switch circuit designed to automatically isolate the two devices anytime the IO power is not valid for both devices. The FET bus switch and control logic are recommended to be powered from an always-on power supply and only enabled by an AND function of power good signals from different power sources.

5.3.7 Reference to Processor-Specific SK

When specific recommendations are not available in the processor-specific data sheet, for implementation examples and values, see the processor-specific SK, as applicable.

5.3.8 High-Speed Interface Design Guidelines

For detailed recommendations on USB2.0 and CSI-Rx signals connection and routing, see the *High-Speed Interface Layout Guidelines*. Include appropriate constraints or routing requirements to be followed during the custom board design.

For USB interface, a common-mode choke can be added to improve the custom board performance when operating in harsh industrial environments. Adding common-mode choke can reduce the signal amplitude and degrade performance. Add provisions to bypass the common-mode choke using 0Ω resistors. Consider adding external ESD protection based on the application requirement.

5.3.9 Recommended Current Source or Sink for LVCMOS (GPIO) Outputs

The DC current outputs sourced must remain less than the maximum I_{OH} and I_{OL} values defined to achieve the V_{OL} maximum and V_{OH} minimum values defined in the respective *Electrical Characteristics* table. The recommendation is to not source or sink currents above the limits defined in the processor-specific data sheet and preferred DC current source or sink is to be significantly less that the limits as to not increase thermal or other problems.

Switching high levels of current can create electrical noise that can couple to other circuits and require additional decoupling capacitors on the respective IO power rail.

5.3.10 Connection of Slow Ramp Inputs or Capacitors to LVCMOS IOs (Inputs or Outputs)

LVCMOS inputs have slew rate requirements specified. Connecting slow ramp signal directly to the LVCMOS inputs or capacitors at the LVCMOS inputs is not recommended. When a slow ramp input is applied, CMOS input has shoot-through current that flow from VDD through the partially turned on P-channel transistor and the partially turned on N-channel transistor to VSS, when the input is at mid-supply. Accumulated exposure to slow ramps results in performance or reliability concerns.

LVCMOS output buffers are not designed to drive large capacitive loads. When LVCMOS type IOs are configured as output and connected to capacitor, follow the data sheet recommendations for the allowed capacitor value or add series resistor to limit the IO output current or perform simulations.

5.3.11 Queries and Clarifications Related to Processor During Custom Board Design

For queries and clarifications related to processor selection, features and guidelines, TI recommends using the *E2E* forum. Use E2E to ask questions or refer to related questions and previous answers.

5.3.12 Before Beginning the Design Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Processor schematics symbol used on custom board schematic follows the ball name, pin numbers and IOSET grouping recommendations for specific peripherals per the corresponding processor data sheet *Pin Attributes* section
3. The required IO functions and PAD configuration are considered
4. Fail-safe operation and loading requirements for processor IOs are considered
5. Buffering of the processor IOs(outputs) based on the use case - to drive higher load
6. Latest version of the selected SK design is referenced

Additional

1. Refer to the relevant collaterals on TI.com to minimize design errors and optimize design efforts
2. Frequently check for the latest revision on TI.com for documents of interest
3. Use E2E to seek clarification

5.3.13 Device Recommendations

TI does not make device recommendations.

The recommendation is to follow the *DDR Electrical Characteristics* section of the data sheet for selection of DDR4/LPDDR4 memory.

The MMCSD host controller and PHY associated with the MMC0 are designed in compliance with the standard, as described in the data sheet and TRM.

The recommendation is to follow the *MMC0 - eMMC/SD/SDIO Interface* section of the data sheet when selecting the eMMC/SD card.

Reference *[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design - Starter kit / EVM variants (versions) and Key components list* as a starting point for key components used on the EVMs and SKs.

6 Processor-Specific Recommendations

6.1 Common (Processor Start-Up) Connection

6.1.1 Power Supply

Follow the recommendations listed below:

- The power requirement for each of the supply rail varies based on the interfaces used and the operating environment.
- The current draw of processor supply rails is estimated using the *Power Estimation Tool (PET)*. If the supply rail powers the other on-board attached (peripheral) devices, include the maximum current draw of the devices.
- For power supply sizing and information on the maximum current rating for different supply rails, see the *AM62x Maximum Current Ratings*. Check the relevant processor product page for availability of updated document.
- Verify the output current ratings of the selected power architecture (including PMIC, DC/DC converters and LDOs) meet the maximum current requirements of processor and all attached devices. Add additional margins for design variances.
- Verify the recommended power supply sequence (power-up and power-down) is followed. For the recommended power sequencing requirements, refer to the *Power Supply Sequencing* section of processor-specific data sheet.

For processor *Recommended Operating Conditions (ROC)*, see the *[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – SOC ROC Recommended Operating Condition*.

Here are some guidelines that needs to be considered when selecting or designing the processor power architecture:

1. Power supplies are configured to the required voltage level and are supplies are within the ROC
2. Power architecture follows the power-up and power-down sequence as specified in the processor data sheet
3. Power architecture meets the supply slew rate requirements specified in the processor data sheet
4. All the power supplies are available before the MCU_PORz is released
5. Monitoring of all the supply rails. Make sure the supplies are enabled only after the voltages are below 0.3V (no residual voltage) after a power cycle
6. The delay between the power supply ramp and the MCU_PORz high is as per the data sheet recommendations (9.5ms min)
7. MCU_PORz input slew is as minimum as possible to avoid internal reset circuit glitch

Refer FAQ related to residual voltage and detection:

[FAQ] AM625 / AM623 / AM62A / AM62D-Q1 / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to Residual Voltage and Detection

6.1.1.1 Supply for Core and Peripherals

For proper operation, connect all power pins (balls) with the supply voltages recommended in the *Recommended Operating Conditions* section of the processor-specific data sheet. Power pins that have specific connectivity requirements are specified in the *Pin Connectivity Requirements* section of the processor-specific data sheet.

Note

Powering the MCU domain and the Main domain independently is not an option. The processor family does not have separate MCU and Main power domains. All power rails need to be powered and sequenced as defined in the processor-specific data sheet. The concept of MCU and Main applies to internal device functions and processor domains.

6.1.1.1.1 Power Supply Ramp (Slew Rate) Requirement and Dynamic Voltage Scaling / Change

All power supplies associated with the processor must allow for controlled supply ramp (supply slew rate). For more information, see the *Power Supply Slew Rate Requirements* section of the processor-specific data sheet.

The processor (family) does not support dynamic voltage scaling.

See *[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – Dynamic Voltage Scaling* for more information about dynamic voltage scaling (DVS) and dynamic frequency scaling (DFS).

6.1.1.1.2 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

Core supplies VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 (available on the AMC package) are recommended to be powered from the same power source and are operated at 0.75V or 0.85V (valid operating ranges defined in the *Recommended Operating Conditions (ROC)* table). When supplies are operating at 0.75V, the recommendation is to ramp 0.75V before all 0.85V supplies.

VDDR_CORE is specified to operate only at 0.85V. When VDD_CORE is operating at 0.85V, VDD_CORE and VDDR_CORE are recommended to be powered from the same source (ramp together).

The recommendation is to always connect the VDDS_OSC0 and VDDA_MCU supplies.

The processor includes multiple analog supply pins that provide power to sensitive analog circuitry like VDDA_MCU, VDDA_PLLx [x = 0-2], VDDA_1P8_CSIRX0, VDDA_1P8_OLDI0 and VDDA_1P8_USB. Filtered ferrite power supplies are recommended.

For more information, see the *Recommended Operating Conditions* and *Power Supply Sequencing* sections of the processor-specific data sheet.

6.1.1.1.3 Additional Information

For more information on processor power-sequencing requirements, see *[FAQ] AM625 / AM623 Custom board hardware design – Processor power-sequencing requirements for power-up and power-down*

For more information on processor power supply rails filtering using ferrite, see *[FAQ] AM625 / AM623 Custom board hardware design – Ferrite (power supply filter) recommendations for SoC supply rails*

The FAQs are generic and can also be used for AM625SIP / AM625-Q1 / AM620-Q1 processor family.

6.1.1.1.4 Processor Core and Peripheral Core Power Supply Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description, and electrical specifications
3. Recommended voltages are applied to the core VDD power supply rails 0.75V or 0.85V
4. Refer *Power-Up Sequencing – Supply / Signal Assignments* section of the processor-specific data sheet for sequencing the core supplies when partial IO low power mode is used and when partial IO low power mode is not used.
5. The potential applied to VDDR_CORE must never exceed the potential applied to VDD_CORE +0.18V during power-up or power-down. The sequencing requires VDD_CORE to ramp up before VDDR_CORE and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V
6. Power VDD_CORE and VDDR_CORE from the same source to ramp together when the VDD_CORE is operating at 0.85V
7. Connection of core supply when specific peripheral is not used as per pin connectivity requirements
8. Connection of core supply (CSIRX0), when a specific peripheral is unused but the boundary scan function is required, as per pin connectivity requirements

Schematic Review

Follow the below list for the custom schematic design:

1. Compare the implementation of the bulk and decoupling capacitors for all the supplies rails with SK schematics
2. Ferrite filters are provided for peripheral core supplies (CSI, USB, CANUART) as per the SK schematics
3. When peripherals are unused but the boundary scan function is required, ferrites and bulk capacitors are optional for peripheral core supplies

4. Supply rails connected follow the ROC

Additional

1. For all supply rails, place a 0Ω resistor or jumper for isolation or current measurement at the output of the supply rails
2. Changing the core voltage is not allowed after the device is released from reset. If the core supply is turned off, turn off and ramp down all power rails per the power-down sequence and wait until all supply rails decay below 300mV before turning on power again
3. When the USB driver is not initialized and the USB calibration procedure does not happen, connecting the supplies and leaving all of the USB pins for USB0, USB1, or both is acceptable. Grounding the USB supplies per pin connectivity requirements when both USB interfaces are unused saves power when low power is a critical requirement
4. Follow the processor-specific SK for implementation of ferrites and capacitors
5. Dynamic voltage scaling (DVS) of the core supplies is not supported (not allowed or recommended)

6.1.1.1.5 Peripheral Analog Power Supply Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description and electrical specifications
3. Recommended voltages are applied to the peripheral analog power supply rail 1.8V
4. Supply rail connections are based on the processor family

   AM62x: VDDA_MCU, VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_CSIRX0, VDDA_1P8_OLDI0, VDDA_1P8_USB, VDDA_TEMP0, VDDA_TEMP1, VMON_1P8_SOC
5. Supply rail VDDA_3P3_USB 3.3V analog supply connection for supporting USB2.0 interface
6. Connection of peripheral analog supply when specific peripheral is not used as per pin connectivity requirements
7. Connection of peripheral analog supply (CSIRX0), when specific peripheral is unused but boundary scan function is required as per pin connectivity requirements

Schematic Review

Follow the below list for the custom schematic design:

1. Compare bulk and decoupling capacitor for all the supplies rails with SK schematics
2. Ferrite filters are provided for peripheral analog supplies (CSI, PLL, USB (1.8V), MCU), as per the SK schematics
3. When specific peripherals are not used and boundary scan function is required, ferrites and bulk capacitors are optional
4. Supply rails are connected and follow the ROC

Additional

1. For all supply rails, use 0Ω resistor or jumper for isolation or current measurements at the output of the supply rails
2. When the USB driver is not initialized and the USB calibration procedure does not happen, connecting the supplies and leaving all of the USB pins for USB0, USB1, or both is acceptable. Grounding the USB supplies per pin connectivity requirements when both USB interfaces are unused saves power when low power is a critical requirement
3. Follow the processor-specific SK for implementation of ferrites and capacitors
4. Dynamic voltage scaling (DVS) of the analog supplies is not supported (not allowed or recommended)

6.1.1.2 Supply for IO Groups

[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – CAP_VDDSn CAP_VDDS provides recommendations on CAP_VDDSn, capacitor value, and the effect of the capacitor mounted or shorted status.

6.1.1.2.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

The processor includes nine dual-voltage IO supply for IO groups (VDDSHVx [x = 0-6]), IO supply for IO CANUART (VDDSHV_CANUART) and IO supply for IO MCU (VDDSHV_MCU), where each domain provides power supply to a fixed set of IOs. Each IO group is configured for 3.3V or 1.8V independently, which determines a common operating voltage for the entire set of IOs powered by the respective IO group power supply.

Processor pads (pins) designated as CAP_VDDSn [n = 0-6], CAP_VDDS_CANUART, and CAP_VDDS_MCU connect the external capacitor to the internal IO supply for IO group regulator when the IO groups connect to 3.3V supply (optional when IO groups supplies connect to 1.8V). A 1µF (connected between CAP_VDDSn pins and VSS, see the processor-specific data sheet) capacitor is recommended. See the processor-specific data sheet for the recommended capacitor voltage rating and allowed capacitance range. When IO groups are connected to 3.3V, the steady state DC output, which is the voltage applied to VDDSHVx/2, is the voltage considered for capacitor DC bias effect derating.

To minimize loop inductance requirements, place the capacitors on the back side of the PCB in the array of the BGA. Choice of capacitor voltage rating influences the capacitor package and size selection.

Select capacitor with ESR < 1Ω, keep the trace loop inductance < 2.5nH.

6.1.1.2.2 Additional Information

Most of the processor IOs are not fail-safe. For information on fail-safe IOs, see the processor-specific data sheet. Power the IO supply of attached devices from the same power source as the respective processor dual-voltage IO supply for IO groups (VDDSHVx supply rail) to verify that the board never applies potential to an IO that is not powered. Taking care of fail-safe operation is recommended to protect the IOs of processor and attached devices.

For more information on power-sequencing requirements between processor and attached devices including signal isolation for fail-safe operation, see *[FAQ] AM625 / AM623 Custom board hardware design – Power sequencing between SOC (Processor) and the Attached devices*. The FAQ is generic and can also be used for AM625SIP / AM625-Q1 / AM620-Q1 processor family.

Note

Verify that a valid supply voltage for the VDDSHVx is present before applying inputs to the associated processor IOs or peripherals.

Connect the VDDSHVx supplies and associated CAP_VDDSn (when IO supply connected is 3.3V, optional for 1.8V) capacitor irrespective of the usage of the processor IOs or peripherals.

6.1.1.2.3 Supply for IO Groups Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description, and electrical specifications
3. Electrical characteristics and additional available information
4. A valid fixed supply source is connected to (VDDSHV_CANUART, VDDSHV_MCU, VDDSHV0, VDDSHV1, VDDSHV2, VDDSHV3) all the IO supply for IO groups as per the ROC
5. A valid supply (that can be dynamically changed) source is connected to VDDSHV4, VDDSHV5, VDDSHV6 IO supply for IO groups as per the ROC
6. Slew rate requirements for IO supply rails are followed
7. Internal LDO output pins have the recommended capacitors connected (across CAP_VDDSn pin and VSS)

8. Power sequence recommendations as per the processor data sheet are followed

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of the recommended capacitor to CAP_VDDSn pins and VSS
2. CAP_VDDSn capacitor package (use the smallest possible (0201 or greater package possible which is closest to 0201) package to minimize loop inductance)
3. Voltage rating of the capacitor selected for the capacitance value to be in the range 0.8 to 1.5µF including aging, temperature and DC bias effect
4. All IO supply rails have a valid supply irrespective of the use of the IOs
5. Supply rails connected follow the ROC
6. Each CAP_VDDSn pin requires a separate 1µF capacitor connected with respect to VSS (ground)
7. Select CAP_VDDSn capacitor with < 1Ω ESR, keep the trace loop inductance < 2.5nH

Additional

1. For all supply rails, use a 0Ω resistor or jumper for isolation or current measurement at the output of the supply rails.
2. When any of the VDDSHVx power rails are sourced from the 3.3V supply, all IOs referenced to the VDDSHVx must operate at 3.3V IO level. If a VDDSHVx power rail is sourced from a 1.8V supply, all IOs referenced to the VDDSHVx must operate at 1.8V IO level.
3. Some interfaces span multiple VDDSHVx, for example MMC2 and GPMC. When using one of the interfaces, all VDDSHVx domains supporting a specific interface must share the same voltage source.
4. Most processor IOs are not fail-safe. Applying input voltage to the IOs while the corresponding VDDSHVx supply is off is not allowed or recommended.
5. Verify all IO pins on each VDDSHVx (or VDDSHV_MCU) only connects to a single voltage level.
6. Follow the processor-specific SK for implementation of ferrites and capacitors.
7. Leaving VDDSHV5 rail unconnected is not recommended. Connect the power pins to either 1.8V or 3.3V, depending on the use case.

6.1.1.3 Supply for VPP (eFuse ROM Programming)

An important requirement is for the processor VPP (eFuse ROM programming supply) to remain within the ROC range during eFuse programming. An LDO powered from a higher input voltage supply (2.5V or 3.3V) is recommended to compensate for the voltage drop through the series pass transistor and maintain the correct operating voltage during high load current transients. Local bulk capacitors are recommended near the processor VPP pin to support the LDO transient response.

Powering VPP from a supply rail with a ±5% variation, or using a load switch or FET can be problematic due to high load current transients and the requirement for the VPP power rail to match the supply range. Load switch or FET topology does not account for the voltage drop going through the load switch. The load switch can be an option if the board designer uses power source with smaller variation, such that the supply variation combined with the voltage drop through the load switch never exceeds the VPP recommended operating range.

For more information, see *[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application*.

6.1.1.3.1 VPP Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description and electrical specifications
3. Electrical characteristics and additional available information
4. Implementation of on-board supply or provision provided to connect external supply
5. An LDO is recommended (use of FET switch or load switch is not allowed or recommended)

6. Choose on-board LDO that supports a minimum of 400mA current, has excellent load current transient response, and quick output discharge (active discharge)
7. Required bulk and bypass capacitors are provided (follow SK schematics)
8. On-board LDO has provision to be enabled by processor IO
9. When external supply is connected, add bulk and decoupling capacitor provision on the processor board near to the processor VPP pin and provided a TP to connect the external supply
10. External supply follows the recommended power sequence and slew rate requirements as per the data sheet
11. The external supply timing is controlled by the processor IO
12. Leave the processor VPP supply pin floating (HiZ) or grounded during power-up sequences, power-down sequences, and normal device operation

Schematic Review

Follow the below list for the custom schematic design:

1. A dedicated LDO or PMIC output is used
2. Nominal voltage connected to VPP is 1.8V and supports current requirements as per data sheet requirements
3. Selected LDO specifications including load current transient response is similar to the LDO used on the SK schematics
4. Processor IO is used to control the EN of the LDO and the required pull is provided
5. Verify the if EN pull holds the LDO is in off-state during power cycling
6. When an adjustable LDO is used, verify the output voltage configuration, output voltage slew and use of over voltage protection
7. A series resistor is provided to isolate the processor VPP supply from the LDO output for testing the timing or LDO output
8. Supply rail connected follows the processor ROC

Additional

1. Always provide provision on the processor board to connect VPP supply (on-board or external supply).
2. Select an LDO with fast transient response and connect LDO output to the processor VPP pin with a low loop inductance path to source the high transient load current, where the VPP pin never drops below the minimum operating voltage.
3. Enable the VPP only during eFuse programming. Connecting the VPP supply to a continuous 1.8V supply rail is not a allowed or recommended or supported option.
4. Due to the transient load current requirement during eFuse programming, using load switch or FET switch is not a recommended approach. A load switch or FET switch is likely to have too much voltage drop that is not compensated when using an LDO.
5. If the use case requires use of load switch or FET switch, characterize the board by measuring the voltage on the processor VPP pin during programming and verify supply never drops below the ROC minimum limit. Several variables in the path of VPP can cause the supply to be out of the ROC when using load switch or FET and must be without characterized before implementing. Check or test if the load switch or FET switch violates the maximum VPP supply slew rate limit of 6000V per second defined in the data sheet.

6.1.1.4 Supply Connection for Partial IO (Low-Power) Mode Configuration

6.1.1.4.1 Partial IO Used

The recommendation is to connect VDD_CANUART and VDDSHV_CANUART to always-on power sources.

VDD_CANUART operates at 0.75V or 0.85V, there is no voltage dependency to the VDD_CORE during normal operation. The only voltage dependency is during power-up and power-down sequencing.

For partial IO low power mode implementation, refer *[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1 Custom board hardware design – Partial IO LPM support*.

6.1.1.4.2 Partial IO Unused

Connect VDD_CANUART to the same power source as VDD_CORE. Connect VDDSHV_CANUART to any valid IO power source.

6.1.1.4.3 Data Sheet Reference for Power Sequence

See the notes related to partial IO in the *Power-Up Sequencing*, *Power-Down Sequencing* and *Partial IO Power Sequencing* sections of the processor-specific data sheet.

6.1.1.4.4 Partial IO (Low-Power) Mode Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description and electrical specifications
3. Connect VDD_CANUART and VDDSHV_CANUART to an always-on power source when implementing Partial IO low power mode
4. Connect VDDSHV_CANUART to a valid IO power source Partial IO low power mode is not implemented
5. Connect VDD_CANUART to the same power source as VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 when Partial IO low power mode is not implemented
6. When VDD_CANUART is connected to an always-on power source, never apply a potential to VDD_CORE which is greater than the potential applied to VDD_CANUART + 0.18V during power-up or power-down. Partial IO low power mode requires VDD_CANUART to ramp up before and ramp down after VDD_CORE

Schematic Review

Follow the below list for the custom schematic design:

1. VDDSHV_CANUART and VDD_CANUART supplies are available before the other processor supplies are available when partial IO mode is implemented
2. VDDSHV_CANUART and VDD_CANUART follow the recommended power sequence when partial IO mode is not used
3. Voltage levels connected to VDDSHV_CANUART and VDD_CANUART
4. Verify the connected supply rails follow the ROC

Additional

1. Verify the IO level compatibility between the processor IO and the attached device (wakeup source)

6.1.1.5 Additional Information

Placement of 0Ω resistor (shunt) or a jumper in line with the core supply and other supply rails are recommended for initial PCB prototype builds. Placement of 0Ω resistor (shunt) or a jumper can help during board bring-up and debug to isolate the supply or for current measurement. Shunt resistors are used to measure the supply rail currents in SK.

Verify the effect of adding 0Ω resistor provisions on the custom board performance.

6.1.2 Capacitors for Supply Rails

6.1.2.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

Perform a PDN analysis, verifying that the required number of decoupling and bulk capacitors are provided for all power supply rails, including dual-voltage IO supply for IO group supply rails.

Place the decoupling capacitors as close as possible to the supply pins. Larger bulk capacitors can be placed further away.

Use low-ESL capacitors and mount the capacitors with the shortest possible traces to keep the mounting inductance low. For more information, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

Use the bulk and decoupling capacitors values from the SK as a reference when PDN analysis is not performed or results are not available. For filtered (ferrite) power supplies implementation, follow the processor-specific SK.

6.1.2.2 Additional Information

6.1.2.2.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

When the processor peripherals (Camera Serial interface (CSIRX0), DDR Subsystem (DDRSS0) and USB2.0 (USB0 and USB1)) are not used, the supplies (core, analog) associated with the peripherals have specific connectivity requirements. For more information, see the *Pin Connectivity Requirements* section of the processor-specific data sheet. Power supply filter (ferrite) and capacitors (bulk) can be optimized.

6.1.2.3 Capacitors for Supply Rails Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description and electrical specifications
3. Use of low ESL capacitors and 3-terminal capacitors connected with short traces to minimize the board loop inductance
4. Voltage rating of the capacitors used (> twice the worst-case applied voltage is a commonly used guideline)

Schematic Review

Follow the below list for the custom schematic design:

1. Compare the capacitors used for all the supply rails with SK schematics
2. Verify each of the power rail pins have a decoupling capacitor and each of the supply rail group has a bulk capacitor

Additional

1. Power supply decoupling is adequate. All processor power rails use both bulk and high frequency decoupling capacitors. The critical power domains that require the most attentions are the low voltage, high current domains (VDD_CORE, VDDR_CORE)
2. As a starting point, the recommendation is to follow the validated SK decoupling strategy
3. Deviations are not recommended without performing static and dynamic PDN analysis to verify that the Reff, Cap LL, and Impedance targets are met
4. In some situations, the SK uses 3-terminal capacitors, due to low inductance packaging and performance. Make sure the 3-terminal capacitors connections in the SK schematics are not implemented as an in-line or filter component
5. Show the connections of the capacitor near to the relevant pin for ease of placement and routing

6.1.3 Processor Clock

6.1.3.1 Clock Inputs

6.1.3.1.1 High Frequency Oscillator (MCU_OSC0_XI / MCU_OSC0_XO)

For the operation of the processor, select a crystal as the clock source or a 1.8V LVCMOS square-wave digital clock source.

A 25MHz external crystal connected to the internal high frequency oscillator (MCU_HFOSC0) is the clock source for the internal reference clock HFOSC0_CLKOUT.

Placed the discrete components used to implement the crystal oscillator circuit as close as possible to the MCU_OSC0_XI and MCU_OSC0_XO pins. For the crystal, follow the *MCU_OSC0 Crystal Circuit Requirements* table of the processor-specific data sheet when choosing the load capacitors.

When a 1.8V LVCMOS square-wave digital clock source is used, connect the processor XO pin according to the processor-specific data sheet recommendation.

For information on clock selection, refer to *[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding Crystal selection*.

Refer to *[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding MCU_OSC0 Start-up Time*.

Note

25MHz is the only crystal frequency that is currently supported. See the processor-specific data sheet for more details on the recommended crystal parameters.

The next revision of the data sheet includes LVCMOS clock requirements as part of the *MCU_OSC0 LVCMOS Digital Clock Source* section. Refer *Section 3.1* of the application note.

AM62Px processor data sheet as a reference for LVCMOS clock requirements, refer *MCU_OSC0 LVCMOS Digital Clock Source*, *MCU_OSC0 LVCMOS Digital Clock Source Requirements* section of the data sheet.

6.1.3.1.2 Low Frequency Oscillator (WKUP_LFOSC0_XI / WKUP_LFOSC0_XO)

WKUP_LFOSC0 has limited use cases and is optional. Based on the use case, select a 32.768kHz crystal as the clock source or a 1.8V LVCMOS square-wave digital clock source.

For more information, see the *[FAQ] AM625: LFOSC usage in the device*. The FAQ is generic and can also be used for AM623 / AM625SIP / AM625-Q1 / AM620-Q1 processor family.

Place all discrete components used to implement the oscillator circuit as close as possible to the WKUP_LFOSC0_XI and WKUP_LFOSC0_XO pins. For the crystal, the load capacitance selected is required to be in the range recommended in the *WKUP_LFOSC0 Crystal Electrical Characteristics* table of the processor-specific data sheet.

If WKUP_LFOSC0_XI / WKUP_LFOSC0_XO is not used, recommended is to connect the XI directly to the VSS and to leave the XO unconnected.

For more information on connecting the unused WKUP_LFOSC0, see the *WKUP_LFOSC0 Not Used* section of the processor-specific data sheet.

6.1.3.1.3 EXT_REFCLK1 (External Clock Input to Main Domain)

EXT_REFCLK1 pin is routed to clock multiplexers as a selectable input clock source to the Timer modules (DMTIMER/WDT), DMTIMER in Security Subsystem (SMS), MCAN, and CPTS (Time Stamping Module). The EXT_REFCLK1 is an option for when an application requires a specific clock frequency to be fed to the timer modules. An example of the application is time synchronization or for clock quality reasons.

When EXT_REFCLK1 is used as a clock source, depending on the availability of external clock, a pulldown is required.

6.1.3.1.4 Additional Information

MCU_OSC0_XI / MCU_OSC0_XO has specific routing requirements. See the *Clock Routing Guidelines* section of the *AM62Ax Sitara™ Processors data sheet*. The clock routing guidelines are same for AM62x processor family and processor-specific data sheet will be updated in the next revision to include these guidelines.

6.1.3.1.5 Clock Input Checklist - MCU_OSC0

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description, and electrical specifications
3. Electrical characteristics, timing parameters and any additional available information

4. Selection of processor clock input source, either crystal or oscillator
5. 25MHz is the clock input frequency currently supported, refer processor-specific data sheet for supported clock input frequency
6. Selection of crystal load capacitor versus data sheet recommendations
7. PCB capacitance for MCU_OSC0 is included in the calculation of crystal load capacitance value
8. When oscillator is used, add a decoupling capacitor and bulk capacitor near to the oscillator supply pin

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of 25MHz MCU_OSC0 clock is mandatory
2. Connections of the crystal circuit (MCU_OSC0), as per the data sheet recommendations
3. Direct connection of crystal without series or parallel resistor
4. Selection of crystal load and load capacitance including around 4pF board capacitance
5. Load capacitor is recommended to be twice the crystal load, including board capacitance
6. Connection of XO when external oscillator is used, ground XO

Additional

1. Refer to the *Applications, Implementation, and Layout* section of the data sheet for clock routing guidelines
2. Select crystal and load capacitor such that the load capacitor value can be a standard value
3. Connect the 25MHz crystal directly to the processor XI and XO pins, no series or parallel resistors are recommended. The internal oscillator implements Automatic Gain Control (AGC) for amplitude control
4. The processor is validated only with a 25MHz (only frequency currently supported) clock source.
5. Processor-specific data sheet shows that MCU_OSC0 does not start until the core voltage ramps because there are some cases where the oscillator does not start until the VDD_CORE ramps. In most cases the oscillator start when VDDS_OSC0 ramps, although oscillator start when VDDS_OSC0 ramps is not always the case. The oscillator start-up diagram in the data sheet shows the maximum start-up time, which includes the case where the delay is based on VDD_CORE is valid
6. Recommendation is to retain the HFOSC0 registers in the default state
7. Refer processor-specific data sheet to select the crystal circuit components

6.1.3.1.6 Clock Input Checklist - WKUP_LFOSC0

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description, and electrical specifications
3. Electrical characteristics, timing parameters, and any additional available information
4. Selection of WKUP clock input source - crystal or oscillator
5. 32.768kHz is the WKUP clock input frequency supported, refer to the processor-specific data sheet for supported clock input frequency
6. Selection of the crystal load versus data sheet recommendations
7. Selection of load capacitor versus data sheet recommendations
8. WKUP_LFOSC0 has limited use cases, provide provisions to ground the XI input when the clock option is not used

Schematic Review

Follow the below for the custom schematic design:

1. Connections of the clock circuit (WKUP_LFOSC0), as per the data sheet recommendations
2. Selection of crystal load and load capacitance, with the load capacitance being twice the crystal load
3. Connection of the clock circuit when external oscillator is used (XO is grounded)
4. Connection of the XI input when the WKUP_LFOSC0 is unused (XI is grounded)

Additional

1. Crystal load capacitance versus LFOSC0 registers. The only LFOSC0 register bits board designers change are BP_C, PD_C, and CTRLMMR_WKUP_LFXOSC_TRIM[18:16], where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source. The CTRLMMR_WKUP_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the *Load Capacitance Equation*.
2. Refer to the processor-specific data sheet for the recommended circuit configuration during preproduction PCB and the production PCB

6.1.3.2 Clock Outputs

Processor IOs (pins) named CLKOUT0 and WKUP_CLKOUT0 can be configured as clock outputs. The clock outputs can be used as clock source for the attached devices (external peripherals).

WKUP_CLKOUT0 is a buffered output of the high frequency oscillator (HFOSC0) available after reset for the AM62x processor family.

6.1.3.2.1 Clock Output Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description, and electrical specifications
3. Connection of WKUP_CLKOUT0, 25MHz output is available at the output after reset

Schematic Review

Follow the list below for the custom schematic design:

1. Connection of the clock output to single or multiple loads. When connected to multiple inputs (loads), each of the inputs are recommended to be connected through a buffer
2. Required pulls are provided near to the attached device clock input

Additional

1. CLKOUT0: EXT_REFCLK1 is used as CLKOUT0. Always connect a clock signal point-to-point, without any branches. When connecting CLKOUT0 to multiple clock inputs, use a buffer (with one input and multiple outputs or individual buffers based on the use case)

6.1.4 Processor Reset

6.1.4.1 External Reset Inputs

MCU_PORz is the external MCU and Main Domain cold reset input to the processor. The recommendation is to hold the MCU_PORz pulled low during the supply ramp and oscillator start-up. Follow the recommended MCU_PORz timing in the *Power-Up Sequencing* diagram of the processor-specific data sheet.

For the MCU_PORz (3.3V tolerant, fail-safe input), applying a 3.3V input is acceptable. The input thresholds are a function of the 1.8V IO supply voltage (VDDS_OSC0).

Slow rising reset signal causes internal processor reset circuit to glitch. Use a fast rise time discrete push-pull output buffer as MCU_PORz input and add a capacitor (22pF) filter provision.

When PMIC is used, connect the output through push-pull output type logic gate or discrete buffer (with fast rise time) as an MCU_PORz input, rather than a slow rising open-drain output (can glitch the internal reset circuit).

Provision to connect a filter capacitor at the MCU_PORz input is recommended. The capacitor value and mounting is use-case dependent. Verify the capacitor value does not cause the LVCMOS input to violate the slew rate requirements or glitch internally due to slow ramp.

Not connecting a valid input to MCU_PORz is not a recommended use case and can cause unpredictable and random behavior. Due to the device not going through a valid reset, internal circuits are in random (undefined) states.

Connect external warm reset inputs MCU_RESETz and RESET_REQz as per the *Pin Connectivity Requirements* section of the processor-specific data sheet. Warm reset inputs (LVCMOS inputs) have input slew rate requirements specified. Connecting a capacitor directly at the input is not recommended due to the slow ramp input. A schmitt trigger-based debouncing circuit is recommended. For implementing the debouncing logic, see the processor-specific SK schematic.

Usage note for MCU_RESETz

Refer to the silicon errata advisory i2407- RESET. MCU_RESETSTATz is unreliable when MCU_RESETz is asserted low

6.1.4.2 Reset Status Outputs

PORz_OUT is the main domain POR (cold reset) status output, RESETSTATz is the main domain warm reset status output, and MCU_RESETSTATz is the MCU domain warm reset status output.

When reset status outputs PORz_OUT, MCU_RESETSTATz and RESETSTATz are used to drive the attached device reset inputs (/reset), pulldowns are recommended for reset status outputs to assert the reset (hold the attached devices in reset) to the attached devices during power-up and reset.

Note

An external pulldown holds the attached device reset inputs low, in use cases where none of the attached devices have internal pullups. In cases where an attached device has an internal pullup, the reset signal is pulled to a mid-supply voltage. Verify specific use-case and add pulldown on the reset status outputs.

RESETSTATz can be used to reset on-board memories or peripherals with reset functionality (eMMC, OSPI, or EPHY) or SD card power switch. The PORz_OUT can be used to latch the hardware strap configurations during reset including latching the Ethernet PHY strap configurations.

Connect the reset status outputs to a test point for testing or future enhancements when not used. Optionally a pulldown can be provided and be a DNI.

Note

MCU_RESETz and MCU_RESETSTATz have specific use case recommendations. Refer to the advisory i2407 of the processor-specific silicon errata.

6.1.4.3 Additional Information

The BOOTMODE00..15 inputs that are used to configure the processor boot mode need to be held in a known state to select the appropriate boot mode configuration as defined in the processor-specific TRM, until the boot mode configuration is latched during the rising edge of the PORz_OUT.

6.1.4.4 Processor Reset Input Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description, and electrical specifications
3. Electrical characteristics, timing parameters, and any additional available information
4. The processor is required to restart (release reset) only after the voltages are below 0.3V after power-down
5. Reset input is asserted (low) while the processor supplies are ramping up or ramping down
6. MCU_PORz (POR) input is 3.3V tolerant and fail-safe. The threshold follows the VDDS_OSC0 IO level

7. IO level of warm reset for MCU and main domains RESET_REQz (VDDSHV0), MCU_RESETz (VDDSHV_MCU) matches the IO supply for IO group supply (1.8V or 3.3V)
8. Reset inputs follow the slew rate requirements (FS RESET, LVCMOS)
9. Slew rate when open-drain output is connected (connecting through discrete push-pull output is recommended) directly to the reset input
10. Follow reset requirements including slew rate and MCU_PORz hold time when a non-TI power architecture is used

Schematic Review

Follow the below list for the custom schematic design:

1. Cold and warm reset inputs slew rate requirements are considered
2. Cold reset input (MCU_PORz) deassertion hold time (MCU_PORz input delay after all the supplies ramp, 9.5ms minimum) after all supplies ramps are provided as per the data sheet requirement
3. Provision for filter capacitor is provided at the input of the reset inputs (add 22pF (place holder) capacitor as a filter option and DNI)
4. Connection of reset inputs when not used as per pin connectivity requirements
5. Connection of push button warm reset inputs through debouncing circuit (Schmitt trigger buffer output based)

Additional

1. MCU_PORz input has slew rate requirements specified. When connecting PMIC_POWERGOOD (open-drain output) to MCU_PORz is the only available option, adjust the pullup to optimize the rise time (< 200ns)
2. MCU_PORz is a fail-safe input and 3.3V tolerant
3. Connect the output from a discrete push-pull output buffer (fast rise time) as MCU_PORz input rather than slow rising open-drain output
4. Not connecting a valid MCU_PORz causes unpredictable and random behavior, since processor does not get a valid reset input and the internal circuits are in random states. Slow ramp reset input causes internal processor reset circuit to glitch
5. LVCMOS inputs have slew rate requirements specified. A schmitt trigger based debouncing circuit is recommended for the slow ramp push button RC connected to the processor warm reset inputs. Schmitt trigger based debouncing circuit is recommended when using a push button or an RC reset
6. Provision for external ESD protection for manual reset input added near to the reset signal
7. Fail-safe operation when connected to external reset inputs. Applying an external input before supply ramps causes voltage feed and affects the processor performance
8. Reviewed MCU_RESETz related errata

6.1.4.5 Processor Reset Status Output Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal descriptions, and electrical specifications
3. Electrical characteristics, timing parameters, and any additional available information
4. PORz_OUT is used as input to latch the processor boot mode configuration or attached device strap configuration during reset
5. RESETSTATz output is used for resetting the attached devices that requires a reset when the processor undergoes any type of global reset (cold or warm).
6. IO level compatibility between the processor reset status output and attached device reset input (can cause residual voltage affecting performance)
7. Loading of the reset status output (capacitor > 22pF (place holder) connected directly to the output)
8. Reviewed MCU_RESETSTATz related errata

Schematic Review

Follow the below list for the custom schematic design:

1. RESETSTATz, MCU_RESETSTATz, and PORz_OUT have pulldown to hold the attached devices in reset during supply ramp and reset.
2. Connection of capacitor directly on the reset output near to the reset input of the attached device (capacitor > 22pF). Perform simulation to use higher value capacitor

Additional

1. External ESD protection for the reset status outputs when connected to carrier board or external connector

6.1.5 Configuration of Boot Modes (for Processor)

Boot mode inputs do not have internal pullup or pulldown resistors that are active during processor reset. The recommendation is to connect external pullups or pulldowns to set the required boot mode.

When dip switches are used, use a resistor divider ratio of 470Ω (pullup) and 47kΩ (pulldown) for improved noise performance.

When the boot mode is configured using only resistors, a standard resistor (same value for pullup and pulldown) value. As an example a 10kΩ or similar resistor can be used since either the pullup or pulldown is populated.

The recommendation is to connect pullup or pulldowns to boot mode pins marked as Reserved or not used.

BOOTMODE 14 and BOOTMODE 15 pins are Reserved for AM62x processor family.

Add provision for pullup and pulldown for all the boot mode pins that have configuration capability for debugging, design flexibility, and future enhancement. Populate either pullup or pulldown for each boot mode pins. Direct connection of boot mode pins to ground or IO supply rail is not recommended or allowed since IOs have alternate configuration and, intentionally or unintentionally, are configured as output by the software.

Consider that the boot mode input pins are not fail-safe when boot mode configurations are driven from an external input or a base board.

Based on the application requirement, a buffer that is driven only when reset (MCU_PORz) is asserted (low) is used to present the boot configuration to the processor.

If the boot mode pins are configured as an output during normal operation, a series resistor (approximately 1kΩ) is recommended at the output of the buffers. For more information, see the processor-specific SK for implementation.

6.1.5.1 Processor Boot Mode Inputs Isolation Buffers Use Case and Optimization

In the SK, the boot mode pins BOOTMODE [15:00] are asserted through two isolation buffers. The buffers make sure that the SYSBOOT pulls (boot mode configured using resistors) control the IO level of the signals when the boot mode signals are latched (around the PORz_OUT rising edge) by the processor. Since boot mode signals are used for other functions after processor boot and are connected to attached devices or peripherals. The boot mode configuration resistors are isolated from other connected peripherals so that the other connected peripherals do not conflict with the intended boot mode configuration (IO levels).

The buffers are enabled when PORz_OUT is driven low by the processor. Once PORz_OUT is asserted, the buffer outputs are Hi-Z so the signals are not pulled or influenced by the boot mode resistors.

For optimizing the design (including BOM), the buffers can be optimized or deleted depending on the use case. The boot mode pull resistors value are selectable so that the resistors do not affect the operation of attach devices.

6.1.5.2 Boot Mode Selection

For configuring the required processor boot mode, refer to the *ROM Code Boot Modes* table in the *Initialization* chapter of the processor-specific TRM.

6.1.5.2.1 Notes for USB Boot Mode

USB0 interface supports USB DFU boot mode. When the USB0 is configured for device firmware upgrade (DFU) boot mode. Permanent or switched 3.3V supply is not recommended to connect directly to the USB0_VBUS pin. Connecting a permanent supply is not recommended (equivalent to the divider value) to the USB0_VBUS pin since connection of supply without resistor divider violate fail-safe operation.

A 5V supply from the host (switched) connected through the USB connector is recommended to connect to USB0_VBUS pin through the resistor voltage divider, as per the processor-specific data sheet recommendations. The zener diode can be deleted and the two resistors can combined to a 20kΩ resistor for the *USB VBUS Detect Voltage Divider, Clamp Circuit* if the custom board design does not apply a VBUS potential > 5.5V, and the supply is on-board.

6.1.5.3 Boot Mode Implementation Approaches

Below FAQs captures the boot mode implementation approach when boot mode buffers are used and unused.

[FAQ] AM625 / AM623 / AM644x / AM243x / AM62A / AM62P - Bootmode implementation with buffers

[FAQ] AM625 / AM623 / AM644x / AM243x / AM62A / AM62P - Bootmode implementation without buffers

6.1.5.4 Additional Information

When external inputs drive the boot mode configuration, the recommendation is to stabilize the boot mode configuration inputs before the processor MCU_PORz (cold reset) is released.

When using an Ethernet boot and a Reduced Gigabit Media Independent Interface (RGMII), implement an EPHY into the design that starts RGMII_ID mode on the EPHY RX data path and disables RGMII_ID mode on the TDn data path (the processor implements RGMII_ID on the TDn outputs). Processor ROM does not enable or disable RGMII_ID mode on attached EPHYs programmatically. Typically, RGMII_ID setting is accomplished via pin strapping on the EPHY.

Select a EPHY with the capability to set the RGMII internal delay through a pin strap, see the processor-specific SK. For more information, see the advisory *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS)* of the processor-specific silicon errata.

6.1.5.5 Configuration of Boot Modes (for Processor) Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description, and electrical specifications
3. Electrical characteristics and any additional available information
4. All BOOTMODE pins have external pulls or a circuit to drive the required boot mode. Leaving any of the boot mode inputs unconnected is not recommended or allowed
5. Connecting the boot mode inputs directly to supply or VSS is not recommended. Shorting of multiple boot mode inputs together and connecting a common resistor is not recommended. (Board designers can have problems with the firmware configuration, where the LVCMOS GPIOs that are intended as inputs are mistakenly configured as outputs, driving a logic high signal instead of remaining in a high-impedance state)
6. Boot mode inputs are connected to the processor using resistor divider or through buffers as per the SK implementation
7. Boot mode configuration using dip switches or resistors. When only resistors are used, a resistor divider is optional. A pullup or pulldown can be used
8. IO compatibility (1.8V or 3.3V referenced to VDDSHV3, boot mode inputs are not fail-safe)
9. The boot mode inputs are stable before cold reset status output is pulled high
10. Boot mode pins connected to alternate functions through 0Ω for isolation or testing

Schematic Review

Follow the below list for the custom schematic design:

1. Use a common resistor value (10kΩ or similar) when dip switch is not used for boot mode configuration
2. Use 470Ω and 47kΩ resistors when dip switches are used to configure the boot
3. Series resistor 1kΩ is used at the output of the buffer when boot mode is implemented with buffers or driven by external control signals
4. Boot mode configuration for PLL clock, primary and secondary boot

Additional

1. BOOTMODE pins do not have internal pullup or pulldown resistors that are active during power reset.
2. For early designs, recommend that all boot mode pins are brought out to an optional PU/PD pair with pop and no-pop options, depending on the required boot mode. See processor-specific TRM for complete boot mode definitions.
3. Boot values are latched at the release of power-on reset. If the boot mode pins are reconfigured for alternate function during operation, boot mode pins must be released/set back to the proper configuration to select the boot mode whenever the device enters the power-on reset state. Boot mode configuration specifically is a concern if signal is driven from external peripheral.
4. Add external ESD protection in case the boot mode switches are configured in an uncontrolled environment.
5. Boot mode inputs are not fail-safe. No input can be applied before the processor IO supplies ramp. Applying an external input before supply ramps can cause voltage feed and can affect the custom board functions.
6. Boot mode buffers are optional and are provided on the SK for test automation
7. When using buffers or logic gates to configure the boot mode, verify the device used has OE (output enable feature).

6.2 Board Debug Using JTAG and EMU

6.2.1 JTAG and EMU Used

The recommendation is to connect the JTAG (TDI, TCK, TMS and TRSTn) and EMU (EMU0 and EMU1) signals as per the *Pin Connectivity Requirements* section of the processor-specific data sheet.

Optionally, connect a series resistor (22Ω) on the TDO (close to processor) signal for matching buffer impedance. The recommendation is to add external ESD protection for all JTAG and EMU signals when the signals interface to external connector. EMU 0/1 signals support boot sequence debug after cold reset (MCU_PORz).

Pullup for TDO is optional and depends on the debugger used.

Refer to the *On-Chip Debug* chapter of the processor-specific TRM.

For more information, see the below FAQs:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1/ AM6442 / AM2432 Custom board hardware design – JTAG

[FAQ] AM625: JTAG Pulldown/Pullup

6.2.2 JTAG and EMU Not Used

For connecting the JTAG and EMU signals, refer to the *Pin Connectivity Requirements* section of the processor-specific data sheet.

During custom board design, TI recommends provisioning at least a minimal JTAG port including EMU0/1 connected to test points or a header footprint to support early prototype debugging. JTAG components can be DNI in the production version of the board. Also, provide provision to add recommended pulls per the *Pin Connectivity Requirements* section, and external ESD protection.

6.2.3 Additional Information

Buffering of clock and signals are recommended whenever the JTAG interface connects to more than one attached device. Buffering of clock is recommended even for single device implementations. For implementation, see the processor-specific SK.

If trace operation is used, connect TRC_DATAn signals directly to the emulation connector. All TRC_DATAn signals are pin-MUXed with other signals. Use either trace functionality or a GPMC interface. Short and skew matched connections (board trace) for TRC_DATAn signals are used for trace functionality. The trace signals are referenced to VDDSHV3, and can be at a different supply voltage from the other JTAG signals. For additional recommendations on TRC/EMU design and layout, see the *Emulation and Trace Headers Technical Reference Manual*. A summary is available in the *XDS Target Connection Guide*.

If boundary scan is used, connect EMU0 and EMU1 pins directly to the JTAG connector.

For proper implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual* and the *XDS Target Connection Guide*.

6.2.4 Board Debug Using JTAG and EMU Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal descriptions, and electrical specifications
3. Electrical characteristics, timing parameters, and any additional available information
4. JTAG signals IO compatibility (IO supply referenced to VDDSHV_MCU)
5. Connection of the required pulls as per the pin connectivity requirements near to the processor JTAG pins

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of supply voltage to the JTAG connector including filter capacitor (connect the voltage source that connects to VDDSHV_MCU)
2. Pullup and pulldown values (use 47kΩ or 10kΩ)

Additional

1. TI recommends that all custom board designs contain at least a minimal JTAG port connection to test points or header for early prototype debugging. The minimum connections are TCK, TMS, TDI, TDO and TRSTn. If desired, delete JTAG routes and component footprints (except the pulldown on TRSTn and the pullups on TMS and TCK) in the production version of the board
2. Provision to configure EMU0 and EMU1 signals is recommended
3. If trace operation is needed, the TRC_DATAn signals must connect to the emulation connector. All TRC_DATAn signals are pin-muxed with other signals. If the trace connections are needed, do not use other muxed interfaces on the pins. Use short and shew matched routes for TRC_DATAn signals. Trace signals are on a separate power domain and can be at a different voltage from the other JTAG signals
4. Provision for external ESD protection. Populate when JTAG interface is used
5. Verify fail-safe operation when connected to external signals. Applying an external input before supply ramps can cause voltage feed and can affect the custom board functions

7 Processor Peripherals

7.1 Supply Connections for IO Groups

7.1.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

Each dual-voltage IO supply for IO group (VDDSHVx [x = 0-6], VDDSHV_MCU and VDDSHV_CANUART) provides power supply to a fixed set of IOs (peripherals). Connect either 3.3V or 1.8V supply voltage to each of the dual-voltage IO supply for IO group.

VDDSHV4, VDDSHV5, and VDDSHV6 are designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. Dynamic voltage change capability is required to support UHS-I SD cards.

SDIO or LVCMOS type IO buffers are implemented for processor IOs. The IO supply requirements depends on the IO buffer type.

Based on the selected memory type (DDR4 or LPDDR4), DDR PHY IO supply and DDR clock IO supply as per the ROC are connected.

For AM625SIP additionally SDRAM IO supply and SDRAM Core supply to power the integrated LPDDR4 supplies are required to be connected to the processor pins assigned as supply pins.

7.1.2 Supply Connections for IO Groups Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin connectivity requirements, pin attributes, and signal description
3. Standards referenced in the electrical characteristics including recommended operating conditions and any additional available information
4. IO buffer type implemented and the allowed supply configuration (LVCMOS fixed (1.8V/3.3V) or SDIO dynamic voltage change)
5. Connection of valid supply to all the IO supply for IO groups (VDDSHVx, VDDSHV_MCU, and VDDSHV_CANUART)
6. Sequencing of the IO supply
7. 3.3V IO supply connection
8. Connection of processor DDRSS IO supplies (PHY IO and Clock IO) based on the selected memory

Schematic Review

Follow the below list for the custom schematic design:

1. Attached device IO supply and the IO supply for IO group referenced by the interface signals are connected to the same supply source
2. Pullups are connected to the same supply rail that is connected to the processor VDDSHVx and attached device
3. Connecting the 3.3V supply connected to the PMIC input directly to the IO supply for IO groups VDDSHVx is not recommended since the IO supply is available for an undefined time in case the PMIC does not start-up and generate the other processor supply rails

Additional

1. Note the power sequencing requirements based on the IO supply rail voltage level used
2. Dynamic voltage change are supported by some specific IO supply for IO groups (VDDSHV4, VDDSHV5 and VDDSHV6)
3. Dynamic voltage change of the IO supply for IO groups referenced to LVCMOS IO buffers are not recommended or allowed (VDDSHV0-3, VDDSHV_MCU, VDDSHV_CANUART)
4. AM625SIP has power pins assigned for the Memory IO and Memory Core supplies. These supplies are required to be connected

7.2 Memory Interface (DDRSS (DDR4/LPDDR4), MMCSD (eMMC/SD/SDIO), OSPI/QSPI and GPMC)

7.2.1 DDR Subsystem (DDRSS)

See the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – DDR4 / LPDDR4 MEMORY Interface

7.2.1.1 DDR4 SDRAM (Double Data Rate 4 Synchronous Dynamic Random-Access Memory)

7.2.1.1.1 AM625 / AM623 / AM625-Q1 / AM620-Q1

For implementation guidelines and routing topologies, see the *AM62x DDR Board Design and Layout Guidelines*.

7.2.1.1.1.1 Memory Interface Configuration

The allowed memory configurations are 1 × 16-bit or 2 × 8-bit.

1 × 8-bit memory configuration is not a valid configuration.

Verify connection of DDRSS Bank Groups (DDR0_BG0, DDR0_BG1) based on the selected memory size.

Verify the connection of DDRSS Chip Selects (DDR0_CS0_n, DDR0_CS1_n) based on memory selection (Single-Rank or Dual-Rank).

7.2.1.1.1.2 Routing Topology and Terminations

When one memory (DDR4) device (1 × 16-bit) is used, consider point-to-point topology.

Summary of point-to-point topology implementation:
- External VTT terminations for address and control signals are optional (not required).
- For differential clock DDR0_CK0, DDR0_CK0_n, AC differential termination 2 × R in series (value = Zo − Single-ended impedance) and a filter capacitor 0.01µF or value recommended by the memory manufacturer connected to the center of two resistors and DDR PHY IO supply VDDS_DDR is recommended.
- VREFCA (VDDS_DDR/2) is the reference voltage used for control, command, and address inputs to the memory (DDR4) devices. VREFCA is derived from VDDS_DDR using a resistor divider (two resistors (recommended resistor value is 1kΩ, 1%) connected to VDDS_DDR and VSS) with filter capacitor (recommended value is 0.1µF) connected in parallel to both the resistors. An additional decoupling capacitor is connected to the VREFCA pin (close to memory (DDR4) device).

Alternatively, VTT terminations on the address and control signal for one memory (DDR4) device and Sink or Source DDR Termination Regulator to generate the VTT supply can be used.

When two memory (DDR4) devices (2 × 8-bit) are used, the recommendation is to follow the Fly-by topology.

Summary of Fly-by topology implementation:
- External terminations (VTT) for address, control, and clock signals are recommended.
- Sink or Source DDR Termination Regulator is recommended to generate the VTT supply.
- The Sink or Source DDR Termination Regulator generates the reference voltage VREFCA (VDDS_DDR/2).
- Add decoupling capacitors for the reference voltage.

7.2.1.1.1.3 Resistors for Control and Calibration

Connect pulldown for DDR0_RESET0_n (DDR_RESET#) and DDR0_CKE0 (optionally DDR_CKE), and pullup for DDR0_ALERT_n (DDR_ALERTn) close to the memory (DDR4) device. Provide pulldown for DDR4 device test enabled (TEN) close to the memory (DDR4) device. For implementation and resistor value, see the processor-specific SK.

Connect recommended resistors for DDR0_CAL0 (close to processor) and ZQn (n = 0-1, close to memory (DDR4) device).

7.2.1.1.1.4 Capacitors for the Power Supply Rails

Verify adequate bulk and decoupling capacitors are provided for the processor DDR supply rails and memory (DDR4) device supply rails.

Follow the processor-specific SK implementation whenever recommendations are not available.

7.2.1.1.1.5 Data Bit or Byte Swapping

If bit swapping is required during custom board design, bit swaps within a data byte, and swapping of byte 0 / 1 are allowed, with some restrictions. Do not swap the DM and DQS bits with any other signals. Bit swapping of the address or control bits is not allowed.

For more information, see the *Bit Swapping* section in the *DDR4 Board Design and Layout Guidance* chapter of the *AM62x DDR Board Design and Layout Guidelines*.

Update the schematics with the bit swapping changes for future reference or reuse.

7.2.1.1.1.6 VTT Termination Schematics Reference

When two memory (DDR4) devices (2 × 8-bit) are used, each device is connected to each data byte. The address signals or control signals are connected in Fly-by topology with VTT termination.

Refer to *AM64x evaluation module for Sitara processors* for implementing VTT termination.

The recommendation is to perform board-level simulations to verify signal integrity.

7.2.1.1.1.7 DDR4 Implementation Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description, and electrical specifications
3. Electrical characteristics, timing parameters, and any additional available information
4. Connection of address, clock, control and data signals, follow the processor-specific DDR design guidelines
5. Routing topology based on number of memory devices connected (data bus topology is always point-to-point). 1 x 16 (point-to-point) and 2 x 8 (daisy) are the allowed configurations
6. Connection of signals based on the selected memory size (CS0-1, BG0-1)
7. Differential clock termination using 2 x resistors and filter capacitor for point-to-point and daisy chain memory interface configuration
8. DDR0_CAL0, DDRSS IO pad calibration resistor (240Ω, 1%) connected to VSS
9. Resistor divider configuration (1kΩ, 1%) for DDR reference generation DDR_VREFCA. Place decoupling capacitor 0.1µF across the resistor divider and near to the memory pin
10. Termination (VTT) of address and control signals when x 2 memory device are used (optional for point-to-point connection)
11. VTT resistor and capacitor (1 for every 2 VTT resistors) quantity and values - follow EVM and design guide
12. VTT termination LDO implementation and configuration for when x 2 memory devices are used
13. ZQ0..1, Memory device IO calibration resistor (240Ω, 1%) connected to VSS
14. Connection of alert (10kΩ pullup) and TEN (1kΩ pulldown)
15. Connection of ODT from DDRSS to memory device - external pull is optional
16. Connection of processor DDRSS RESETn signal directly to DDR_RESETn memory reset input. To hold the signal low during power-on initialization, add pulldown (10kΩ) near the memory device
17. Connection of unused DDRSS interface signals as per pin connectivity requirements
18. DDR design guidelines for swapping of the data group signals
19. Connection of required DDRSS signals for memory expansion

Schematic Review

Follow the below list for the custom schematic design:

1. Compare the bulk and decoupling capacitors used and the values with SK schematics
2. Value and tolerance used for the calibration resistors
3. Value of the VTT resistors and capacitors
4. DDR reference voltage divider value and tolerance
5. Reset pulldown value and connection of alert, TEN pulls
6. Memory selected confirms to the JEDEC standards
7. Supply rails connected follow the ROC

Additional

1. Refer TMDS64EVM for implementing VTT terminations for DDR4 address and control signals and LDO for generating VTT supply
2. Add layout notes on the schematic (for DDR routing to follow the recommended guidelines)

7.2.1.1.2 AM625SIP

Not Applicable. The DDRSS0 pins are reassigned due to integrated LPDDR4 and have connection recommendations recommended in the *Pin Attributes and Signal Descriptions* section of the processor-specific data sheet (*AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*).

7.2.1.2 LPDDR4 SDRAM (Low-Power Double Data Rate 4 Synchronous Dynamic Random-Access Memory)

7.2.1.2.1 AM625 / AM623 / AM625-Q1 / AM620-Q1

For implementation guidelines and routing topology, see the *AM62x DDR Board Design and Layout Guidelines*.

7.2.1.2.1.1 Memory Interface Configuration

The allowed memory configuration is 1 × 16-bit.

7.2.1.2.1.2 Routing Topology and Terminations

Follow point-to-point topology for clock (CK), address, control (ADDR_CTRL) and data signals.

VTT termination does not apply for LPDDR4. Terminations required for address and control signals are handled internally (on-die).

7.2.1.2.1.3 Resistors for Control and Calibration

Connect a pulldown for DDR0_RESET0_n (LPDDR4_RESET_N) close to memory (LPDDR4) device. For implementation and resistor value, see the processor-specific SK.

Connect recommended resistors for DDR0_CAL0 (close to processor), ODT_CA_A (close to memory (LPDDR4) device) and ZQ (close to memory (LPDDR4) device).

7.2.1.2.1.4 Capacitors for the Power Supply Rails

Verify adequate bulk and decoupling capacitors are provided for the processor DDR supply rails and memory (LPDDR4) device supply rails.

Follow the processor-specific SK implementation whenever recommendations are not available.

7.2.1.2.1.5 Data Bit or Byte Swapping

During custom board design in case bit swapping is required, bit swaps within a data byte, and swapping of byte 0/1 are allowed. Address or control bit swapping is not allowed.

The recommendation is to update the schematics with the bit swapping changes for future reference or reuse.

7.2.1.2.1.6 LPDDR4 Implementation Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes, signal description, and electrical specifications
3. Electrical characteristics, timing parameters, and any additional available information
4. Connection of address, clock, control and data signals - follow the processor-specific DDR design guidelines
5. DDR0_CAL0 and DDRSS IO pad calibration resistor (240Ω, 1%) connected to VSS
6. ZQ0..1, Memory device IO calibration resistor (240Ω, 1%) connected to VDD_LPDDR4
7. Memory device on-die termination (ODT) pulled up through a resistor (2.2kΩ or similar, no connection from DDRSS)
8. Connection of chip select CSn0..1
9. For LPDDR4, x 16 is the supported data bus width
10. Connection of DDRSS RESETn signal directly to LPDDR4_RESET_N memory reset input. To hold the signal low during power-on initialization, add a pulldown (10kΩ) and placed near the memory device
11. Connection of DDRSS to 16-bit memory device - refer DDR design guide
12. Termination of unused DDRSS interface signals as per DDR design guide

Schematic Review

Follow the below list for the custom schematic design:

1. Compare the bulk and decoupling capacitors used and the values with SK schematics
2. Value and tolerance used for the calibration resistors
3. Reset pulldown value and connection of ODT pullup
4. Memory selected confirms to the JEDEC standards
5. Supply rails connected follow the ROC

Additional

1. Add layout notes on the schematic (for DDR routing to follow the recommended guidelines)

7.2.1.2.2 AM625SIP

LPDDR4 memory is integrated internally within the AM625SIP processor. The DDSSS0 pins are reassigned to provided the required power supplies and external calibration resistor (DDR_ZQ).

For connecting the power supplies and the calibration resistor including the value, tolerance and resistor supply connection, see the processor-specific data sheet (*AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*).

AM625SIP is a System In Package (SIP) derivative of the ALW packaged AM6254 device, with the addition of an integrated LPDDR4 SDRAM. *AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM* document only defines differences or exceptions to the ALW packaged *AM6254 device defined in AM62x Sitara Processors Data sheet* (revision B or later).

7.2.1.2.2.1 AM625SIP LPDDR4 Connection Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes (including Reassigned DDRSS0 Pins on the AMK Package), signal description, and electrical specifications
3. Electrical characteristics, timing parameters, and any additional available information
4. Connection of VDDS_MEM_1P1 (SDRAM IO supply) and VDDS_MEM_1P8 (SDRAM Core supply) supplies
5. Connection of bulk and decoupling capacitors for VDDS_MEM_1P1 and VDDS_MEM_1P8
6. DDR_ZQ (SDRAM Calibration Reference) Memory device IO calibration resistor (240Ω, 1%) connected to VDD_DDR (VDDS_MEM_1P1)
7. DDR0_CAL0 DDRSS IO pad calibration resistor (240Ω, 1%) connected to VSS
8. To hold the reset signal low during power-on initialization, connection of pulldown directly to DDR0_RESET0_N reset input pin

Schematic Review

Follow the below list for the custom schematic design:

1. Compare the bulk and decoupling capacitors used and the values with SK schematics
2. Value and tolerance used for the calibration resistors
3. Reset pulldown value (add a pulldown (10kΩ) and placed near the reset input pin DDR0_RESET0_N)
4. Supply rails connected follow the ROC (process and LPDDR4 memory)

Additional

1. Note the Recommended Operating Conditions including Operating junction temperature range
2. Refer to processor-specific data sheet for LPDDR4 SDRAM data sheet
3. AM625SIP is a System In Package (SIP) derivative of the ALW packaged AM6254 device, with the addition of an integrated LPDDR4 SDRAM. *AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM* document only defines differences or exceptions to the ALW packaged AM6254 device defined in *AM62x Sitara Processors Data sheet* (revision B or later)

7.2.2 Multi-Media Card/Secure Digital (MMCSD)

The processor supports three MMCSD instances. The MMCSD Host Controller provides an interface to 1 × eMMC (8-bit) and 2 × SD/SDIO (4-bit) instances.

7.2.2.1 MMC0 - eMMC (Embedded Multi-Media Card) Interface

See the following FAQs:

[FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – eMMC MEMORY Interface

[FAQ] AM62A7: MMC0 Pull Resistor Requirements

7.2.2.1.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

For more information, see the *MMC0 - eMMC/SD/SDIO Interface* section of the processor-specific data sheet.

7.2.2.1.1.1 IO Power Supply

The processor IOs used for MMC0 interface are powered by VDDSHV4 supply rail (IO supply for IO group 4).

VDDSHV4 is designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails.

The recommendation is to connect VDDSHV4 and the IO supply rail of the attached device to the same supply source.

VDD (core voltage) of the attached device can be powered from an independent supply source.

7.2.2.1.1.2 eMMC (Attached Device) Reset

The recommendation is to implement the attached device reset using a 2-input ANDing logic. Processor general purpose input/output (GPIO) is connected as one of the input to the AND gate with provision for pullup (to support boot) near to the input and 0Ω to isolate the GPIO for testing or debug. The other AND gate input is the main domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and processor main domain warm reset status output (RESETSTATz) is used to reset the attached device, match the IO voltage level of the attached device and RESETSTATz. A level translator is recommended to match the IO voltage level.

7.2.2.1.1.3 Signals Connection

Make the following connections with the attached device

- Add a series resistor 0Ω for MMC0_CLK signal as close to the processor as possible to dampen the reflections (MMC0_CLK signal is used/looped back internally on read transactions, and the series resistor is needed to eliminates possible signal reflections, which can cause false clock transitions. Use series resistor value of 0Ω initially and adjust to match the PCB trace impedance as required)
  - Connect an external pulldown for MMC0_CLK signal (close to eMMC device). (To prevent the eMMC device inputs from floating until software initializes the host controller and processor IOs associated with MMC0 and the clock is stopped or paused in a low logic and the pulldown option is consistent with the logic state)
- Connect the external pullup for the data line MMC0_DAT0 close to eMMC device (To prevent the eMMC device inputs from floating until software initializes the host controller and processor IOs).
  - Provision for external pullups is optional for DAT1-7. (The eMMC device (as long as the eMMC device is compliant to the eMMC standard) has the pullups enabled for data signals MMC0_DAT1-7. The eMMC device turns off the MMC0_DAT1-3 pulls when entering 4-bit mode and MMC0_DAT1-7 pulls when entering 8-bit mode. The eMMC host software turns on the respective DAT pulls when the software changes the mode)
- Connect the pullup (10kΩ or 47kΩ) for MMC0_CMD signal and pulldown with test point (optional) for DS signal (close to eMMC device)

7.2.2.1.1.4 Capacitors for the Power Supply Rails

Verify the required bulk and decoupling capacitors are provided for VDDSHV4 supply rail and the attached device (core and IO supplies).

Follow the processor-specific SK implementation whenever recommendations are not available.

7.2.2.1.1.5 MMC0 (eMMC) Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links.
2. Pin attributes, signal description, and electrical specifications.
3. Electrical characteristics, timing parameters, and any additional available information.
4. MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)
5. AM62x processor family implements a soft PHY. The pulls required for DAT0, clock, and control signals are recommended to be implemented externally.
6. Include a series resistor (0Ω) on MMC0_CLK placed as close to processor clock output pin as possible to dampen reflections. MMC0_CLK is looped back internally on read transactions, and the resistor eliminates possible signal reflections, which cause false clock transitions. Use 0Ω initially and adjust as required to match the PCB trace impedance.
7. Add pullups (10kΩ or 47kΩ) for DAT0 and CMD signals. Connect the pullup to the IO supply for IO group VDDSHV4 (MMC IO rail). For DAT1-7 eMMC device is expected to have the pullups enabled during reset. The eMMC host/PHY disables the eMMC device pullups and enables processor internal pullups. Provision for external pullups is optional, or delete the pullups.
8. VDDSHV4 (1.8V or 3.3V) and the attached eMMC device IO supply is required to be powered from the same power source.
9. Add a pulldown (10kΩ) to the eMMC attached device clock input near to the attached device.
10. For implementing eMMC device reset, use a 2-input ANDing logic when the memory is used for boot. Connect RESETSTATz as one of the input and processor IO as another input. Add a pullup for the processor IO input near the AND gate input pin and an isolation resistor near to the processor IO output. Alternatively, RESETSTATz is used as the reset source. When RESETSTATz is used as the reset source, verify the IO voltage level compatibility with the eMMC IO supply. Use a level shifter as required.
11. When eMMC boot is not configured, the eMMC attached device reset can be controlled by the processor IO. The recommendation is to pulldown the reset of the eMMC memory device during board power reset.
12. Add additional decoupling capacitors for attached memory device as required. Refer SK-AM62P-LP schematics.

Schematic Review

Follow the below list for the custom schematic design:

1. Required bulk and decoupling capacitors are provided for processor and attached device rails. Compare with the SK schematics
2. Pull values for the data, command, and clock signals. Compare with the relevant SK schematics
3. Series resistor value and placement on the clock output signal near to the processor clock output
4. Implementation of reset logic including the IO level compatibility. Adding a capacitor at the reset input of eMMC attached device is not recommended when RESETSTATz or processor IO is connected directly to control the reset. A stand-alone reset connection to reset the eMMC memory device is not recommended
5. Supply rails connected follow the ROC

Additional

1. Connect an external pulldown on CLK, and external pullups on CMD and DAT0 to prevent the eMMC device inputs from floating until software initializes the host controller and processor IOs associated with MMC0. The eMMC standard mandates that eMMC devices have internal pullups enabled during reset on DAT1-7, external pullups are not required for DAT1-7 signals. Software turns on the respective internal DAT pullups when the bus width is increased from 1-bit mode to 4-bit or 8-bit mode. External pulls are required

because the IOs associated with MMC0 are implemented with standard dual-voltage LVCMOS IO cells with the capability of multiplexing additional signal functions to the respective device pins. MMC0 IOs buffers are disabled during reset because the interface connected to MMC0 pins is unknown.

2. Verify eMMC_RSTn reset input is enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional. The GPIO reset option enables software to reset the attached device (eMMC, OSPI, SD card, OLDI, or EPHY) without resetting the entire processor in cases where the peripheral becomes unresponsive. Eliminate the GPIO option and use the reset output, either warm or cold. Software forces a warm reset if the peripheral becomes unresponsive. However, using warm reset resets the entire device, rather than trying to recover the specific peripheral without resetting the entire device. When RESETSTATz is used to reset the attached device, verify the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level. Alternatively, use a resistor divider and select an optimum impedance value. A slow rise or fall time of the eMMC reset input causes too much delay. Low reset input causes the processor to source too much steady-state current during normal operation.
3. ANDing logic additionally performs IO level translation. Verify the reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch can cause supply leakage and affect processor operation
4. Pulldown is selected for eMMC, SD card or other peripherals since there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with the logic state.

7.2.2.1.2 Additional Information on eMMC PHY

See the notes in the *Signal Descriptions, MMC, MAIN Domain* section of the processor-specific data sheet.

Note

Note the potential implementation differences in the eMMC Controller and eMMC PHY IPs used on different processor families. Pay attention on the interface including terminations recommended when migrating to a different processor family.

The recommendation is to review the processor-specific data sheet, TRM, and following the connection recommendations for the processor and attached device.

Processor-specific SK implementation can be followed as required.

7.2.2.1.3 MMC0 – SD (Secure Digital) Card Interface

The CD (Card Detect) and WP (Write Protect) pins are not available on MMC0 interface. MMC0 can be used to interfaces with fixed SDIO devices (on-board). For more information, see the *MMC0 - eMMC/SD/SDIO Interface* section of the processor-specific data sheet.

7.2.2.2 MMC1/MMC2 – SD (Secure Digital) Card Interface

For more information, see to the *MMC1/MMC2 - SD/SDIO Interface* section of the processor-specific data sheet.

7.2.2.2.1 IO Power Supply

Processor MMC1 (CMD, CLK and Data) interface IOs are powered by VDDSHV5 supply rail (IO supply for IO group 5) and MMC2 (CMD, CLK and Data) interface IOs are powered by VDDSHV6 supply rail (IO supply for IO group 6).

VDDSHV5 and VDDSHV6 are designed to support power-up, power-down, or dynamic voltage change independently of other power rails, allowing the operating voltage to change from 3.3V to 1.8V as the transfer speed increases.

VDDSHV5 and VDDSHV6 supplies are required to start with 3.3V and allow changing to 1.8V when software is ready to change the supply voltage.

Recommend using separate supply sources (LDO or similar) for VDDSHV5 and VDDSHV6 supply rails when configured as SD card interface.

Processor MMC1 SD Card Detect (CD) and Write Protect (WP) signals are powered by VDDSHV0 supply rail (IO supply for IO group 0). The recommendation is to connect the pullups for MMC1_SDCD, MMC1_SDWP from the SD card to the same supply rail VDDSHV0.

SD Card Detect (CD) input to the processor connects directly to ground when the SD card is inserted. A series resistor to limit the current in case the IO is configured as output due to programming error is recommended.

Processor MMC2 SD Card Detect (CD) and Write Protect (WP) signals are powered by VDDSHV6 (IO supply for IO group 6) supply rail or VDDSHV0 supply rail (IO supply for IO group 0).

7.2.2.2.2 SD Card Supply Reset and Boot Configuration

The recommendation is to provision for a software-enabled (controlled) power switch (load switch) that sources the SD card power supply (VDD). A fixed 3.3V supply (processor IO supply) is connected as an input to the power switch.

Use of power switch allows power cycling of the SD card (since resetting the power switch is the only way to reset the SD card) and resetting the SD card to the default state.

Recommendation is to implement the SD card power switch enable reset logic using a 3-input ANDing logic. Processor general purpose input/output (GPIO) is connected as one of the input to the AND gate with provision for pullup (to support boot) near to the input and 0Ω to isolate the GPIO for testing or debug. The other two AND gate inputs are the main domain POR (cold reset) status output (PORz_OUT) and main domain warm reset status output (RESETSTATz) signals.

If the SD card is configured as a boot device, the external power switch sourcing the SD card power supply must default to ON (powered state).

For the implementation details, see the processor-specific SK.

7.2.2.2.3 Signals Connection

Make the following connections:

- Connect a series resistor (0Ω) for MMC1_CLK and MMC2_CLK (close to processor) and external pulldown for MMC1_CLK and MMC2_CLK (close to attached device or SD card socket).
- Add external pullups (47kΩ) for the data lines (MMC1_DAT0-3 and MMC2_DAT0-3) and CMD signal (MMC1_CMD and MMC2_CMD) and connect to the respective dual-voltage IO supply for IO group (MMC1 = VDDSHV5, MMC2 = VDDSHV6) supply rails (place close to attached device or SD card socket).
- Add external pullups for the MMC1_SDCD and MMC1_SDWP signals connected to the VDDSHV0 supply rail (close to attached device or SD card socket).
- For supporting SD card interface, configure MMC2_SDCD and MMC2_SDWP signals referenced to VDDSHV0. Add external pullups for the MMC2_SDCD and MMC2_SDWP signals connected to VDDSHV0 supply rail close to attached device or SD card socket.

See the following FAQs:

[FAQ] AM62A7: Why is MMC1 powered by two different voltage supplies, VDDSHV0 and VDDSHV5?

[FAQ] AM62A7-Q1: how to connect the pin net VDDSHV4, VDDSHV5, and VDDSHV6 if SD card is not used

[FAQ] AM6442: AM6442 MMC1

FAQ] AM625: MMC interface

The FAQs are generic and can also be used for the AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 processor family.

7.2.2.2.4 ESD Protection

External ESD protection is recommended for data, clock, and control signals. Internal ESD protection is not designed to handle the board or system level ESD requirements.

7.2.2.2.5 Capacitors for the Power Supply Rails

Verify the required bulk and decoupling capacitors are provided for VDDSHV5 and VDDSHV6 supply rails and attached device.

Follow the processor-specific SK implementation whenever recommendations are not available.

Note

Follow the processor-specific connection recommendations for data and control signals. The recommendation is to place the series resistor for the clock output close to processor clock output pin.

7.2.2.2.6 MMC1 SD Card Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links.
2. Pin attributes, signal description, and electrical specifications.
3. Electrical characteristics, timing parameters and any additional available information.
4. Include a series resistor (0Ω) on MMC1_CLK placed as close to processor clock output pin as possible to dampen reflections. MMC1_CLK is looped back internally on read transactions, and the resistor can be needed to eliminates possible signal reflections, which can cause false clock transitions. Use 0Ω initially and adjust as required to match the PCB trace impedance.
5. The MMC1 CLK, CMD, and DAT0-3 signal functions are implemented with SDIO buffers on pins powered from VDDSHV5 (power source that changes the operating voltage from 3.3V to 1.8V as the transfer speed increases).
6. The MMC1 SDCD and SDWP signal functions are implemented with LVCMOS buffers on pins powered from VDDSHV0, which operate at fixed 1.8V or 3.3V.
7. The SDIO buffers are designed to support dynamic voltage change. Dynamic voltage change is necessary since UHS-I SD cards begins operating with 3.3V signaling and changes to 1.8V signaling when the SD card transitions to one of the higher speed data transfer modes.

   Processor IO buffers are off during reset. An external pullup is required for any of the processor or attached device IOs that can float. Pullups are needed on all data and command signals. Verify internal pullups are not configured when (improves noise immunity) external pullups are used.
8. To meet the SD card specification, a 47kΩ pullup is recommended when internal pulls are unexpectedly enabled. The 47kΩ pullup verifies the resulting pull resistance is within the specified range.
9. When UHS-I speed support is required, implementing an LDO supply that switches between 3.3V and 1.8V is required. Switching IO supply can be an external discrete implementation or internal to the PMIC. Connect the switchable voltage output to the IO supply for IO group, referencing the SD interface signals (VDDSHV5).
10. When UHS-I speed support is required, while the IO voltage for SD card interface is either 1.8V or 3.3V, the SD card VDD supply is connected to a fixed 3.3V source.
11. When UHS-I speed support is required, the 3.3V SD card power is required to be switched through a load switch to allow resetting of the SD card IO supply to 3.3V. Provision to enable the SD card load switch during reset is required.
12. Provide provision to reset the load switch using the SD card load switch EN signal during cold reset, warm reset and normal operation using processor IO is required to be provided. An option is to use a 3-input ANDing logic.
13. During boot, the ROM code checks the status of the card detect pin (SDCD, pin P23). The signal is expected to be low to indicate SD card is detected (inserted).

Schematic Review

Follow the below list for the custom schematic design:

1. Required bulk and decoupling capacitors are provided. Compare with the SK schematics.
2. Pull values used for the data, command and clock signals. Compare with the relevant SK schematics.
3. Series resistor value and placement on the clock output signal near to the processor.
4. When UHS-I speed support is required, verify IO supply rail switching and the SD card power switching circuits are added.

5. Supply rail connected to the SD card power supply (use SYS voltage).
6. Implementation of reset logic for resetting the SD card power control load switch. Provision for slew rate control of the SD card supply control power switch is provided.
7. Supply rails connected follow the ROC.
8. Required external ESD protection are provided for the SD interface signals.

Additional

1. The logic state of the MMC1_SDCD and MMC1_SDWP inputs to the host must not change when a UHS-I SD card changes the IO operating voltage. Maintaining a valid logic state is not possible if the signals propagate through an input buffer of a dual-voltage SDIO cell that changes voltage. The signal functions are assigned to IOs that do not change voltage dynamically. Signals only connect to switches in the SD card connector, so there is no reason for the signals to change voltage when the SD card signals change operating voltage. The MMC1_SDCD and MMC1_SDWP signals are required to connect to the SD card connector switches and pull high with external pull resistors connected to the VDDSHV0. The other MMC1 SD card signals with pullups are required to have pulls powered by the VDDSHV5 source that dynamically changes voltage.
2. The MMC2_SDCD and MMC2_SDWP pins are referenced to the same IO supply for IO group the other MMC2 pins. Connecting an UHS-I SD card to MMC2 requires avoiding the use of the control for the MMC2_SDCD and MMC2_SDWP signal functions. For SD card use case, the signal functions needs to implemented using one of the other pin multiplexing options that uses an IO cell powered from a fixed voltage source. The MMC2 assignments differ because MMC2 was originally intended for use with on-board fixed voltage SDIO devices, such as Wi-Fi® or Bluetooth® transceivers.
3. SD card power switch, along with the power switch supply EN pin reset logic, and the host IO power supply circuit is required to support UHS-I SD cards which begins communication using 3.3V IO level and later change to 1.8V IO level when changing to one of the faster data transfer speeds.

   Cycling power to the SD card is the only way to put the SD card back into 3.3V mode, because SD cards do not have a reset pin. The host IO power supply must power off and on, and change voltage at the same time as the SD card. The circuits and the software driver operating the signals sourcing the circuits verifies that both devices are off, or on and operating at the same IO voltage at the same time.
4. To optimize the ANDing logic, use a dual input AND gate with RESETSTATz and the processor IO as inputs.
5. Add a series resistor 100Ω to the SDCD pin since processor IO connects directly to the ground when the SD card is inserted.

7.2.2.3 MMC1 / MMC2 SDIO (Embedded) Interface

For more information, see to the *MMC1/MMC2 - SD/SDIO Interface* section of the processor-specific data sheet.

7.2.2.3.1 IO Power Supply

The processor MMC1 (CMD, CLK and Data) interface IOs are powered by VDDSHV5 supply rail (IO supply for IO group 5) and MMC2 (CMD, CLK and Data) interface IOs are powered by VDDSHV6 supply rail (IO supply for IO group 6).

Processor MMC1 SD Card Detect (CD) and Write Protect (WP) signals are powered by VDDSHV0 supply rail (IO supply for IO group 0). The recommendation is to connect the pullups for MMC1_SDCD, MMC1_SDWP from the SDIO to the same supply rail VDDSHV0.

Processor MMC2 SD Card Detect (CD) and Write Protect (WP) signals are powered by VDDSHV6 (IO supply for IO group 6) supply rail or VDDSHV0 supply rail (IO supply for IO group 0). The recommendation is to connect the pullups for MMC2_SDCD, MMC2_SDWP from the SDIO to the same supply rail VDDSHV6 or VDDSHV0.

7.2.2.3.2 Signals Connection

Make the following connections:

- Connect a series resistor (0Ω) for MMC1_CLK and MMC2_CLK (close to processor) and external pulldown for MMC1_CLK and MMC2_CLK (close to attached device).

- Add external pullups for the data lines (MMC1_DAT0-3 and MMC2_DAT0-3) and CMD signal (MMC1_CMD and MMC2_CMD) connected to the respective dual-voltage IO supply for IO group (MMC1 = VDDSHV5, MMC2 = VDDSHV6) supply rails (close to attached device).
- Add external pullups for the MMC1_SDCD and MMC1_SDWP signals connected to the VDDSHV0 supply rail (close to attached device).
- Add external pullups for the MMC2_SDCD and MMC2_SDWP signals connected to the VDDSHV6 or VDDSHV0 supply rail (depending on the pins (IOs) selected) (close to attached device).

7.2.2.3.3 MMC2 SDIO (Embedded) Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links.
2. Pin attributes, signal description, and electrical specifications.
3. Electrical characteristics, timing parameters, and any additional available information.
4. Include a series resistor (0Ω) on the MMC2_CLK, placed as close to processor clock output pin as possible to dampen reflections. To prevent signal reflections and false clock transitions, use a resistor to eliminate possible signal reflections on MMC2_CLK, which is looped back internally on read transactions. Use 0Ω initially and adjust as required to match the PCB trace impedance.
5. The MMC2 CLK, CMD, and DAT0-3 signal functions are implemented with SDIO buffers on pins powered from VDDSHV6, which operate at fixed 1.8V or 3.3V.
6. The MMC2 SDCD and SDWP signal functions are implemented with LVCMOS buffers on pins powered from VDDSHV6 or VDDSHV0, which are operated at fixed 1.8V or 3.3V.
7. The SDIO buffers are designed to support dynamic voltage change. When SDIO interface is used, connecting a fixed IO voltage (1.8V or 3.3V) is recommended.
8. Processor IO buffers are off during reset. An external pullup is required for any of the processor or attached device IOs that can float.

   Pullups are needed on all data and command signals. Verify internal pullups are not configured when (improves noise immunity) external pullups are used. As a good design practice, a 47kΩ pullup is recommended for the pullup value to be within the SDIO specification, when internal pulls are enabled unexpectedly. With 47kΩ the resulting pull resistance are still within the specified.
9. Attached device reset implementation using processor IO. Verify the IO level compatibility and the connection of required pull (polarity is attached device dependent).

Schematic Review

Follow the below list for the custom schematic design:

1. Required bulk and decoupling capacitors are provided. Compare with the SK schematics.
2. Pull values used for the data, command and clock signals. Compare with the relevant SK schematics.
3. Series resistor value and placement on the clock output signal near to the processor.
4. Implementation of reset logic.
5. Supply rails connected follow the ROC and is a fixed supply.

Additional

1. Verify required external ESD protection are provided for the interface signals when connected over an add-on card.
2. Follow similar guidelines when using MMC1. When using MMC1, software changes are required because the SK only implements the SDIO interface on MMC2.
3. There are no specific guidelines about SDIO devices providing or not providing internal pulls. The board designer implementing an embedded SDIO device must understand what the SDIO device provides and apply the appropriate external pull if not provided by the SDIO device. Most of the processor IOs buffers are off during reset and are not enabled until the board has booted and the software configures. To prevent floating inputs, use external pulls on any signals connected to the inputs of attached devices.

4. For embedded SDIO application, the recommendation is to power IO supply rail from the same fixed 1.8V or 3.3V power source that is used to power the IOs of the SDIO attached device (an example is a Wi-Fi module).

7.2.2.4 Additional Information

See the notes in the *Signal Descriptions, MMC, MAIN Domain* section of the processor-specific data sheet.

7.2.3 Octal Serial Peripheral Interface (OSPI) or Quad Serial Peripheral Interface (QSPI)

For more information, see the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the processor-specific data sheet.

See the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – OSPI/QSPI MEMORY Interface

7.2.3.1 IO Power Supply

The processor IOs used for the OSPI or QSPI are powered by VDDSHV1 supply rail (IO supply for IO group 1).

The recommendation is to connect VDDSHV1 and the IO supply rail of the attached device to the same supply source.

VDD (core voltage) of the attached device can be powered from an independent supply source.

7.2.3.2 OSPI/QSPI Device Reset

The recommendation is to implement the attached device reset using a 2-input ANDing logic. Processor general purpose input/output (GPIO) is connected as one of the input to the AND gate with provision for pullup (to support boot) near to the input and 0Ω to isolate the GPIO for testing or debug. The other AND gate input is the main domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and processor main domain warm reset status output (RESETSTATz) is used to reset the attached device, match the IO voltage level of the attached device and RESETSTATz. A level translator is recommended to match the IO voltage level.

7.2.3.3 Signals Connection

Make the following connections:

- Provision for a series resistor (0Ω) for OSPI0_CLK and OSPI0_LBCLKO (close to processor) and external pulldown for OSPI0_CLK (close to attached device).
- Provision for external pullups for CS pin and INT# pin (close to attached device).
- Provision for external pullups for the data lines (DAT0:7) (close to processor). Depending on the availability of pulls internal to the attached device, populate the external pulls.

7.2.3.4 Loopback Clock

Verify the required loopback clock configuration. Different configuration of clock loopback can be made using OSPI0_LBCLKO (OSPI0 Loopback Clock Output) and OSPI0_DQS (OSPI0 Data Strobe or Loopback Clock Input). For the following loopback configurations, see the processor-specific data sheet:

- *No Loopback, Internal PHY Loopback, and Internal Pad Loopback*

External Board Level Loopback

Processor DQS or Loopback Clock is used along with the DS data strobe of attached memory device

When DS (Read Data Strobe) pin is available on the attached device, connect the DS pin of the attached device to the OSPI0_DQS pin of the processor. Leave the OSPI0_LBCLKO pin unconnected.

In case DS pin is not being currently used, to configure the external loopback connect the OSPI0_LBCLKO output pin of the processor to the OSPI0_DQS input pin of the processor.

If External Loopback is not used, the recommendation is to leave the OSPI0_LBCLKO and OSPI0_DQS pins unconnected.

Note

D0 and D1 pins of the processor OSPI0 interface must be connected to D0 and D1 pins of the OSPI/QSPI memory device to support legacy x1 commands. Data bit swapping is not allowed

7.2.3.5 Interface to Multiple Devices

Connecting an OSPI0 interface to multiple memory devices is currently not supported. Connect the OSPI0 interface (processor) to a memory device. In case the OSPI0 is interfaced to multiple memory devices, the interface creates a split data bus which can severely degrade signal integrity at higher speeds. For accessing OSPI memory device at high speeds, a point-to-point connection of the data bus is recommended.

7.2.3.6 Capacitors for the Power Supply Rails

Verify the required bulk and decoupling capacitors are provided for VDDSHV1 supply rail and the attached device (core and IO supplies).

Follow the processor-specific SK implementation whenever recommendations are not available.

7.2.3.7 OSPI and QSPI Interface Implementation Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links
2. Pin attributes, signal description and electrical specifications
3. Electrical characteristics, timing parameters and any additional available information
4. Required memory interface configuration and recommended connections for the attached device are provided
5. The attached device IO supply and IO supply for IO group VDDSHV1 referenced to the interface signals are connected to the same supply source
6. Series resistor 0Ω provision for clock signal is provided near to the processor clock output pin
7. Provision for pullups are provided for data and control signals that can float. Verify the supply source connected to the pullups
8. Pulldown 10kΩ is provided for the clock input near to the attached (memory) devices
9. Reset logic implementation when used for boot using a 2-input (RESETSTATz and processor IO) ANDing logic or using warm reset status output RESETSTATz is recommended
10. Verify the reset IO level compatibility between processor and attached device
11. Pulling up the reset input to a high state during reset or supply ramp is not recommended
12. Clock loop back configuration based on the memory device and interface selected (OSPI/QSPI)
13. In case OSPI/QSPI boot mode is implemented, verify the Errata, selected memory meets the boot mode criteria described in the TRM (or verify with TI using E2E)

Schematic Review

Follow the below list for the custom schematic design:

1. Compare the implementation with SK schematics for parallel pulls and series resistors for values
2. Compare implementation of attached device reset logic with the SK schematics
3. Connecting the interface to multiple attached devices (more than 1 attached device) is not allowed or recommended
4. Supply rails connected follow the ROC
5. Implementation of external loopback based on the use case

Additional

1. Verify that the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the data sheet is followed
2. Review and follow the electrical, timing and switching characteristic

7.2.4 General-Purpose Memory Controller (GPMC)

7.2.4.1 IO Power Supply

The processor IOs used for GPMC interface are powered by VDDSHV3 supply rail (IO supply for IO group 3).

The recommendation is to connect VDDSHV3 and the IO supply rail of the attached device to the same supply source.

VDD (core voltage) of the attached device can be powered from an independent supply source.

7.2.4.2 GPMC Interface

Verify the number of attached devices connected to the GPMC interface.

The recommendation is to connect the GPMC interface to one device in synchronous mode. Using multiple devices or CSns requires splitting the GPMC clock (and other interface signals) on-board, which can cause signal integrity issues.

A detailed timing analysis is recommended when interfacing multiple devices in asynchronous mode. Interfacing multiple devices is not recommended. When interfacing multiple devices in asynchronous mode, the control signals are required to be routed to multiple devices. The split routing and loading (trace length and number of devices) issues have an affect on custom board performance.

7.2.4.3 Memory (Attached Device) Reset

When using NAND flash or NOR flash with GPMC, many memories interfaced over GPMC can lack a reset pin.

In case the reset pin is available, review the reset requirements and connect the reset pin to the relevant reset source.

7.2.4.4 Signals Connection

Provide a series resistor (0Ω) for GPMC0_CLK (close to processor).

Recommend provisioning for external pullups on GPMC0_CSn0-3 (depending on the configuration) to hold the signal high when processor is held in reset, or after reset, before software has configured the PADCONFIG registers to enable the TX buffer.

7.2.4.4.1 GPMC NAND

The active high ready and active low busy (R/B#) output from the NAND flash is open-drain and is connected to the GPMC0_WAIT0 and GPMC0_WAIT1 signals (depending on the configuration). The recommendation is to provide the pullup (commonly used value 4.7kΩ or 10kΩ) close to the attached device.

7.2.4.5 Capacitors for the Power Supply Rails

Verify the required bulk and decoupling capacitors are provided for VDDSHV3 supply rail and the attached device (core and IO supplies).

Follow the processor-specific SK implementation whenever recommendations are not available.

7.2.4.6 GPMC Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links
2. Pin connectivity requirements, pin attributes and signal description
3. Electrical characteristics, Timing parameters and any additional available information
4. GPMC interface configuration and recommended connections
5. IO level compatibility between processor and attached device
6. GPMC memory interface configuration (NAND or NOR flash), interface mode used - Async or Sync clock mode
7. Connection to multiple devices in allowed in Async mode, perform timing and load calculation before use
8. Series resistor 0Ω near to the processor GPMC clock output pin

9. The attached device IO supply and IO supply for IO group VDDSHV3 referenced to the GPMC interface signals are connected to the same supply source
10. Verify the recommended or required pulls are provided
11. Verify the required interface configuration and recommended connections are provided
12. Attached device IO compatibility with the processor GPMC controller signals
13. Supported address and data range (IOs pinned out of the device as mentioned in the data sheet)
14. GPMC interface timing required versus feasible and effect of layout
15. Addition of pulls as required
16. Connection of GPMC memory NAND/ NOR, address and data signals - multiplexed or non-multiplexed, synchronous or asynchronous, data bit width as per the TRM

Schematic Review

Follow the below list for the custom schematic design:

1. Required pulls are provided based on the memory interfaced
2. Pulls are provided for any of the interface signals that can float
3. Supply rails connected follow the ROC

7.3 External Communication Interface (Ethernet (CPSW3G), USB2.0, PRUSS, UART and Controller Area Network (CAN))

7.3.1 Ethernet Interface Using CPSW3G (Common Platform Ethernet Switch 3-Port Gigabit)

CPSW3G supports the RGMII (10/100/1000) and RMII (10/100) interfaces.

7.3.1.1 IO Power Supply

The processor Gigabit Ethernet Media Access Controller (GEMAC) IOs (used for Ethernet interface) are powered by VDDSHV2 supply rail (IO supply for IO group 2).

The recommendation is to connect VDDSHV2 and the IO supply rail of the attached device to the same supply source.

VDD (core voltage) of the attached device can be powered from an independent supply source.

7.3.1.2 Ethernet PHY Reset

The recommendation is to implement the attached device reset using a 3-input ANDing logic. Processor general purpose input/output (GPIO) is connected as one of the input to the AND gate with provision for pullup (to support boot) near to the input and 0Ω to isolate the GPIO for testing or debug. The other two AND gate inputs are the main domain POR (cold reset) status output (PORz_OUT) and main domain warm reset status output (RESETSTATz) signals.

If a dual input AND gate is used, PORz_OUT or RESETSTATz can be connected as one of the input along with the processor GPIO input as the second input based on the use case. When more than one EPHY is used, provide provision to reset the EPHYs individually.

A pullup or pulldown at the output of the ANDing logic is recommended based on the EPHY reset input pin configuration. The EPHYs are required to be held in reset for a specified minimum reset hold time after the respective clocks are valid.

In case an ANDing logic is not used and processor main domain warm reset status output (RESETSTATz) is used to reset the attached device, match the IO voltage level of the attached device and RESETSTATz. A level translator is recommended to match the IO voltage level.

7.3.1.3 Ethernet PHY Pin Strapping

Many of the TI EPHYs configure the outputs as inputs during reset and captures the configuration (Pin strapping is done through resistors) information on strap inputs when the processor reset is released. Appropriate pullup or pulldown can be necessary on strap inputs (IOs) that also connect to processor IOs. TI EPHYs used on the processor-specific SK use a combination of pullup and pulldown allowing multiple configuration modes to be configured using each pin. During processor reset, the IO buffers and internal pullup or pulldown are disabled,

which minimizes concern of a mid-supply potential being applied to the processor input buffer by the EPHY. The EPHYs are required to be configured to normal state from reset state to drive a valid logic state before enabling any of the associated processor input buffers.

7.3.1.4 Ethernet PHY (and MAC) Operation and Media Independent Interface (MII) Clock

Verify the clock input option used for Ethernet PHY and MAC based on the interface.

7.3.1.4.1 Crystal

If a crystal is used as the clock source for the EPHY, the recommendation is to match crystal (clock) specifications with the processor crystal (clock) specifications to optimize performance.

7.3.1.4.2 Oscillator

Using an external clock (LVCMOS) oscillator as the clock source for the processor and the EPHY allows for the use of either a shared oscillator or a separate oscillator. When using one oscillator, buffer the clock output before connecting to the processor and EPHY.

Use one output, individual buffer, or dual or multiple output buffer to connect the clock output of the oscillator to the processor and EPHYs.

For specific use case (requirement for some of the industrial applications using one Time Sensitive Networking (TSN)) input or two or more outputs (based on number of EPHYs used) buffer is recommended for the processor and the EPHYs.

Verify that the crystal XO of the EPHY is connected according to the recommended guidelines.

7.3.1.4.3 Processor Clock Output (CLKOUT0)

For optimizing the design, the processor clock output (CLKOUT0) can be used as clock input to the EPHY. Clock output is buffered internally and is intended to used for a point-to-point clock topology. A series resistor is recommended at the source end of the CLKOUT0 to minimize reflections.

RGMII EPHYs require a 25MHz clock input that is not synchronous to any other signals. 25MHz clock signal does not have any timing requirements, but is important the EPHY does not receive any non-monotonic transitions on the clock input.

RMII EPHY clocking option changes with the EPHY controller or device configuration.

When configured as controller, most RMII EPHYs require a 25MHz input clock that is not synchronous to any other signals, the 25MHz clock signal does not have any timing requirements, but is important to make sure the EPHY does not receive any non-monotonic transitions on the clock input.

The RMII EPHY provides the 50MHz clock output to the MAC. For RMII use case, the 50MHz data transfer clock is delayed to the MAC relative to the EPHY. The delay shifts clock to data timing relationship which can erode the timing margin. Eroded timing margin can be problematic for some designs if the delay is too large.

When configured as device, the MAC and the EPHY uses a 50MHz common clock that is synchronous to both transmit and receive data. The 50MHz clock is defined in the RMII specification as a common data transfer clock signal that is used by both the MAC and the EPHY, where transitions are expected to arrive simultaneously at the MAC and EPHY device pins. The common clock provides better timing margin for both transmit and receive data transfers. Important requirement is that the MAC and EPHY do not receive any non-monotonic transitions on the clock inputs. To take care of the clock signal integrity, recommendation is to route the common clock signal through a two-output phase aligned buffer. Recommend using equal length signal traces that are half the length of the data signals for connecting the clock buffer outputs, where one clock output connects to the MAC and the other connects to the EPHY.

For RMII interface, the recommended configuration is *RMII Interface Typical Application (External Clock Source)* explained in the processor-specific TRM. If *RMII Interface Typical Application (Internal Clock Source)* configuration explained in the processor-specific TRM is used, the performance has to be validated on a board level. Provision for an external clock for initial performance testing and comparison is recommended. The Ethernet performance (RGMII) is validated on the processor and the EPHY with 25MHz clock.

The CLKOUT0 function can be used to source a 25MHz or a 50MHz clock input to EPHY. However, using CLKOUT0 signal function requires the software to configure the clock output. The CLKOUT0 clock configuration cannot be used if the board design must support Ethernet boot. CLKOUT0 connected as EPHY clock is likely to glitch anytime the configuration is changed.

AM62x processor family, automatically begins sourcing the device reference clock (MCU_OSC0_XO, enabled during reset) to the WKUP_CLKOUT0 pin as soon as the device is released from reset (MCU_PORz 0 to 1). The clock output does not glitch after the clock begins to toggle. However, the first high or low pulse can be short because reset is released asynchronous to the HFOSC0 clock.

The EPHYs are required to be held in reset for a specified minimum reset hold time after the respective clocks are valid.

Processor clock output performance is not defined because clock performance is influenced by many variables unique to each custom board design. The board designer must validate timing of all peripherals by using the actual PCB delays, minimum or maximum output delay characteristics, and minimum setup and hold requirements of each device to confirm there is enough timing margin.

7.3.1.5 MAC (Data, Control and Clock) Interface Signals Connection

Series resistors are recommended for the Ethernet MAC interface signals. Use smallest possible package (0402 or smaller) and place series resistors close to source. To start with place series resistor (22Ω) for the TDn signals near to the processor pins. For the RDn signals the internal impedance control (series resistors) of the EPHY can be used. Providing provision for external series resistors (0Ω) are recommended on the RDn signals.

The interrupt output of the EPHY can be connected to the processor EXTINTn (interrupt) pin. The recommendation is to connect a pullup for the EXTINTn close to processor.

7.3.1.6 External Interrupt (EXTINTn)

EXTINTn is an open-drain output type buffer, fail-safe IO. The recommendation is to connect an external pullup resistor when a PCB trace is connected to the pad and an external input is not being actively driven. Open-drain output type buffer IO has slew rate requirements specified when the IO is pulled up to 3.3V. An RC is recommended for limiting the slew rate.

For more information, see the *[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1/ AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1 Custom board hardware design – EXTINTn pin pullup connection*.

7.3.1.6.1 External Interrupt (EXTINTn) Checklist

General

Review and verify the following for the custom schematic design:

1. The above section including relevant application notes and FAQ links
2. Pin attributes (open-drain output IO buffer) and signal description
3. Electrical characteristics (fail-safe and slew rate requirements when pulled to 3.3V), timing parameters and any additional available information
4. An external pullup is recommended when a signal trace is connected and not being actively driven
5. EXTINTn is an open-drain output type buffer, fail-safe IO. An external pullup is recommended when a trace or external input is connected
6. Open-drain output type IO. EXTINTn has slew rate requirements specified when pulled to 3.3V supply. Add an RC at the input to limit the slew rate. Refer TMDS64EVM

Schematic Review

Follow the below list for the custom schematic design:

1. Pullup value used. Compare with the SK schematics
2. Pullup referenced to the processor VDDSHVx (pullup connected to correct IO voltage level)
3. RC provision for slew rate control and RC values used. Refer TMDS64EVM

7.3.1.7 MAC (Media Access Controller) to MAC Interface

For applications requiring EPHY-less (MAC-to-MAC) connection between processors, using the RGMII interface is recommended (check with TI if the MAC-to-MAC interface is officially supported on the selected processor family) since the clocks are source synchronous.

When MAC-to-MAC interface between 2 processors are used, verify fail-safe operation, matching of clock specifications, and IO level compatibility.

7.3.1.8 MDIO (Management Data Input/Output) Interface

The processor IOs used for MDIO interface are powered by VDDSHV2 supply rail (IO supply for IO group 2).

The recommendation is to connect an external pullup (close to the EPHY) for the MDIO0_MDIO (MDIO data) signal.

Before configuring the MDIO interface, see the advisory *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS)* of the processor-specific silicon errata.

7.3.1.9 Ethernet MDI (Medium Dependent Interface) Including Magnetics

In case the EPHY and MDI interface including the magnetics and the RJ45 connector are implemented on the processor board, follow the processor-specific SK for MDI interface connections, recommended magnetics used on the SK, external ESD protection, and connection of RJ45 connector shield to circuit ground.

7.3.1.10 Capacitors for the Power Supply Rails

Verify the required bulk and decoupling capacitors are provided for VDDSHV2 supply rail and the attached device (core and IO supplies).

Follow the processor-specific SK implementation whenever recommendations are not available.

7.3.1.11 Ethernet Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links.
2. Pin attributes and signal description.
3. Electrical characteristics, timing parameters, and any additional available information.
4. MAC interface configuration and recommended connections including series resistors (on the TDn signals near to processor MAC TDn output pins and optional 0Ω series resistors near the attached device for the RDn signals.
5. IO level compatibility between processor MAC and EPHY (attached device). The attached device IO supply and IO supply for IO group VDDSHV2 referenced by the interface signals are recommended to be connected to the same supply source.
6. Matching of processor and EPHY clock specifications.
7. Clocking of EPHY and processor MAC including addition of buffers based on the EPHY configuration and clock architecture (use of common Oscillator and Buffer or RMII interface). When the clock output connects to more than one inputs, each of the clock inputs must be buffered using individual buffers.
8. Interface connections, IO level compatibility, fail-safe operation (when MACs are powered by different power sources) and matching of clock specifications when MAC-to-MAC interface is used.
9. MDIO interface connection including pullup for MDIO data added near to the EPHY. MDIO connection to multiple devices and the addition of pullup near each EPHY.
10. When 2 EPHYs are used, configuration of EPHY device address to read the internal registers through the MDIO interface.
11. Implementation of EPHY reset logic. When 2 EPHYs are used, the recommendation is to provide provision to reset the EPHYs individually. When used for boot a 2 or 3 input ANDing logic can be used.
12. In case implementing an Ethernet boot is required, verify the errata, supported EPHY interface configurations, MAC interface port used versus recommended, and the recommended clock and interface connection.

Schematic Review

Follow the below list for the custom schematic design:

1. Provision for series resistor for the processor MAC transmit signals TDn near to the processor output pins have been provided and the initial value (0Ω or 22Ω).
2. Verify the EPHY reset implementation including ANDing logic, EPHY reset input pull and compare with SK as required.
3. Verify EPHY device address configuration when two EPHYs are used and MDIO interface is required
4. MDIO data pullup is provided near to the EPHY.
5. Verify the IO level compatibility - the attached device IO supply and IO supply for IO group referenced by the processor interface signals are connected to the same supply source.
6. Compare the bulk and decoupling capacitors used for all the EPHY supply rails with SK schematics when TI EPHY is used.
7. Pullup is provided for processor GPIO input of the EPHY reset ANDing logic.
8. Pullup on the MDIO clock can be optional (EPHY can have internal pulldown; verify in the data sheet).
9. Supply rails connected follow the ROC.
10. When more than 1 EPHY is connected, provision to reset the EPHYs individually is provided. Addition of pull at the EPHY reset input as required.

Additional

1. Follow the below steps when TI EPHY is used:
   - Obtain a review of the implementation done with the EPHY business unit or product line
   - Verify the power sequence requirements for two-supply configuration and three-supply configuration
   - Verify the RBIAS resistor tolerance as per the EPHY data sheet
   - Selection of the RJ45 connector with integrated magnetics, follow SK
   - Provision for external ESD protection for the MDI signals
   - Connection of RJ45 connector shield to circuit ground
   - The recommended bulk and decoupling capacitors are provided (refer SK as required)
2. Use one output, individual buffer device, or dual or multiple output buffer to connect the clock output of the oscillator to the processor and EPHYs. For specific use case (requirement for some of the industrial applications using a Time Sensitive Networking (TSN)) input and two or more output (based on number of EPHYs used) buffer is recommended for the processor and the EPHYs.
3. When EPHY is configured as RMII slave (peripheral), two-output phase aligned buffer with a common input is recommended.
4. If space is not a constraint, consider adding 0Ω series resistors on the RDn signals near to the EPHY.
5. ANDing logic additionally performs IO level translation. Verify the reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch can cause supply leakage and affect processor operation.
6. To simplify the ANDing logic, use a dual input AND gate with RESETSTATz and the processor GPIO as inputs.
7. Verify recommendations as per the data sheet or EVM implementation are considered for the attached device, including terminations and external ESD protection.

7.3.2 Universal Serial Bus (USB2.0)

The processor provides 2 USB2.0 interfaces that are configurable as host, device, or dual-role device (DRD).

USBn_VBUS (n = 0-1) is recommended to connect in accordance with the *USB Design Guidelines* section of the processor-specific data sheet. The supply voltage range for the USBn_VBUS pins is defined in the *Recommended Operating Conditions* section of the processor-specific data sheet. The nominal voltage value applied is equal to the resistor divider output when VBUS supply voltage level is 5V.

USBn_ID functionality is supported through any of the processor GPIOs.

Note

USBn_VBUS are fail-safe inputs. The fail-safe input is valid only if the VBUS supply is connected through recommended *USB VBUS Detect Voltage Divider / Clamp Circuit*.

7.3.2.1 USBn (n = 0-1) Used

The recommendation is to connect the USB supplies VDDA_CORE_USB (USB0 and USB1 core supply), VDDA_1P8_USB (USB0 and USB1 1.8V analog supply), and VDDA_3P3_USB (USB0 and USB1 3.3V analog supply) to the recommended power supply rails in the processor-specific data sheet.

Connect USBn_DM (n = 0-1) and USBn_DP (n = 0-1) signals directly (without any series resistors or capacitors). Route USBn signals with traces that does not include any stubs or test points.

Connect a resistor between USBn_RCALIB (n = 0-1) (close to processor) and VSS. Refer to the processor-specific data sheet for recommended resistor value and tolerance.

7.3.2.1.1 USB Host Interface

The recommendation is to provide a power switch to control the VBUS supply to externally connected device and protect power switch input supply from being overloaded.

The power switch output connects to the USB type A connector. The recommendation is to connect a capacitor (> 120µF) to the VBUS supply close to the connector.

The USBn_DRVVBUS (n = 0-1) signals with an internal pulldown is used to enable the VBUS power switch. An external pulldown near to the power switch enable (EN) pin is recommended. Connection of USBn_VBUS (VBUS supply input including Voltage Divider, Clamp) is optional.

If the power switch used has an OC (over current) indication output, pullup the OC indication output and connect to the processor IO (input).

7.3.2.1.2 USB Device Interface

The VBUS power is sourced by an external host. USB standard for device operation recommends connecting < 10µF capacitor to the VBUS close to the USB type B connector.

Follow the *USB VBUS Design Guidelines* section of the processor-specific data sheet to scale the USB VBUS voltage (supply near the USB interface connector) before connecting to USBn_VBUS pins.

Based on the use case, the zener diode can be deleted if the one is absolutely sure that the board never undergoes a VBUS signal potential > 5.5V (sourced on-board).

7.3.2.1.3 USB Dual-Role-Device Interface

If the custom board design uses USB Micro-AB connector, the USBn_ID signal from the connector can be routed to the processor GPIO pin. USBn_ID can be connected to any available GPIO pin. The GPIO pin is specified in the board device tree file, including the pinmux setting of the GPIO pin.

Note

Full compliant USB On-The-Go (OTG) feature is not supported. The ID pin is not bonded out.

7.3.2.1.4 USB Type-C®

If the custom board design uses USB Type-C® connector, the USBn_ID signals connection is not a requirement. The DRD mode switching is controlled by the USB Type-C companion device.

DRP (Dual Role Port) requires a controller, primarily to switch power based on the negotiated role. In a Device Mode only, USB2.0 only, USB Type-C implementations where the device is not powered by the USB Type-C connector, no USB Type-C controller is required.

- The CC pins at the connector are required to be independently grounded via 5.1kΩ resistors.
- The USB DP and USB DM connector pins are shorted on the PCB (DM=B7:A7, DP=B6:A6). Shorting allows for USB2.0 connectivity regardless of cable orientation. Keep the resulting stubs as short as possible.

Refer to the *USB VBUS Design Guidelines* section of the processor-specific data sheet for more details on USBn_VBUS input scaling recommendations.

The AM62 SK USB0 interface design can be a reference for implementation of the USB Type-C interface.

7.3.2.2 USBn (n = 0-1) Not Used

When USB0 and USB1 are not used or USB0 or USB1 is not used, the interface signals and the USB supplies have specific connectivity requirements.

For connecting the interface signals and USB supply pins, see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

The recommendation is to connect the USB supplies (VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB) to VSS through separate 0Ω resistors.

In case USB0 or USB1 are used for future expansion, connect the signals (USBn_DM, USBn_DP, USBn_RCALIB and USBn_VBUS) with the shortest possible traces and connect at test points or connectors. Additionally, recommendation is to provide provision to connect the required USB supplies.

7.3.2.3 Additional Information

Connect USBn_DM and USBn_DP signals directly from the processor to the USB hub upstream port. The hub then distributes USBn signals to the downstream ports as needed. As each hub has different implementation requirements, follow the hub manufacturer recommendations.

For more information on USB2.0 interface, see the *[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – USB2.0 interface*.

7.3.2.4 USB Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links.
2. Pin connectivity requirements, pin attributes and signal description.
3. Referenced specific standard for electrical characteristics, timing parameters and any additional available information.
4. Required USB interface configuration (Host or Device) and recommended connections.
5. USB VBUS design guidelines based on the USB interface configuration. USBn_VBUS connection is optional for Host configuration. Connecting 5V supply from the USB connector directly to the USBn_VBUS pin is not allowed or recommended. Changing the data sheet VBUS recommended divider value is not allowed or recommended. VBUS fail-safe capability of the IO is valid only when the recommended divider values are implemented.
6. Connection of recommended IO calibration resistor.
7. Connection of the recommended USB supplies including filtering.
8. Direct connection of the USB signals.
9. Common-mode chokes can be used for EMI control. Adding common-mode choke can reduce the signal amplitude and degrade performance. Add provision to bypass the CMC using 0Ω resistors.
10. Marking of differential signals and the differential impedance value.
11. Implementation of USB power switch when USB interface is configured as HOST.
12. USB power switch enable control using DRVVBUS (internal pulldown is enabled during reset).
13. Connection of the power switch OC output to processor IO.
14. Connection of the USB signals to the USB connector.
15. Provision for recommended capacitors on the USB VBUS pin of the USB connector.
16. Provision for required external ESD protections for the USB interface.
17. In case USB boot is implemented, verify the errata, supported interface configuration, USB port and the connections.

Schematic Review

Follow the below list for the custom schematic design:

1. USB interface connection matches the required USB interface configuration (Host or Device). Compare the interface connection with the SK.

2. External ESD protection and CMC implementation with provision to bypass using 0Ω resistors.
3. VBUS voltage divider values (follow data sheet) and tolerance (1%). Follow the data sheet recommendations. Use of multiple resistors is allowed provided the value, tolerance and ratio is maintained.
4. VBUS capacitor values used versus requirements (refer SK).
5. Power switch enable connection (in case processor USBn_DRVVBUS is used, pullup is not recommended or allowed since the DRVVBUS has an internal pulldown enabled).
6. Connection of power switch OC output to the processor IO and IO level compatibility.
7. Supply rails connected follow the ROC.

Additional

1. In case a Type-C USB interface is implemented using TI devices, obtain a review of the implementation done with the relevant business unit or product line.
2. A filtered supply (ferrite and capacitors) is used for VDDA_CORE_USB and VDDA_1P8_USB. VDDA_3P3_USB can be connected to the 3V3 SYS voltage. Refer specific and latest SK for implementation as filters are being continuously optimized.
3. Verify fail-safe operation of USB interface. Applying an external interface signal before supply ramps can cause voltage feed and can affect the custom board functions.
4. When a CMC is used on the USB data lines, verify the connections including the polarity. Reversing the polarity can short the data signals.
5. DNI USBn_DRVVBUS pullup and pulldown to implement wakeup from deep sleep.

7.3.3 Programmable Real-Time Unit Subsystem (PRUSS)

7.3.3.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

For availability of the PRUSS features and supported functionalities, see the *Device Comparison* section of the processor-specific data sheet.

The programmable nature of the PRU cores, along with the capability to access the pins, events and all processor resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

The PRUSS has a large number of IO signals available. Most of the IOs are multiplexed with other functional signals at the processor level. PRUSS pins allow for MUXing using the PADCONFIGx registers.

Review the interface connection supports the required functionalities during schematic design.

To understand the PRUSS supported functionalities, see the processor-specific data sheet and TRM.

7.3.3.1.1 PRU Subsystem

The PRU subsystem is a dual-core Programmable Real-Time Unit Subsystem (PRUSS) that runs up to 333MHz.

The PRU subsystem is intended for driving GPIO for cycle-accurate protocols such as additional:

- General Purpose Input/Output (GPIO)
- Universal Asynchronous Receiver/Transmitter (UART)
- Inter-Integrated Circuit (I2C)
- External ADC interface

7.3.3.1.2 PRUSS Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links
2. Pin attributes and signal description
3. Electrical characteristics, timing parameters and any additional available information
4. Provision for series resistors added for all the interface signals to minimize reflections and to isolate for testing
5. Parallel pull added for any of the processor or attached IOs that can float

6. External ESD protection when the interface signals are connected directly to external connector
7. Industrial communication subsystem features including Ethernet (MII signals and MDIO signals are not pinned out) are not supported

7.3.4 Universal Asynchronous Receiver/Transmitter (UART)

Verify the application requirements for UART interface (external communication interface or debug) and configuration (2-wire or 4-wire with flow control). For the number of UART instances supported, see the processor-specific data sheet.

When an external transceiver is used, match the external interface signal IO levels and the dual-voltage IO supply for IO group voltage level. The recommendation is to power the IO supply of the transceiver and the processor IO supply rail from the same source. Verify fail-safe operation and the pullup voltage reference as required.

The recommendation is to provision the series resistors on the interface signals, close to source, for isolation or debug.

A pullup is recommended on the processor UART receive pins (UARTn_RXD (n = 0-6), MCU_UART0_RXD, and WKUP_UART0_RXD). Verify the availability of pulls on the external interface signal and configure the pull accordingly.

External ESD protection is recommended in case the interface signals from the processor are directly connected to external inputs.

The UART interface is frequently hooked up incorrectly. Connect the signals as below:
- TX to RX
- RX to TX

Verify the connections if additional interface signals are used.

When the debug interface UART signals are directly connected to external interface, take note of fail-safe operation, IO levels. Provide provision for external ESD protection.

7.3.4.1 Universal Asynchronous Receiver/Transmitter (UART) Checklist

General

Review and verify the following for the custom schematic design:
1. Above section including relevant application notes and FAQ links
2. Pin attributes and signal description
3. Electrical characteristics, timing parameters, and any additional available information
4. Provision for series resistors near to source added for all the interface signals to minimize reflections or isolate for testing
5. Parallel pull added for any of the processor or attached IOs that can float
6. Interface signal polarity and connection
7. External ESD protection when the interface signals are connected directly to external inputs
8. Required speed, programmed Baud rate versus supported baud rate, and required versus calculated error due to clock divider mismatch

Schematic Review

Follow the below list for the custom schematic design:
1. Pullup values used (10kΩ or similar) and compare with the SK schematics.
2. Series resistor value used (22Ω) and the placement (near to source).
3. Pullup referenced to the processor VDDSHVx for corresponding UART instance and signals.
4. Processor VDDSHVx and the attached device IO supply sourced from the same supply.
5. Processor IOs are not fail-safe. Applying an input before the processor supply ramps is not allowed or recommended.
6. Supply rails connected follow the ROC.

Additional

1. Verify fail-safe operation when connected to external interface signals. Applying an external input signal before processor supply ramps can cause voltage feed and can affect the custom board functions.
2. Verify recommendations as per the data sheet or EVM implementation have been considered for the attached device including terminations and external ESD protection.

7.3.5 Controller Area Network (CAN)

For the number of CAN instances supported, see the processor-specific data sheet. The CAN interface to the processor includes external CAN transceiver.

When an external transceiver is used, match the external interface signal IO levels with the dual-voltage IO supply for IO group voltage level.

Provide the required terminations for the CAN transceiver.

Recommend provisioning for series resistors on the interface signals (close to source) for isolation or debug.

7.3.5.1 Controller Area Network Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes and signal description
3. Electrical characteristics, timing parameters, and any additional available information
4. Provision for series resistors added for all the interface signals to minimize reflections or isolate for testing
5. Parallel pull added for any of the processor or attached device IOs that can float

Schematic Review

Follow the below list for the custom schematic design:

1. Series resistor value used (0Ω) and the placement (near to source)
2. Pullup referenced to the processor VDDSHVx for corresponding CAN instance and pins
3. Processor VDDSHVx and the attached device IO supply sourced from the same supply
4. Processor IOs are not fail-safe. No input can be applied before the processor supply ramps
5. Supply rails connected follow the ROC

Additional

1. Verify fail-safe operation when connected to external interface signals. Applying an external input signal before processor supply ramps can cause voltage feed and can affect the custom board functions.
2. Verify recommendations as per the data sheet or EVM implementation have been considered for the attached device including terminations and external ESD protection.

7.4 On-board Synchronous Communication Interface (MCSPI, MCASP and I2C)

7.4.1 Multichannel Serial Peripheral Interface (MCSPI) and Multichannel Audio Serial Ports (MCASP)

Provide series resistors (22Ω) for SPI clock outputs SPI0..2_CLK (MCSPI 0..2) and MCU_SPI0..1_CLK (MCU_MCSPI 0..1) (close to processor).

Provide series resistors (22Ω) for transmit clock (Transmit Bit Clock) outputs MCASP0..2_ACLKX and Transmit Frame Sync signals MCASP0..2_AFSX (close to processor).

Provide series resistors (22Ω) for receiver clock (Receive Bit Clock) outputs MCASP0..2_ACLKR and Receive Frame Sync signals MCASP0..2_AFSR (close to attached device).

Processor IO buffers are off during reset. Verify external parallel pulls are provided for SPI Chip Select signals SPI0..2_CS0..3 (MCSPI 0..2) and MCU_SPI0..1_CS0..3 (MCU MCSPI 0..1) (close to attached device). Add pulls to the processor and the attached device inputs that can float.

7.4.1.1 MCSPI Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links
2. Pin attributes and signal description
3. Electrical characteristics, timing parameters and any additional available information
4. Interface configuration and recommended connections (including IOSET)
5. Series resistor (22Ω) added to the clock outputs near to the processor clock output pin
6. Parallel pull (pulldown for attached device clock input) added for any of the processor or attached IOs that can float
7. Performance and signal integrity related concerns have been analyzed (simulated) when connecting to multiple attached devices
8. Provision for series resistors added for all the interface signals to minimize reflections or isolate for testing
9. Configuration of SPI data D0 and SPI data D1 bits (data direction)

Schematic Review

Follow the below list for the custom schematic design:

1. Pullup values used (10kΩ or similar)
2. Series resistor value used (22Ω) and the placement (near to processor pin)
3. Pullup referenced to the processor VDDSHVx for corresponding MCSPI instance and pins
4. Processor VDDSHVx and the attached device IO supply are sourced from the same supply
5. Supply rails connected follow the ROC

Additional

1. Verify fail-safe operation when connected external interface connector (carrier or add-on board). Applying an external input before supply ramps can cause voltage feed and can affect the custom board functions
2. Verify recommendations as per the data sheet or EVM implementation have been considered for the attached device including terminations

7.4.1.2 MCASP Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links
2. Pin attributes and signal description
3. Electrical characteristics, timing parameters and any additional available information
4. MCASP interface configuration and recommended connections (including IOSET)
5. Series resistor 22Ω added to the clock outputs (transmit bit clock, frame sync) near to the processor clock output pin
6. Parallel pull (pulldown for clock output) added for any of the processor or attached IOs that can float
7. Performance and signal integrity related concerns have been analyzed (simulated) when connecting to multiple attached devices
8. Provision for series resistors added for all the interface signals to minimize reflections or isolate for testing

Schematic Review

Follow the below list for the custom schematic design:

1. Pullup values used (10kΩ or similar) and compare with the SK schematics
2. Series resistor value used (22Ω) and the placement (near to processor pin)
3. Pullup referenced to the processor VDDSHVx for corresponding MCASP instance and pins
4. Processor VDDSHVx and the attached device IO supply sourced from the same supply
5. Supply rails connected follow the ROC

Additional

1. Verify fail-safe operation when connected to external signals. Applying an external input before supply ramps can cause voltage feed and can affect the custom board functions
2. Verify recommendations as per the data sheet or EVM implementation have been considered for the attached device including terminations and external ESD protection
3. Two devices can be connected to MCASP. The recommendation is to follow good or recommended layout practices when routing the bit clock (transmit bit clock and receive bit clock). Perform simulations using IBIS model.

7.4.2 Inter-Integrated Circuit (I2C)

Verify if the application requires an I2C interface that is fully compliant to I2C-bus specification. The MCU_I2C0 and WKUP_I2C0 are fail-safe, true open-drain output type buffers, and are fully compliant to the I2C specifications. I2C can support 3.4Mbps I2C operations (when the IO buffers (interface) are operating at 1.8V).

Note

For I2C interfaces with open-drain output type buffer (MCU_I2C0 and WKUP_I2C0), an external pull is recommended, irrespective of peripheral usage and the IO configuration.

Refer to the *Pin Connectivity Requirements* section of the processor-specific data sheet. A pullup (4.7kΩ, adjust after testing) is recommended.

When the open-drain output type buffer I2C interfaces are pulled to 3.3V supply, the IOs have slew rate requirements specified. An RC can be used to limit the slew rate. For RC implementation, refer *Starter Kit SK-AM62P-LP* for implementation.

For more information, see the *Connecting Supply Rails to Pullups* section.

In the case that additional I2C interfaces are required, use I2C0-3 interfaces.

I2C0-3 interface uses LVCMOS output type buffer IOs to emulate an open-drain output type buffer and are not fully compliant with the I2C specification, in particular falling edges are fast (< 2ns). Any devices connected to I2C0-3 ports need to function properly with the faster fall time. I2C0-3 ports support 100kHz and 400kHz operation. Pullups are recommended for I2C signals when the IOs are configured for I2C interface. Connect the pullups with the shortest possible stub.

For I2C0-3 interface, use series resistors to control the falling edge rate. The value depends on the custom board design and is recommended to be finalized during testing.

For more information, see the following FAQs:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – I2C interface

[FAQ] AM62A7-Q1: Internal pull configuration registers for MCU_I2C0 and WKUP_I2C0

If the plan is to use TI provided software, connect the recommended processor I2C (I2C0 for AM62x - TPS65219) interface to the PMIC, as I2C0 is the I2C interface used for PMIC control.

Note

When an I2C3 interface is used, refer to the I2C3 note (can be multiplexed to more than one pin) in the *Timing and Switching Characteristics, Peripherals, I2C* section of the processor-specific data sheet.

Note

Refer to the *Exceptions* in the *Timing and Switching Characteristics, I2C* section of the processor-specific data sheet during the custom board design. Take note of the exceptions for the simulated I2C interface in the data sheet. Add a low pass filter to reduce the fall time or interface speed to match the timing.

7.4.2.1 I2C (Open-drain Output Type Buffer) Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links.
2. Pin connectivity requirements (during reset, RX buffers are enabled. A pullup (4.7kΩ, adjust after testing) is recommended irrespective of IO configuration), pin attributes and signal description.
3. Electrical characteristics (fail-safe and slew rate requirements when pulled to 3.3V), timing parameters and any additional available information including exceptions.
4. RC at the input of the open-drain IOs for slew rate control when pulled to 3.3V.
5. Attached device address pin connected to IO supply through a resistor (> 1kΩ).
6. Verify the target I2C interface clock rates. The I2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I2C port.
7. Verify that there are no I2C address conflicts on any of the I2C interface utilized. There are multiple I2C ports available on the processor, so if a conflict is seen, move the conflicting devices to a different I2C bus. If this is not possible, use an I2C bus switch.
8. Do not place more than one set of pullup resistors on the I2C lines. This can result in excessive loading and potential incorrect operation. Choose the pullup value commensurate with the bus speed being utilized.
9. Make sure that the supply rail powering the processor I2C IO supply for IO group matches the supply voltage used for the pullup resistors and the attached I2C devices. Proper pullup can prevent device damage or incorrect operation due to voltage mismatch.

Schematic Review

Follow the below list for the custom schematic design:

1. WKUP_I2C0 and MCU_I2C0 controllers have dedicated I2C compliant open-drain output type buffers.
2. Verify the pullup values used. Compare with the SK schematics or calculate based on the load.
3. The I2C pullup supply amplitude connected follows the steady-state maximum voltage at all fail-safe IO pins requirements. The supply threshold depends on the supply voltage connected to IO supply for IO group.
4. Provision for RC to limit slew rate and RC values.
5. Processor VDDSHVx and the attached device IO sourced from the same supply.
6. Supply rails connected follow the ROC.

Additional

1. Verify recommendations as per the data sheet or EVM implementation have been considered for the attached device.
2. Review the *Timing and switching characteristics*, *I2C Exceptions* sections of the data sheet during the design stage.

7.4.2.2 I2C (Emulated Open-drain Output Type Buffer) Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links
2. Pin attributes and signal description
3. I2C interface configuration and recommended connections (including IOSET)
4. Electrical characteristics, timing parameters and any additional available information including exceptions
5. Attached device address pin connected to IO supply through a resistor (> 1kΩ)
6. A pullup is recommended when IO is configured as I2C interface
7. Note the I2C exceptions in the timing and switching characteristics section of the processor-specific data sheet

Schematic Review

Follow the below list for the custom schematic design:

1. Verify the pullup resistor values used
2. Pullup referenced to the processor VDDSHVx (I2C pullup connected to correct voltage)
3. Addition of series resistor (low pass filter) for fall time control
4. Fail-safe interface (emulated IOs are not fail-safe, no input can be applied before the processor supply ramps)
5. Processor VDDSHVx and the attached device IO sourced from the same supply
6. Supply rails connected follow the ROC

Additional

1. Verify fail-safe operation when connected to external interface signals. Applying an external input before supply ramps can cause voltage feed and can affect the custom board functions
2. Review the *Timing and switching characteristics*, *I2C Exceptions* section of the data sheet during the design stage
3. I2C controllers are multiplexed with standard LVCMOS IO, connected to emulate open-drain

7.5 User Interface (CSIRX0, DPI, OLDI0), GPIO and Hardware Diagnostics

7.5.1 Camera Serial Interface (CSI-Rx (CSI-2 port, CSIRX0 Instance))

Refer to the processor-specific data sheet for supported data rate.

7.5.1.1 CSIRX0 Used

The processor CSIRX0 interface is powered by CSIRX0 core supply VDDA_CORE_CSIRX0 and CSIRX0 1.8V analog supply VDDA_1P8_CSIRX0.

Connect a resistor between CSI0_RXRCALIB (close to processor) and VSS. Refer to the processor-specific data sheet for recommended resistor value and tolerance.

For more information on CSIRX0, see the *[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM62A / AM62P Custom board hardware design – CSI-2 capabilities*.

7.5.1.2 CSIRX0 Not Used

CSIRX0 when not used has specific connection requirements for interface signals and power supplies.

For connecting the interface signals, power supplies (core and analog), see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

When boundary scan function is used, CSIRX0 supplies (VDDA_CORE_CSIRX0 and VDDA_1P8_CSIRX0) are required to be connected to the recommended supply rails. Decoupling capacitors on the supply pins are recommended. Bulk capacitors and ferrites are optional.

When the boundary scan function is not used, connect CSIRX0 supplies (VDDA_CORE_CSIRX0 and VDDA_1P8_CSIRX0) to VSS through separate 0Ω resistors. Decoupling capacitors, bulk capacitors and ferrites are not recommended to be populated.

7.5.1.3 CSIRX0 Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links
2. Pin connectivity requirements, pin attributes and signal description
3. Electrical characteristics, timing parameters and any additional available information
4. Connection of recommended IO calibration resistor
5. Connection of the CSIRX0 interface signals with attached devices including the polarity
6. Marking of differential signals and the differential impedance value

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of the CSIRX0 interface signals to the attached device
2. Ferrite and capacitors used for CSIRX0 analog and core supply, when CSIRX0 interface is used
3. Connection of CSIRX0 analog and core supply with optional ferrite and bulk caps and IO calibration resistor, when CSIRX0 interface not used. But, boundary scan functionality is required
4. Pin connectivity requirement when boundary scan is not used
5. Supply rails connected follow the ROC

Additional

1. Need for external ESD protection based on the use case
2. Verify fail-safe operation when connected to external signals. Applying an external input before supply ramps can cause voltage feed and affect the processor performance

7.5.2 Display Subsystem

7.5.2.1 Display Parallel Interface (DPI)

7.5.2.1.1 AM625 / AM623 / AM625SIP / AM625-Q1

Refer below FAQ:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 Custom board hardware design – Display Parallel Interface (DPI) 24-bit RGB.

7.5.2.1.1.1 IO Power Supply

The processor DPI interface is powered by VDDSHV3 supply rail (IO supply for IO group 3).

7.5.2.1.1.2 DPI (Attached Device) Reset

The recommendation is to implement the attached device reset using a 2-input ANDing logic. Processor general purpose input/output (GPIO) is connected as one of the input to the AND gate with provision for pullup (to support boot) near to the input and 0Ω to isolate the GPIO for testing or debug. The other AND gate input is the main domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and processor main domain warm reset status output (RESETSTATz) is used to reset the attached device, match the IO voltage level of the attached device and RESETSTATz. A level translator is recommended to match the IO voltage level.

7.5.2.1.1.3 Connection

Verify display (RGB) connections.

Interface support includes 12-, 16-, 18-, and 24-bit RGB active matrix displays. When connecting only 16-bit data to an 18-bit panel (BGR565 to BGR666), connect D0-D4 to B1-B5 on LCD, D5-D10 to G0-G5 on the LCD, and D11-D15 to R1-R5 on LCD. On the 18-bit panel, connect B0 to B5 and R0 to R5.

7.5.2.1.1.4 Signals Connection

Provide provision for connecting a series resistor (0Ω) for VOUT0_PCLK (Pixel Clock Output) (close to processor). If space is not a constraint, recommend adding series resistors (0Ω) for all other control and data pins.

7.5.2.1.1.5 Capacitors for the Power Supply Rails

Verify the required bulk and decoupling capacitors are provided for VDDSHV3 supply rail and the attached device.

Follow the processor-specific SK implementation whenever recommendations are not available.

7.5.2.1.1.6 DPI (VOUT0) Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links
2. Pin connectivity requirements, pin attributes and signal description
3. Electrical characteristics, timing parameters and any additional available information
4. Addition of series resistor 0Ω for the clock output near to the processor
5. Optional series resistors for the control and data interface signals

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of the interface signals including DPI pin mapping of the processor with the attached device RGB and control signals
2. Supply rails connected follow the ROC
3. Compare the decoupling capacitor of DPI IO supply used versus relevant SK

Additional

1. Need for external ESD protection based on the use case

7.5.2.1.2 AM620-Q1

Interface Not Supported.

7.5.2.2 Open LVDS Display Interface (OLDI)

Refer to the processor-specific data sheet for supported display resolution.

7.5.2.2.1 AM625 / AM623 / AM625SIP / AM625-Q1

7.5.2.2.1.1 OLDI0 Used

Refer below FAQ:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM62P Custom board hardware design – OLDI (Open LVDS Display Interface) capabilities.

7.5.2.2.1.1.1 IO Power Supply

The processor OLDI interface is powered by VDDA_1P8_OLDI0 (OLDI0 1.8V analog supply rail).

7.5.2.2.1.1.2 OLDI (Attached Device) Reset

The recommendation is to implement the attached device reset using a 2-input ANDing logic. Processor general purpose input/output (GPIO) is connected as one of the input to the AND gate with provision for pullup (to support boot) near to the input and 0Ω to isolate the GPIO for testing or debug. The other AND gate input is the main domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and processor main domain warm reset status output (RESETSTATz) is used to reset the attached device, match the IO voltage level of the attached device and RESETSTATz. A level translator is recommended to match the IO voltage level.

7.5.2.2.1.1.3 OLDI Interface Compatibility

For verifying the voltage level compatibility, see the *OLDI LVDS (OLDI) Electrical Characteristics* section of the processor-specific data sheet.

7.5.2.2.1.1.4 Capacitors for the Power Supply Rails

Verify the required bulk and decoupling capacitors are provided for VDDA_1P8_OLDI0 supply rail.

Follow the processor-specific SK implementation whenever recommendations are not available.

7.5.2.2.1.1.5 OLDI0 Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links
2. Pin connectivity requirements, pin attributes and signal description
3. Electrical characteristics, timing parameters and any additional available information
4. Connection of the OLDI0 interface signals with attached devices including the polarity of the signals
5. Marking of differential signals and the differential impedance value
6. Configuration of the required terminations
7. When not used, connection of the recommended power supply and signals as per the pin connectivity requirements

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of 1 x 8 lane (dual link mode) and 2 x 4 lane (single link, mirror mode) OLDI0 signals
2. Supply rails connected follow the ROC

Additional

1. Need for external ESD protection based on the use case

7.5.2.2.1.2 OLDI0 Not Used

OLDI0 when not used has specific connection requirements for interface signals. For connecting the interface signals, see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

The OLDI0 1.8V analog supply rail (VDDA_1P8_OLDI0) is recommended to be powered by a valid 1.8V source. Ferrite and bulk capacitor are optional.

7.5.2.2.1.3 Additional Information

The signals are recommended to be connected as a point-to-point interface from the processor to a connector (display). without stubs.

Any board-level implementation is required to comply with the physical layer definition of *IEEE1596.3* standard and *ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) interface Circuits)*.

7.5.2.2.2 AM620-Q1

Not Supported.

7.5.3 General Purpose Input/Output (GPIO)

Refer below FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Data sheet Pin Attributes and Pin connectivity related queries

7.5.3.1 Availability of CLKOUT on Processor GPIO

Buffered output of MCU_OSC0_XO is available after reset on the WKUP_CLKOUT0 for AM62x processor family.

7.5.3.2 Connection and External Buffering

The recommendation is to add a series resistor (with a value that is use case dependent) to limit the current. Externally buffer the GPIO outputs when higher (above the data sheet specified value) current sourcing is required.

Common processor LVCMOS IO interface guidelines:

1. Most of the processor IOs are not fail-safe. No input can be applied before supply ramps.

2. Processor LVCMOS IOs have slew rate requirements specified, applying a slow ramp input or connecting a capacitor directly at the input is not recommended.
3. Connecting a capacitor load > 22pF at the output is not recommended. DNI capacitor or perform simulations based on the use case.
4. Processor IO buffers are off during reset. A pull is required near to the attached device being driven by the processor IO that can float.
5. A parallel pull is recommended for any processor IO pad that has a trace connected. When adding pull is not feasible, route the traces away from noisy signals.

Verify capacitor loading of the processor GPIO output (when capacitor value > 22pF is connected, perform simulations), slew rate of the input signal (LVCMOS input slew is 1000ns or less), IO compatibility, and fail-safe operation between the processor IOs and attached devices.

7.5.3.3 Additional Information

Pins or Pads on unused interfaces can typically be left unconnected, unless otherwise stated. Many of the IOs have a *Pad Configuration Register* that provides control over the input capabilities of the IO (RXENABLE field in each conf_<module>_<pin> register). For more details, refer to the *Control Module* chapter of the processor-specific TRM. Software can disable the IO receive buffers (that is, RXENABLE=0) that are not connected in the design as soon as possible during initialization. Software must not accidentally enable the receiver of an IO (by setting the RXENABLE bit) when the associated pin is floating.

Note

For specific guidance on configuring certain unused pins, refer to the *Pin Connectivity requirements* section of the processor-specific data sheet.

Note

For specific guidance on configuring IOs, refer to the *Pad Configuration Registers* chapter of the processor-specific TRM.

For more information on processor unused peripherals and IOs, see the *[FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – SOC Unused peripherals and IOs*.

For more information on used pins, unused pins, and peripherals handling, see the *[FAQ] AM62x, AM64x, AM243x, Custom board hardware design – How to handle Used / Unused Pins / Peripherals ? (e.g. GPIOs, SERDES, USB, CSI, MMC (eMMC, SD-card), CSI, OLDI, DSI, CAP_VDDSn, ...)*.

7.5.3.4 GPIO Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links.
2. Pin connectivity requirements and pin attributes.
3. Electrical characteristics and any additional available information.
4. Input signal applied to the processor LVCMOS inputs follow the slew rate requirements. Connecting a capacitor directly at the input increases the signal slew and is not recommended.
5. Connection of capacitor load directly to the processor output for control or enabling of attached device is not allowed (recommend simulation when capacitor load > 22pF (place holder) is used).
6. All IO pins referenced to VDDSHVx or VDDSHV_MCU or VDDSHV_CANUART connect to one voltage level. Each IO has an associated supply voltage used to power the IO cell (VDDSHVx). If VDDSHVx is sourced from 3.3V (1.8V) supply, all IO referenced to VDDSHVx rail operate at 3.3V (1.8V) levels.
7. No input voltage applied to the processor IOs before the VDDSHVx supply ramps (excluding fail-safe IOs). Most processor IOs are not fail-safe. Applying voltage to the IOs is not recommended or allowed, while the corresponding IO supply for IO group (VDDSHVx) is off. Fail-safe IOs include MCU_PORz, WKUP_I2C0_SCL, WKUP_I2C0_SDA, MCU_I2C0_SCL, MCU_I2C0_SDA, EXTINTn, and USBn_VBUS (n = 0-1), when a recommended VBUS divider is used.

8. One of the common use case for the IO interface is driving LEDs for indication. The designer can review the LED source or sink current and the effect on the voltage level and adjust the LED current accordingly.
9. Shorting of multiple IOs together directly is not recommended.
10. Pad configuration based on the required IO direction.
11. Directly connecting processor IOs with alternate functions to supply or VSS is not allowed or recommended, including boot mode inputs. The board designer can have errors with the firmware and miss-configure the LVCMOS GPIOs that are intended as inputs, to be outputs driving logic high instead.

Schematic Review

Follow the below list for the custom schematic design:

1. Pulls are added for any of the processor or attached device IOs that can float.
2. Pullups are connected to the same IO supply for IO group VDDSHVx referenced by the IOs.
3. The supply voltage for all pullups that are connected to processor IOs matches the voltage applied to the corresponding IO supply for IO group (VDDSHVx). Pulling a signal to the wrong IO voltage causes voltage leakage between the IO rails of the device.
4. IO level compatibility for externally applied inputs from a add-on or carrier board or through an external connector.
5. Supply rails connected follow the ROC.

Additional

1. Common processor LVCMOS IO interface guidelines, refer to *Section 7.5.3.2*.
   - Most of the processor IOs are not fail-safe. This is not allowed or recommended to apply input before supply ramps.
   - Processor LVCMOS IOs have slew rate requirements specified, applying a slow ramp input or connecting a capacitor directly at the input is not recommended.
   - Connecting a capacitor load > 22pF (place holder) at the output is not recommended. DNI capacitor or perform simulations based on the use case.
   - Processor IO buffers are off during reset. A pull is required near to the attached device being driven by the processor IO that can float.
2. A parallel pull is recommended for any processor IO pad that has a trace connected. When adding pull is not feasible, route the traces away from noisy signals. Processor IO buffers are off during reset. A pullup is recommended near to the attached device, to hold the attached device IO inputs that can float in a known state. Use of pulls are attached-device dependent.
3. IO compatibility and fail-safe operation between the processor IOs and attached devices connected through IOs.
4. Fail-safe operation when connected to external signals. Applying an external input before supply ramps cold causes voltage feed and affects the processor performance.
5. Capacitor loading of the processor output (when capacitor value > 22pF (place holder) is connected, designer must simulate), slew of the input signal (LVCMOS input slew is 1000ns or less).
6. IO current sink or source follows the data sheet recommendations.
7. External ESD protection is provided when the IOs connect directly to external interface signals.

7.5.4 On-board Hardware Diagnostics

7.5.4.1 Monitoring of On-board Supply Voltages Using Processor Voltage Monitors

Voltage monitor pins can be used to monitor the external supply rails. The VMON_1P8_SOC and VMON_3P3_SOC can be directly connected to 1.8V or 3.3V. The VMON_VSYS is connected through an external voltage divider and provides flexibility to monitor any of the supply rail.

7.5.4.1.1 Voltage Monitor Pins Used

The recommendation is to connect the main DC voltage rail powering the board (such as 5V or higher) to the VMON_VSYS pin through an external resistor voltage divider (0.45V ± 3 %) for early supply failure indication. The recommendation is to implement a noise filter (capacitor) across the resistor voltage divider output since

VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients as described in the *System Power Supply Monitor Design Guidelines* section of the processor-specific data sheet.

Connect VMON_1P8_SOC and VMON_3P3_SOC pins directly to the respective supplies. See the *Recommended Operating Conditions* section of the processor-specific data sheet for the allowed supply voltage range.

Note

For VMON_VSYS, the fail-safe condition is valid when the recommendations in section *System Power Supply Monitor Design Guidelines* of processor-specific data sheet are followed.

For VMON_1P8_SOC and VMON_3P3_SOC pins, the fail-safe condition is valid when the supply voltage connected is within the *Recommended Operating Conditions* section of processor-specific data sheet.

For more information, see the *[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – POK VMON Voltage Monitor*

7.5.4.1.1.1 Voltage Monitor Checklist

General

Review and verify the following for the custom schematic design:

1. Above section including relevant application notes and FAQ links
2. Pin attributes and signal description
3. The recommendation is to provide provision to connect an external resistor divider as per *System Power Supply Monitor Design Guidelines* section of the data sheet for early detect using VMON_VSYS
4. For VMON_VSYS detection to be effective, connect a DC voltage of 5V or higher
5. VMON_VSYS - add a filter capacitor. Refer processor data sheet section *System Power Supply Monitor Design Guidelines*. The value of the capacitor is determined by the designer based on the trip time requirement
6. Direct connection of 1.8V to VMON_1P8_SOC and 3.3V to VMON_3P3_SOC pins without any external filter capacitors

Schematic Review

Follow the below list for the custom schematic design:

1. 1% tolerance resistors are used for the VMON voltage divider resistors
2. Addition of filter capacitor and selection of capacitor value (select based on the power architecture)

Additional

1. The recommendation is to always implement the voltage monitoring functionality using VMON_VSYS for early detection of supply failure. VMON_VSYS is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example: 5V, 12V, or 24V. The error associated with the VMON_VSYS monitor requires setting the threshold significantly lower than the nominal to avoid false trigger. Refer to the *System Power Supply Monitor Design Guidelines* section of the data sheet

7.5.4.1.2 Voltage Monitor Pins Not Used

The recommendation is to use VMON_VSYS for early supply failure indication. When not used, connect VMON_VSYS and VMON_3P3_SOC pins to VSS through separate 0Ω resistors and add a test point for future expansion.

The recommendation is to connect the VMON_1P8_SOC pin to respective supply. Grounding VMON_1P8_SOC pin shorts the internal 1.8V supply.

7.5.4.2 Internal Temperature Monitoring

The temperature monitors are placed near the anticipated hot spots of the processor. Read the on-die temperature sensors in Linux and perform thermal management. See the *E2E thread*.

The Voltage and Thermal Manager (VTM) module on the processor supports voltage and thermal management of the processor by providing control of on-chip temperature sensors.

The processor supports one VTM module, VTM0, which is located in the WKUP domain.

For more information, see *[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – VTM*.

7.5.4.2.1 Internal Temperature Monitoring Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Pin attributes and signal description
3. Connection of the recommended supply

Schematic Review

Follow the below list for the custom schematic design:

1. Addition of filter capacitors for the TEMPn (n = 0-1) supply pins

7.5.4.3 Connection of Error Signal Output (MCU_ERRORn)

The recommendation is to connect the MCU_ERRORn signal as per the *Pin Connectivity Requirements* section of the processor-specific data sheet for testing or when using the signal for other board level functions.

7.5.4.4 High Frequency Oscillator (MCU_OSC0) Clock Loss Detection

The processor supports HFOSC0 clock loss detection circuitry to detect HFOSC0_CLK malfunction (stops). Dedicated hardware logic monitors HFOSC0 clock using CLK_12M_RC clock. When HFOSC0_CLK stops toggling for 9 CLK_12M_RC clock periods, a HFOSC0 clock stop loss condition is detected. If CTRLMMR_MCU_PLL_CLKSEL [8] CLKLOSS_SWTCH_EN is set, the reference clock is switched from HFOSC0_CLKOUT to CLK_12M_RC to allow the processor to operate with a slower clock.

During clock-loss condition, the processor reports the error to the external device through MCU_ERRORn pin by driving the pin low. The recovery mechanism is up to the external device (such as a PMIC to take action).

Example, doing a full board power cycle to see if the board recovers. If the board does not recover then the processor has to indicate board designer to take alternate actions or perform board level tests such as checking on-board system clocks, external crystal or supply rails.

7.6 Verifying Board Level Design Issues

7.6.1 Processor Pin Configuration Using PinMux Tool

Recommend verifying the processor peripheral and IO configuration using the TI *SysConfig-PinMux* tool to take care valid IOSETs have been configured.

For more information, see the PinmuxConfigSummary.csv file provided by the SysConfig-PinMux tool.

7.6.2 Schematics Configurations

Verify the circuit options provided for alternate functionality or testing that are optional for the normal functioning of the board or can affect or influence custom board performance are marked as DNI.

7.6.3 Connecting Supply Rails to Pullups

Connecting a signal pullup to the wrong IO supply rail can cause leakage between the IO rails of the processor and affect the custom board performance or processor reliability. Each signal has an associated IO supply

for IO group (for example, VDDSHVx [x = 0-6]). For more information, see the *Pin Attributes* table in the processor-specific data sheet.

For example, to pullup SPI0_CLK signal in any MUX mode (EHRPWM1_A, GPIO1_17, and so forth), pullup the signal supply rail connected to VDDSHV0.

7.6.4 Peripheral (Subsystem) Clock Outputs

For any of the processor peripheral that has a clock output, configure the RXACTIVE bit of the appropriate CTRLMMR_MCU_PADCONFIGx, CTRLMMR_PADCONFIGy registers. The bit configuration is required for the clock output to work properly.

7.6.5 General Board Bring-up and Debug

Board bring-up tips:

Before starting the board bring-up, verify the following:

- The processor and the attached devices used match the design requirements
- Boards have been checked for component assembly (DNI (Do Not Install) and inspected for assembly (soldering of the components))
- No external inputs are connected to the processor IO inputs before the board supply is applied and processor supply ramps

Refer to *[FAQ] Board bring up tips for Sitara devices (AM64x,AM243x, AM62x, AM62Ax, AM62Px)*.

7.6.5.1 Clock Output for Board Bring-Up, Test, or Debug

The following clock outputs are available on the processor for test and debug purposes only:

- OBSCLK0, MCU_OBSCLK0 (recommended): Observation clock outputs

  OBSCLK0, MCU_OBSCLK0 are observation clock outputs for test and debug purposes only. OBSCLK pins can be used to select one of the several different clocks as output. The OBSCLK signal is not expected to be used as a clock source for any external device. As stated in the data sheet, OBSCLK0 signal is provided for test and debug purposes only.
- SYSCLKOUT0 (optional): SYSCLK0 is divided by four and then sent out of the processor as a LVCMOS clock signal (SYSCLKOUT0)
- MCU_SYSCLKOUT0 (optional): MCU_SYSCLK0 is divided by four and then sent out of the processor as a LVCMOS clock signal (MCU_SYSCLKOUT0)

In case the processor pins designated OBSCLK0 (available on two pins in AM62x), MCU_OBSCLK0, SYSCLKOUT0, MCU_SYSCLKOUT0 are not used, provide a test point for test or debug. Recommend adding pull resistors to the pads.

In case clock output pins are used, a test point can be inserted on the trace and provision to isolated the signals from the attached devices can be provided for test or debug.

System clock output pins (MCU_SYSCLKOUT0 and SYSCLKOUT0) are hardwired to dedicated clock resources.

7.6.5.2 Additional Information

The recommendation is to provide test points for MCU_RESETSTATz, RESETSTATz and PORz_OUT for testing or debug when not used.

For other on-board devices (DC/DC Converter or LDO or Sensor) that have an alert output, over-current indication output or PG (power good) output that is not used, provide a pullup and test point for testing or future enhancements.

7.6.5.3 General Board Bring-up and Debug Checklist

General

Review and verify the following for the custom schematic design:

1. Add provision to isolate the IOs that can be used for debug from alternate function

2. Add provision for connecting UART interfaces for debug during initial board build
3. Add provision for JTAG connector or Test points for JTAG interface connection including external ESD protection. Place the pulls as per pin connectivity requirements near to the processor JTAG interface pins

Schematic Review

Follow the below list for the custom schematic design:

1. The required pullup and series resistors are provided for the UART interfaces used for debug when external interface signals are directly connected to the processor UART signals
2. External ESD protection when external interface signals are directly connected to the processor UART signals

Additional

1. Processor UART and most of the IO signals are not fail-safe. Recommendation is to apply external inputs only after the processor supplies ramp
2. The recommendation is to disconnect the external interface signals when processor board is powered off

Refer [FAQ] SK-AM62: Purpose Of Different UARTs.

8 Self-Review of the Custom Board Schematics Design

Once the schematics design is completed following the design guidelines provided in the application note and referring to the SK schematics and other available collaterals, customer can do a self review using the check list provided at the end of each design guidelines section.

Example:

Processor Core and Peripheral Core Power Supply Checklist

General Board Bring-up and Debug Checklist

The below FAQ lists the collaterals and steps that can be followed for performing self-review of custom board schematics:

[FAQ] AM625 / AM623 / AM625SIP / AM620-Q1 / AM625-Q1 Design Recommendations / Custom board hardware design - Custom board schematics self-review

The below FAQ lists common errors observed while reviewing customer schematics. The recommendation is to read the list and make the required updates:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - List of errors observed during customer schematics review

9 Layout Notes (Added on the Schematic)

Recommend adding required design notes for the processor peripherals (Example: USB2.0 interface, Ethernet interface, Camera interface, Display (OLDI0) interface (AM625 / AM623 / AM625SIP / AM625-Q1), eMMC, OSPI, SD, and other available processor peripherals). Notes added can include Board Boot mode configurations, placement of series and parallel resistors, placement of decoupling and bulk capacitors.

Consider adding the required or applicable design notes to the processor attached devices and on-board devices.

Mark all differential signals, critical signals and specify the target impedance (as required). See the following examples:

- *AM62x DDR Board Design and Layout Guidelines* for the recommended target impedance for DDR4 and LPDDR4 signals. Additionally refer to the *AM62Ax / AM62Px DDR Board Design and Layout Guidelines*.
- The differential impedance for the USB2.0 data lines must be within the specified tolerance for a nominal value of 90Ω.
- The differential impedance for the CSI-Rx and OLDI signals must be within the specified tolerance for a nominal value of 100Ω.

See the following FAQs:

[FAQ] AM625: PCB Pattern Recommendations for Specific Peripherals

[FAQ] AM625: MMC0 PCB Connectivity Requirements

AM6442: PCB layout guidelines for MMCSD0(eMMC) and MMCSD1(SD card)

9.1 Layout Checklist

General

Review and verify the following for the custom schematic design:

1. Above sections, including relevant application notes and FAQ links
2. Is the custom board designed to be compliant to the PCB trace delay requirements defined in the *Timing Conditions* table found in the *Timing and Switching Characteristics* section of the processor data sheet
3. *Applications, Implementation, and Layout* section of the data sheet and followed the relevant sections

10 Custom Board Design Simulation

The baseline drive impedance and ODT settings for memory (DDR4/LPDDR4) derived from the signal integrity (SI) simulations performed on the SK.

The recommendation is to perform simulation for the custom design as the configuration values can differ.

Refer below FAQs:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1/ AM6442 / AM2432 Custom board hardware design – S-parameter and IBIS model of IO-buffer

[FAQ] Using DDR IBIS Models for AM64x, AM62x, AM62Ax, AM62Px

To get an overview of the board extraction, simulation, and analysis methodologies for high speed LPDDR4 interface, see *LPDDR4 Board Design Simulations* chapter of the *AM62x DDR Board Design and Layout Guidelines* application note.

The drive strength is adjustable using the *DDR Register Configuration Tool* on SysConfig.

For more information, see the *[FAQ] AM62A7 or AM62A3 Custom board hardware design – Processor DDR Subsystem and Device Register configuration*. The FAQ is generic and can also be used for AM625 / AM623 / AM625-Q1 / AM620-Q1 processor family.

Refer *[FAQ] AM62A3-Q1: AM62A3-Q1 PDN Power SI SIMULATION Questions*. The FAQ is generic and can also be used for AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 processor family.

11 Additional References

Additional references include FAQs and *Hardware Design Considerations for Custom Board Design* document for specific processor. Schematics for attached devices including PMIC and EPHY.

11.1 FAQ Covering AM6xx Processor Family

The following FAQ summarizes key collaterals that can be referenced during custom board design:

[FAQ] AM64x, AM243x, AM62x, AM62Ax, AM62Px Custom board hardware design - Collaterals for Reference during Schematic design and Schematics Review

Note

While using the SK PDF schematics for custom board schematics review and follow the FAQ links for additional information.

11.2 FAQs - Processor Product Family Wise and Sitara Processor Families

Based on interactions with board designers, queries from multiple board designers and learning from board designer queries, FAQs have been created to answer some of the commonly asked design question or provide design guidelines to support board designers during custom board design. Refer to the following list of FAQs that can be used during custom board design along with other available design collaterals including the *Hardware Design Considerations for Custom Board Design* and the *Schematic Design Guidelines and Schematic Review Checklist*:

AM62x Processor Family:

[FAQ] AM625, AM623, AM625SIP, AM625-Q1, AM620-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

AM62Ax Processor Family:

[FAQ] AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

Above FAQ includes the FAQs relevant to AM62D-Q1 processor family.

AM62Px Processor Family:

[FAQ] AM62P, AM62P-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

Sitara Processor Families:

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM64x, AM243x, AM335x) families

See the following FAQ link that lists all the available FAQs including software related FAQs:

[FAQ] AM6x: Latest FAQs on AM62x, AM64x, AM24x, AM3x, AM4x Sitara devices

11.3 Processor Attached Devices

Ethernet PHY PCB Design Layout Checklist

TPS65219 Schematic, Layout Checklist

TPS65931211-Q1 PMIC User Guide for AM62A

Note

Verify availability of device-specific schematic review checklist on TI.com for the attached devices and verify the custom board schematic implementation using the available checklist.

12 Summary

This application note is provided as a design guide for use by board designers during the custom board schematic design and review. The recommendations provided in the document can help designers simplify the board design, reduce schematic errors, reduce board bring-up time, board debug time and can possibly minimize future board re-spins.

13 References

13.1 AM625, AM623, AM625SIP, AM625-Q1, AM620-Q1

- Texas Instruments, *AM62x Sitara™ Processors Data Sheet*
- Texas Instruments, *AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM*
- Texas Instruments, *AM62x Sitara Processors Technical Reference Manual*
- Texas Instruments, *AM62x Silicon Errata*
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM623, AM625, AM625SIP, AM620-Q1, AM625-Q1 Family of Processors*
- Texas Instruments, *Starter Kit SK-AM62B-P1*
- Texas Instruments, *Starter Kit SK-AM62B for discrete power solution*
- Texas Instruments, *Starter Kit SK-AM62-LP*
- Texas Instruments, *Starter Kit SK-AM62-SIP*
- Texas Instruments, *AM62x Power Consumption*
- Texas Instruments, *AM62x Maximum Current Ratings*
- Texas Instruments, *AM62x Power Estimation Tool*
- Texas Instruments, *Powering the AM62x With the TPS65219 PMIC*
- Texas Instruments, *Powering the AM625SIP With the TPS65219 PMIC*
- Texas Instruments, *Discrete Power Solution for AM62x*
- Texas Instruments, *AM625 / AM623 (ALW) Escape Routing PCB Design*
- Texas Instruments, *AM625-Q1 / AM620-Q1 (AMC) Escape Routing for PCB Design*
- Texas Instruments, *AM625SIP (AMK) Escape Routing for PCB Design*
- Texas Instruments, *AM625 / AM623 / AM625-Q1 / AM620-Q1 DDR Board Design and Layout Guidelines*
- Texas Instruments, *PRU-ICSS Feature Comparison*
- Texas Instruments, *How the AM625SIP Processor Accelerates Development by Integrating LPDDR4*
- Texas Instruments, *AM625SIP: System In Package Explained*
- Texas Instruments: *SK-AM62B-P1 Design Package Content Overview (Rev. A)*
- Texas Instruments: *SK-AM62-LP Design Package Content Overview*

- Texas Instruments: *SK-AM62-SIP Design Package Folder and Files List*
- Texas Instruments: *SK-AM62B Design Package Folder and Files List*

13.2 AM62A7 , AM62A3 , AM62A7-Q1 , AM62A3-Q1

- Texas Instruments, *AM62Ax Sitara™ Processors Data Sheet*
- Texas Instruments, *AM62Ax Sitara Processors Technical Reference Manual*
- Texas Instruments, *AM62Ax Silicon Errata*
- Texas Instruments, *Starter Kit SK-AM62A-LP*
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM62A3, AM62A7, AM62A3-Q1, AM62A7-Q1 and AM62D-Q1 Processor Families*
- Texas Instruments, *AM62A3, AM62A7, AM62A3-Q1, AM62A7-Q1 and AM62D-Q1 Processor Families Schematic Design Guidelines and Schematic Review Checklist*
- Texas Instruments, *AM62Ax Maximum Current Ratings*
- Texas Instruments, *AM62Ax Power Estimation Tool*
- Texas Instruments, *PMIC Solution for AM62Ax*
- Texas Instruments, *AM62Ax/AM62Dx Escape Routing for PCB Design*
- Texas Instruments, *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*
- Texas Instruments: *SK-AM62A-LP Design Package Folder and Files List*

13.3 AM62P , AM62P-Q1

- Texas Instruments, *AM62Px Sitara™ Processors Data Sheet*
- Texas Instruments, *AM62Px Sitara Processors Technical Reference Manual*
- Texas Instruments, *AM62Px Silicon Errata*
- Texas Instruments, *Starter Kit SK-AM62P-LP*
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM62P, AM62P-Q1 Family of Processors*
- Texas Instruments, *AM62P, AM62P-Q1 Processor Family Schematic Design Guidelines and Schematic Review Checklist*
- Texas Instruments, *AM62P Power Estimation Tool*
- Texas Instruments, *PMIC for Powering AM62Px Devices*
- Texas Instruments, *AM62Px Escape Routing for PCB Design*
- Texas Instruments, *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*
- Texas Instruments: *SK-AM62P-LP Design Package Folder and Files List (Rev. A)*

13.4 AM62D-Q1

- Texas Instruments, *AM62Dx Sitara Processors data sheet*
- Texas Instruments, *AM62Dx Sitara Processors technical reference manual*
- Texas Instruments, *AM62Dx Sitara Processors Silicon Errata, Silicon Revision 1.0*
- Texas Instruments, *AUDIO-AM62D-EVM*
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM62A3, AM62A7, AM62A3-Q1, AM62A7-Q1 and AM62D-Q1 Processor Families*
- Texas Instruments, *AM62A3, AM62A7, AM62A3-Q1, AM62A7-Q1 and AM62D-Q1 Processor Families Schematic Design Guidelines and Schematic Review Checklist*
- Texas Instruments, *AM62Ax/AM62Dx Escape Routing for PCB Design*
- Texas Instruments, *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*

13.5 Common for all Processor Families

- Texas Instruments, *AM623, AM625, AM625SIP, AM620-Q1, AM625-Q1, AM62A3, AM62A7, AM62A7-Q1, AM62D-Q1, AM62P-Q1 Schematic Design Guidelines and Review Checklist*
- Texas Instruments, *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments, *High-Speed Interface Layout Guidelines*
- Texas Instruments, *High-Speed Layout Guidelines*
- Texas Instruments, *Jacinto7 AM6x, TDA4x, and DRA8x High-Speed Interface Design Guidelines*
- Texas Instruments, *Thermal Design Guide for DSP and Arm Application Processors*
- Texas Instruments, *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments, *XDS Target Connection Guide*

- Texas Instruments, *Interface Circuits for TIA/EIA-644 (LVDS)*
- Texas Instruments, *General Hardware Design/BGA PCB Design/BGA Decoupling*
- Texas Instruments, *MSL Ratings and Reflow Profiles*
- Texas Instruments, *Moisture sensitivity level search*
- Texas Instruments, *Clocking Design Guide for KeyStone Devices*
- Texas Instruments, *Hardware Design Guide for KeyStone II Devices*
- Texas Instruments, *TIDA-01413 - ADAS 8-Channel Sensor Fusion Hub Reference Design*
- Texas Instruments, *Jacinto™ 7 DDRSS Register Configuration Tool*
- Texas Instruments, *Using IBIS Models for Timing Analysis*
- Texas Instruments: *Display Interfaces: A Comprehensive Guide to Sitara MPU Visualization Designs*

13.6 Master List of Available FAQs - Processor Family Wise

A master list of the FAQs are available that can be used to quickly view the available list of FAQs for the selected processor or processor families.

[FAQ] AM625, AM623, AM625SIP, AM625-Q1, AM620-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

[FAQ] AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

Above FAQ includes the FAQs relevant to AM62D-Q1 processor family.

[FAQ] AM62P, AM62P-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

13.7 Master List of Available FAQs - Sitara Processor Families

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM64x, AM243x, AM335x) families

13.8 FAQs Including Software Related

[FAQ] AM6x: Latest FAQs on AM62x, AM64x, AM24x, AM3x, AM4x Sitara devices

13.9 FAQs for Attached Devices

[FAQ] DP83869-EP: Ethernet compliance Testing failure

[FAQ] TPS65219: Benefits of a PMIC vs discrete solution to power Sitara AM62x MPU

[FAQ] List of FAQs for TPS6594-Q1, TPS6593-Q1, LP8764-Q1 PMICs

14 Terminology

BOM	Bill of Materials
CAN	Controller Area Network
CPPI	Communications Port Programming Interface
CPSW3G	Common Platform Ethernet Switch 3-port Gigabit
CSIRX	Camera Streaming Interface Receiver
DDR0_CAL0	IO Pad Calibration Resistor
DFU	Device Firmware Upgrade
DNI	Do Not Install
DPI	Display Parallel Interface
DRD	Dual-Role Device
E2E	Engineer to Engineer
ECC	Error-Correcting Code
EMC	Electromagnetic Compatibility

EMI	Electromagnetic Interference
eMMC	embedded Multi-Media Card
EMU	Emulation Control
EOS	Electrical Over-Stress
ESD	Electrostatic discharge
ESL	Effective Series Inductance
ESR	Effective Series Resistance
FAQ	Frequently Asked Question
FET	Field-Effect Transistor
GEMAC	Gigabit Ethernet Media Access Controller
GPIO	General Purpose Input/Output
GPMC	General-Purpose Memory Controller
HS-RTDX	High Speed Real Time Data eXchange
I2C	Inter-Integrated Circuit
IBIS	Input/Output Buffer Information Specification
IEP	Industrial Ethernet Peripheral
JTAG	Joint Test Action Group
LDO	Low Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signaling
MAC	Media Access Controller
MCASP	Multichannel Audio Serial Ports
MCSPI	Multichannel Serial Peripheral Interface
MCU	Micro Controller Unit
MDI	Medium Dependent Interface
MDIO	Management Data Input/Output
MMC	Multi-Media Card
MMCSD	Multi-Media Card/Secure Digital
ODT	On-die Termination
OLDI	Open LVDS Display Interface
OPN	Orderable Part Number
OSPI	Octal Serial Peripheral Interface
PCB	Printed Circuit Board
PDN	Power Distribution Network
PET	Power Estimation Tool
PMIC	Power Management Integrated Circuit
POR	Power-on Reset
PRUSS	Programmable Real-Time Unit Subsystem
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
ROC	Recommended Operating Condition

SD	Secure Digital
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
TCK	Test Clock Input
TDI	Test Data Input
TDO	Test Data Output
TEN	Test Enable
TMS	Test Mode Select Input
TRC_DATAn	Trace Data n
TRM	Technical Reference Manual
TRSTn	Reset
UART	Universal Asynchronous Receiver/Transmitter
WKUP	Wake-up
XDS	eXtended Development System
ZQ	Devices Calibration reference

15 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2024) to Revision A (January 2025) **Page**

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