TMS320C6474 Hardware Design Guide

Ronald Lerner

ABSTRACT

This document describes hardware system design considerations for the TMS320C6474 device.

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1 Introduction

1.1 Purpose and Scope

This document is intended to aid in the hardware design and implementation of a C6474-based system. The document should be used along with the data manual and other relevant user guides and application reports.

1.2 Terms and Abbreviations

AIF	Antenna Interface
BGA	Ball Grid Array
CML	Current Mode Logic, I/O type
CPU	Central Processing Unit
DDR2	Double Data Rate 2 (SDRAM Memory)
EMAC	Ethernet Media Access Controller
EMIF	External Memory Interface
FC-BGA	Flip-Chip BGA
FSM	Frame Sync Module
GPIO	General-Purpose Input/Output I/O
HSTL	High-Speed Transceiver
I2C	Inter-IC Control Bus
JEDEC	Joint Electronics Device Engineering Council
LJCB	Low Jitter Clock Buffer: Differential clock input buffer type, compatible with LVDS and LVPECL
LVDS	Low Voltage Differential Swing, I/O type
LVPECL	Low-Voltage Positive-Reference Emitter Coupled Logic
McBSP	Multi-Channel Buffered Serial Port
MDIO	Management Data Input/Output
NSMD	Non-Solder Mask Defined BGA Land
OBSAI	Open Base Station Architecture Initiative
PCB	Printed Circuit Board
PHY	Physical Layer of the Interface
PLL	Phase-Locked Loop
SerDes	Serializer/De-Serializer
SGMII	Serial Gigabit Media Independent Interface
SRIO	Serial RapidIO
SSTL_18	Stub Series Terminated Logic
TBD	To Be Determined. Implies something is currently under investigation and will be clarified in a later version of the specification.
UI	Unit Interval
XAUI	10 Gigabit (X) Attachment Unit Interface standard

2 Mechanical

2.1 Ball Grid Array (BGA) Layout Guidelines

The BGA footprint and pin escapes can be laid-out as defined in *Flip Chip BGA Users Guide* (SPRU811) [14]. If the DDR2 interface is used, there are specific recommendations for the BGA pad and pin escape vias given in *TMS320C6474 DDR2 Implementation Guidelines* (SPRAAW8) [18]. Given the 0.80 mm-pitch, it is recommended that non-solder mask defined (NSMD) PCB lands be used for mounting the device to the board. With the NSMD method, the land area is etched inside the solder mask area. While the size control is dependent on copper etching and is not as accurate as the SMD method, the overall pattern registration is dependent on the copper artwork, which is quite accurate. The tradeoff is between accurate dot placement and accurate dot size. NSMD lands are recommended for small-pitch BGA packages because more space is left between the copper lands for signal traces. Dimensioning for the pad and mask are provided in *Flip Chip BGA Users Guide* (SPRU811) [14].

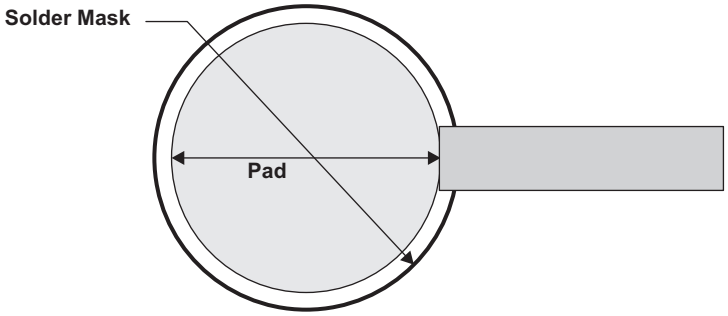

Figure 1. Non-Solder-Mask Defined (NSMD) PCB Land

2.2 Thermal Issues

A proper understanding of the thermal characteristics of the C6474 is critical for proper design of the board and system. The maximum case temperature of the device must not be exceeded, which requires adequate heat dispersion through a heat sink to be a part of the thermal design.

2.2.1 C6474 Power Consumption Estimate

The C6474 device can consume up to 8 W of power, though the exact power dissipation depends heavily on the exact device usage. Expectation is that a typical system configuration calls for approximately 6 W - 7 W, assuming that a majority of the interfaces are used and assuming that CV_{DD} is scaled to process by following the SmartReflex™ circuit design and software - Class 0.

The expected power consumption by the C6474 device is highly dependent on processing load and environmental conditions. The worst-case power consumption numbers are under analysis, assuming the maximum operating temperature and strong device process corner. Estimates on the maximum power numbers are provided in Section 5.3. For more information, see the *TMS320C6474 Power Consumption Summary* application report (SPRAAX3) [46].

Table 1 shows an estimate on the breakdown of how power is consumed (assuming SmartReflex).

Table 1. Example of C6474 Worst-Case Power Consumption Breakdown

Modules	Dynamic Power	Leakage Power	Total Power
Core 0	6.5%	4.5%	11%
Core 1	6.5%	4.5%	11%
Core 2	6.5%	4.5%	11%
Memory	8.6%	6.8%	15.4%
Peripheral Logic	10.4%	3.7%	14.1%
Peripheral I/O	21.1%	0%	21.1%
Total	**69.1%**	**30.9%**	**100%**

2.2.2 System Thermal Analysis

For an overview on performing a thermal analysis and suggestions on system level thermal solutions, refer to the *TMS320C6474 Thermal Reference Document* (available upon request).

3 Device Configurations and Initialization

On the C6474 device, boot mode and certain device configuration selections are determined at device reset via certain general-purpose I/O (GPIO) pins, while peripheral usage (enabled/disabled) is determined by the peripheral configuration registers after the device reset. Most of the peripherals on the C6474 device are "enabled" after reset but some default disabled. The basic information on configuration options, boot modes options and use of the power configuration registers can be found in the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552) (referred to as the C6474 data manual throughout the remainder of this document).

3.1 Device Reset

There are several ways to reset the C6474 and these are described in the C6474 data manual. The 2 external resets, $\overline{\text{POR}}$ and $\overline{\text{XWRST}}$, need to be at valid logic levels at all times. $\overline{\text{POR}}$ must be asserted (low) on a power-up while the clocks and power planes become stable. $\overline{\text{XWRST}}$ should be de-asserted before $\overline{\text{POR}}$ on a power-up, otherwise the C6474 comes up in the warm reset condition. $\overline{\text{XWRST}}$ can be used after the powered-up state to issue a warm reset, which performs the same as a $\overline{\text{POR}}$ except:

- Test and emulation logic are not reset
- AIF and FSMs are not reset
- Configuration strapping options (via GPIO pins) are not latched

The warm reset ($\overline{\text{XWRST}}$) does not reset the AIF and FSM modules so that the serial link connections can be maintained and do not lose synchronization.

If warm reset is not needed, $\overline{\text{XWRST}}$ can be pulled up to DV_{DD18}.

The $\overline{\text{RESETSTAT}}$ signal indicates the internal reset state. The $\overline{\text{RESETSTAT}}$ is asserted (low) on power-on reset (issued by $\overline{\text{POR}}$), warm reset (issued by $\overline{\text{XWRST}}$), max reset (issued by an emulator), or system reset (issued by the emulator or the SRIO peripheral). The only reset that does not cause $\overline{\text{RESETSTAT}}$ to be asserted is a CPU reset (issued by watchdog timers).

3.2 Device Configuration

Some C6474 device configuration strapping options are multiplexed on the GPIO[9:0] pins. There are two dedicated configuration pins: CORECLKSEL and DDRSLRATE. The state of these pins is not latched and must be held at the desired state at all times. For details on the configuration options, see the C6474 data manual. If the GPIO signals are not used, the internal pullup and pulldown resistors can be used to set the input level and an external pullup/down resistors are only needed if the opposite setting is desired. If the GPIO pins are connected to other components, the internal pullup/pulldown resistor should not be relied upon; 1-kΩ pullup and pulldown resistors are recommended for all desired settings.

The PLL multiplier can only be set by CPU register writes. The registers are not accessible through boot peripherals. All boot modes except No Boot automatically change the PLL multiplier to 16×, so the core PLL reference clock (either SYSCLKP/N or ALTCORECLKP/N) must be no more than 66 MHz.

For details on the configuration of the PLL, see the *TMS320C6474 DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (SPRUG09) [30] and the C6474 data manual.

3.3 Peripheral Configuration

Other than the device reset configuration covered in Section 3.1, all other configurations are done by register accesses. Peripherals that default disabled can be enabled using the peripheral configuration registers. If the boot-mode selection specifies a particular interface for boot (SRIO, Ethernet, I2C), it is automatically enabled and configured. For more details on peripheral configuration refer to the Device Configuration section of the C6474 data manual.

For some peripherals, the peripheral operating frequency is dependent on the CPU core clock frequency. This should be accounted for when configuring the peripheral.

3.4 Configuration Tables in I2C ROM

I2C ROM contents can contain configuration tables that allow customer defined memory map accesses during the I2C-boot mode. These accesses can be used to configure peripherals during the boot process. For details, see *TMS320C645x/C647x Bootloader User's Guide* (SPRUEC6) [33].

3.5 Boot Modes

The interfaces which support a boot loading process are: I2C, Serial RapidIO® and EMAC. For a summary of the boot modes supported, see the C6474 data manual. For details regarding boot modes, see the *TMS320C645x/C647x Bootloader User's Guide* (SPRUEC6) [33].

Regardless of the boot mode selected, an emulator connection can always reset the device to acquire control.

4 Clocking

4.1 PLL Reference Clock Solutions

This section describes the clock requirements and a system solution for the PLL reference clocks. There are two types of PLLs and each type has different needs for their reference clocks. The core PLL and DDR2 PLL source clocks for digital logic, whereas, the AIF, SRIO, and SGMII PLLs source clocks for serializer/deserializer SERDES links.

Figure 2 is a functional representation of how the reference clocks are connected in the C6474 device.

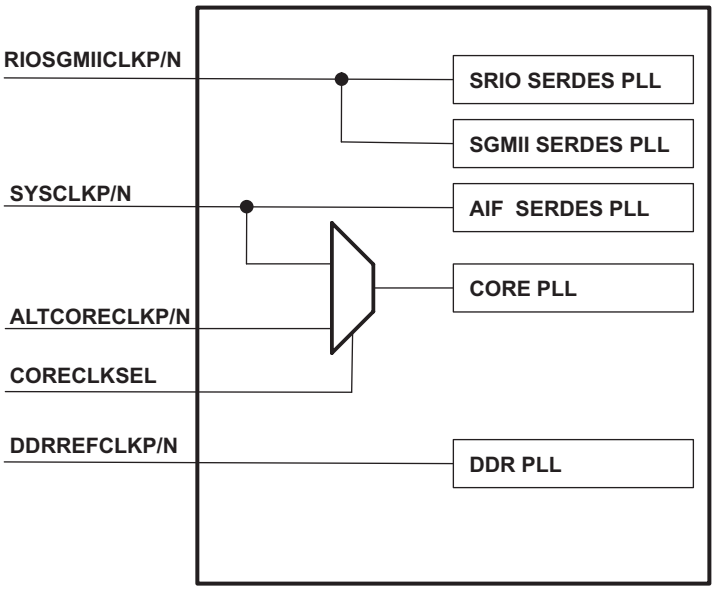

Figure 2. C6474 Reference Clocks

The core PLL can be configured with multiplier values from 4× to 32× and any integer value in between, as long as the PLL output frequency does not violate the maximum operating frequency for the C6474 device. There are minimum core clock frequency requirements for some peripherals so the datasheet should be referenced to check for any limitations with the desired core clock frequency. The DDR2 PLL always uses a multiplier of 10× (40 MHz input for DDR2-400 operation to 66 MHz for DDR2-667 operation). Note that the PLL output is 2× the DDR2 interface clock frequency. The SERDES PLL multipliers are covered in the peripherals section.

All differential clock input buffers are LJCBs. These input buffers include a 100 Ω termination (P to N) and a common-mode biasing. Because the common-mode biasing is included, the clock source must be ac coupled. LVDS and LVPECL clock sources are compatible with the LJCBs.

Any unused LJCB inputs should be connected to produce a valid logic level. The recommended connections are shown in Figure 3. The 1 K resistor is to reduce power.

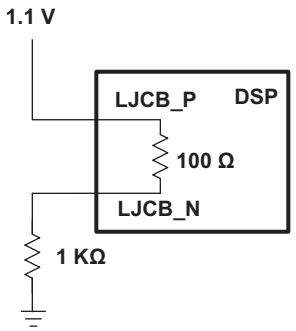

Figure 3. Unused LJCB Connections

4.1.1 Clock Requirements

The clock requirements are given in Table 2.

Table 2. PLL Reference Clock Requirements

	Logic	Input Jitter	T_{rise}/ T_{fall}	Duty Cycle	Stability	Frequency Range
ALTCORECLKP/ ALTCORECLKN	LVDS or LVPECL	100 pS pk-pk(1)	50 - 1300 pS	40/60%	± 100 PPM	50 MHz - 61.44 MHz
SYSCLKP/ SYSCLKN	LVDS or LVPECL	2 pS RMS (OBSAI, 1x10E-15) 4 pS RMS (CPRI, 1x10E-12) 100 pS pk-pk(2)	50 - 1300 pS	40/60%	± 100 PPM	61.44MHz (CORECLKSEL = 0) 61.44 MHz 153.6 MHz (CORECLKSEL = 1)
DDRREFCLKP/ DDRREFCLKN	LVDS or LVPECL	2.0% of DDRREFCLKP/N input period pk-pk	50 - 1300 pS	40/60%	± 100 PPM	40 MHz - 66 MHz
RIOSGMIICLKP/ RIOSGMIICLKN (if RIO is used)	LVDS or LVPECL	4 pS RMS 56 ps pk-pk @ $1\times10E^{-12}$ BER	50 - 1300 pS	40/60%	± 100 PPM	125 MHz, 156.25 MHz, 312.5 MHz
RIOSGMIICLKP/ RIOSGMIICLKN (if only SGMII is used)	LVDS or LVPECL	8 pS RMS 112 ps pk-pk @ $1\times10E^{-12}$ BER	50 - 1300 pS	40/60%	± 100 PPM	125 MHz, 156.25 MHz, 312.5 MHz

(1) Peak-to-peak accumulated total jitter values for ALTCORECLK and DDRREFCLK is for 10,000 sample points.
(2) Total RMS jitter values (SYSCLK and RIOSGMIICLK) are specified for a target BER for the associated SERDES interfaces.

T_{rise}/T_{fall} values are given for 10% to 90% of the voltage swing.

The concerns for the differential reference clocks are low jitter and proper termination. Either LVDS or LVPECL clock sources can be used but they require different terminations. The input buffer sets its own common mode voltage so ac coupling is necessary. It also includes a 100 Ω differential termination resistor, eliminating the need for an external 100 Ω termination when using an LVDS driver. For generation information on ac termination schemes, see *AC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML* (SCAA059). For information on dc coupling, see *DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CM* (SCAA062)

4.1.2 Single Device Solution

It is assumed that the source clock is an oscillator on the same board as the device. Use of distributed clocks can require a jitter cleaner device such as the CDCL6010. If an on-board oscillator is used with one device, no other components should be needed except for terminations.

Examples of 3.3 V differential oscillators are:

- Pletronics LVDS LV77D oscillator
  - http://www.pwgdev.com/~datasheets/lv77d%203.3v.pdf
- Pletronics LVPECL PE77D oscillator
  - http://www.pwgdev.com/~datasheets/pe77d%203.3v.pdf

These oscillators have not been tested but are examples of oscillators that meet the specification requirements for all TMS320C6474 differential reference clocks. Note that these oscillators require 3.3 V. No availability of 1.8 V differential oscillators that meet the clocking requirements was found, although they may exist.

Figure 4 shows an LVDS-based solution including terminations.

Figure 4. Differential Single Device LVDS Clock Solution

Figure 5 shows an LVPECL-based solution including terminations.

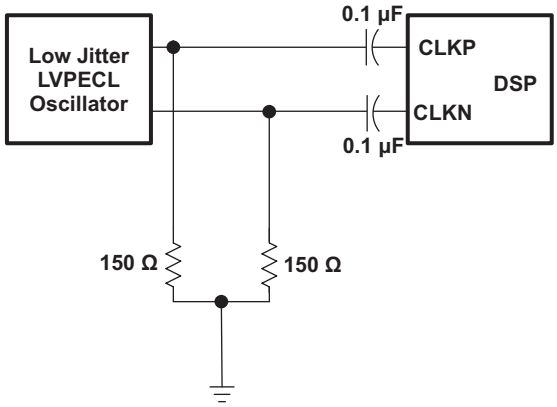

Figure 5. Differential Single Device LVPECL Clock Solution

A single ended oscillator plus an LVDS transmitter can provide a lower cost solution and still meet the clocking requirements. An example of this is shown in Figure 6.

Figure 6. Single Ended Oscillator for Differential Inputs

4.1.3 Multiple Device Fanout Solutions

For systems with multiple TMS320C6474 devices, you may prefer to use one oscillator and a fanout buffer instead of multiple oscillators. This would allow for fewer components as well as lower cost. The fanout buffer can increase the jitter at the clock input, so take care when selecting the combination of oscillator and fanout buffer.

In most cases, the same oscillators described in Section 4.1.2 can be used for the fan out case. The oscillator output specifications should be compared to the fanout buffer input specifications to make sure they are compatible.

If 3.3 V is available, there are many options for clock oscillators and fanout buffers. There are fewer options for 1.8 V fanout buffers but TI does offer one: the CDCL1810 (see Figure 9).

For an all 1.8 V solution, a 1.8 V single-ended oscillator can be used with the CDCL6010. Since the CDCL6010 is a jitter cleaner,the single-ended oscillator does not need to be low-jitter which allows it to be low cost. Also, if a distributed clock with jitter exceeding the input jitter specification is the source (either single ended or differential), the TI CDCL6010 can be used for both jitter cleaning and distribution. The solution using the CDCL6010 is described in Section 4.1.3.2.

4.1.3.1 Fanout Solutions (No jitter cleaning)

Suggested 3.3 V fanout buffers are:

- TI SN65LVDS108 LVDS 1:8 clock fanout buffer (see Figure 7)
  - *SN65LVDS108 8-Port LVDS Repeater Data Sheet* (SLLS399)
- TI CDCLVP110 LVPECL 2:10 clock fanout buffer (see Figure 8)
  - *CDCLVP110 Low-Voltage 1:10 LVPECL/HSTL With Selectable Input Clock Driver Data Sheet* (SCAS683)

There are also 4-port and 16-port versions of the SN65LVDS108.

Texas Instruments also has a 1.8 V fanout buffer that includes some options for providing divided down outputs. This is:

- TI CDCL1810 1:10 clock fanout buffer (see Figure 9)
  - New Product: see TI representative for details

These buffers have not been tested but are examples of buffers that meet the specification requirements for all of the TMS320C6474 differential clock inputs.

Examples in this section show differential oscillators; however, depending on clocking specifications for the particular clock input, it may be possible to use a single ended oscillator to reduce cost. Many differential buffers can support a single ended input. Another option would be to use a single ended to differential transmitter such as the SN65LVDS1 as shown in Figure 6.

Jitter performance for the SN65LVDS108 is found in its datasheet - *SN65LVDS108 8 - Port LVDS Repeater Data Sheet* (SLLS399). For the CDCLVP110, see *Advantage of Using TI's Lowest Jitter Differential Clock Buffer Application Report* (SCAA068)

The fanout buffer outputs should not be used to drive additional fanout buffers since the jitter accumulates.

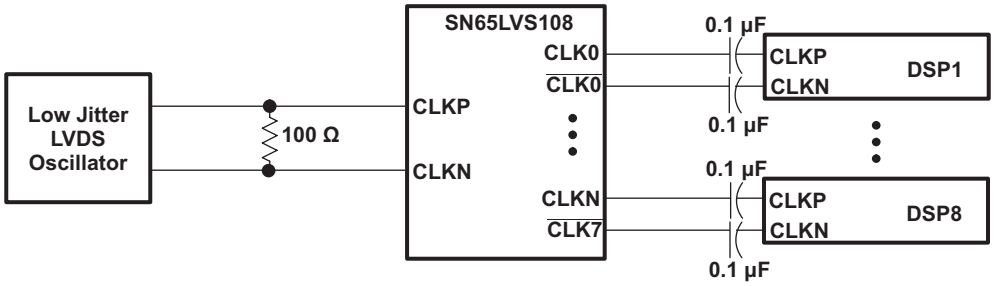

Figure 7. Multiple Devices LVDS Clock Solution

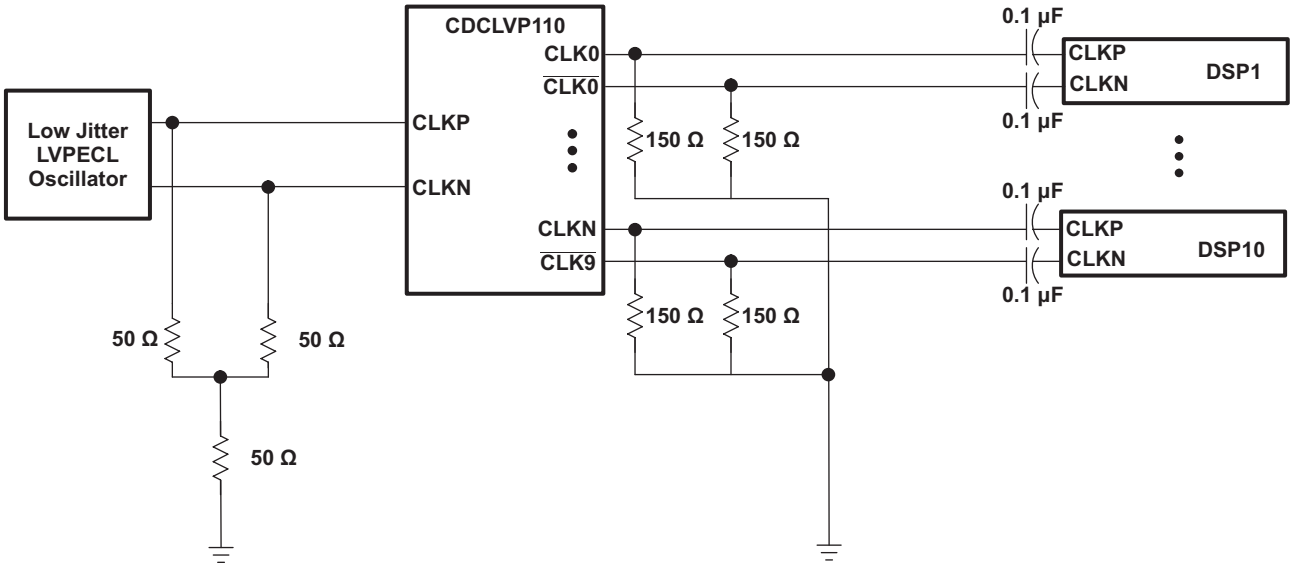

Figure 8. RIOCLK Multiple Devices LVPECL Clock Solution

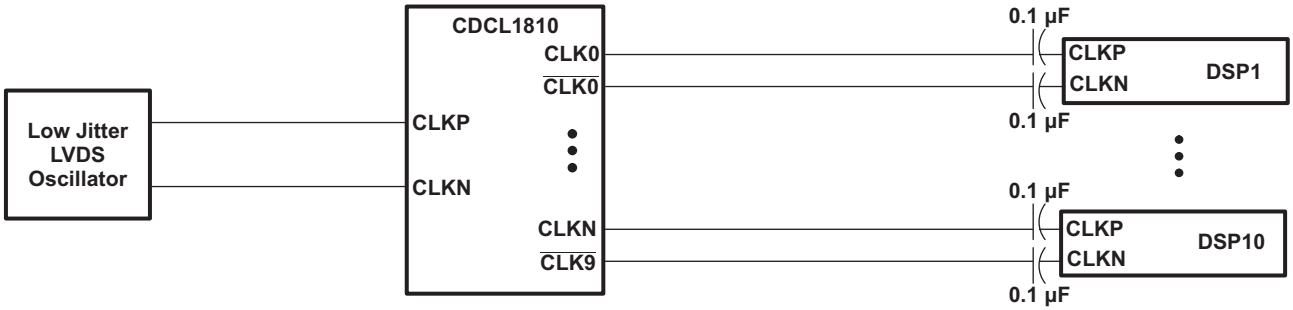

Figure 9. Multiple Devices 1.8 V LVDS Clock Solution

4.1.3.2 CDCL6010 Based Solutions (jitter cleaning)

The CDCL6010 is a jitter cleaner and 1:10 fanout buffer that is well suited for use with the TMS320C6474 device. It operates from 1.8 V and meets the jitter requirements for all differential clock inputs on the C6474 device. Figure 10 an example of the connections when using an LVDS signal as the source.

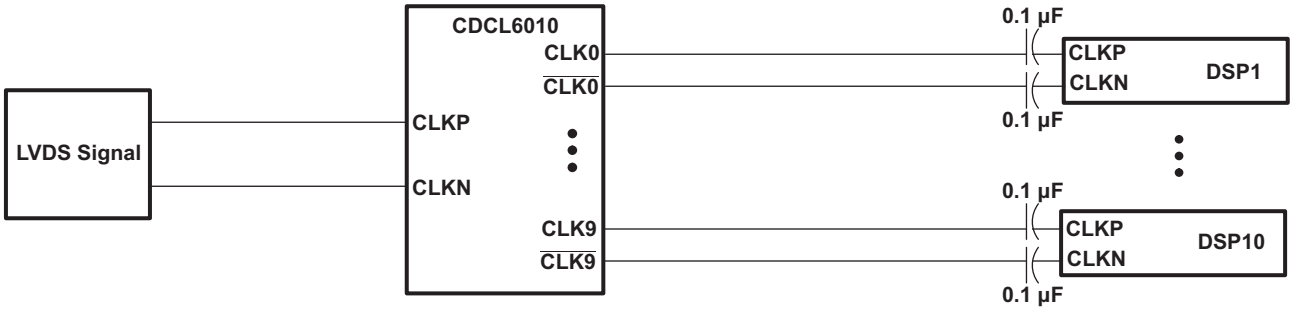

Figure 10. CDCL6010 Solution With LVDS Input

The connection of a single ended input clock to CDCL6010 is given in Figure 11. This source could be a 1.8 V source or, using a voltage divider, a 3.3 V source such as the CDCE706 or the CDCE906. The *CDCx706/x906 Termination and Signal Integrity Guidelines* (SCAA080) describes the interface between the CDCE706/CDCE906 and the CDCL6010 in detail.

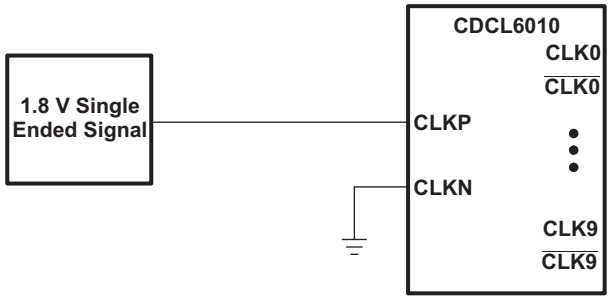

Figure 11. CDCL6010 With Single Ended Input

4.1.4 Layout Recommendations (LVDS and LVPECL)

Placement:

- The oscillator, buffer, and DSPs should be placed as close to each other as practical
- Fanout buffers should be placed in a central area to equalize the trace lengths to each DSP
- ac coupling capacitors should be placed near the receivers
- 50 Ω resistors used in LVPECL dc termination should be placed near the receiver
- 150 Ω resistors used in LVPECL ac termination should be placed near the driver

Trace routing:

- A GND plane should be placed below the oscillator
- Digital signals should not be routed near or under the clock sources.
- Traces should be 100 Ω differential impedance and 50 Ω single ended impedance
- Clock routes should be routed as differential pairs with no more than 2 vias per connection (not counting pin escapes)
- The number of vias on each side of a differential pair should match
- Differential clock routes must be length matched to within 10 mils
- Maintain at least 25 mil spacing to other traces

4.2 Non-PLL Reference Clock Solutions

There are several peripherals that use reference clock inputs for operation. These are:

- Frame Sync Module: FSYNCCLKP/N, ALTFSYNCCLK, TRTCLK
- McBSP: CLKS0, CLKS1
- Timers: TIMI0, TIMI1

With the exception of FSYNCCLKP/N, these are all single-ended clocks with 1.8-V LVCMOS inputs. The specific requirements for these clocks are given in Table 3. Use of standard oscillators and buffers should be adequate for these clocks with the exception that they do require 1.8-V operation. For updated information, see the C6474 data manual.

Table 3. Non-PLL Clock Requirements

	Logic	Input Jitter	Duty Cycle	Frequency Range
FSYNCCLKP/N	LVDS	2.5% of input clock period	40/60%	3.84 MHz - 122.88 MHz
ALTFSYNCCLK	1.8 V LVCMOS	2.5% of input clock period	40/60%	3.84 MHz - 122.88 MHz
TRTCLK	1.8 V LVCMOS	2.5% of input clock period	40/60%	3.84 MHz - 122.88 MHz
CLKS0, CLKS1 (McBSP)	1.8 V LVCMOS	Not specified	Not specified	0 Hz - 104.448 MHz
TIMI0, TIMI1 (Timer)	1.8 V LVCMOS	Not specified	Not specified	0 Hz - 43.52 MHz

There are some 1.8-V LVCMOS oscillators and 1.8 V 1:N clock buffers available, although the selection is limited. One alternative is to have a 3.3-V oscillator supply multiple loads of a dual-supply buffer, such as TI's SN74AVCH4T245. 3.3-V tolerant buffers should not be used for clocks due to the duty cycle distortion that occurs.

5 Power Supplies

5.1 Power Plane Generation

All power supplies can be generated from switching supplies. Filters are recommended for some C6474 device voltages. An overview of the recommended power supply generation architecture is shown in Figure 12. All power planes are required even if the peripheral associated with the supply is not used.For C6474 reference designs, look at
http://focus.ti.com/analog/docs/refdesignovw.tsp?familyId=64&contentType=2&genContentId=51423

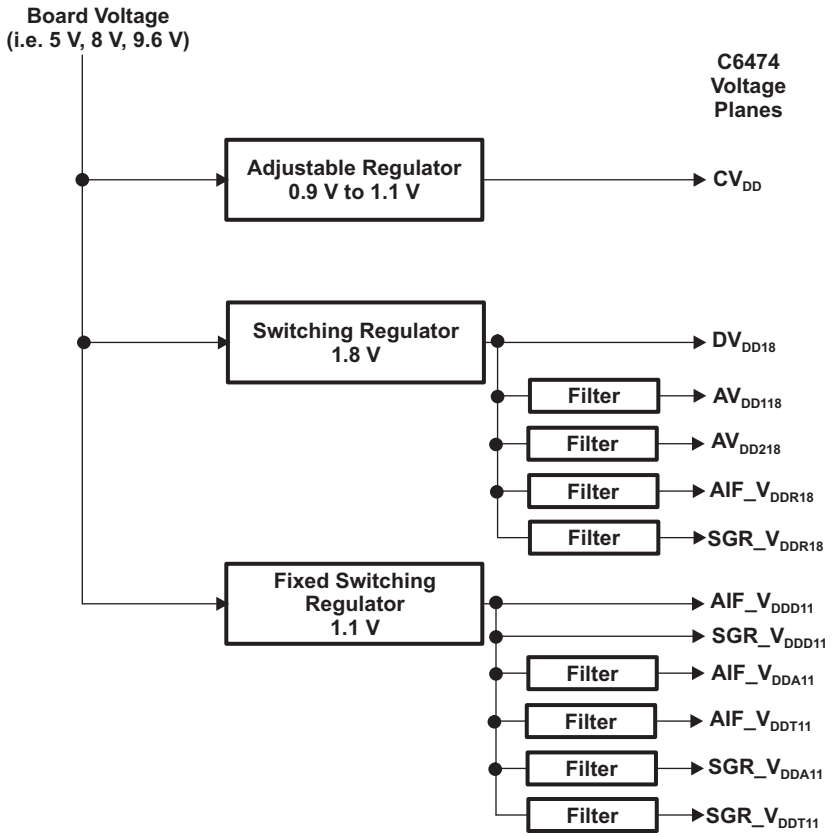

Figure 12. C6474 Power Supplies

The recommended filter circuit is given in Figure 13. The filter component shown is an EMI filter from Murata. If the peripheral associated with the power supply is not used, it still needs to be powered but the filters are not required.

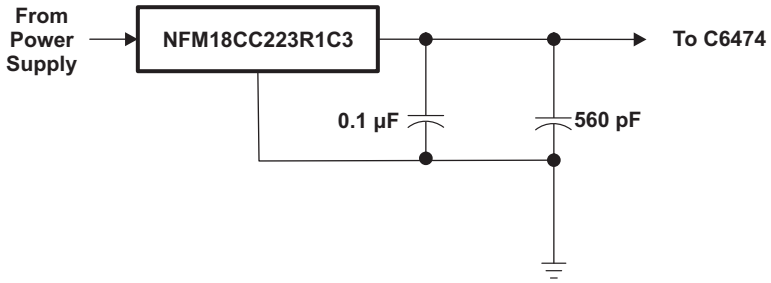

Figure 13. Recommended Power Supply Filter

A reference voltage is needed for the SSTL DDR2 interface. This is done through a simple voltage divider as shown in Figure 14. For additional details, see Section 5.4.

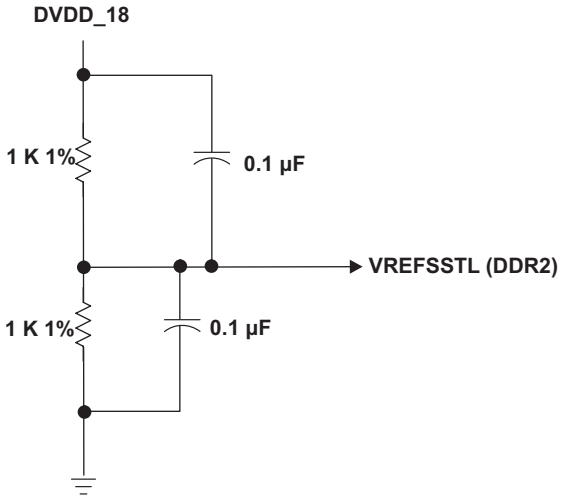

Figure 14. $V_{REFSSTL}$ Reference Voltage

5.2 Power Supply Sequencing

The recommended power supply sequencing is:

DV_{DD18} followed by CV_{DD} and all 1.1 V voltages ramping together. The delay between DV_{DD18} and the other supplies is 500 µS minimum, 200 mS maximum.

The CV_{DD} and other 1.1-V voltages must ramp to a valid level within 15 mS of each other.

For more details, see the C6474 data manual [19].

5.3 Voltage Plane Power Requirements

Power requirements are highly dependent on the usage of the device. This includes which peripherals are used as well as the operating frequencies. For more detailed information, see the *TMS320C6474 Power Consumption Summary* application report (SPRAAX3) [46]. The recommended power supplies and margins are based on initial silicon power measurements. Depending on your design and usage, the worse-case transient conditions should be taken into account when evaluating power supplies and associated capacitors (5.61 and 5.62). Designs outside of the approximate maximum values should re-examine power supply selection and design layout. These values should not be used to estimate thermal performance.

5.4 Power Supply Layout Recommendations

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the C6000™ platform of DSPs, the PCB should include separate power planes for core, I/O, and ground, all bypassed with high-quality low-ESL/ESR capacitors.

For $V_{REFSSTL}$, one reference voltage divider should be used for both the C6474 and the reference voltage input on the SDRAMs. The V_{REF} resistor divider should be placed between the two devices and the routes made as directly as possible with a minimum 20 mil wide trace.

There should be a 2× trace width clearance between the routing of the reference voltage and any switching signals.

5.5 Voltage Tolerances, Noise, and Transients

The voltage tolerances specified in the data sheet include all dc tolerances and the transient response of the power supply. These specify the absolute maximum and minimum levels that must be maintained at the pins of the C6474 device under all conditions. Special attention to the power supply solution is needed to achieve this level of performance, especially the 3% tolerance on the core power plane (CV_{DD}).

To maintain the 3% tolerance at the pins, the tolerance must be a combination of the power supply dc output accuracy and the effect of transients. A reasonable goal for the dc power supply output accuracy is 1.5%, leaving 1.5% for the transients. For example, at CV_{DD} of 1.0 V, 3% tolerance is ±30 mV. This allows 15 mV of dc accuracy from the output of the power supply and another 15 mV due to transients.

5.5.1 Using Remote Sense Power Supplies

Use of a power supply that supports the remote sense capability allows the power supply to control the voltage at the load. Special layout care must be used to keep this sense trace from being lost during PCB layout. One solution is placement of a small resistor at the load and connecting the sense trace to the voltage plane through it. If a power plane is shared by a group of DSPs, the sense resistor should be placed at the center of this group. If a negative sense pin is supported by the voltage regulator, it should be handled in a similar way. An example of this type of implementation is shown in Figure 15 for DV_{DD18}.

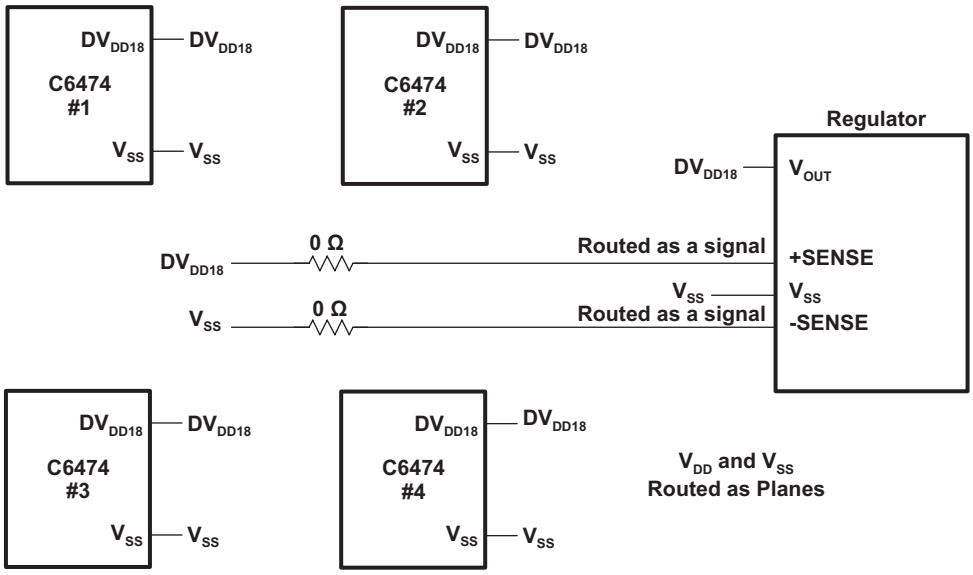

Figure 15. Multiple DSP Remote Sense Connections

If the connection is between one DSP and one voltage regulator, there are voltage monitor pins that can be used for this case (CV_{DDMON} and $DV_{DD18MON}$). The monitor pins indicate the voltage on the die and, therefore, provide the best remote sense voltage. These monitor pins should be connected directly to the positive side sense pin of the voltage regulator.

NOTE: If the monitor pins are not used to monitor the voltage, they should be connected to their respective power planes (i.e., CV_{DDMON} connects to CV_{DD}, $DV_{DD18MON}$ connects to DV_{DD18}).

The voltage regulator output could become unstable and drive to a high voltage if the positive sense line does not receive the correct voltage. Some voltage regulators (i.e., TI's PTH08T240F) include a low-impedance path between the V_{OUT} and +SENSE so that this would only result in a small drop in performance. If this feature is not present in the voltage regulator, place a 100 Ω resistor near the DSP between the voltage plane and the monitor pin. If the V_{DD} monitor connection to the DSP (i.e., C_{VDDMON}) is not present, the positive sense still regulates to the proper voltage. If a negative sense pin is provided by the regulator, this should be connected to the GND plane near the DSP using a 0 Ω resistor. The single DSP remote sense connections are shown in Figure 16 for the CV_{DD} plane. The same solution could be used for all/any planes.

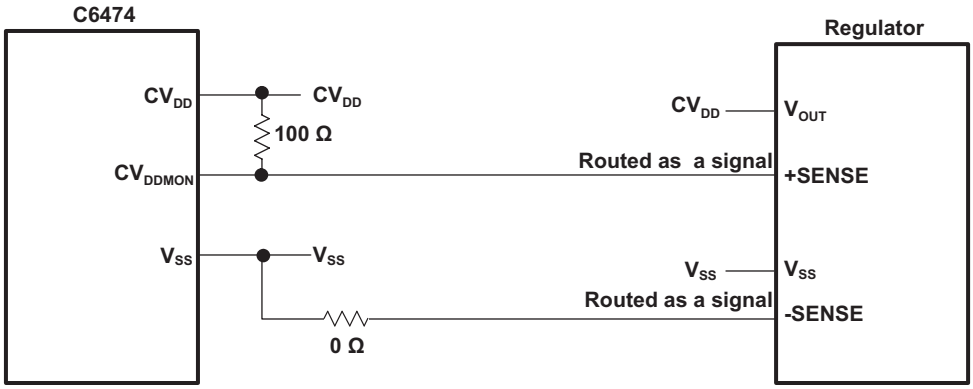

Figure 16. Single DSP Remote Sense Connections

5.5.2 Voltage Plane IR Drop

The voltage gradient (IR drop) needs to be considered whether or not a supply with the remote sense capability is used. The DSPs closer to the supply have a slightly higher voltage and the DSPs farther from the supply have a slightly lower voltage. This voltage differential can be minimized by making the copper planes thicker or by spacing the DSPs across a wider area of the plane. Be sure to consider both the core power plane(s) and the ground plane(s). The resistance of the plane can be determined by the following formula:

R = rho * length/(width * thickness)

where rho is the resistivity of copper equal to 1.72E-8 Ω-meters. PCB layer thickness is normally stated in *ounces*. One ounce of copper is about 0.012 inches or 30.5E-6 meters thick. The width must be de-rated to account for vias and other obstructions. A 50 mm wide strip of 1 oz copper plane de-rated 50% for vias has a resistance of 0.57 mΩ per inch.

5.6 Power-Supply Decoupling and Bulk Capacitors

To properly decouple the supply planes from system noise, decoupling and bulk capacitors are required. Given current technology, 0402 sized capacitors should be used for standard decouplers where possible. Proper board design and layout allow for correct placement of all capacitors (see Table 4 for capacitor recommendations and values).

Generically speaking, bulk capacitors are used to minimize the effects of low frequency current transients (see Section 5.6.1) and decoupling or bypass capacitors are used to minimize higher frequency noise (see Section 5.6.3). Proper printed circuit board design is required to assure functionality and performance. One key element to consider during the circuit board (target) design is added lead inductance or the pad-to-plane length. Where possible, attachment for decoupler and bypass capacitors to the respective power planes should be made using multiple vias in each pad that connects the pad to the respective plane. The inductance of the via connect can eliminate the effectiveness of the capacitor so proper via connections are important. Trace length from the pad to the via should be no more than 10 mils (0.0.1") and the width of the trace should be the same width as the pad.

As with selection of any component, verification of capacitor availability over the product's production lifetime should be considered. Additionally the effects of the intended operating environment (temperature, humidity, etc.) should also be considered when selecting the appropriate decoupling and bulk capacitors.

NOTE: All values and recommendations are based on a single TMS320C6474 device. The use of recommended on-board power supply modules, alternate power supplies and decoupling/bulk capacitor values require additional evaluation.

For further information in determining the minimal amount of bulk and decoupling capacitance required [for PTH08T240Fxx module only], see the *TMS320C6474 Capacitor Selection Guide - Using the PTH08T240F Power Module* (SPRAAX0) and the selection spreadsheet.

5.6.1 Selecting Bulk Capacitance

Two factors need to be considered when selecting the bulk capacitance:

- Effective impedance for the power plane to stay within the voltage tolerance
- Amount of capacitance needed to provide power during the entire period when the voltage regulator cannot respond (sometimes referred to as the transient period)

The effective impedance of the core power plane is determined by:

(Allowable Voltage Deviation due to Current Transients) / (Max Current)

In the example in Section 5.5, it was suggested that the allowable voltage deviation allowed due to transient response is 15 mV (based on 1.5% of CV_{DD}). Using this 15 mV and a max current of 5 amps, the maximum allowable impedance can be calculated:

15 mV/5 Amps = 3 mΩ

The effective ESR of the bulk capacitors should not exceed this impedance value. Multiple bulk capacitors in parallel help achieve this overall ESR. Therefore, to achieve a maximum transient voltage peak deviation of 15 mV, the power supply output impedance, which is a function of the power supply bandwidth and the low impedance output capacitance, should not exceed 3 mΩ.

The expected maximum current change for the C6474 device is on the order of 3 Amps. This current assumes a transient from a device operating with a minimal activity and no peripheral usage to a worst case power condition. It does not include current transients that occur during power-on. Care should be taken during power-on that the device does not transition from the OFF state to a max power state faster than 100 mS. TI has tested the PTH08T240Fxx power module (that has been optimized for the C6474 device) and currently recommends the use of ~3000 μF of low ESR capacitance (see Section 5.6.3 for specific requirements).

Capacitance values should not be less than those specified in Section 5.6.3. Final capacitor selection is determined using the provided capacitor selection tool. For more information, see the *TMS320TCI6488 Capacitor Selection Guide - Using the PTH08T240F Power Module* application report (SPRAAM9).

This covers both the output capacitance requirements of the module and the bulk capacitance needs for the C6474 device. TI has also tested an optimized SWIFT TPS54010-based solution that requires a similar amount of capacitance. An additional power supply has also been developed by TI (TPS40197); the total capacitance and inductor size differs and must be recalculated when used with your C6474 DSP. All three power supplies utilize slightly different components. For additional details, see the C6474 data manual. Other regulators solutions should be analyzed and, if possible, tested in a lab environment to determine the optimal output capacitance.

Some intermediate size ceramic bulk capacitors (i.e., 22 μF and 47 μF as listed under Section 5.6.3) are recommended to cover the response time between the bypass capacitors and the larger bulk capacitors.

5.6.1.1 Bulk Capacitor Details and Placement

Place all bulk capacitors in close proximity to the power supply module. For the purpose of this document and related devices, a bulk capacitor should be defined as any capacitor ≥ 22 μF unless otherwise noted.

Figure 17 shows an example of the bulk capacitor placement with the use of the recommended PTH08T240F module and the capacitance recommendations from Table 4. Each bulk capacitor in this example has reduced trace lengths less than 10 mils and contain multiple vias to tie the pad to the respective power plane; it is recommended that all bulk capacitors be low ESR. The acceptability of each output capacitors should be based on the following criteria:

$$1000 < \text{capacitance} \times \text{ESR} \leq 5000$$

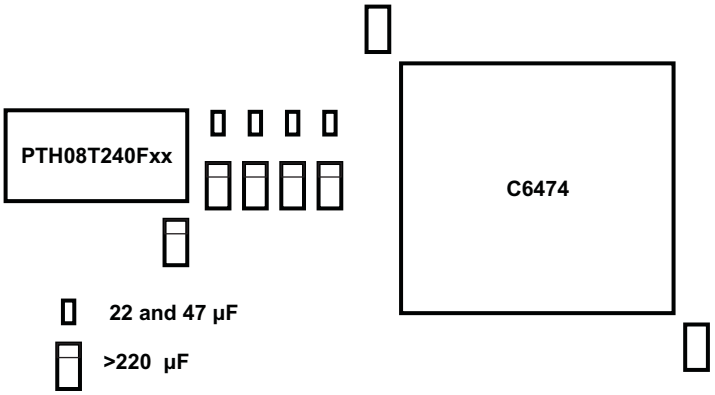

Figure 17. Bulk Capacitor Placement

5.6.2 Selecting Decoupling Capacitors

All decoupling or bypass capacitors need to be close to the DSP, in practice they should be within 1.25 cm maximum distance to be effective. Ideally, these caps should be connected directly to the via attached to the BGA power pin. Parasitic inductance limits the effectiveness of the decoupling capacitors; therefore, physically smaller capacitors (0402 or 0201) are recommended.

Proper capacitance values are also important. Place small bypass caps (near 560 pF) closest to the power pins on the target DSP. Medium bypass caps (100 nF or as large as can be obtained in a small package such as an 0402) should be the next closest. TI recommends placing decoupling capacitors immediately next to the BGA vias, using the *interior* BGA space and at least the corners of the *exterior*.

The inductance of the via connect can eliminate the effectiveness of the capacitor so proper via connections are important. Trace length from the pad to the via should be no more than 10 mils and the width of the trace should be the same width as the pad. If necessary, placing decoupler capacitors on the back side of the board is acceptable provided the placement and attachment is designed correctly.

5.6.2.1 Decoupling Capacitor Details and Placement

All decoupling capacitors should be placed in close proximity to the DSP. For the purpose of this document and related devices, a decoupler or bypass capacitor is defined as any capacitor < 22 μF, unless otherwise noted.

See Table 4 for recommended decoupler capacitor values. Each decoupler or bypass capacitor should be directly coupled to the DSP via. Where direct coupling is impractical, use a trace 10 mil (0.010"/0.254 mm) or shorter, and having the same width as the capacitor pad is strongly recommended.

5.6.3 Example Capacitance

An example of an adequate capacitor selection is given in Table 4. This is the capacitance that should be dedicated for the C6474 device and does not cover the decoupling needed for any other components or for the filters outlined in Section 5.1. The bulk capacitance assumes the use of the PTH08T240F power module. Power modules that do not support a Turbo-Trans type of feature would require additional output capacitance.

Table 4. Bulk and Bypass Capacitor Recommendations

Voltage Supply	Capacitors	Total Capacitance	Description
CV_{DD}	10 * 560 pF Ceramic	2,027.003006 μF	Scalable Core
	30 * 100 nF Ceramic		
	3 * 22 μF Ceramic		
	3 * 47 μF Ceramic		
	1 * 220 μF Low ESR		
	2 * 330 μF Low ESR		
	2 * 470 μF Low ESR		
AIF_VDDD_11 SGR_VDDD_11	4 * 560 pF	20 μF	Fixed 1.1 V
	6 * 100 nF		
	2 * 10 μF (ceramic)		
DV_{DD18}	10 * 560 pF	352 μF	1.8 V I/O
	20 * 100 nF		
	1 * 22 μF (ceramic)		
	1 * 330 μF		

Final CV_{DD} capacitor value should not be less than the value specified in Table 4. The final selection is determined using the provided capacitor selection tool. For more information, see the *TMS320TCI6488 Capacitor Selection Guide - Using the PTH08T240F Power Module* application report (SPRAAM9). This takes into account the board impedance, variation in the CV_{DD} supply voltage, and the ESR of the bulk and decoupling capacitors selected.

5.7 SmartReflex

In order to reduce device power, SmartReflex provides a feature that allows the core voltage to be optimized based on the process corner of the device. This requires a voltage regulator for each C6474 device. The voltage selection is done using four VCNTL pins that are used to select the output voltage of the core voltage regulator. The mapping of the VCNTL pins state to the CV_{DD} is shown in Table 5.

Table 5. VCNTL Pin Mapping

VCNTL #	VCNTL[3:0]	CV_{DD}
0	0000	0.900
1	0001	0.920
2	0010	0.940
3	0011	0.960
4	0100	0.980
5	0101	1.000
6	0110	1.020
7	0111	1.040
8	1000	1.060
9	1001	1.080
10	1010	1.100
11	1011	1.120
12	1100	1.140
13	1101	1.160
14	1110	1.180
15	1111	1.200

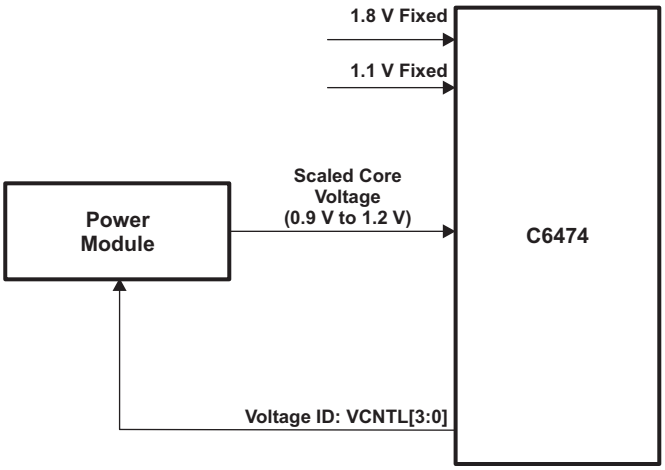

Figure 18. SmartReflex Operation

5.7.1 SmartReflex Power Supply Solution

A recommended power supply solution used to implement the C6474 scalable core voltage with full support for the SmartReflex feature can be implemented with TI's PTH08T240F power module. This solution is shown in Figure 19. The NFET shown (NTA4153NT1) is a low voltage FET available from ON Semiconductor.

The NFET selection is critical to meeting the ±3% tolerance for CV_{DD}. The NFET specifications must meet the following requirements:

- Max 48 Ω impedance @ 100 μA load at Vgs of 1.62 V (1.8 V - 10%)
- Idss (leakage current) ← 1 nA @ 25°C
- All SmartReflex resistors (resistor divider network) must be 0.5% or better tolerance. Other values and combinations may also be suitable, provided the same values are derived. Please note that the incremental steps of SmartReflex voltages must be uniform.

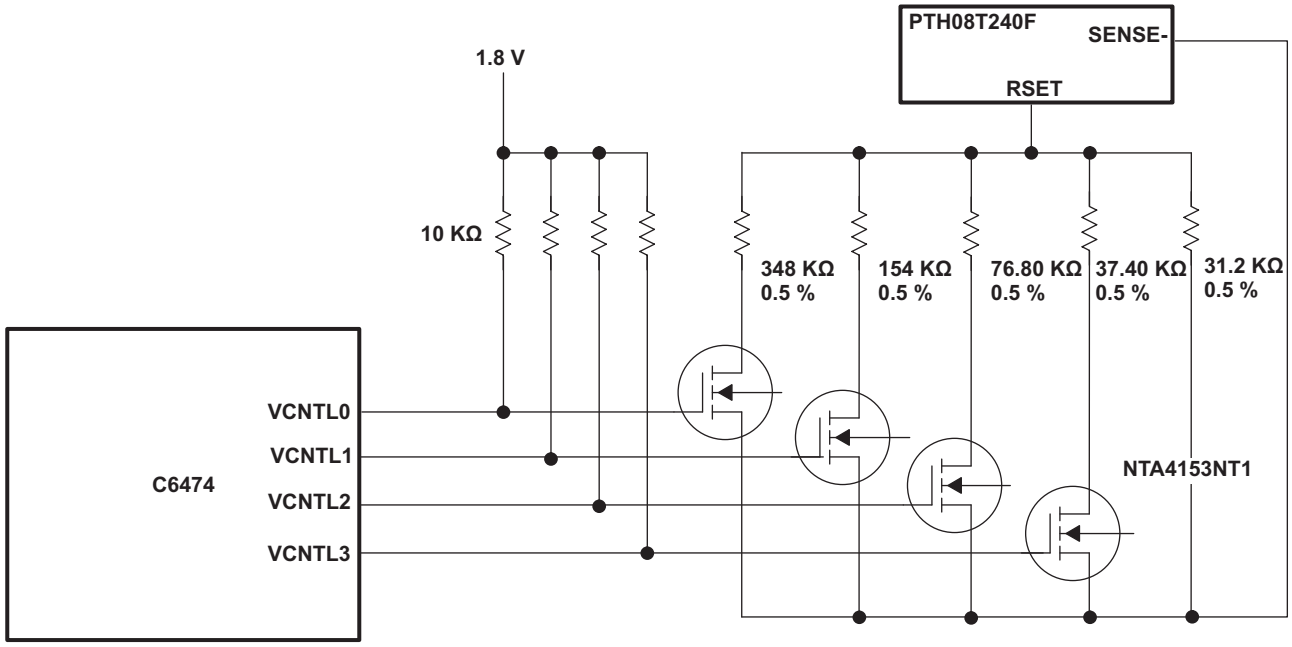

Figure 19. TI SmartReflex System Solution

5.8 Power Saving Options

5.8.1 Clock Gating Unused Peripherals

The C6474 device can keep (or put) inactive/unused peripherals into a low-power state, which is discussed in the C6474 data manual. After power-up, only those peripherals that are needed should be left enabled.

5.8.2 General Power Saving Techniques

The following are some additional methods for reducing power:

- Lower frequency operation means lower power. The core and peripherals should be operated at the lowest frequency that meets your requirements and the device requirements
- SERDES link power does not scale linearly with data rate. For SRIO and AIF, ports with higher link rates have a higher bandwidth/watt than slower links. Generally, running fewer high-speed links is more power efficient than multiple slower links.

6 I/O Buffers

6.1 Process, Temperature, Voltage (PTV) Compensated Buffers

The impedance of I/O buffers is affected by process, temperature, and voltage. For the DDR2 interface, these impedance changes can make it difficult to meet specifications across the full range of these parameters. For that reason, the C6474 device uses PTV compensated I/O buffers for the DDR2 interface. The PTV compensation works by adjusting internal impedances to nominal values based on an external reference resistance. This is implemented by connecting a resistor between the PTV18 pin and V_{SS}. For details, see the *TMS320C6474 DDR2 Implementation Guidelines* (SPRAAW8) [18].

6.2 I/O Timings

The I/O timings in the C6474 data manual are given for the tester test load. These timings need to be adjusted based on the actual board topology. It is highly recommended that timing for all high speed interfaces (with the exception of SERDES-based interfaces) on a C6474 design be checked using IBIS simulations. For more details on performing IBIS simulations, see *Using IBIS Models for Timing Analysis* (SPRA839) [28].

6.3 External Terminators

Series impedance is not always needed but is useful for some interfaces to avoid over-shoot/under-shoot problems. Check the recommendations in the peripherals sections and/or perform IBIS simulations on the interface.

6.4 Signaling Standards

6.4.1 1.8 V LVCMOS

All LVCMOS I/O buffers are JEDEC compliant 1.8-V LVMOS I/Os as defined in [16]. There are several different LVCMOS buffers used in the C6474 device. The differences are mainly whether an internal pullup or pulldown resistor is implemented. There are also some differences in the drive strength for some I/Os. For details on different LVCMOS buffer types, see the C6474 data manual [19].

Some LVCMOS I/Os include internal pullup or pulldown resistors. These internal pullup and pulldown resistors can be can be considered a 100 μA current source (with a range of 45 μA to 170 μA). This equates to a nominal pullup/pulldown resistor of 18-kΩ (with a possible range of 10-kΩ to 42-kΩ)

The 1.8-V LVCMOS interfaces are not 2.5-V or 3.3-V tolerant so connections to 2.5-V or 3.3-V CMOS logic require voltage translation. For input buffers at moderate frequencies, TI's LVC logic family can be operated at 1.8-V and is 3.3-V tolerant. For faster signaling, TI's AUC family is optimized to operate at 1.8-V and is also 3.3-V tolerant. Good options for voltage translation for 1.8-V outputs that need to drive 2.5-V or higher inputs would be the CBTLV family (for a non-buffered solution) or the AVC family (for a buffered solution). Some useful TI application reports on voltage translation options are:

- *Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards With the TI AVCA164245 and AVCB164245 Dual-Supply Bus-Translating Transceivers Application Report* (SCEA030)
- *Selecting the Right Level-Translation Solution Application Report* (SCEA035)

6.4.2 SSTL

The DDR2 interface is compatible with the *JEDEC JESD8-15 (SSTL-1.8V) Specification* [5]. The I/O buffers are optimized for use with direct connections to up to 2 DDR2 SDRAMs and are not intended to drive DDR2 DIMM modules. It is not intended that external parallel terminations be used with the DDR2 I/Os, but both series resistors and/or on-die-terminations (ODT) are supported. For more details, see [18].

6.4.3 SERDES Interfaces

There are three peripherals on the C6474 device that use high-speed serial interfaces: SGMII EMAC, AIF, and SRIO. These serial interfaces all use 8b/10b encoded links and SERDES macros. These interfaces use a clock recovery mechanism so that a separate clock is not needed. Each link is a serial stream with an embedded clock so there are no ac timings or drive strengths as found in the LVCMOS or SSTL interfaces. There are several programmable settings for each SERDES interface that affect the electrical signaling. The most important of these are: transmitter output amplitude, transmitter de-emphasis, and receiver adaptive equalization. Recommendations for these settings for particular board topologies are provided in

TMS320C6474 SERDES Implementation Guidelines (SPRAAW9) [21].

The SERDES interfaces use CML logic. Compatibility to LVDS signals is possible and is described in Section 8.1

7 Peripherals Section

This section covers each of the C6474 device's peripherals/modules. This section is intended to be used in addition to the information provided in the C6474 data manual, the Module Guides provided for each of the peripherals and relevant Application Reports. The four types of documents should be used as follows:

- Data Manual: ac Timings, register offsets
- Module Guide: Functional Description, Programming Guide
- Applications Reports: System level issues
- This Chapter: Configuration, system level issues not covered in a separate application report

Each peripheral section includes recommendations on how to handle pins on interfaces that are disabled or for unused pins on interfaces that are enabled. Generally, if internal pullup or pulldown resistors are included, the pins can be left floating. Any pin that is output only can always be floated. Normally, if internal pullup and pulldown resistors are not included, pins can still be floated with no functional issues for the device. However, this normally causes additional leakage currents that can be eliminated if external pullup or pulldown resistors are used. Inputs that are not floating have a leakage current of approximately 100 μA per pin. Leakage current is the same for a high- or low-input (either pullup or pulldown resistors can be used). When the pins are floating, the leakage can be several milliamps per pin. Connections directly to power or ground can be used only if the pins can be assured to never be configured as outputs and the boundary scan is not run on those pins.

7.1 Multichannel Buffered Serial Port (McBSP)

Relevant documentation for McBSP:

- *TMS320C6474 Multichannel Buffered Serial Port (McBSP) User's Guide* (SPRUG17) [26]
- TMS320C6474 IBIS Model File (SPRM336)
- *Using IBIS Models for Timing Analysis* (SPRA839) [28]

7.1.1 Configuration of McBSP

McBSP0 and McBSP1 are not multiplexed with any other peripherals and are enabled after power up.

Each McBSP port can either be driven by an external clock (CLKS), by an internal CLKS, or by the internal sample rate generator in the McBSP. The internal CLKS clock rate is core clock / X, where X is programmable from 6 to 32. Default is X = 10. CLKS (either sourced internally or externally) cannot exceed 104.448 MHz. The sample rate generator clock rate is core clock / 6 and can be further divided down inside the McBSP module. Please note that if this clock is used, it must be divided down at least by /2.

If a McBSP port is not used or some of the signals are not used, the pins can be left unconnected since internal pullup/down resistors are included. The CLKS also has an internal pulldown resistor so that it can be left unconnected if not used.

All standard McBSP modes are supported (as compared to the TMS320C6474) with the exception of SPI mode.

7.1.2 System Implementation of McBSP

The maximum McBSP performance is achievable only when using source synchronous modes and point-to-point connections. In this case, use series resistance to reduce over/under-shoot. Generally acceptable values are 10 Ω, 22 Ω, or 33 Ω. To determine the optimum value simulations using the IBIS, models should be performed to check signal integrity and ac timings.

Multiple DSPs can be connected to a common McBSP bus using TDM mode. The additional loads require a reduction in the operating frequency. Also, the specific routing topology becomes much more significant as additional DSPs are included. The way to determine the best topology and maximum operating frequency are by performing IBIS simulations.

7.2 GPIO/Device Interrupts

Documentation for GPIO/Interrupts:

- *TMS320C6474 DSP General-Purpose Input/Output (GPIO) User's Guide* (SPRUG16) [25]
- TMS320C6474 IBIS Model File (SPRM336)
- *Using IBIS Models for Timing Analysis* (SPRA839) [28]

7.2.1 Configuration of GPIO/Interrupts

None of the GPIOs are multiplexed with other peripherals but several of the GPIOs are used for device configuration strapping options. The strapping options are latched by $\overline{\text{POR}}$ going high. After $\overline{\text{POR}}$ is high the pins are available as GPIO pins.

GPIOs are enabled at power-up and default to inputs.

All GPIOs can be used as interrupts and/or EDMA events to any of the cores.

All GPIOs have internal pulldown resistors, except GPIO4, which has an internal pullup resistor. Because the internal pullup and pulldown resistors are present, the pins can be no-connects if not used. If the opposite configuration settings is desired, use an external 1-kΩ resistor to overcome the internal pullup/down resistor.

7.2.2 System Implementation of GPIO/Interrupts

It is recommended that GPIO's used as outputs have a series resistance (22 or 33 Ω being typical values). The value (or need) for the series resistor can be determined by simulating with the IBIS models.

If you want to have a GPIO input default to a particular state (low or high), use an external resistor. A pullup resistor value of 1-kΩ is recommended to make sure that it over-rides the internal pulldown resistor present on some GPIOs. If this GPIO is also used as a strapping option, the default state needs to also be the desired boot strapping option. The RESETSTAT signal can be used to tri-state logic that drives a GPIO boot strapping state during the $\overline{\text{POR}}$ transition.

7.3 Timers

Documentation for Timers:

- *TMS320C6474 DSP 64-Bit Timer User's Guide* (SPRUG18) [27]
- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (SPRU732) [29]
- TMS320C6474 IBIS Model File (SPRM336)
- *Using IBIS Models for Timing Analysis* (SPRA839) [28]

7.3.1 Configuration of Timers

There are six timer peripherals and they are enabled at power-up.

Each timer can be configured as a single 64-bit timer, as two 32-bit timers or as a watch-dog timer. There are two external timer input signals and two external timer output signals. Each of the six timers can select either one of the two timer input pins as a source, between two internal sources from the frame sync module, or an internal clock that is core clock /6. Each of the two timer output pins can be driven by any of the six timers. When a timer is used as two 32-bit timers, the timer input and output can only be used with the lower 32-bit timer. When used as a watchdog timer, Timers 3, 4, and 5 correspond to CPU cores 0, 1, and 2, respectively. When in watchdog mode, a watchdog timeout on any of these timers can optionally reset that particular CPU automatically.

The timer module is clocked from CPU core clock frequency/6.

If the external timer input signals are not used, the pins can be left unconnected and the internal pulldown resistors bring the input to a low state.

In addition to the timer peripherals, each CPU core has a 64-bit free running counter that advances each CPU clock after counting is enabled. The counter is accessed using two 32-bit read-only control registers in the CPU. For more details on this timer, see the Time Stamp Counter Registers described in the *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (SPRU732) [29].

Timer inputs can optionally be used as general-purpose inputs. Timer outputs can optionally be used as general-purpose outputs.

7.3.2 System Implementation of Timers

It is recommended that external timer signals use series resistance (22 Ω or 33 μ being typical values). The value (or need) for the series resistor can be determined by simulating with the IBIS models.

External timer input signals are synchronized to the internal timer clock. Since the timer operates at CPU core/6, the timer input can be delayed from the timer input as much as one CPU core clock period * 6 (seconds).

7.4 Inter-Integrated Circuit (I2C)

Documentation for I2C:

- *TMS320C6474 DSP Inter-Integrated Circuit (I2C) Module User's Guide* (SPRUG22) [24]
- TMS320C6474 IBIS Model File (SPRM336)
- *Using IBIS Models for Timing Analysis* (SPRA839) [28]
- Philip's I2C Specification, Version 2.1

7.4.1 Configuration of I2C

The I2C peripheral powers up enabled. The input clock for the I2C module is core clock /6. There is a prescaler in the I2C module that needs to be set up to reduce this frequency to an internal module clock of 7 MHz to 12 MHz.

If the I2C signals are not used, the SDA and SCL pins can be left floating. This causes a slight increase in power due to leakage, which can be avoided by having pullup resistors.

7.4.2 System Implementation of I2C

External pullup resistors to 1.8 V are needed on the I2C signals (SCL, SDA). The recommended pullup resistor value is 4.7-kΩ.

Multiple I2C devices can be connected to the interface, but the speed may need to be reduced (400 KHz is the maximum) if many devices are connected.

The I2C pins are not 2.5 V or 3.3 V tolerant. For connection to 2.5 V or 3.3 V I2C peripherals, the *PCA9306 Dual Bidirectional I2C Bus and SMBus Voltage-Level Translator Data Sheet* (SCPS113) [38] can be used.

7.5 Ethernet

Documentation for EMAC:

- *TMS320C6474 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) User's Guide* (SPRUG08) [23]
- *SGMII Specification (ENG-46158)*, Version 1.8, dated April 27, 2005 [6]
- *TMS320C6474 SERDES Implementation Guidelines* (SPRAAW9) [21]

7.5.1 Configuration of EMAC, SGMII and MDIO

The EMAC interface is compliant with the *SGMII Specification (ENG-46158)*, Version 1.8 [6] that specifies LVDS signals. Only the data channels are implemented so that the connected device must support clock recovery and not require a separate clock signal. When EMAC is enabled, the MDIO interface is enabled. The MDIO interface (MDCLK, MDIO) uses 1.8 V LVCMOS buffers.

EMAC must be enabled via software before it can be accessed unless the Boot over Ethernet bootmode is selected.

If EMAC is used, a RIOSGMIICLKP/N clock must be provided and the SERDES must be setup to generate a 1.25Gbps link. The PLL multiplier settings for the three recommended RIOSGMIICLKP/N clocks frequencies are given in Table 6. Although the SGMII SERDES share a reference clock with the SRIO SERDES, they have separate PLLs which can be setup with different multipliers.

Table 6. SGMII PLL Multiplier Settings

Reference Clock	PLL Multiplier	Full Rate	Half Rate	Quarter Rate
125 MHz	10	Not used	1.25 Gbps	Not used
156.25 MHz	8	Not used	1.25 Gbps	Not used
312.5 MHz	4	Not used	1.25 Gbps	Not used

If EMAC is not used, the SERDES signals can be left unconnected. MDIO can be left unconnected, but results in an increase in leakage current. This could be avoided by adding an external pullup resistor. If both EMAC and SRIO are not used, the RIOSGMIICLKP/N pins should be terminated as shown in Figure 3.

7.5.2 System Implementation of SGMII

SGMII specifies LVDS signaling as defined in [7]. The C6474 uses a CML based SERDES interface that requires ac coupling to interface to LVDS levels; use 0.1 μF ac coupling capacitors for this purpose. The SERDES receiver includes a 100 Ω termination so an external 100 Ω termination is not needed. Examples of SERDES to LVDS connections are given in Section 8.1.

If the connected SGMII device does not provide common-mode biasing, external components need to be added to bias the LVDS side of the ac-coupling capacitors to the nominal LVDS offset voltage, normally 1.2 V.

For information regarding supported topologies and layout guidelines,see *TMS320C6474 SERDES Implementation Guidelines* (SPRAAW9) [21].

The SGMII interface supports hot-swap, where the ac coupled inputs of the device can be driven without a supply voltage applied.

Suggestions on SGMII reference clocking solutions can be found in Section 4.1.

SRIO/SGMII SERDES power planes and power filtering requirements are covered in Section 5.

7.5.3 SGMII MAC to MAC Connection

The SGMII interface can be connected from the C6474 device to PHY or from the C6474 device to MAC, including C6474-to-C6474 device direct connects. An example of the hardware connections is shown in Figure 20. For auto-negotiation purposes, the C6474 device can be configured as a master or a slave or it can be setup for fixed configuration. If the C6474 device is connected to another MAC, the electrical compatibility must be evaluated to determine if additional terminations are needed.

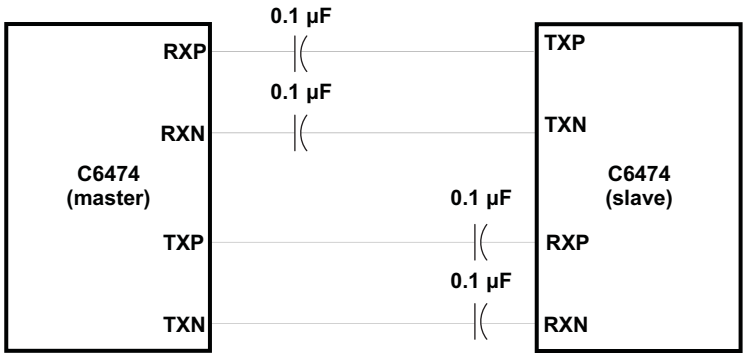

Figure 20. SGMII MAC to MAC Connection

7.6 Serial RapidIO (SRIO)

Relevant documentation for SRIO:

- *TMS320C6474 DSP Serial RapidIO User's Guide* (SPRUG23) [20]
- *RapidIO Interconnect Part VI: Physical Layer 1x/4x LP-Serial Specification*, Version 1.2 [9]
- *TMS320C6474 SERDES Implementation Guidelines* (SPRAAW9) [21]

7.6.1 Configuration of SRIO

SRIO defaults disabled and with internal memories for the module in a sleep state. The memories, followed by the module, must be enabled by software before use (unless Boot over SRIO is selected).

There are two SRIO lanes. A simple form of SRIO forwarding is supported to allow a daisy chain implementation.

The SRIO requires a differential reference clock: RIOSGMIICLKP/N. Supported frequencies for this clock are 125 MHz, 156.25 MHz, and 312.5 MHz. The SERDES used in the SRIO solution has a PLL that needs to be configured based on this reference clock and the desired link rate. Link rates can be full, half or quarter rate relative to the PLL frequency. Refer to Table 7 for PLL multiplier settings relative to link rate.

Table 7. SRIO PLL Multiplier Settings

Reference Clock	PLL Multiplier	Full Rate	Half Rate	Quarter Rate
125 MHz	12.5	3.125 Gbps	Not used	Not used
156.25 MHz	10	3.125 Gbps	Not used	Not used
125 MHz	10	2.5 Gbps	1.25 Gbps	Not used
156.25 MHz	8	2.5 Gbps	1.25 Gbps	Not used
312.5 MHz	5	3.125 Gbps	Not used	Not used
312.5 MHz	4	2.5 Gbps	1.25 Gbps	Not used

It is possible to configure the C6474 device to boot load application code over the SRIO interface. Boot over SRIO is a feature that is selected using boot strapping options. For details on boot strapping options, see the C6474 data manual.

If the SRIO peripheral is not used, the SRIO link pins can be left floating and the SERDES links should be left in the disabled state. If the SRIO and SGMII peripherals are both unused, the link pins can be left floating; however, the RIOSGMIICLKP/N should be terminated as shown in Figure 3.

The SRIO SERDES ports support hot-swap, where the ac coupled inputs of the device can be driven without a supply voltage applied.

If the SRIO peripheral is enabled but only 1 link is used, the pins of the unused link can be left floating.

7.6.2 System Implementation of SRIO

The Serial RapidIO implementation is compliant to the *RapidIO Interconnect Part VI: Physical Layer 1x/4x LP-Serial Specification*, Version 1.2 [9].

For information regarding supported topologies and layout guidelines, see *TMS320C6474 SERDES Implementation Guidelines* (SPRAAW9) [21].

Suggestions on SRIO reference clocking solutions can be found in Section 4.1.

SRIO/SGMII SERDES power planes and power filtering requirements are covered in Section 5.

7.7 Antenna Interface (AIF)

Relevant documentation for AIF:

- OBSAI RP3 Specifications [1] and [2]
- CPRI Specification Version 2.0 [4]
- XAUI Electrical Specification (IEEE-802.3ae-2002), dated 2002 [8]
- *TMS320C6474 DSP Antenna Interface User's Guide* (SPRUG12) [31]
- *TMS320C6474 SERDES Implementation Guidelines* (SPRAAW9) [21]

7.7.1 Configuration of AIF

AIF defaults disabled and with the internal memories for the module in a sleep state. The memories, followed by the module, must be enabled by software before use.

There are two protocol modes supported on the AIF interface: OBSAI and CPRI. The mode is selected by software after power-up. All links are the same mode.

The AIF module requires the AIF reference clock (SYSCLKP/N) to drive the SERDES PLLs and requires frame sync timing signals provided by the frame sync module. The frame sync clock provided to the FSM has the following requirements:

- RP1 mode:
  - FSYNCCLKP/N must be 30.72 MHz (8× UMTS chip rate)
  - FRAMEBURSTP/N must provide a UMTS frame boundary signal
- Non-RP1 mode:
  - ALTFSYNCCLK must be 1×, 2×, 4×, 8×, or 16× UMTS chip rate
  - ALTFSYNCPULSE must provide UMTS frame boundary pulse

For proper operation of the AIF, the SYSCLKP/N (which is the antenna interface SERDES reference clock) and the frame sync clock (either FSYNCCLKP/N or ALTFSYNCCLK) must be generated from the same clock source and must be assured not to drift relative to each other.

The AIF reference clock and the SERDES PLL multiplier are used to select the link rates. Both CPRI and OBSAI have 3 supported line rates that run at 1×, 2×, and 4× the base line rate. The SERDES line rates can be operated at full rate, half rate, or quarter rate of the PLL output. For that reason, it is suggested that the AIF SERDES PLL be run at the 4× line rate. Each link pair can be configured as full rate (4×), half rate (2×), or quarter rate (1×). Table 8 shows AIF SERDES suggested clocking options.

If OBSAI 4× links are used, the CPU minimum frequency is 1 GHz. If OBSAI 1×/2× links or used, or if CPRI is used, the CPU minimum frequency is 800 MHz.

Table 8. AIF SERDES Clocking Options

	Reference Clock	PLL Multiplier	Full Rate	Half Rate	Quarter Rate
CPRI	61.44 MHz	20	2.4576 Gbps	1.2288 Gbps	614.4 Mbps
	122.88 MHz	10			
	153.6 MHz	8			
OBSAI	61.44 MHz	25	3.072Gbps	1.536 Gbps	768 Mbps
	122.88 MHz	12.5			
	153.6 MHz	10			

The AIF SERDES ports supports hot-swap, where the ac coupled inputs of the device can be driven without a supply voltage applied.

Any TX/RX links not used can be left floating. If the AIF peripheral is not used, the link pins can be left floating. The reference clock should be terminated as shown in Figure 3.

7.7.2 System Implementation of AIF

In OBSAI RP3 mode, the interface is electrically compatible with the *OBSAI RP3 Specification*, Version 3.0 [1]. From a protocol implementation, the interface is compatible with RP3, February 5th 2004 [2] and partly compatible with Version 3.0 [1].

In CPRI mode, the interface is electrically compatible with the *XAUI Electrical Specification* (IEEE-802.3ae-2002) [8].

For information regarding supported topologies and layout guidelines, see the *TMS320C6474 SERDES Implementation Guidelines* (SPRAAW9) [21].

Suggestions on AIF reference clocking solutions can be found in Section 4.1.

AIF SERDES power planes and power filtering requirements are covered in Section 5.

7.8 Frame Sync Module (FSM)

Relevant documentation for FSM:

- OBSAI RP1 Version 1.0 [3]
- *TMS320C6474 DSP Frame Synchronization Module User's Guide* (SPRUG13) [32]

7.8.1 Configuration of FSM

The FSM provides system timing events for the entire C6474 device and is required for proper operation of the AIF. At a minimum, the FSM requires two external signals: a frame clock and a synchronization event. At most, the FSM can support two reference clocks and two synchronization events.

For an OBSAI RP1 compliant interface, supply the FSYNCLKP/N input with a 30.72 MHz clock and the FrameBurstP/N should provide the frame burst signaling as defined in the RP1 specification.

The software can select singled ended pins for frame clock and a synchronization event instead of the LVDS inputs as mentioned above. In this case, FSYNCLKP/N is replaced with ALTFSYNCLK and ALTFSYNCPULSE replaces FrameBurstP/N. These are 1.8 V CMOS input buffers. ALTSYNCPULSE can be used to indicate a synchronization event, but cannot be used to transmit a serial data pattern as is done with FrameBurstP/N. With ALTFSYNCPULSE, the frame boundary is indicated the first time ALTFSYNCPULSE is latched high by the frame clock after the FSM has been configured to latch a new frame boundary. Once the frame boundary is latched, it is not latched again unless the FSM is configured to do so. Because of this, the pulse duration time of ALTFSYNCPULSE is not critical.

For proper operation of the AIF, the SYSCLKP/N (which is the antenna interface SERDES reference clock) and the frame sync clock (either FSYNCCLKP/N or ALTFSYNCCLK) must be generated from the same clock source and assured not to drift relative to each other.

The FSM has one counter used to generate AIF timing and events and can be used to generate other events as well. This counter is controlled by the signals mentioned above. The FSM includes a second counter that can generate multiple chip events. This can be controlled by either the same signals mentioned above or by a separate clock and synchronization event. The alternate clock and sync event that can control the system counter are: TRTCLK and TRT (time reference tick). These are both 1.8 V CMOS inputs.

The valid FSM synchronization and clocking options are described in Table 9.

Table 9. Frame Sync Module Config Options

AIF Timer Sync	AIF Timer Clock	System Timer Sync	System Timer Clock	Intended Used
FRAMEBURSTP/N	FSYNCCLKP/N	FRAMEBURSTP/N	FSYNCCLKP/N	RP1 or non-RP1 differential sync, differential clock
ALTFSYNCPULSE	ALTFSYNCCLK	ALTFSYNCPULSE	ALTFSYNCCLK	RP1 or non-RP1 single-ended sync, single-ended clock
ALTFSYNCPULSE	FSYNCCLKP/N	ALTFSYNCPULSE	FSYNCCLKP/N	RP1 or non-RP1 single-ended sync, differential clock
ALTFSYNCPULSE	ALTFSYNCCLK	TRT	TRT_CLK	Non-RP1 or non-UMTS single-ended sync, single-ended clock

Single-ended inputs have internal pulldown resistors; if these inputs are not used, they can be left unconnected.

If the LVDS inputs (FSYNCCLKP/N pins AD7/AD8 and FRAMEBURST pins AD9/AD10) are not used, external connections should be provided to generate a valid logic level. The recommended connections for unused LVDS inputs are shown in Figure 21. The 1-kΩ resistor is used to reduce power.

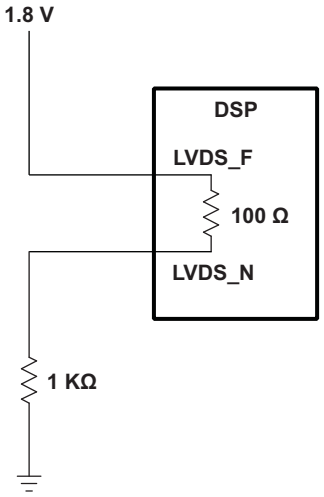

Figure 21. Unused LVDS Connections

7.8.2 System Implementation of FSM

For an RP1 compliant interface, the frame sync clock and frame sync burst signal defined by the RP1 Specification [3] should be connected to FSYNCCLKP/N and FRAMEBURSTP/N, respectively.

LVDS 1:N buffers (such as the SN65LVDS108 or CDCL1810) can be used to connect these signals to multiple DSPs on a single board. The 100 Ω LVDS termination resistor is included in the C6474 LVDS receiver so an external 100 Ω resistor is not needed. These are standard LVDS inputs so, unlike the LJCB inputs, these inputs should not be ac coupled. They should be driven directly by an LVDS compliant driver.

The SMFRAMECLK output is available to generate a frame sync output to other devices based on the frame clock and frame sync inputs. Its switching frequency and offset are programmable in the FSM. This output edge is not aligned with the frame clock input so take care if this output needs to be latched based on this clock.

For information on clocking distribution options for the single-ended frame sync clocks, see Section 4.2.

7.9 DDR2

Relevant documentation for DDR2:

- *TMS320C6474 DSP DDR2 Memory Controller User's Guide* (SPRUG19) [22]
- *TMS320C6474 DDR2 Implementation Guidelines* (SPRAAW8) [18]
- JEDEC JESD79-2B [10]

7.9.1 Configuration of DDR2

The DDR2 peripheral is enabled at power-up.

The DDR2 output clock is derived from the DDR2 PLL that uses DDRREFCLKP/N as a reference clock. The DDR2 PLL operates at 10× the DDRREFCLKP/N frequency and the DDR2 output clock is 1/2 of the PLL output clock. For example, a 66.6 MHz reference clock results in a 667 MHz PLL output and a DDR2 output clock of 333 MHz for DDR2-667 support.

If the DDR2 peripheral is disabled, all interface signals (including reference clocks) can be left floating and the input buffers are powered down.

If the DDR2 is operated in 16-bit mode, pull the upper DDR2 bi-directional pins to valid states through 1-kΩ resistors. DDRDQS2, DDRDQS3, and DDRD[31:16] should have 1-kΩ pullup resistors to DV_{DD18}. DDRDQS2 and DDRDQS3 should have 1-kΩ pulldown resistors to GND. DDRDQM2, DDRDQM3, and DDRCLKOUT1P/N can be left unconnected.

7.9.2 System Implementation of DDR2

For information regarding supported topologies and layout guidelines, see the *TMS320C6474 DDR2 Implementation Guidelines* (SPRAAW8) [18].

Suggestions on DDR2 reference clocking solutions can be found in Section 4.1.

7.10 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual* (SPRU655) (but note differences defined below) [15]
- Boundary Scan Test Specification (IEEE-1149.1) [11]
- AC Coupled Net Test Specification (IEEE-1149.6) [12]

7.10.1 Configuration of JTAG/Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant to both IEEE-1149.1 and 1149.6 (for SERDES ports). Boundary scan can be used regardless of the device configuration.

As an emulation interface, the JTAG port can be used in various modes:

- Standard emulation: requires only five standard JTAG signals
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in this mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU[18:00] pins to output the trace data, however, the number of pins used is configurable.

Emulation can be used regardless of the device configuration.

For supported JTAG clocking rates (TCLK), see the C6474 data manual. The EMU[18:00] signals can operate up to 166 Mbps, depending on the quality of the board level implementation.

Any unused emulation port signals can be left floating.

7.10.2 System Implementation of JTAG / Emulation

For most system level implementation details, see the *Emulation and Trace Headers Technical Reference Manual* (SPRU655). However, there are a few differences for the C6474 device implementation compared with this document:

- Although the document implies 3.3-V signaling, 1.8-V signaling is supported as long as the TVD source is 1.8 V.

For a single DSP connection where the trace feature is used, the standard non-buffered connections can be used along with the standard 14 pin connector. If the trace feature is used, which requires the 60-pin emulator connector, the five standard JTAG signals should be buffered and TCLK and RTCLK should be buffered separately. It is recommended to have the option for an ac parallel termination on TCLK since it is critical that the TCLK have a clean transition. EMU0 and EMU1 should not be buffered since these are used as bidirectional signals when used for HS-RTDX.

For a system with multiple DSPs that do not use the trace analysis features, the JTAG signals should be buffered as described above but the standard 14 pin connector can be used.

There are two recommended solutions if trace analysis is desired in a system with multiple DSPs.

Emulator with trace, solution #1: trace header for each DSP (see Figure 22)

- Pros
  - Most simple
  - Most *clean* solution electrically
- Cons
  - Expensive (multiple headers)
  - Takes up board real estate
  - No global breakpoints, synchronous run/halt

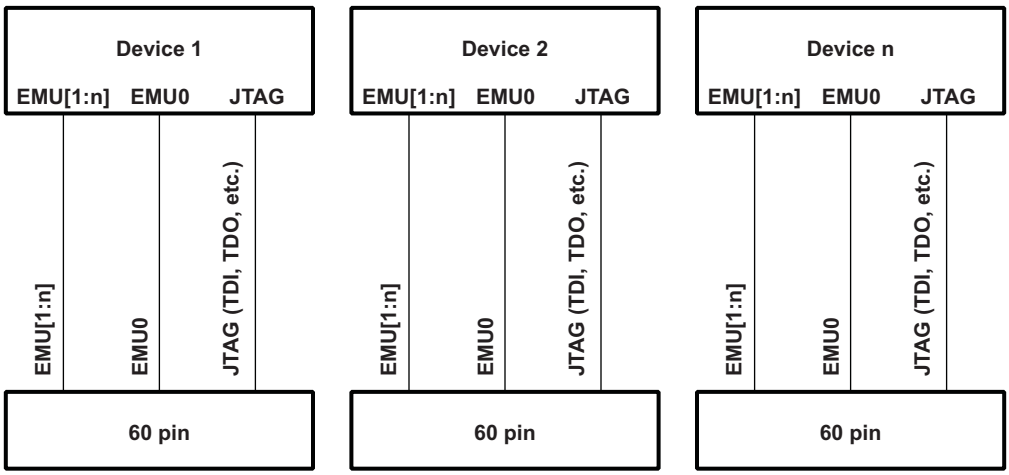

Figure 22. Emulator With Trace, Solution #1

Emulator with trace, solution #2: single trace header (see Figure 23)

- Pros
  - Fairly *clean* solution electrically
  - Supports global breakpoints, synchronous run/halt
- Cons
  - Supports trace on only one device
  - Less bandwidth for trace (EMU0 used for global breakpoints)
  - Loss of AET action points on EMU1 (only significant if EMU1 has been used as a trigger input/output between devices. EMU0 can be used instead if needed).

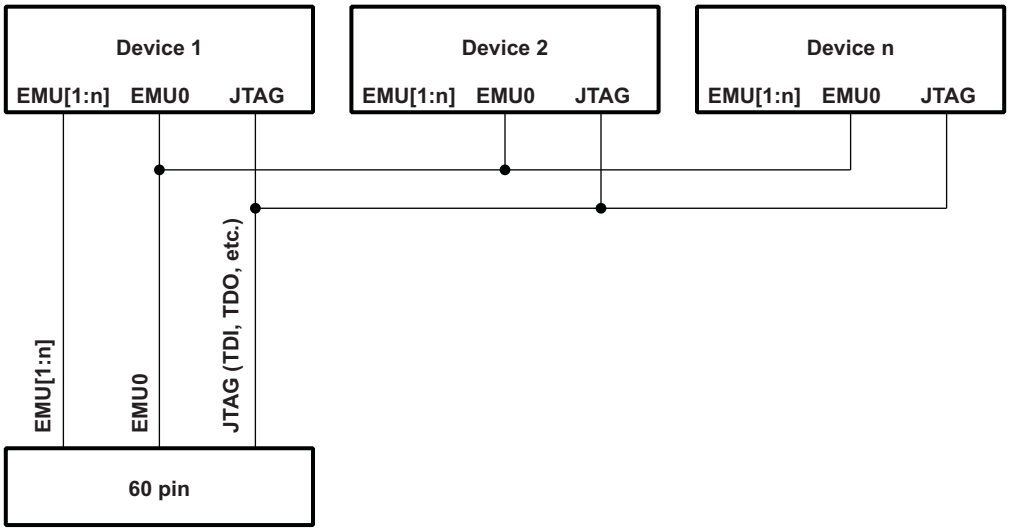

Figure 23. Emulation With Trace, Solution #2

No external pullup/down resistors are needed since there are internal pullup/down resistors on all emulation signals.

Although no buffer is shown, for multiple DSP connections it is recommended to buffer the five standard (TDI, TDO, TMS, TCK, and TRST) JTAG signals.

If trace is used, it is not recommended to add both a 60-pin header and a 14-pin header due to signal integrity concerns. 60-pin to 14-pin adapters are available to allow connection to emulators that only support the 14-pin connector.

Some emulators may not support 1.8 V I/O levels. Check emulators intended to operate with the C6474 device for supported I/O levels. If 1.8 V is not supported, a voltage translator circuit is needed or a voltage converter board may be available. If the C6474 device is in a JTAG chain with devices that have a different voltage level than 1.8 V (i.e., 3.3 V), voltage translation is needed.

Figure 24 shows a dual voltage JTAG solution using buffers to perform the voltage translation. The ALVC family for 3.3 V and the AUC family for 1.8 V are both used because they have similar propagation delays and high-drive outputs.

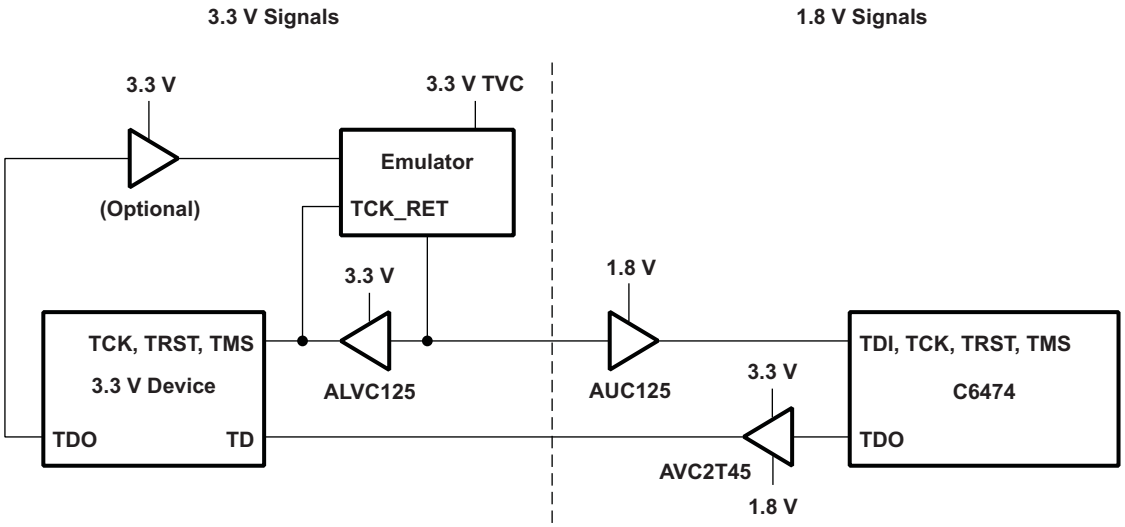

Figure 24. Emulator Voltage Translation With Buffers

Figure 25 shows an example of using FET switch devices for voltage translation. If EMU0 and EMU1 are connected, use this approach since these are bi-directional signals.

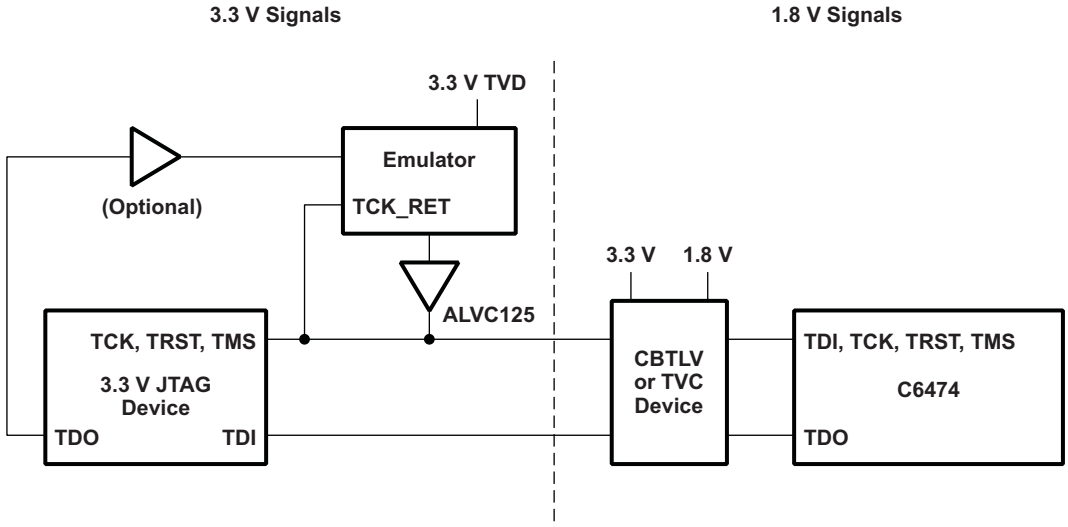

Figure 25. Emulator Voltage Translation With Switches

If the trace signals are supported, they may need to have voltage translation as well. Due to the speed of that interface, connect these signals directly to the emulation header.

8 SERDES-LVDS Termination Options

TI SERDES are CML implementations and do not directly support LVDS levels. Compatibility with standard LVDS signals is achievable with proper terminations as described in this section.

8.1 LVDS to CML Example

The following is an example of an LVDS to CML connection.

- Requires ac termination because the LVDS common-mode voltage is too high for the C6474 device SERDES receivers
- CML receivers include 100 Ω termination needed by LVDS and include internal biasing (no external biasing needed)
- Refer to Figure 26.

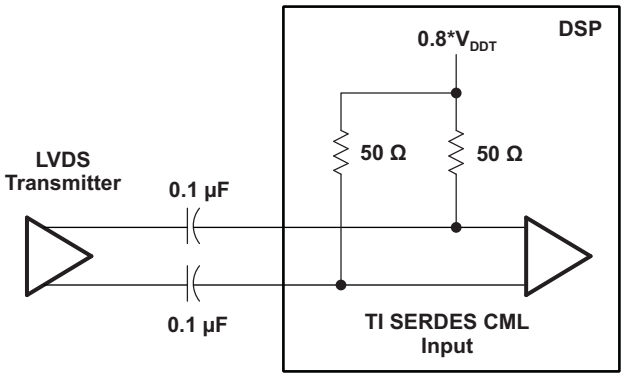

Figure 26. LVDS to CML Connection

8.2 CML to LVDS Example

The following is an example of a CML to LVDS connection:

- Requires ac termination because C6474 device CML output voltage is too low for LVDS receiver and the common-mode voltages are incompatible.
- LVDS receivers require 100 Ω terminations and proper biasing.
- Some LVDS receivers include 100 Ω termination and some do not.
- Some LVDS receivers include internal biasing and some do not.
- The basic connection diagram is shown in Figure 27.

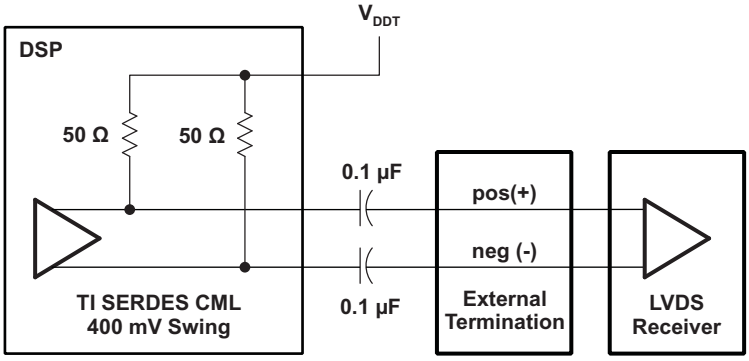

Figure 27. CML to LVDS Connection Basic Diagram

- If the LVDS receiver includes the 100 Ω termination and internal biasing, there is no need for external

terminations.

- If the LVDS receiver includes neither the 100 Ωs or biasing, use the external terminations shown in Figure 28.

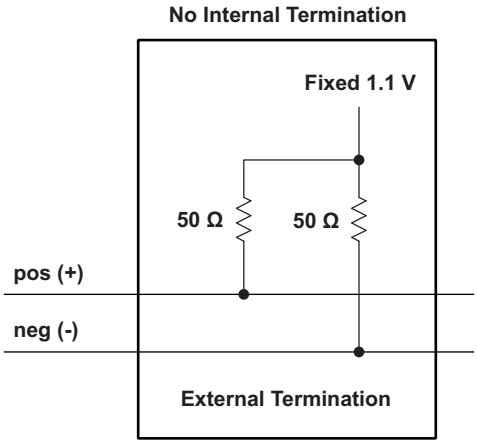

Figure 28. External Terminations: Receiver Has No Internal Terminations

- If the LVDS receive includes the 100 Ω termination but no biasing, use the external terminations shown in Figure 29.

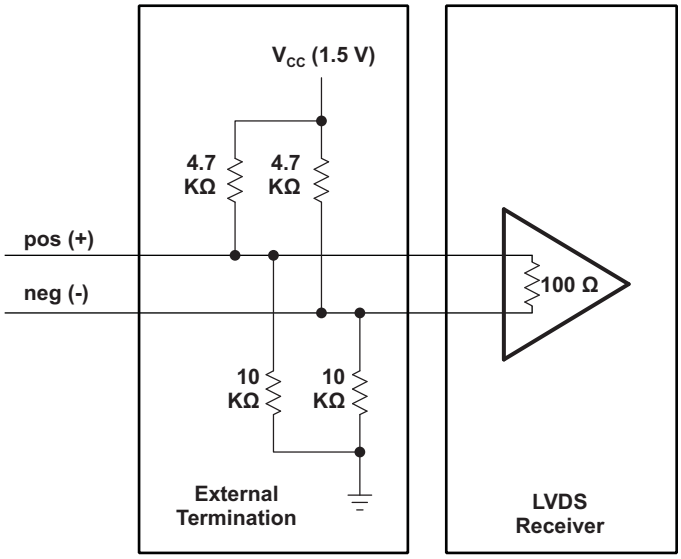

Figure 29. External Terminations: Receiver With 100 Ω

- If the LVDS receiver includes 100 Ω terminations and internal pullup resistors (sometimes used for fail-safe), use the type of termination shown in Figure 30. Adjust the external resistor values based on the V_{CC} and internal resistors to generate a bias voltage of 1.0 V to 1.2 V.

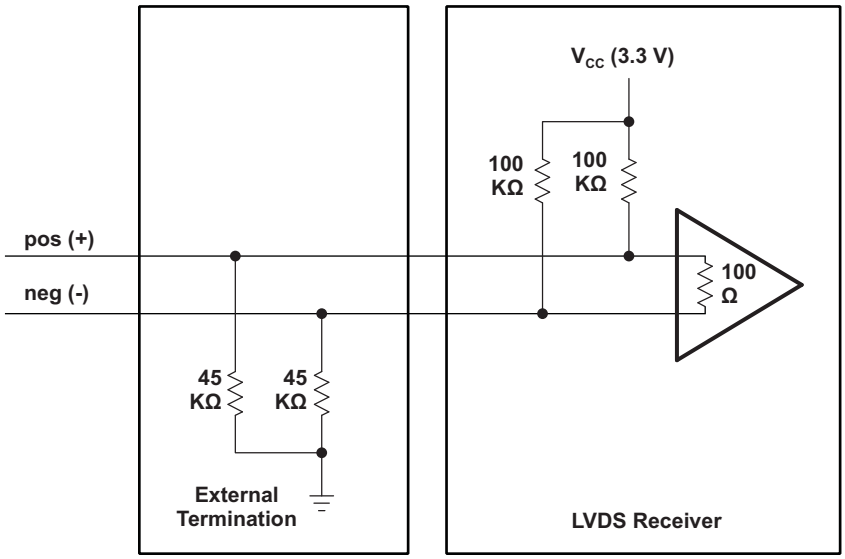

Figure 30. External Terminations: Receiver With 100 Ω

- There are other combinations that may be needed for other types of input buffers. The important factors are that there is a 100 Ω impedance and a bias voltage set around 1.2 V.

9 References

1. *OBSAI Reference Point 3 Specification*, Version 3.0
2. *OBSAI Reference Point 3 Specification*, February 5th, 2004
3. *OBSAI Reference Point 1 Specification*, Version 1.0, dated October 16, 2003
4. *CPRI Specification*, Version 2.0
   http://www.cpri.info/spec.html
5. *JEDEC JESD8-15 (SSTL-1.8V) Specification (EAI/JESD8-15a)*, dated September 2003
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6. *SGMII Specification (ENG-46158)*, Version 1.8, dated April 27, 2005
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8. *XAUI Electrical Specification (IEEE-802.3ae-2002)*, dated 2002
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10. *JEDEC DDR2 SDRAM Specification (EAI/JESD79-2B)*
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12. *AC Coupled Net Test Specification (IEEE-1149.6)*
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16. *JEDEC 2.5 V ± 0.2 V (Normal Range), and 1.8 V to 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit Specification (EAI/JESD8-5)*, dated October 1995
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    http://www.jedec.org/download/search/JESD8-7.pdf
18. *TMS320C6474 DDR2 Implementation Guidelines* (SPRAAW8)
19. *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)
20. *TMS320C6474 DSP Serial RapidIO User's Guide* (SPRUG23)
21. *TMS320C6474 SERDES Implementation Guidelines* (SPRAAW9)
22. *TMS320C6474 DSP DDR2 Memory Controller User's Guide* (SPRUG19)
23. *TMS320C6474 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) User's Guide* (SPRUG08)
24. *TMS320C6474 DSP Inter-Integrated Circuit (I2C) Module User's Guide* (SPRUG22)
25. *TMS320C6474 DSP General-Purpose Input/Output (GPIO) User's Guide* (SPRUG16)
26. *TMS320C6474 Multichannel Buffered Serial Port (McBSP) User's Guide* (SPRUG17)
27. *TMS320C6474 DSP 64-Bit Timer User's Guide* (SPRUG18)
28. *Using IBIS Modes for Timing Analysis* (SPRA839)
29. *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (SPRU732)
30. *TMS320C6474 DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (SPRUG09)
31. *TMS320C6474 DSP Antenna Interface User's Guide* (SPRUG12)
32. *TMS320C6474 DSP Frame Synchronization Module User's Guide* (SPRUG13)
33. *TMS320C645x/C647x Bootloader User's Guide* (SPRUEC6)
34. *Filtering Techniques: Isolating Analog and Digital Power Supplies in TI's PLL-Based CDC Devices* (SCAA048)
35. *PTH08T240F 10-A, 4.5-V to 14-V Input, Non-Isolated Power Module for 3-GHz DSP Systems* (SLTS277)
36. *CDCx706/x906 Termination and Signal Integrity Guidelines* (SCAA080)
37. *TMS320TCI6487/88 Capacitor Selection Guide - Using the PTH08T240F Power Module* (SPRAAM9)

38. *Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards With the TI AVCA164245 and AVCB164245 Dual-Supply Bus-Translating Transceivers Application Report* (SCEA030)
39. *Selecting the Right Level-Translation Solution Application Report* (SCEA035)
40. *PCA9306 Dual Bidirectional I2C Bus and SMBus Voltage-Level Translator Data Sheet* (SCPS113)
41. *TMS320C6474 Thermal Reference Document* (ask for availability)
42. *AC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML* (SCAA059)
43. *DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CM* (SCAA062)
44. *SN65LVDS108 8-Port LVDS Repeater Data Sheet* (SLLS399)
45. *CDCLVP110 Low-Voltage 1:10 LVPECL/HSTL With Selectable Input Clock Driver Data Sheet* (SCAS683)
46. *TMS320C6474 Power Consumption Summary* application report (SPRAAX3)

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