

Technical Reference Manual

LP873244-Q1 Technical Reference Manual



ABSTRACT

This document provides the register bit values for the one-time programmable (OTP) bits of the orderable part number, LP873244RHDRQ1.

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1 Introduction

This technical reference manual can be used as a reference for the LP873244-Q1 default register bits after OTP memory download. This technical reference manual does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the [LP8732xx -Q1 Dual High-Current Buck Converter and Dual Linear Regulator data sheet](#).

2 OTP Memory Device Settings

This section lists all of the device settings that are downloaded from OTP memory.

[Table 2-1](#) lists the device settings for I²C and OTP revision ID values.

Table 2-1. Device Identification and I²C Settings

	Description	Bit Name	LP873244-Q1
I ² C address			61h
DEVICE_ID	Device specific ID code	DEVICE_ID	1h
OTP_ID	Identification code for OTP version	OTP_ID	44h

[Table 2-2](#) lists the device settings for BUCK0 and BUCK1. The maximum allowed slew-rate for BUCKx depends on the output capacitance. Refer to the for output capacitance boundary conditions.

Table 2-2. BUCK0 and BUCK1 OTP Settings

	Description	Bit Name	LP873244-Q1
	Buck phase configuration (2 single phase Bucks or combined 2 phase, denoted as 1+1 or 2-phase)		1+1
	Switching frequency		2 MHz
	Spread spectrum	EN_SPREAD_SPEC	Enabled

Table 2-2. BUCK0 and BUCK1 OTP Settings (continued)

	Description	Bit Name	LP873244-Q1
BUCK0	Output voltage	BUCK0_VSET	0.90 V
	Enable, EN-pin or I ² C register	BUCK0_EN_PIN_CTRL	EN-pin
	Control for BUCK0	BUCK0_EN	High
	Force PWM mode or auto mode	BUCK0_FPWM	Force PWM
	Peak current limit	BUCK0_ILIM	3.0 A
	Maximum load current limit	NA	2.0 A
	Slew rate	BUCK0_SLEW_RATE	3.8 mV/μs
	Startup delay	BUCK0_STARTUP_DELAY	0 ms
	Shutdown delay	BUCK0_SHUTDOWN_DELAY	3 ms
BUCK1	Output voltage	BUCK1_VSET	1.1 V
	Enable, EN-pin or I ² C register	BUCK1_EN_PIN_CTRL	EN-pin
	Control for BUCK1	BUCK1_EN	High
	Force PWM mode or auto mode	BUCK1_FPWM	Force PWM
	Peak current limit	BUCK1_ILIM	3.0 A
	Maximum load current limit	NA	2.0 A
	Slew rate	BUCK1_SLEW_RATE	3.8 mV/μs
	Startup delay	BUCK1_STARTUP_DELAY	3 ms
	Shutdown delay	BUCK1_SHUTDOWN_DELAY	0 ms

Table 2-3 lists the device settings for LDO0 and LDO1.

Table 2-3. LDO0 and LDO1 OTP Settings

	Description	Bit Name	LP873244-Q1
LDO0	Output voltage	LDO0_VSET	1.800 V
	Enable, EN-pin or I ² C register	LDO0_EN_PIN_CTRL	EN-pin
	Control for LDO0	LDO0_EN	High
	Startup delay	LDO0_STARTUP_DELAY	1 ms
	Shutdown delay	LDO0_SHUTDOWN_DELAY	2 ms
LDO1	Output voltage	LDO1_VSET	3.3 V
	Enable, EN-pin or I ² C register	LDO1_EN_PIN_CTRL	EN-pin
	Control for LDO1	LDO1_EN	High
	Startup delay	LDO1_STARTUP_DELAY	2 ms
	Shutdown delay	LDO1_SHUTDOWN_DELAY	1 ms

Table 2-4 lists the device settings for GPIOs.

Table 2-4. EN, CLKIN, and GPIO Pin Settings

	Description	Bit Name	LP873244-Q1
EN pin	EN pin pull-down resistor enable or disable	EN_PD	Enabled
CLKIN pin	CLKIN or GPO2 mode selection	CLKIN_PIN_SEL	GPO2
	CLKIN pin pull-down resistor enable or disable (applicable for both CLKIN and GPO2 modes.)	CLKIN_PD	Enabled
	Frequency of external clock when connected to CLKIN	EXT_CLK_FREQ	2 MHz
	Enable for the internal PLL. When PLL disabled, internal RC OSC is used	EN_PLL	Disabled
GPO	GPO output type (push-pull or open drain)	GPO_OD	OD
	Enable, EN-pin or I ² C register	GPO_EN_PIN_CTRL	EN-pin
	Control for GPO	GPO_EN	High
	Startup delay	GPO_STARTUP_DELAY	15 ms
	Shutdown delay	GPO_SHUTDOWN_DELAY	0 ms

Table 2-4. EN, CLKIN, and GPIO Pin Settings (continued)

	Description	Bit Name	LP873244-Q1
GPO2	GPO2 output type (push-pull or open drain)	GPO2_OD	OD
	Enable, EN-pin or I ² C register	GPO2_EN_PIN_CTRL	I ² C
	Control for GPO2	GPO2_EN	Low
	Startup delay	GPO2_STARTUP_DELAY	0 ms
	Shutdown delay	GPO2_SHUTDOWN_DELAY	0 ms

Table 2-5 lists the device PGOOD settings.

Table 2-5. PGOOD OTP Settings

	Description	Bit Name	LP873244-Q1
Signals monitored by PGOOD	BUCK0 output voltage	EN_PGOOD_BUCK0	No
	BUCK1 output voltage	EN_PGOOD_BUCK1	No
	LDO0 output voltage	EN_PGOOD_LDO0	No
	LDO1 output voltage	EN_PGOOD_LDO1	No
	Thermal warning	EN_PGOOD_TWARN	No
PGOOD mode selections	PGOOD thresholds for BUCK0, BUCK1 (Undervoltage and Window (undervoltage and overvoltage))	PGOOD_WINDOW_BUCK	Window
	PGOOD thresholds for LDO0, LDO1 (Undervoltage and Window (undervoltage and overvoltage))	PGOOD_WINDOW_LDO	Window
	PGOOD operating mode (detecting UNUSUAL situations or detecting UNVALID situations)	PGOOD_MODE	Detecting UNUSUAL situations
	PGOOD signal mode (status or latched until fault source read)	PG_FAULT_GATES_PGOOD	Status
	PGOOD output mode (push-pull or open drain)	PGOOD_OD	OD
	PGOOD polarity (active high or active low)	PGOOD_POL	Valid level high

Table 2-6 lists the device protection settings.

Table 2-6. Protections OTP Settings

	Description	Bit Name	LP873244-Q1
Protections	Thermal warning level (125°C or 137°C)	TDIE_WARN_LEVEL	140°C
	Input overvoltage protection	NA	Enabled

Table 2-7 lists the device settings for interrupts. When an interrupt from an event is unmasked, an interrupt is generated on the nINT pin.

Table 2-7. Interrupt Mask Settings

	Interrupt event	Bit Name	LP873244-Q1
General	PGOOD pin changing active to inactive	PGOOD_INT_MASK	Masked
	Sync clock appears or disappears	SYNC_CLK_MASK	Masked
	Thermal warning	TDIE_WRN_MASK	Unmasked
	Load measurement ready	I_MEAS_MASK	Masked
	Register reset	RESET_REG_MASK	Masked
BUCK0	Buck0 PGood active	BUCK0_PGR_MASK	Masked
	Buck0 PGood inactive	BUCK0_PGF_MASK	Masked
	Buck0 current limit	BUCK0_ILIM_MASK	Masked
BUCK1	Buck1 PGood active	BUCK1_PGR_MASK	Masked
	Buck1 PGood inactive	BUCK1_PGF_MASK	Masked
	Buck1 current limit	BUCK1_ILIM_MASK	Masked
LDO0	LDO0 PGood active	LDO0_PGR_MASK	Masked
	LDO0 PGood inactive	LDO0_PGF_MASK	Masked
	LDO0 current limit	LDO0_ILIM_MASK	Masked

Table 2-7. Interrupt Mask Settings (continued)

	Interrupt event	Bit Name	LP873244-Q1
LDO1	LDO1 PGood active	LDO1_PGR_MASK	Masked
	LDO1 PGood inactive	LDO1_PGF_MASK	Masked
	LDO1 current limit	LDO1_ILIM_MASK	Masked

3 Power-up and Power Down Sequence

This section shows the power-up and power-down sequence for the device. The power-up and power-down delays for each rail are shown in [Figure 3-1](#).

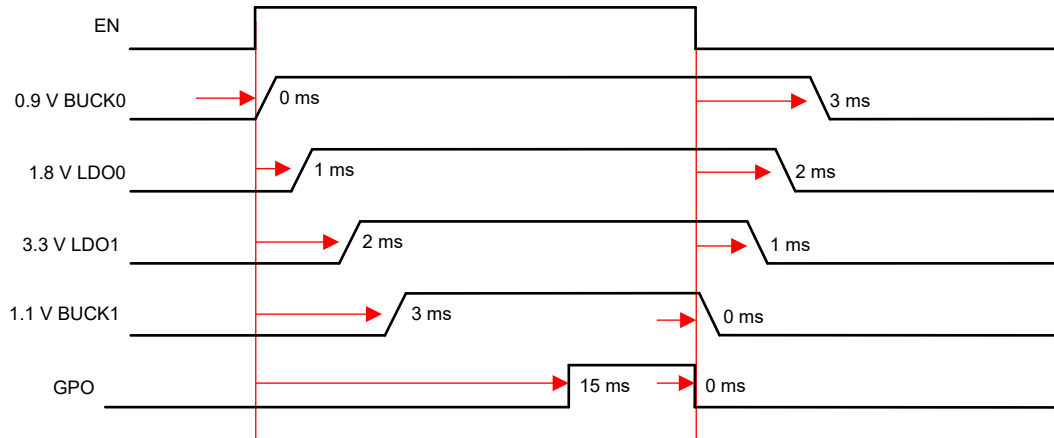


Figure 3-1. LP873244-Q1 Power-up and Power Down Sequence

4 Register Bits Loaded From OTP Memory

Table 4-1 lists the register bit values loaded from the OTP memory during device start-up.

Table 4-1. Summary of Control Registers

Address	Register Name	Bit	LP873244-Q1 Value
0x00	DEV_REV	DEVICE_ID[1:0]	1h
0x01	OTP_REV	OTP_ID[7:0]	44h
0x02	BUCK0_CTRL_1	BUCK0_FPWM	1h
0x02	BUCK0_CTRL_1	BUCK0_EN_PIN_CTRL	1h
0x02	BUCK0_CTRL_1	BUCK0_EN	1h
0x03	BUCK0_CTRL_2	BUCK0_ILIM[2:0]	3h
0x03	BUCK0_CTRL_2	BUCK0_SLEW_RATE[2:0]	4h
0x04	BUCK1_CTRL_1	BUCK1_FPWM	1h
0x04	BUCK1_CTRL_1	BUCK1_EN_PIN_CTRL	1h
0x04	BUCK1_CTRL_1	BUCK1_EN	1h
0x05	BUCK1_CTRL_2	BUCK1_ILIM[2:0]	3h
0x05	BUCK1_CTRL_2	BUCK1_SLEW_RATE[2:0]	4h
0x06	BUCK0_VOUT	BUCK0_VSET[7:0]	39h
0x07	BUCK1_VOUT	BUCK1_VSET[7:0]	61h
0x08	LDO0_CTRL	LDO0_EN_PIN_CTRL	1h
0x08	LDO0_CTRL	LDO0_EN	1h
0x09	LDO1_CTRL	LDO1_EN_PIN_CTRL	1h
0x09	LDO1_CTRL	LDO1_EN	1h
0x0A	LDO0_VOUT	LDO0_VSET[4:0]	0Ah
0x0B	LDO1_VOUT	LDO1_VSET[4:0]	19h
0x0C	BUCK0_DELAY	BUCK0_SHUTDOWN_DELAY[3:0]	3h
0x0C	BUCK0_DELAY	BUCK0_STARTUP_DELAY[3:0]	0h
0x0D	BUCK1_DELAY	BUCK1_SHUTDOWN_DELAY[3:0]	0h
0x0D	BUCK1_DELAY	BUCK1_STARTUP_DELAY[3:0]	3h
0x0E	LDO0_DELAY	LDO0_SHUTDOWN_DELAY[3:0]	2h
0x0E	LDO0_DELAY	LDO0_STARTUP_DELAY[3:0]	1h
0x0F	LDO1_DELAY	LDO1_SHUTDOWN_DELAY[3:0]	1h
0x0F	LDO1_DELAY	LDO1_STARTUP_DELAY[3:0]	2h
0x10	GPO_DELAY	GPO_SHUTDOWN_DELAY[3:0]	0h
0x10	GPO_DELAY	GPO_STARTUP_DELAY[3:0]	Fh
0x11	GPO2_DELAY	GPO2_SHUTDOWN_DELAY[3:0]	0h
0x11	GPO2_DELAY	GPO2_STARTUP_DELAY[3:0]	0h
0x12	GPO_CTRL	GPO2_OD	1h
0x12	GPO_CTRL	GPO2_EN_PIN_CTRL	0h
0x12	GPO_CTRL	GPO2_EN	0h
0x12	GPO_CTRL	GPO_OD	1h
0x12	GPO_CTRL	GPO_EN_PIN_CTRL	1h
0x12	GPO_CTRL	GPO_EN	1h
0x13	CONFIG	STARTUP_DELAY_SEL	1h
0x13	CONFIG	SHUTDOWN_DELAY_SEL	1h
0x13	CONFIG	CLKIN_PIN_SEL	0h
0x13	CONFIG	CLKIN_PD	1h
0x13	CONFIG	EN_PD	1h
0x13	CONFIG	TDIE_WARN_LEVEL	1h
0x13	CONFIG	EN_SPREAD_SPEC	1h
0x14	PLL_CTRL	EN_PLL	0h
0x14	PLL_CTRL	EXT_CLK_FREQ[4:0]	1h
0x15	PGOOD_CTRL_1	PGOOD_POL	0h

Table 4-1. Summary of Control Registers (continued)

Address	Register Name	Bit	LP873244-Q1 Value
0x15	PGOOD_CTRL_1	PGOOD_OD	1h
0x15	PGOOD_CTRL_1	PGOOD_WINDOW_LDO	1h
0x15	PGOOD_CTRL_1	PGOOD_WINDOW_BUCK	1h
0x15	PGOOD_CTRL_1	EN_PGOOD_LDO1	1h
0x15	PGOOD_CTRL_1	EN_PGOOD_LDO0	1h
0x15	PGOOD_CTRL_1	EN_PGOOD_BUCK1	1h
0x15	PGOOD_CTRL_1	EN_PGOOD_BUCK0	1h
0x16	PGOOD_CTRL_2	EN_PGOOD_TWARN	0h
0x16	PGOOD_CTRL_2	PG_FAULT_GATES_PGOOD	0h
0x16	PGOOD_CTRL_2	PGOOD_MODE	0h
0x20	TOP_MASK_1	PGOOD_INT_MASK	1h
0x20	TOP_MASK_1	SYNC_CLK_MASK	1h
0x20	TOP_MASK_1	TDIE_WARN_MASK	0h
0x20	TOP_MASK_1	I_MEAS_MASK	1h
0x21	TOP_MASK_2	RESET_REG_MASK	1h
0x22	BUCK_MASK	BUCK1_PGF_MASK	1h
0x22	BUCK_MASK	BUCK1_PGR_MASK	1h
0x22	BUCK_MASK	BUCK1_ILIM_MASK	1h
0x22	BUCK_MASK	BUCK0_PGF_MASK	1h
0x22	BUCK_MASK	BUCK0_PGR_MASK	1h
0x22	BUCK_MASK	BUCK0_ILIM_MASK	1h
0x23	LDO_MASK	LDO1_PGF_MASK	1h
0x23	LDO_MASK	LDO1_PGR_MASK	1h
0x23	LDO_MASK	LDO1_ILIM_MASK	1h
0x23	LDO_MASK	LDO0_PGF_MASK	1h
0x23	LDO_MASK	LDO0_PGR_MASK	1h
0x23	LDO_MASK	LDO0_ILIM_MASK	1h

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