# LP8555 High-Efficiency LED Backlight Driver for Tablet PCs

## 1 Features

- Dual High-Efficiency DC/DC Boost Converters
- 2.7-V to 20-V VDD Range
- 12 50-mA High-Precision LED Current Sinks With 12-Bit Brightness Control
- Adaptive LED Current Sink Headroom Controls for Maximum System Efficiency
- LED String Count Auto-Detection
- Phase-Shifted PWM Mode for Reduced Audible Noise
- PWM Input Duty-Cycle and/or I$^2$C-Register Brightness Control
- Hybrid PWM and Current Dimming for Higher LED Drive Optical Efficiency
- Flexible CABC Support
- EPROM, I$^2$C-Register, or External Resistors for Configuration
- Improved Boost EMI Performance with Slew-Rate Control, Spread Spectrum, and Phase-Shifted Switching
- Extensive Fault Detection Schemes

## 2 Applications

- Tablet LCD Display LED Backlight

## 3 Description

The LP8555 is a high efficiency LED driver with integrated dual DC-DC boost converters. It has 12 high-precision current sinks that can be controlled by a PWM input signal, an I$^2$C master, or both.

Dual-boost configuration of LP8555 shares the load to two inductors and allows thinner overall solution size and better efficiency compared to single-boost solutions. 12 LED strings allows driving high number of LEDs with optimal efficiency since boost conversion ratio can be kept low.

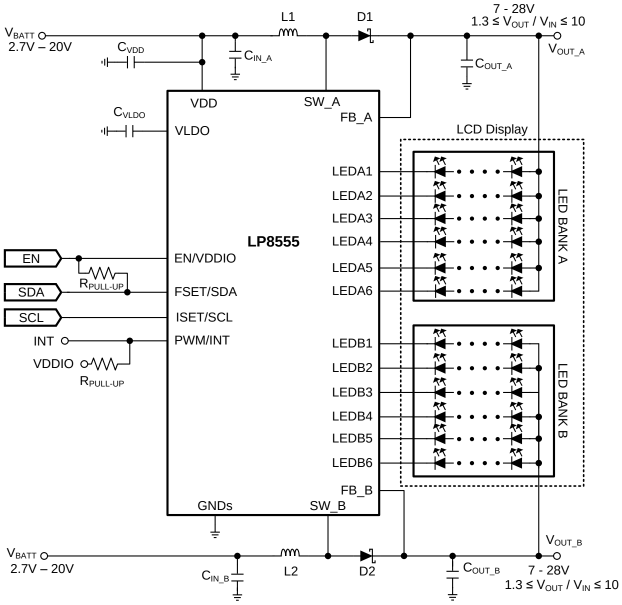
The boost converter has adaptive output voltage control based on the LED current sink headroom voltages. This feature minimizes the power consumption by adjusting the voltage to lowest sufficient level in all conditions.

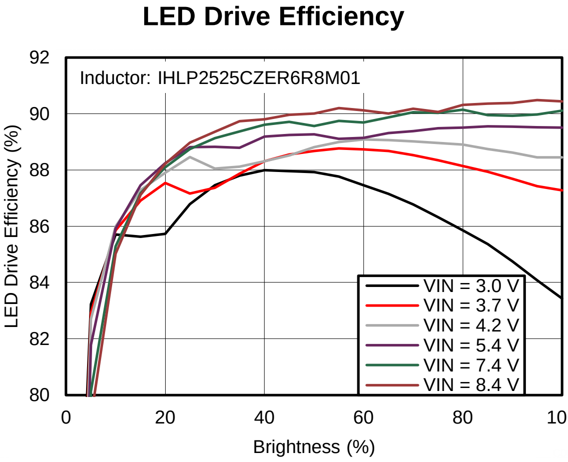
The LED string auto-detect function enables use of the same device in systems with 2 to 12 LED strings for the maximum design flexibility. Proprietary Hybrid PWM and Current dimming mode enables additional system power savings. Phase-shift PWM allows reduced audible noise and smaller boost output capacitors. Flexible CABC support combines brightness level selections based on the PWM input and I$^2$C commands.

**Device Information**

| ORDER NUMBER | PACKAGE | BODY SIZE |
|---|---|---|
| LP8555YFQR | DSBGA (36) | 2,478mm x 2,478mm |

## 4 Simplified Schematic





## Table of Contents

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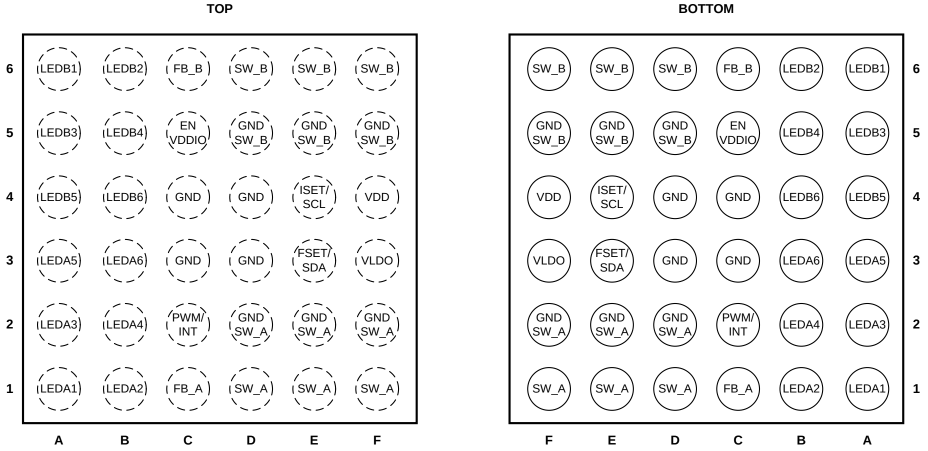
## 5 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| February 21, 2014 | * | Initial Release |

# 6 Terminal Configuration and Functions

**YFQ (DSBGA)**
**36 Bumps**



## Terminal Functions

| TERMINAL | | TYPE | DESCRIPTION |
|---|---|---|---|
| NUMBER | NAME | | |
| A1, A2, A3, B1, B2, B3, | LEDAx | A | LED Bank A Current Sink Terminal. If unused, this terminal may be left floating. |
| A4, A5, A6, B4, B5, B6 | LEDBx | A | LED Bank A Current Sink Terminal. If unused, this terminal may be left floating. |
| C1 | FB_A | A | Feedback terminal for the Bank A Boost Converter. |
| C2 | PWM/INT | I | Dual function terminal. When BRTMODE = 00, 10, or 11, this is a PWM input terminal. When BRTMODE = 01, this terminal is a programmable interrupt terminal. In this mode, this is an open drain output that pulls low when a fault condition occurs. |
| C3, C4, D3, D4 | GND | G | Ground for analog and digital blocks. These terminals should be connected to a noise-free GND plane if possible (separate plane than GND_SW_x terminals). |
| C5 | EN/VDDIO | I | Backlight Enable terminal and VDDIO power terminal + reference terminal for $I^2C$ communication. This terminal should be connected to IO voltage with low impedance route to avoid voltage ripple on this terminal. |
| C6 | FB_B | A | Feedback terminal for the Bank B Boost Converter. |
| D1, E1, F1 | SW_A | A | Bank A Boost Converter Switch |
| D2, E2, F2 | GND_SW_A | G | Bank A Boost Converter Switch Ground. These terminals can be connected to noisy GND due to high current spikes. |
| D5, E5, F5 | GND_SW_B | G | Bank B Boost Converter Switch Ground. These terminals can be connected to noisy GND due to high current spikes. |
| D6, E6, F6 | SW_B | A | Bank B Boost Converter Switch |
| E3 | FSET/SDA | I/O/A | Dual Function terminal. When $I^2C$ is not used (for example, BRTMODE = 00), this terminal can be used to set the boost switching frequency and/or LED PWM frequency by connecting a resistor between the terminal and a ground reference. When $I^2C$ is used (for example, BRTMODE = 01, 10, or 11), this terminal is connected to a SDA line of an $I^2C$ bus. |
| E4 | ISET/SCL | I/A | Dual Function terminal. When $I^2C$ is not used (for example, if BRTMODE=00), this terminal can be used to set the full-scale LED current by connecting a resistor between the terminal and a ground reference. When $I^2C$ is used (for example, BRTMODE = 01, 10, or 11), this terminal is connected to a SCL line of an $I^2C$ bus. |
| F3 | VLDO | P | Internal LDO Output terminal. $C_{VLDO}$ bypass capacitor must be connected between this terminal and ground. |
| F4 | VDD | P | Device power supply terminal. Provide 2.7-V to 20-V supply to this terminal. This terminal is an input of the internal LDO regulator. The output of the internal LDO powers the device blocks. |
| A: Analog, G: Ground Terminal, P: Power Terminal, I: Input Terminal, O: Output Terminal | | | |

# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VDD | Voltage on VDD | –0.3 | 22 | V |
| VLDO | Voltage on VLDO | –0.3 | 6 | |
| V(PWM/INT, EN/VDDIO/ FSET/SDA, ISET/SCL) | Voltage on logic terminals | | | |
| V(SW_A, SW_B, LEDxy, FB_x) | Voltage on analog terminals | –0.3 | 31 | |
| $P_D$ | Continuous Power Dissipation (2) | | Internally limited | |
| $T_A$ | Operating ambient temperature range (3) | –40 | 85 | °C |
| $T_J$ | Maximum operating junction temperature (3) | –40 | 125 | |
| $T_{soldering}$ | Note (4) | | | |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J$ = 150°C (typ.) and disengages at $T_J$ = 137°C (typ.).
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be degraded. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125ºC), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($\theta_{JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} - (\theta_{JA} \times P_{D\text{-}MAX})$.
(4) For detailed soldering specifications and information, please refer to Application Note AN1112.

## 7.2 Handling Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_{STORAGE}$ | Storage temp range | –65 | 150 | °C |
| $V_{HBM}$ | Human body model (HBM) voltage(1) | | 2000 | V |
| $V_{CDM}$ | Charged device model (CDM) (2) | | 250 | |

(1) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Terminals listed as 2 kV may actually have higher performance.
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Terminals listed as 250 V may actually have higher performance

## 7.3 Recommended Operating Conditions(1)(2)

Over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| VDD – Voltage on VDD | 2.7 | 20 | V |
| VLDO – Voltage on VLDO | 2.7 | 5.5 | |
| V (EN/VDDIO) – Supply voltage for digital I/O | 1.7 | 5.5 | |
| V (PWM/INT, FSET/SDA, ISET/SCL) – Voltage on logic terminals | 0 | 5.5 | |
| V (SW_A, SW_B, LEDxy, FB_x) | 0 | 28 | |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device a these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND terminals.

## 7.4 Thermal Information

Over operating free-air temperature range (unless otherwise noted)

| THERMAL METRIC(1) | | DSBGA (36 TERMINALS) | UNIT |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance ($\theta_{JA}$) (2) | 76.2 | °C/W |
| $\theta_{JC}$ | Junction-to-case (top) thermal resistance | 0.3 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 16.3 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 1.8 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 16.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

## 7.5 Electrical Characteristics(1)(2)

Limits apply over the full ambient temperature range –40°C ≤ $T_A$ ≤ 85°C. Unless otherwise specified: VDD = 3.6 V, EN/VDDIO = 1.8 V, L1 = L2 = 6.8 µH, $C_{IN\_A}$ = $C_{IN\_B}$ = 10 µF, $C_{OUT\_A}$ = $C_{OUT\_B}$ = 10 µF, $C_{VLDO}$ = 10 µF, $C_{VDD}$ = 1 µF.(3)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{IN}$ | Shutdown supply current | EN = L and PWM/INT = L | | | 1 | µA |
| | Standby supply current | EN = H and PWM/INT = L, ON bit = 0 | | 19 | 30 | |
| | Normal mode supply current | EN = H, ON bit = 1, no current going through LED outputs | | 4.2 | | mA |
| $f_{OSC}$ | Internal oscillator frequency accuracy | | -7% | | 7% | |
| $T_{TSD}$ | Thermal shutdown threshold | | | 150 | | °C |
| $T_{TSD\_hyst}$ | Thermal shutdown hysteresis | | | 13 | | |
| $t_{START-UP}$ | Start-up time(4) | | | 5 | 7 | ms |
| **BOOST CONVERTER (Applies for both boost converters)** | | | | | | |
| $V_{BST\_MIN}$ | Minimum output voltage | | | 7 | | V |
| $V_{BST\_MAX}$ | Maximum output voltage | VMAX = 00<br>VMAX = 01<br>VMAX = 10<br>VMAX = 11 | | 18<br>22<br>25<br>28 | | V |
| $I_{MAX}$ | SW FET current limit | | 2.7 | 3.1 | 3.5 | A |
| $R_{NMOS}$ | NMOS switch-ON resistance | $I_{SW}$ = 0.5 A | | 0.16 | | Ω |
| $I_{LOAD}$ | Continuous load current | VBATT = 3 V, VOUT = 26.6 V. Typical application. | | 180 | | mA |

(1) All voltages are with respect to the potential at the GND terminals.
(2) Min and Max limits are specified by design, test, or statistical analysis.
(3) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics
(4) Start-up time is measured from the moment the ON bit is set high to the moment when backlight is enabled.

## Electrical Characteristics(1)(2) (continued)

Limits apply over the full ambient temperature range –40°C ≤ $T_A$ ≤ 85°C. Unless otherwise specified: VDD = 3.6 V, EN/VDDIO = 1.8 V, L1 = L2 = 6.8 µH, $C_{IN\_A}$ = $C_{IN\_B}$ = 10 µF, $C_{OUT\_A}$ = $C_{OUT\_B}$ = 10 µF, $C_{VLDO}$ = 10 µF, $C_{VDD}$ = 1 µF.(3)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SW}$ | Switching frequency | BFREQ = 0<br>BFREQ = 1 | | 500<br>1000 | | kHz |
| $f_{SW\_ACCURACY}$ | Boost oscillator accuracy | | –7% | | 7% | |
| $V_{OVP\_THR}$ | Overvoltage protection voltage threshold | | | $V_{BST\_MAX}$ +1.6 V | | V |
| $V_{OUT}/V_{IN}$ | Conversion ratio | No load, BFREQ = 1 | 1.3 | | 10 | |
| $\Delta V_{SW}/t_{off\text{-}on}$ | SW node voltage slew rate during OFF-to-ON transition | Load current 120 mA. Boost slew rate set to fastest (SRON = 00b). | | 12.5 | | V/ns |
| $\Delta V_{SW}/t_{on\text{-}off}$ | SW node voltage slew rate during ON-to-OFF transition | | | 19.5 | | |
| $f_{MOD}$ | Modulation frequency (percentage of the SW frequency) | FMOD_DIV = 00<br>FMOD_DIV = 01<br>FMOD_DIV = 10<br>FMOD_DIV = 11 | | 0.47%<br>0.27%<br>0.17%<br>0.12% | | |
| **CURRENT SINKS** | | | | | | |
| $I_{LEAKAGE}$ | Leakage current | Outputs LEDA1...LEDB6, $V_{LEDxx}$ = 28 V | | | 1 | µA |
| $I_{MAX}$ | Maximum sink current LEDA1...B6 | | | 50 | | mA |
| $I_{OUT}$ | Output current accuracy(5) | Output current set to 23 mA. Current scale set to 23 mA. PWM = 100% | –4% | | 4% | |
| $I_{MATCH}$ | Matching (5) | | | 1% | 5% | |
| $f_{LED\_PWM}$ | LED switching frequency | PFREQ = 000b<br>PFREQ = 111b | | 4.9<br>39.1 | | kHz |
| $V_{SAT}$ | Saturation voltage (6) | Output current set to 23 mA | | 200 | 260 | mV |
| | | Output current set to 30 mA | | 250 | 340 | |
| **PWM INTERFACE CHARACTERISTICS** | | | | | | |
| $f_{PWM}$ | PWM input frequency | | 75 | | 50000 | Hz |
| $t_{MIN\_ON}$ | Minimum pulse ON time | | | 100 | | ns |
| $t_{MIN\_OFF}$ | Minimum pulse OFF time | | | 100 | | |
| $t_{start\text{-}up}$ | Turn-on delay from standby to backlight on | PWM input active, ON bit written high | | | 7 | ms |
| $t_{STBY}$ | Turn-off delay | PWM input low time before entering standby mode (if PWMSB = 1) | | 52 | | ms |
| $PWM_{RES}$ | PWM input resolution | $f_{IN}$ < 2.4 kHz<br>$f_{IN}$ < 4.8 kHz<br>$f_{IN}$ < 9.6 kHz<br>$f_{IN}$ < 19.5 kHz<br>$f_{IN}$ < 25 kHz<br>$f_{IN}$ < 50 kHz | | 12<br>12<br>11<br>10<br>9<br>8 | | bits |
| **UNDERVOLTAGE PROTECTION** | | | | | | |
| $V_{UVLO}$ | VDD UVLO threshold voltage | VDD falling | | 2.5 | | V |
| | | VDD rising | | 2.6 | | |
| **LOGIC INTERFACE** | | | | | | |
| Logic Input EN/VDDIO | | | | | | |
| $V_{EN/VDDIO}$ | Supply voltage range | | 1.7 | | 5.5 | V |
| $I_I$ | Input current | | | 20 | | µA |

(5) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUTA1 to OUTB6), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Matching number is calculated: (MAX-MIN)/AVG. The typical specification provided is the most likely norm of the matching figure for all parts. LED current sinks were characterized with 1 V headroom voltage. Note that some manufacturers have different definitions in use.

(6) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1 V.

## Electrical Characteristics[1][2] (continued)

Limits apply over the full ambient temperature range –40°C ≤ $T_A$ ≤ 85°C. Unless otherwise specified: VDD = 3.6 V, EN/VDDIO = 1.8 V, L1 = L2 = 6.8 µH, $C_{IN\_A}$ = $C_{IN\_B}$ = 10 µF, $C_{OUT\_A}$ = $C_{OUT\_B}$ = 10 µF, $C_{VLDO}$ = 10 µF, $C_{VDD}$ = 1 µF.[3]

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Logic Input PWM/INT, FSET/SDA, ISET/SCL | | | | | | |
| $V_{IL}$ | Input low level | | | | 0.3 x EN/VDDIO | V |
| $V_{IH}$ | Input high level | | 0.7 x EN/VDDIO | | | V |
| $I_I$ | Input current, VIO = 1.7 V to 5.5 V | | -1.0 | | 1.0 | µA |
| Logic Output FSET/SDA, PWM/INT | | | | | | |
| $V_{OL}$ | Output low level | $I_{PULL\text{-}UP}$ = 3 mA | | 0.3 | 0.4 | V |

## 7.6 I²C Serial Bus Timing Parameters (FSET/SDA, ISET/SCL)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency | | | 400 | kHz |
| 1 | Hold Time (repeated) START Condition | 0.6 | | | µs |
| 2 | Clock Low Time | 1.3 | | | µs |
| 3 | Clock High Time | 600 | | | ns |
| 4 | Setup Time for a Repeated START Condition | 600 | | | ns |
| 5 | Data Hold Time | 50 | | | ns |
| 6 | Data Setup Time | 100 | | | ns |
| 7 | Rise Time of SDA and SCL | 20+0.1x$C_b$ | | 300 | ns |
| 8 | Fall Time of SDA and SCL | 15+0.1x$C_b$ | | 300 | ns |
| 9 | Set-up Time for STOP condition | 600 | | | ns |
| 10 | Bus Free Time between a STOP and a START Condition | 1.3 | | | µs |
| $C_b$ | Capacitive Load Parameter for Each Bus Line.<br>Load of One Picofarad Corresponds to One Nanosecond. | 10 | | 200 | ns |
| $t_{response}$ | Delay from EN/VDDIO rising to I²C bus active | | | 1 | ms |

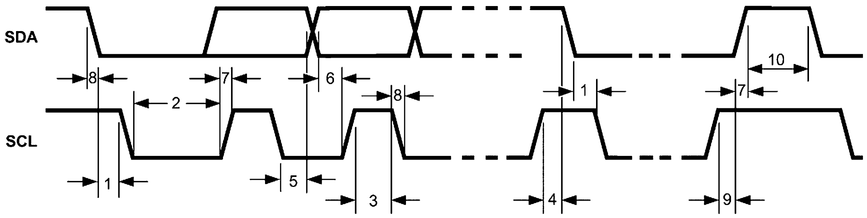


Figure 1. I²C Timing Parameters

## 7.7 Typical Characteristics

Measured at room temperature unless otherwise noted. Maximum LED current set to 23 mA per string. DC-DC Efficiency is defined as $P_{OUT}/P_{IN}$, where $P_{OUT}$ is total output power measured from boost output(s). LED Drive Efficiency is defined as $P_{LED}/P_{IN}$ , where $P_{LED}$ is actual power consumed in LEDs.

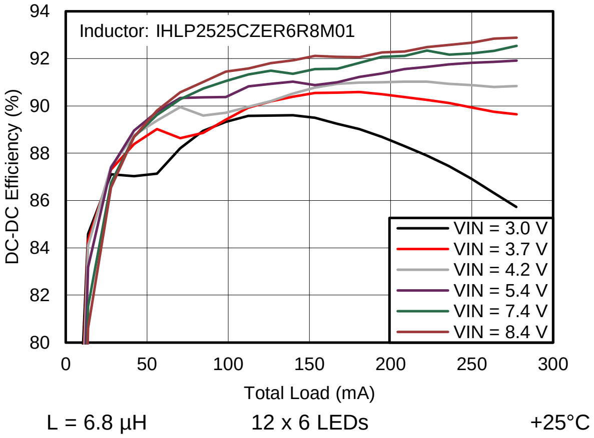


**Figure 2. Boost Efficiency**

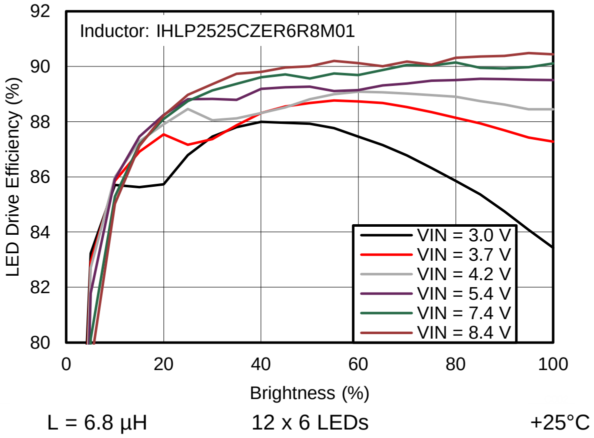


**Figure 3. LED Drive Efficiency**

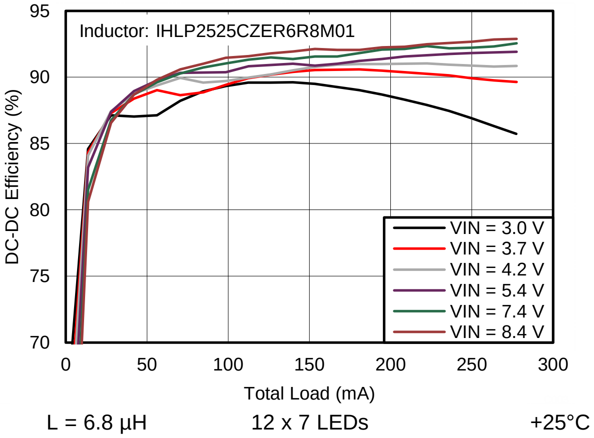


**Figure 4. Boost Efficiency**

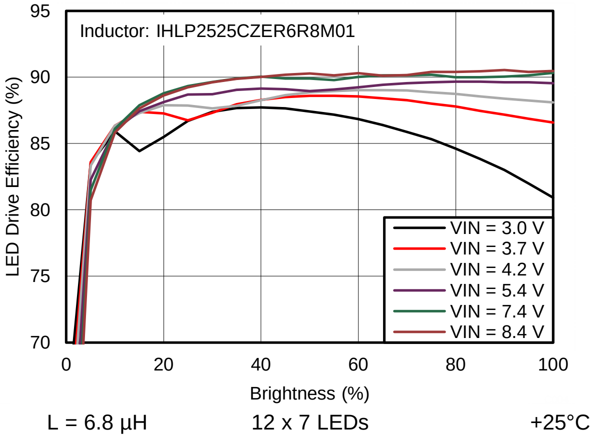


**Figure 5. LED Drive Efficiency**

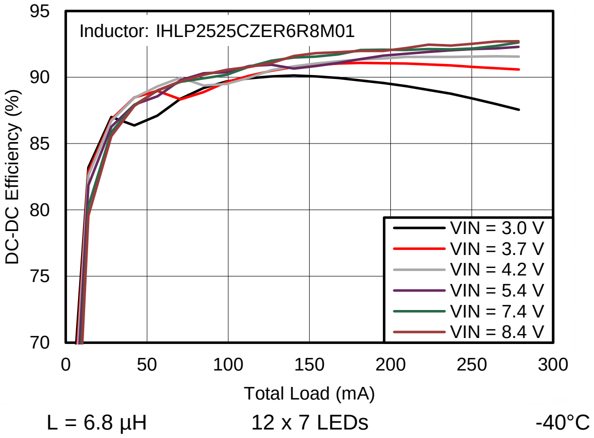


**Figure 6. Boost Efficiency**

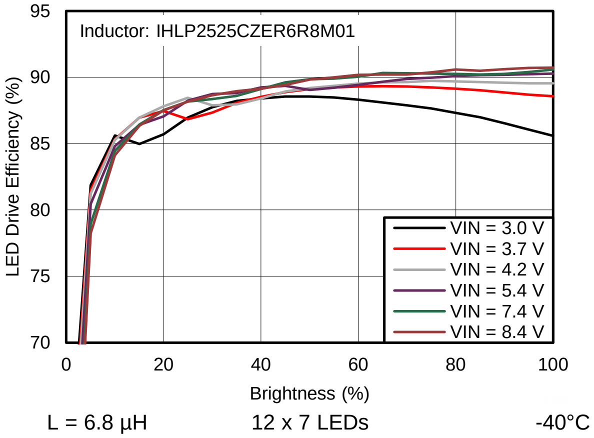
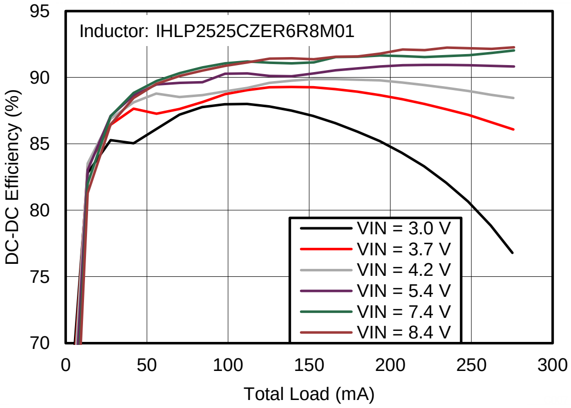


**Figure 7. LED Drive Efficiency**

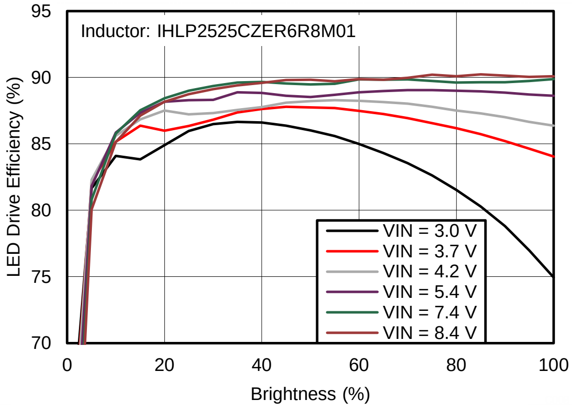
## Typical Characteristics (continued)

Measured at room temperature unless otherwise noted. Maximum LED current set to 23 mA per string. DC-DC Efficiency is defined as $P_{OUT}/P_{IN}$, where $P_{OUT}$ is total output power measured from boost output(s). LED Drive Efficiency is defined as $P_{LED}/P_{IN}$ , where $P_{LED}$ is actual power consumed in LEDs.



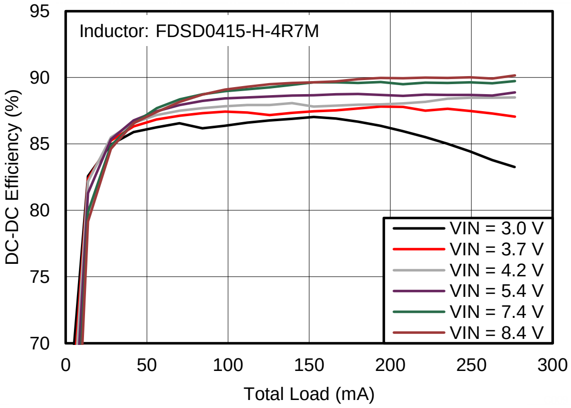
L = 6.8 µH 12 x 7 LEDs +85°C

**Figure 8. Boost Efficiency**



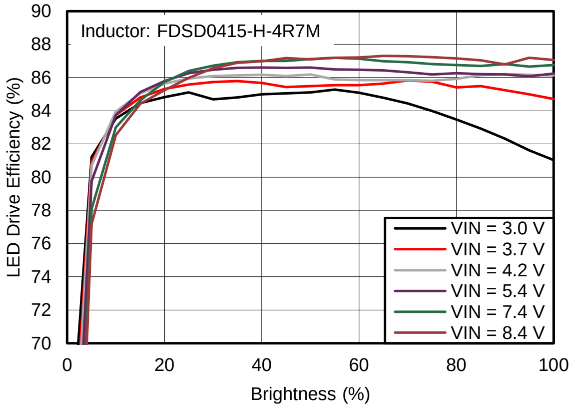
L = 6.8 µH 12 x 7 LEDs +85°C

**Figure 9. LED Drive Efficiency**



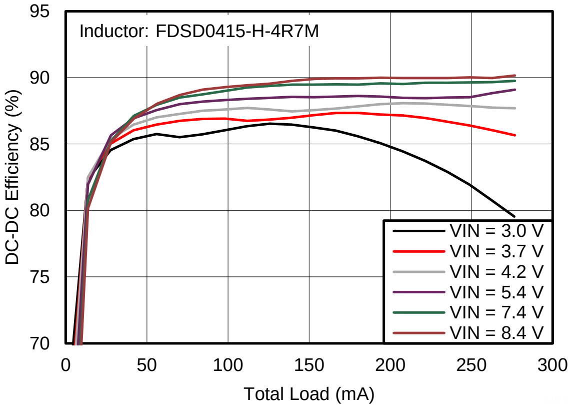
L = 4.7 µH 12 x 6 LEDs +25°C

**Figure 10. Boost Efficiency**



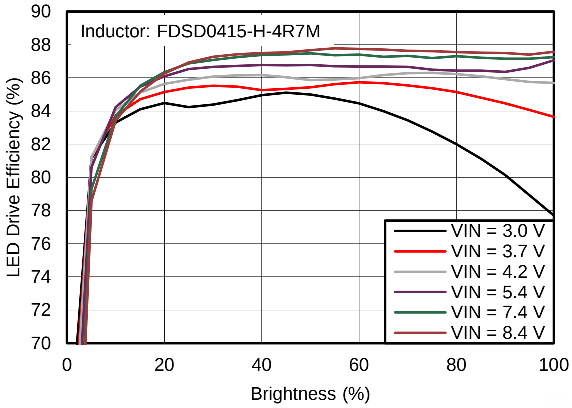
L = 4.7 µH 12 x 6 LEDs +25°C

**Figure 11. LED Drive Efficiency**



L = 4.7 µH 12 x 7 LEDs +25°C

**Figure 12. Boost Efficiency**



L = 4.7 µH 12 x 7 LEDs +25°C

**Figure 13. LED Drive Efficiency**

## Typical Characteristics (continued)

Measured at room temperature unless otherwise noted. Maximum LED current set to 23 mA per string. DC-DC Efficiency is defined as $P_{OUT}/P_{IN}$, where $P_{OUT}$ is total output power measured from boost output(s). LED Drive Efficiency is defined as $P_{LED}/P_{IN}$ , where $P_{LED}$ is actual power consumed in LEDs.

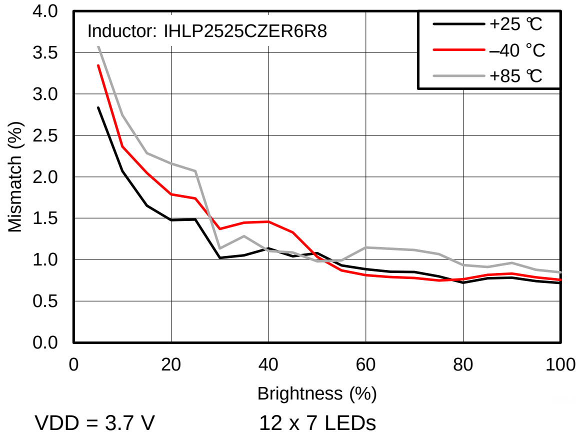


Figure 14. LED Current Mismatch

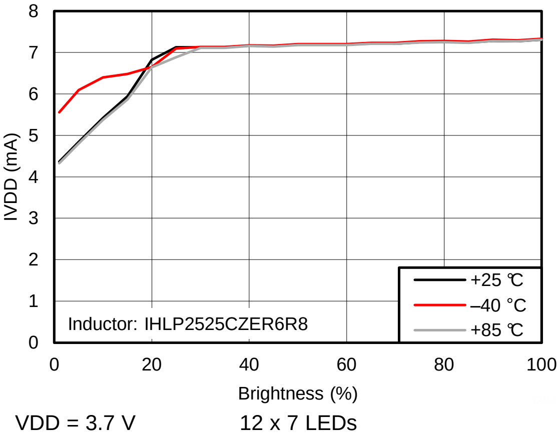


Figure 15. VDD Current vs. Load

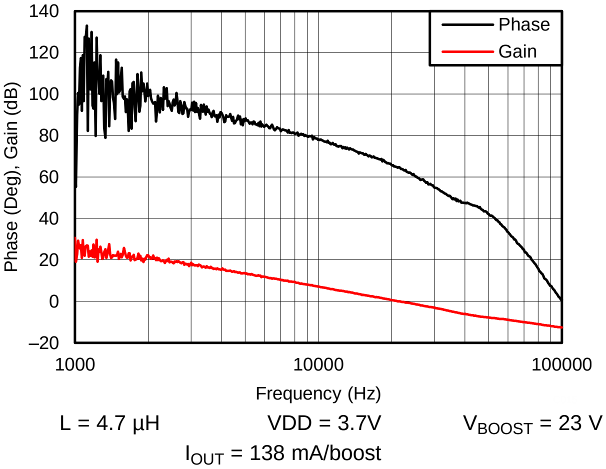


Figure 16. Typical Boost Converter Gain and Phase Plot

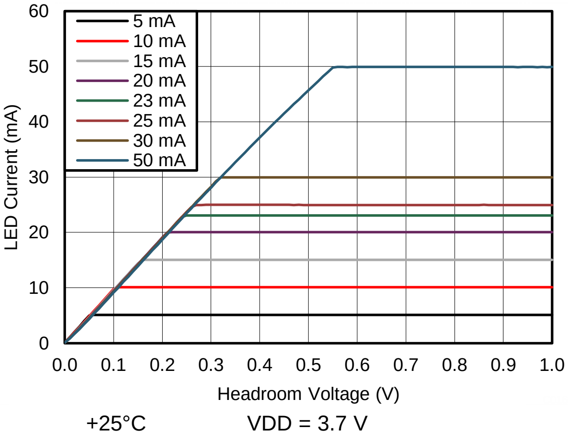


Figure 17. LED Current Vs. Headroom Voltage

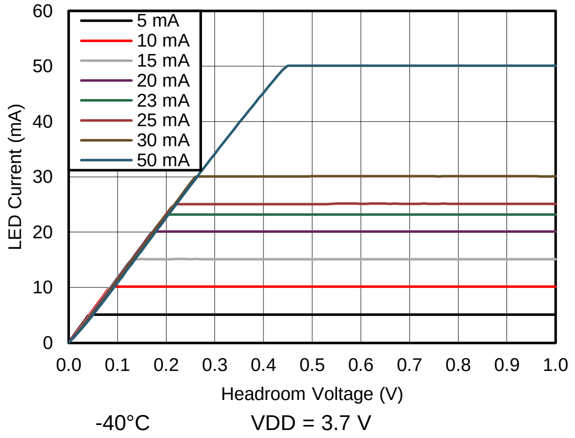


Figure 18. LED Current Vs. Headroom Voltage

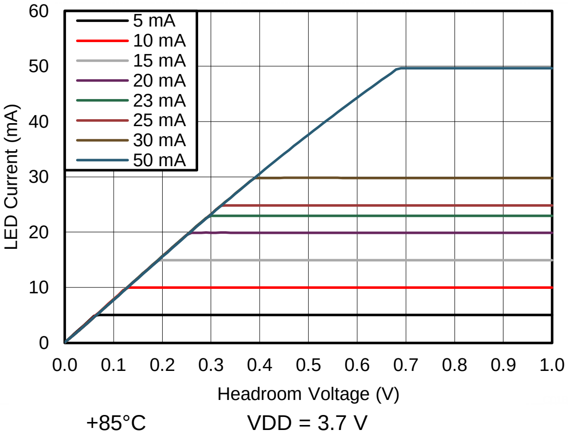


Figure 19. LED Current Vs. Headroom Voltage

# 8 Detailed Description

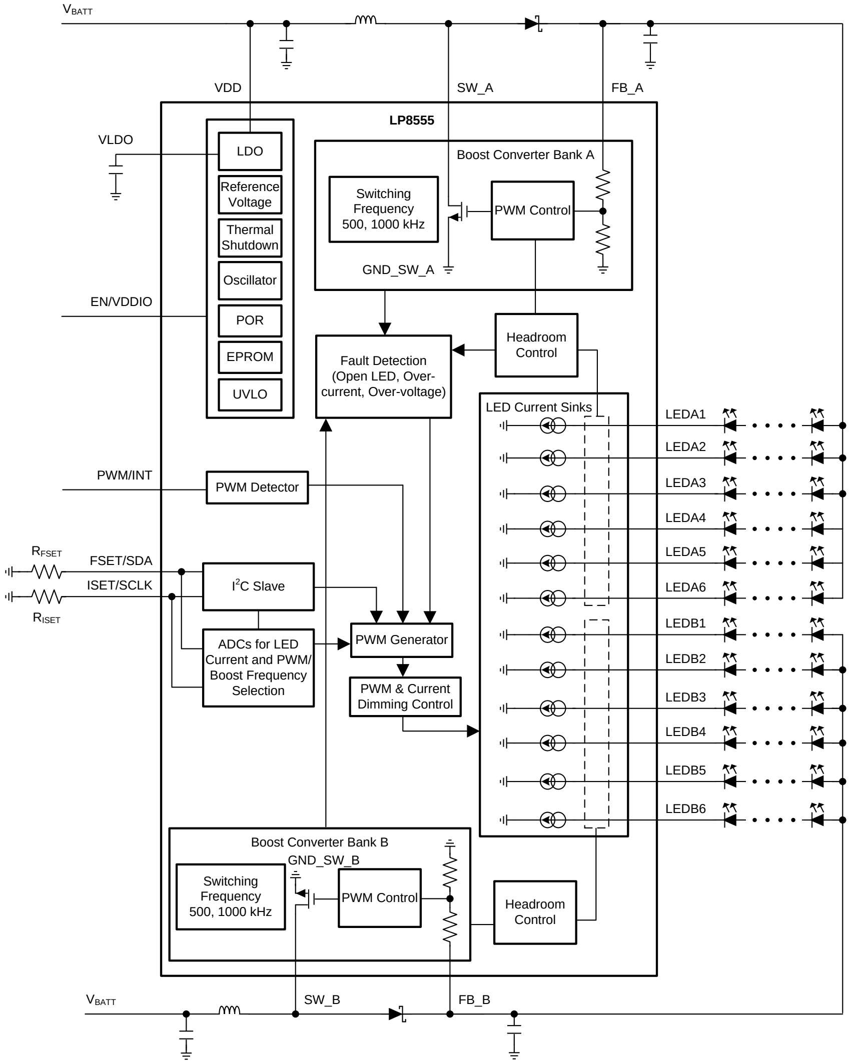
## 8.1 Overview

The LP8555 is a white LED driver featuring an asynchronous boost converter and 12 high-precision current sinks that can be controlled by a PWM input signal, an $I^2C$ master, or both. The boost converter uses adaptive output voltage control for setting the optimal LED driver voltages as high as 28 V. This feature minimizes the power consumption by adjusting the voltage to the lowest sufficient level under all conditions. The converter can operate at two switching frequencies: 500 and 1000 kHz pre-configured via EPROM.

Proprietary Hybrid PWM and Current Dimming mode allows higher system power saving. In addition, phase-shifted LED PWM dimming allows reduced audible noise and smaller boost output capacitors.

The LP8555 has a full set of safety features that ensure robust operation of the device and external components. The set consists of input undervoltage lockout, thermal shutdown, overcurrent protection, four levels of overvoltage protection, and LED open and short detection.

## 8.2 Functional Block Diagram



## 8.3 Features Description

### 8.3.1 Boost Converter Overview

#### *8.3.1.1 Operation*

The boost DC/DC converters generate 7-V to 28-V boost output voltage from a 2.7-V to 20-V boost input voltage (input voltage must be lower than $V_{BOOST}$). The maximum boost output voltage can be set digitally by pre-configuring EPROM memory (VMAX field).

The converter is a magnetic switching PWM mode DC/DC boost converter with a current limit. It uses CPM (current programmed mode) control, where the inductor current is measured and controlled with the feedback. During start-up, the soft-start function reduces the peak inductor current. Figure 20 shows the boost block diagram.

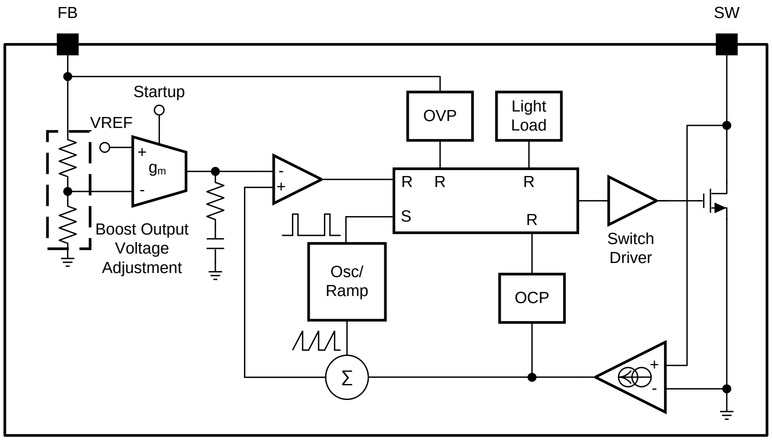


**Figure 20. Boost Converter Functional Block Diagram**

Both boost converters are operating at 180° phase shift to reduce current spikes from the input rail and EMI.

#### *8.3.1.2 Protection*

Three different protection schemes are implemented:

1. Overvoltage protection, limits the maximum output voltage:
   - Overvoltage protection limit changes dynamically based on output voltage setting. If the boost voltage is over 1.6 V higher than the adaptive control set value, the boost will stop switching.
   - Keeps the output below breakdown voltage. The output voltage control limits the boost maximum voltage to 18...28 V (EPROM programmable).
   - Prevents boost operation if battery voltage is much higher than desired output.
2. Overcurrent protection, limits the maximum inductor current to 3.1 A (EPROM programmable).
3. Duty cycle limiting.

#### *8.3.1.3 Setting Boost Switching Frequency*

The LP8555 boost converter switching frequency can be set by pre-configuring EPROM memory with the choice of boost frequency (BFREQ field). Table 1 summarizes setting of the switching frequency.

**Table 1. Setting Boost Switching Frequency**

| BFREQ | $f_{SW}$ [kHz] |
|---|---|
| 0 | 500 |
| 1 | 1000 |

### 8.3.1.4 Adaptive Boost Output Voltage Control

The boost converters operate in adaptive voltage control mode in typical application. The voltages at the LED terminals is monitored by the control loop. It raises the boost voltage when the measured voltage of ANY of the LED strings in a bank falls below the voltage threshold of its corresponding LOW comparator. If the headrooms of ALL of the LED strings in a bank are above the voltage threshold of their corresponding MID comparator, then the boost voltage is lowered. Both banks have independent boost voltage control to save power in case of Vf mismatch between LED strings.

The initial boost voltage is configured with the VINIT field. The VMAX field sets the maximum boost voltage. When an LED terminal is open, the monitored voltage will never have enough headroom and the adaptive mode control loop will keep raising the boost voltage. The VMAX field allows the boost voltage to be limited to stay under the voltage rating of the external components.

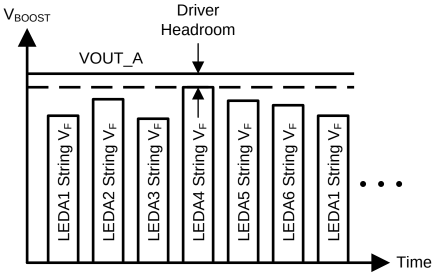


**Figure 21. Boost Adaptive Control Principle for Bank A Boost Converter With Phase Shifted Outputs**

### 8.3.1.5 EMI Reduction

The LP8555 features three EMI reduction schemes.

First scheme, Programmable Slew Rate Control, uses a combination of four drivers for boost switch. Enabling all four drivers allows boost switch on/off transition times to be the shortest. On the other hand, enabling just one driver allows boost switch on/off transition times to be the longest. The longer the transition times, the lower the switching noise on the SW node. It should also be noted that the shortest transition times bring the best efficiency as the switching losses are the lowest. Same controls effect both boost converters.

The second EMI reduction scheme is the Spread Spectrum Scheme which deliberately spreads the frequency content of the boost switching waveform, which inherently has a narrow bandwidth, makes the switching waveform's noise spectrum bandwidth wider and ultimately reduces its EMI spectral density.

The third feature for reducing EMI is Phase Shifted Clocking mode, where boost converters' clocks are operating 180° phase shifted. This prevents boost switches switching on at the same time when operating in PWM mode. This reduces input rail load transient spikes caused by boost inductor current and gate driver currents.

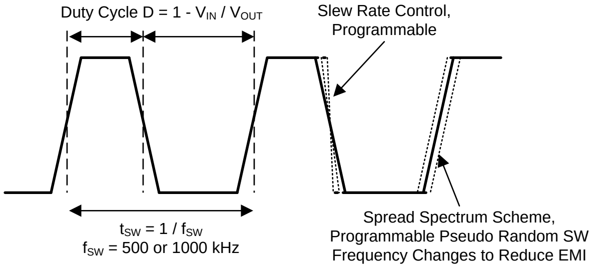


**Figure 22. Boost Converter EMI Reduction Schemes**

### 8.3.2 Brightness Control

The brightness can be controlled using an external PWM signal or the Brightness registers accessible via an $I^2C$ interface, or both. Which of these two input sources are selected is set by the BRTMODE EPROM bits. How the brightness is controlled in each of the four possible modes is described in the following sections.

#### *8.3.2.1 PWM Input Duty Measurement*

When using PWM input for brightness control the input PWM duty cycle is measured as described in following diagram and the brightness is controlled based on the result. When changing the brightness it must be noted that the measurement cycle is from rising edge to next rising edge and brightness change must be done accordingly (time from rising to rising edge is constant (=cycle time) and falling edge defines the brightness).

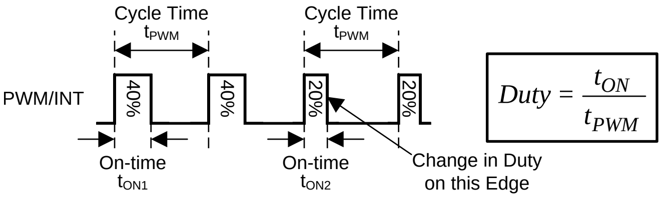


**Figure 23. PWM Input Duty Cycle Measurement**

#### *8.3.2.2 BRTMODE = 00*

With BRTMODE = 00, the LED output current is controlled by the PWM input duty cycle. The PWM detector block measures the duty cycle at the PWM/INT terminal and uses it to generate a PWM-based brightness code. Before the output is generated, the code goes through the curve Shaper block. Then the code goes into the Hybrid PWM and Current Dimming block which determines the range of the PWM and Current control. The outcome of the Hybrid PWM and Current Dimming block is Current and/or up to 6 PWM output signals.

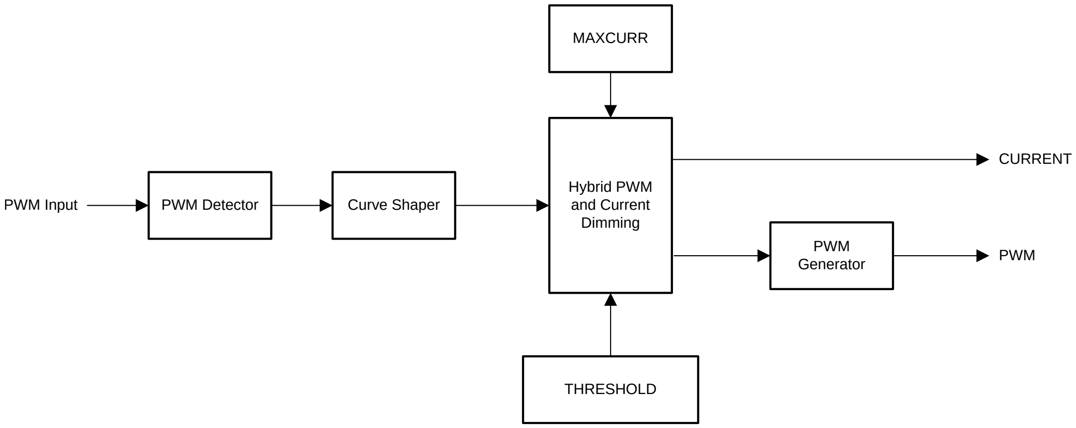


**Figure 24. BRTMODE = 00 Brightness Control**

#### 8.3.2.3 BRTMODE = 01

With BRTMODE = 01, the LED output current is controlled by the BRTHI/BRTLO registers. Before the output is generated the BRTHI/BRTLO registers-based brightness code goes through the Curve Shaper block. Then the code goes into the Hybrid PWM and Current Dimming block which determines the range of the PWM and Current control. The outcome of the Hybrid PWM and Current Dimming block is Current and/or up to 6 PWM output signals.

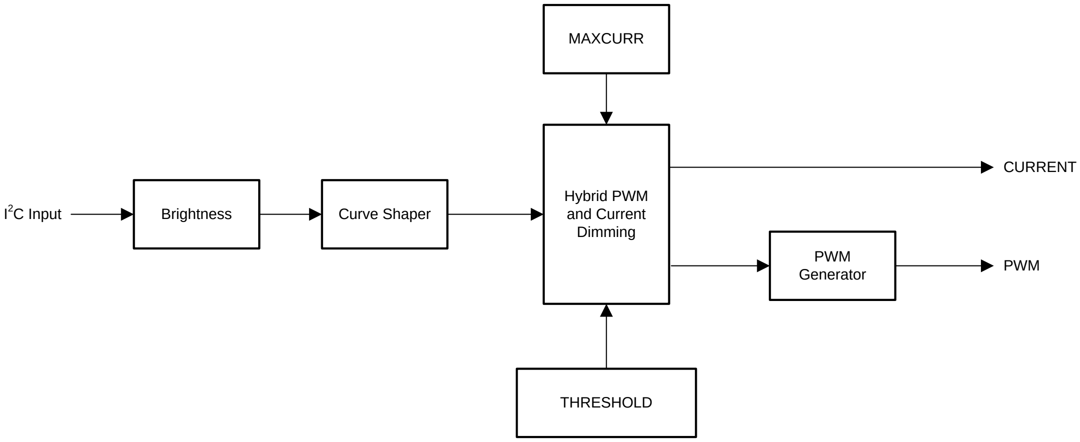


Figure 25. BRTMODE = 01 Brightness Control

#### 8.3.2.4 BRTMODE = 10

With BRTMODE = 10, the LED output current is controlled by PWM input duty cycle and the BRTHI/BRTLO registers. The PWM detector block measures the duty cycle at the PWM/INT terminal and uses it to generate PWM-based brightness code. Before the code is multiplied with the BRTHI/BRTLO registers-based brightness code, it goes through the Curve Shaper block. After the multiplication, the resulting code goes into the Hybrid PWM and Current Dimming block which determines the range of the PWM and Current control. The outcome of the Hybrid PWM and Current Dimming block is Current and/or up to 6 PWM output signals.

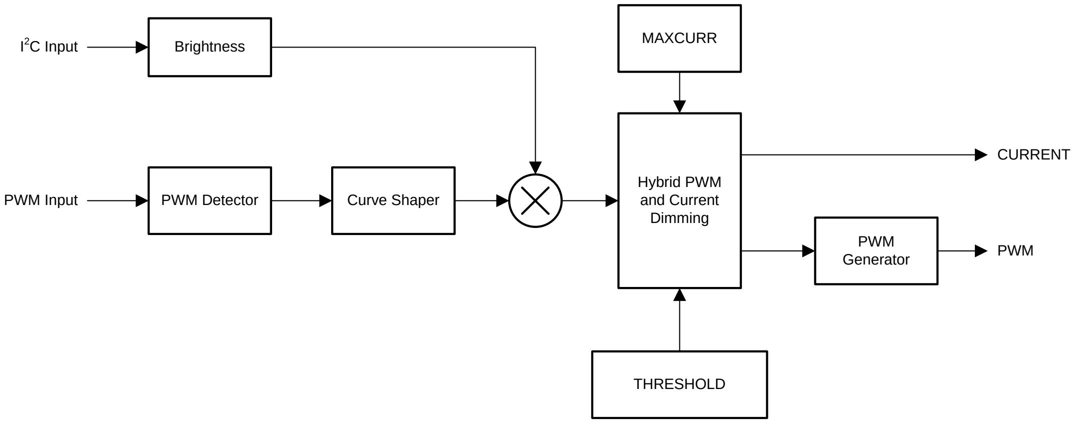


Figure 26. BRTMODE = 10 Brightness Control

### 8.3.2.5 BRTMODE = 11

With BRTMODE = 11, the LED output current is controlled by the PWM input duty cycle and the BRTHI/BRTLO registers. The PWM detector block measures the duty cycle at the PWM/INT terminal and uses it to generate PWM-based brightness code. In this mode, the BRTHI/BRTLO registers-based brightness code goes through the Curve Shaper block before it is multiplied with the PWM input duty cycle-based brightness code. After the multiplication, the resulting code goes into the Hybrid PWM and Current Dimming block which determines the range of the PWM and Current control. The outcome of the Hybrid PWM and Current dimming block is Current and/or up to 6 PWM output signals.

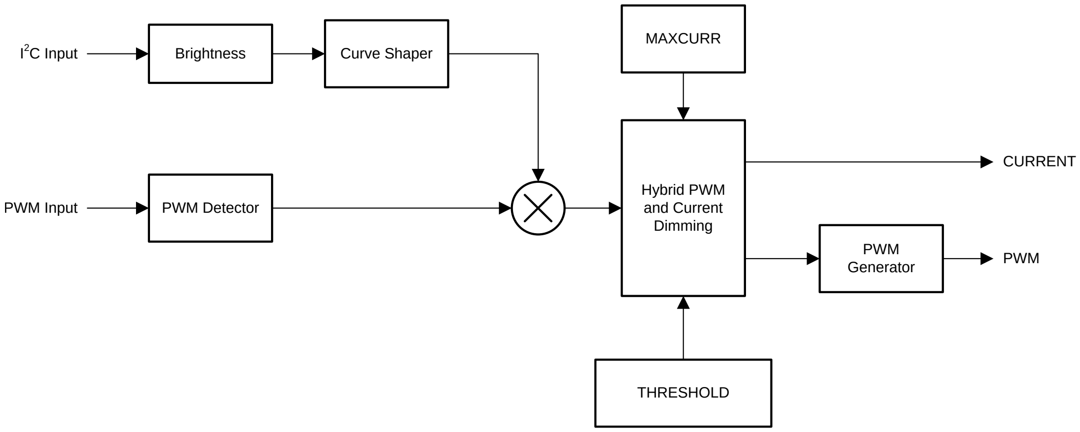


Figure 27. BRTMODE = 11 Brightness Control

#### *8.3.2.6 Hybrid PWM and Current Dimming Control*

Hybrid PWM and Current Dimming control combines PWM dimming and LED current-dimming control methods. With this dimming control, it is possible to achieve better optical efficiency from the LEDs compared to pure PWM control while still achieving smooth and accurate control and low brightness levels. The switch point from current-to-PWM control is set with THRESHOLD EPROM field, available settings are Pure PWM dimming (THRESHOLD = 111b), 25% switch point (THRESHOLD = 101b) and Pure Current Dimming (THRESHOLD = 000b). 25% setting allows good compromise between good matching of the LEDs brightness/white point at low brightness and good optical efficiency.

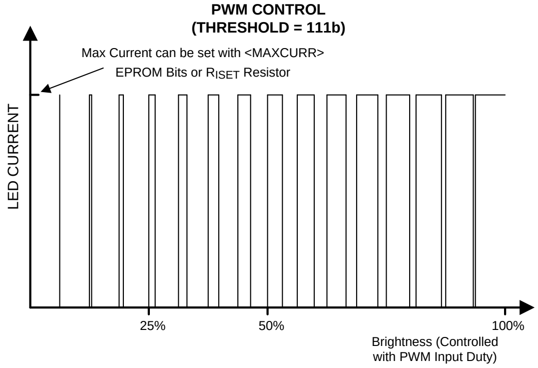


**Figure 28.**

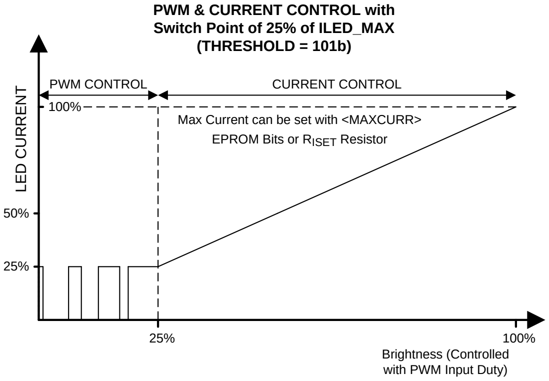


**Figure 29.**

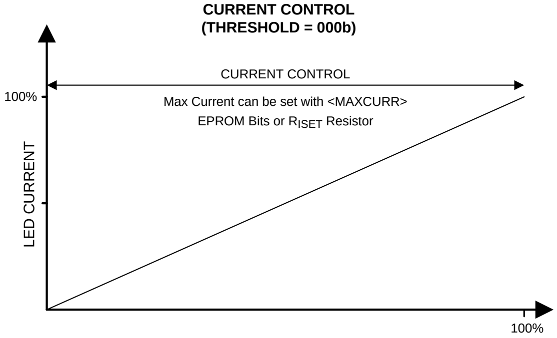


**Figure 30.**

### *8.3.2.7 Setting PWM Dimming Frequency*

The LP8555 LED PWM dimming frequency can be set either by an external resistor (PFSET = 1 selection), $R_{FSET}$, or by pre-configuring EPROM memory with the choice of PWM dimming frequency (PFREQ field). Table 2 summarizes setting of the PWM dimming frequency. Setting the PWM dimming frequency using an external resistor is separately shown in Table 3.

**Table 2. Setting PWM Dimming Frequency**

| PFSET | $R_{FSET}$ | PFREQ | $f_{PWM}$ [kHz] |
|---|---|---|---|
| 1 | See Table 3 | Don't Care | See Table 3 |
| 0 | Don't Care | 000 | 4.9 |
| 0 | Don't Care | 001 | 9.8 |
| 0 | Don't Care | 011 | 19.5 |
| 0 | Don't Care | 111 | 39.1 |

**Table 3. Setting PWM Dimming Frequency With an External Resistor**

| PFSET | $R_{FSET}$ [Ω] (Tolerance) | $f_{PWM}$ [kHz] |
|---|---|---|
| 1 | 63.4k (±1%) | 4.9 |
| 1 | 52.3k, 53.6k (±1%) | 9.8 |
| 1 | 39.2k (±1%) | 19.5 |
| 1 | 23.2k (±1%) | 39.1 |
| 1 | Grounded or floating | 19.5 |

### 8.3.2.8 Setting Full-Scale LED Current

The LP8555 full-scale LED current can be set either by an external resistor $R_{ISET}$ (ISET = 1 selection), or by pre-configuring EPROM memory with the choice of full-scale LED current (MAXCURR field, ISET = 0). This register can be also written with $I^2C$ before turning on backlight. Table 4 summarizes setting of the full-scale LED current.

**Table 4. Setting Full-Scale LED Current**

| ISET | $R_{ISET}$ [Ω] (Tolerance) | MAXCURR | ILED [mA] |
|---|---|---|---|
| 1 | Floating | Don't Care | 23 |
| 1 | 63.4k (±1%) | Don't Care | 5 |
| 1 | 52.3k, 53.6k (±1%) | Don't Care | 10 |
| 1 | 44.2k, 45.3k (±1%) | Don't Care | 15 |
| 1 | 39.2k (±1%) | Don't Care | 20 |
| 1 | 34.0k (±1%) | Don't Care | 23 |
| 1 | 30.1k (±1%) | Don't Care | 25 |
| 1 | 26.1k (±1%) | Don't Care | 30 |
| 1 | 23.2k (±1%) | Don't Care | 50 |
| 1 | 0 (grounded) | Don't Care | 23 |
| 0 | Don't Care | 000 | 5 |
| 0 | Don't Care | 001 | 10 |
| 0 | Don't Care | 010 | 15 |
| 0 | Don't Care | 011 | 20 |
| 0 | Don't Care | 100 | 23 |
| 0 | Don't Care | 101 | 25 |
| 0 | Don't Care | 110 | 30 |
| 0 | Don't Care | 111 | 50 |

#### *8.3.2.9 Phase-Shift PWM Scheme*

The Phase-Shift PWM Scheme (PSPWM) allows delaying of the time when each LED current sink is active. When the LED current sinks are not activated simultaneously, the peak load current from the boost output is greatly decreased during PWM dimming. This reduces the ripple seen on the boost output and allows smaller output capacitors to be used. Reduced ripple also reduces the output ceramic capacitor audible ringing. The PSPWM scheme also increases the load frequency seen on the boost output by up to six times and therefore transfers the possible audible noise to the frequencies outside of the audible range.

The phase difference between each active driver is automatically determined and is 360º / number of active drivers in a bank.

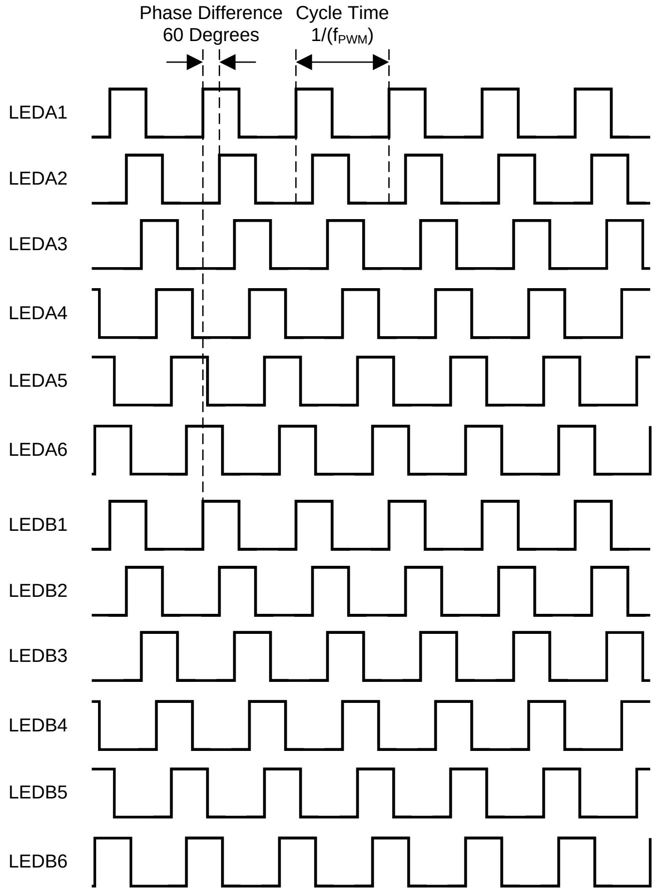


**Figure 31. Phase Shifting Example With All 12 Channels Active. (Note: Bank A And Bank B are in the Same Phase.)**

### 8.3.3 LED Brightness Slopes, Normal and Advanced

The transition time between two brightness values can be programmed with the STEP EPROM field from 0 to 200 ms. The same slope time is used for sloping up and down. With advanced slope the brightness changes can be made more pleasing to the human eye. It is implemented with a digital smoothing filter. The filter strength is set with SMOOTH EPROM field.

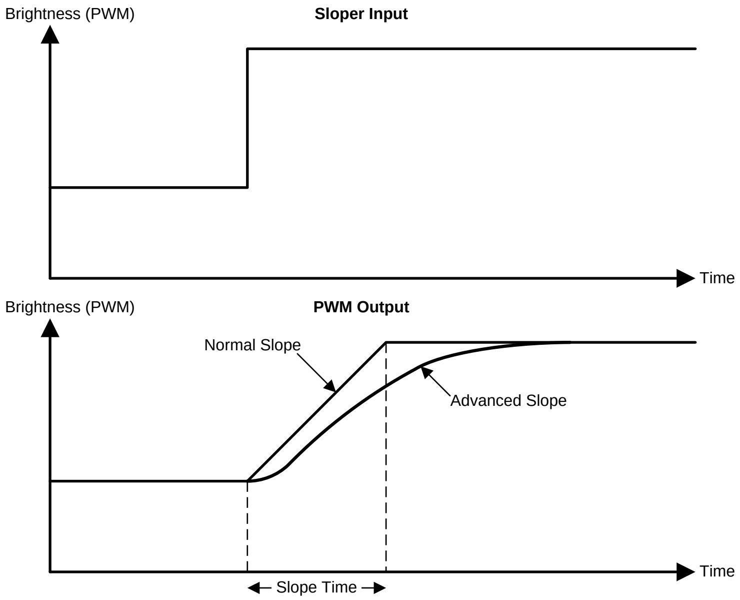


Figure 32. Sloping Principle

### 8.3.4 Start-up and Shutdown Sequences

Depending on brightness control mode the LP8555 can be started up or shut down differently. Below are explained typical start-up/shutdown sequences with corresponding timings for operation states. Diagrams have more details and illustrated waveforms for typical usage cases.

#### *8.3.4.1 Start-up With PWM Input Brightness Control Mode (BRTMODE = 00b)*

When VDD and EN/VDDIO are above min operational value the LP8555 enters start-up mode. During start-up mode the LDO is started, and EPROM values are read. $I^2C$ is available after the start-up sequence has ended.

In standby mode the device waits for the ON bit to go high to start the boost start-up sequence. In standby mode PWM input duty cycle measurement is active.

Once the ON bit is set to 1 (it can be also programmed to 1 by default in EPROM, and no $I^2C$ write is then needed for entering active mode), boost is started, and device enters active mode with brightness set by PWM input duty cycle. If no brightness is set, the backlight stays off until two PWM pulses are received in the PWM input, or if PWM input is set high for more than 1/75 Hz time. Boost starts initially to the level programmed in EPROM, and after backlight is turned on the adaptive control adjusts the voltage to get to the minimal headroom voltage.

#### *8.3.4.2 Shutdown With PWM Input Brightness Control Mode (BRTMODE = 00b)*

The backlight can be turned off by setting PWM input low or by writing the ON bit low. After a 1/75Hz timeout period in the PWM input, the backlight slopes down (if slope is enabled), and boost is returned to the initial voltage level programmed to the EPROM. If the backlight is shut down with the ON bit, it shuts down immediately even if slopes are enabled and boost turns off as well. To enter standby mode where boost is disabled and the power consumption is minimal, the ON bit must be written to 0. If PWMSB bit has been programmed to 1, then the LP8555 enters standby mode when PWM input has been low for more than 50 ms even if the ON bit is high.

The device shuts down completely by setting EN/VDDIO and/or VDD to low state.

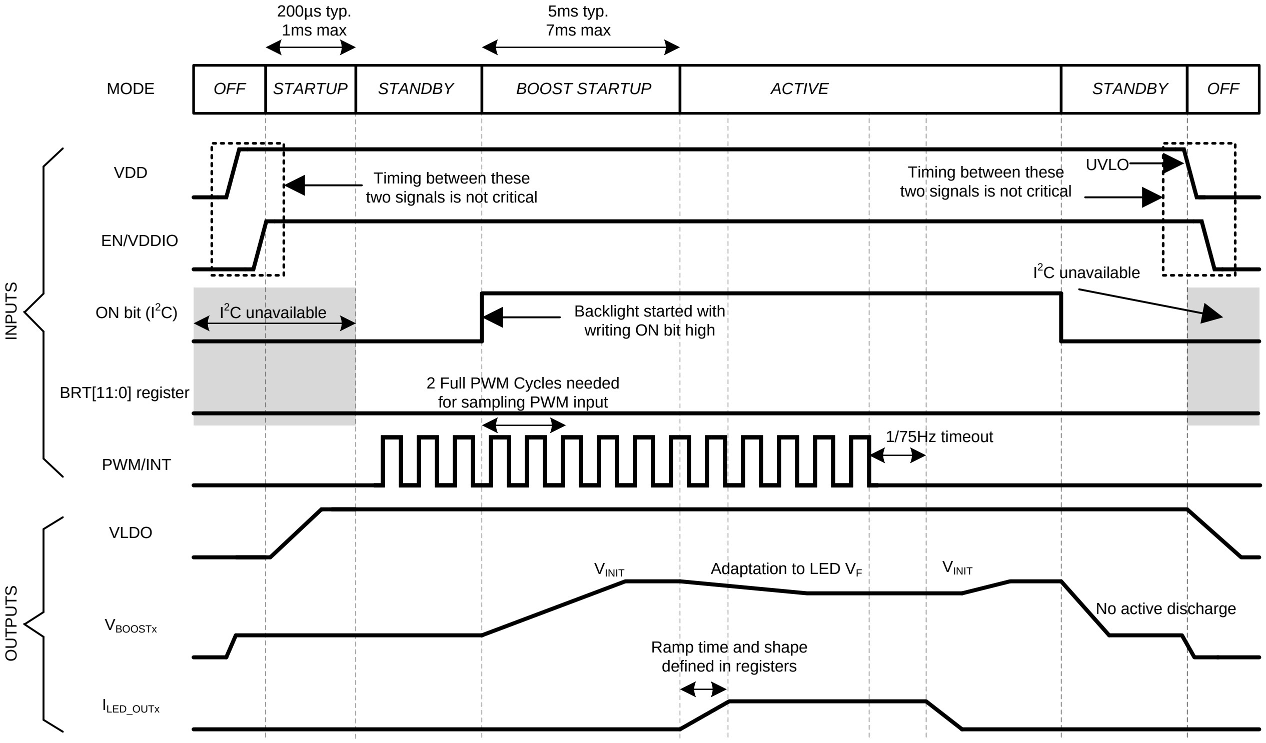


**Figure 33. Start-up and Shutdown with PWM Input Control, ON Bit = 0 (BRTMODE = 00b)**

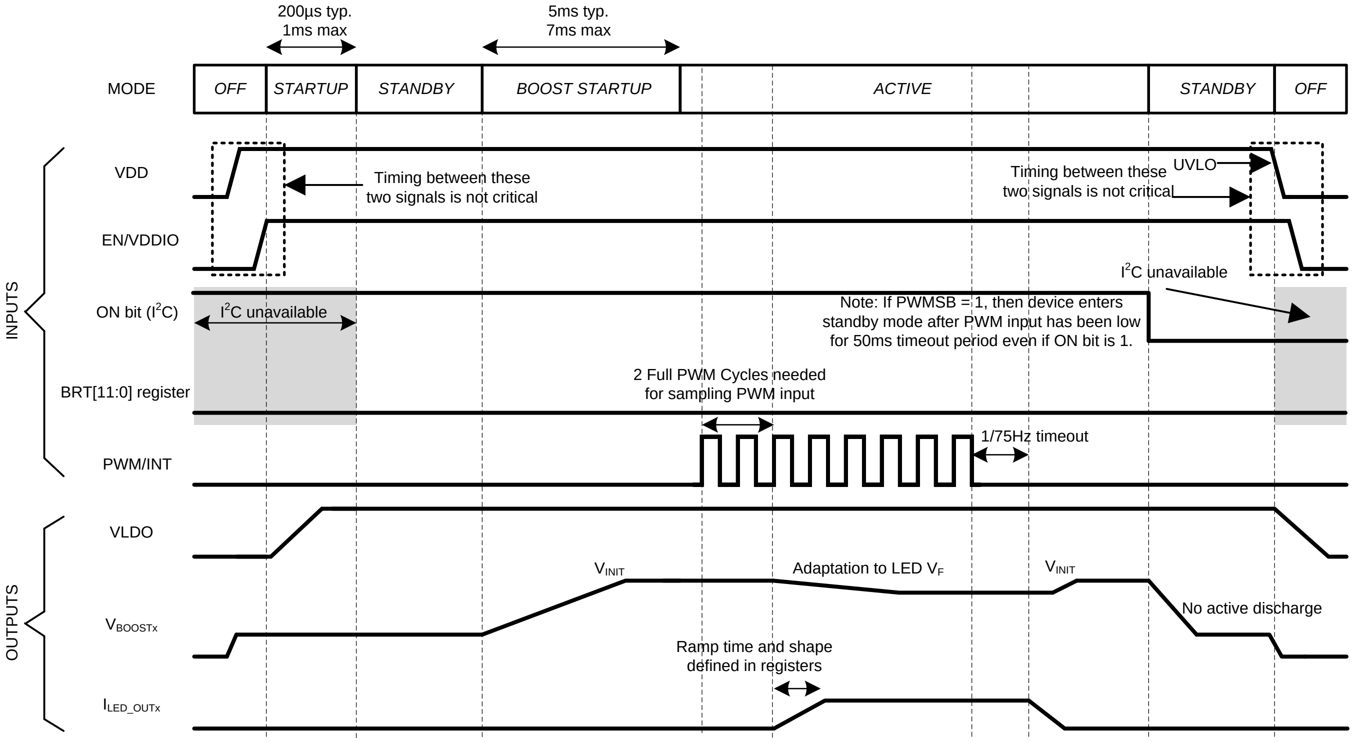


**Figure 34. Start-up and Shutdown with PWM Input Control, ON Bit = 1 (BRTMODE = 00b)**

### 8.3.4.3 Start-up With I$^2$C Brightness Control Mode (BRTMODE = 01b)

When VDD and EN/VDDIO are above min operational value, the LP8555 enters start-up mode. During start-up mode the LDO is started, and EPROM values are read. I$^2$C is available after the start-up sequence has ended.

In standby mode the device waits for the ON bit to go high to start the boost start-up sequence. In standby mode I$^2$C is active, and brightness / other registers can be written.

Once the ON bit is set to 1 (it can be also programmed to 1 by default in EPROM and no I$^2$C write is then needed for entering active mode), boost is started, and device enters active mode with brightness set by I$^2$C brightness registers. If no brightness is set, the backlight stays off until brightness value is written to the I$^2$C register(s). Boost starts initially to the level programmed in EPROM and, after backlight is turned on, the adaptive control adjusts the voltage to get to the minimal headroom voltage.

### 8.3.4.4 Shutdown With I$^2$C Brightness Control Mode (BRTMODE = 01b)

The backlight can be turned off by setting the ON bit low, or by writing brightness to 0. The backlight shuts down immediately if the ON bit is written low even if slope is enabled. If the backlight is turned off by writing brightness to 0, brightness control does slope (if enabled), and the boost is returned to the initial voltage level programmed to EPROM. To enter standby mode where boost is disabled and the power consumption is minimal, the ON bit must be written to 0.

The device shuts down completely by setting EN/VDDIO and/or VDD to low state.

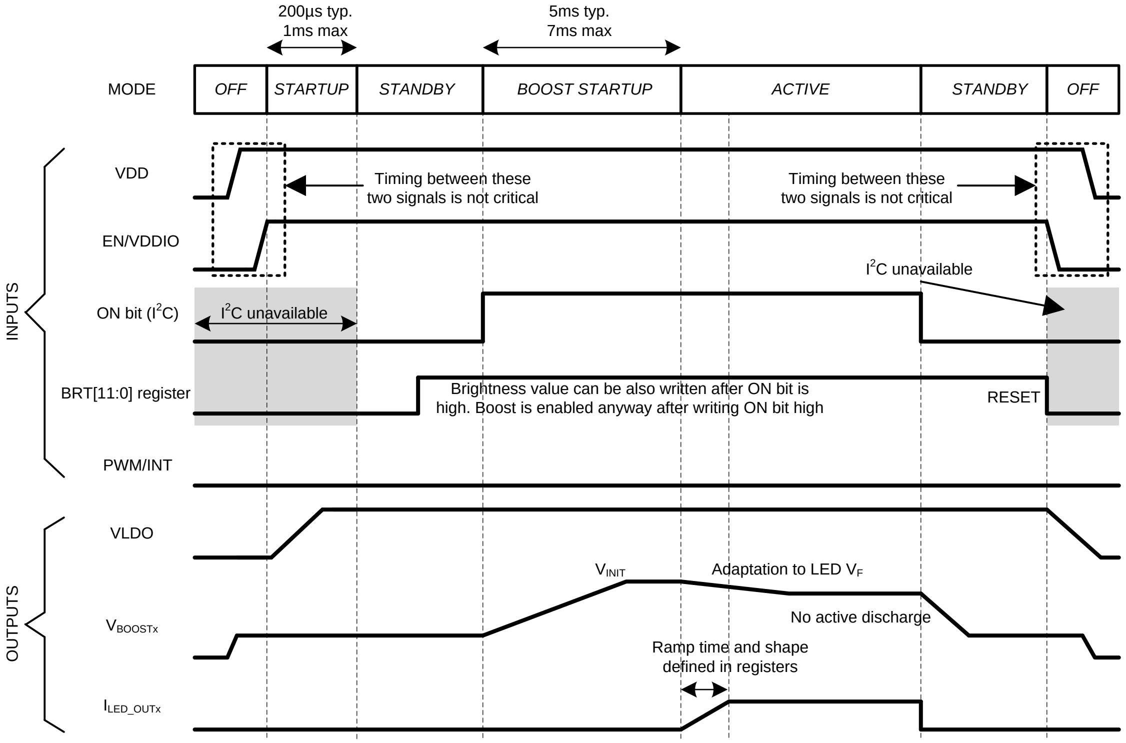


Figure 35. Start-up And Shutdown With I$^2$C Brightness Control Mode (BRTMODE = 01b)

#### 8.3.4.5 Start-up with I$^2$C + PWM Input Brightness Control Mode (BRTMODE = 10 or 11b)

When VDD and EN/VDDIO are above min operational value, the LP8555 enters start-up mode. During start-up mode the LDO is started, and EPROM values are read. I$^2$C is available after the start-up sequence has ended.

In standby mode the device waits for the ON bit to go high to start the boost start-up sequence. In standby mode I$^2$C registers can be written and PWM input duty cycle measurement is active.

Once the ON bit is set to 1 (it can be also programmed to 1 by default in EPROM and no I$^2$C write is then needed for entering active mode), boost is started, and device enters active mode with brightness set by PWM input duty cycle multiplied by I$^2$C brightness register value. If no brightness is set, the backlight stays off until I$^2$C brightness register receives value and two PWM pulses are received in the PWM input, or if PWM input is set high for more than 1/75 Hz time. Boost starts initially to the level programmed in EPROM and after backlight is turned on, the adaptive control adjusts the voltage to get to the minimal headroom voltage.

#### 8.3.4.6 Shutdown with I$^2$C + PWM Input Brightness Control Mode (BRTMODE = 10 or 11b)

The backlight can be turned off by setting the ON bit low, or by setting brightness to 0 either by PWM input (same 1/75 Hz timeout applies here as in PWM input control mode) or by I$^2$C brightness register writes. The backlight shuts down immediately if the ON bit is written low even if slope is enabled. If the backlight is turned off by setting brightness to 0, brightness control does slope (if enabled, depending on which input is used – see brightness control modes for details), and the boost is returned to the initial voltage level programmed to EPROM. To enter standby mode where boost is disabled and the power consumption is minimal, the ON bit must be written to 0.

The device shuts down completely by setting EN/VDDIO and/or VDD to low state.

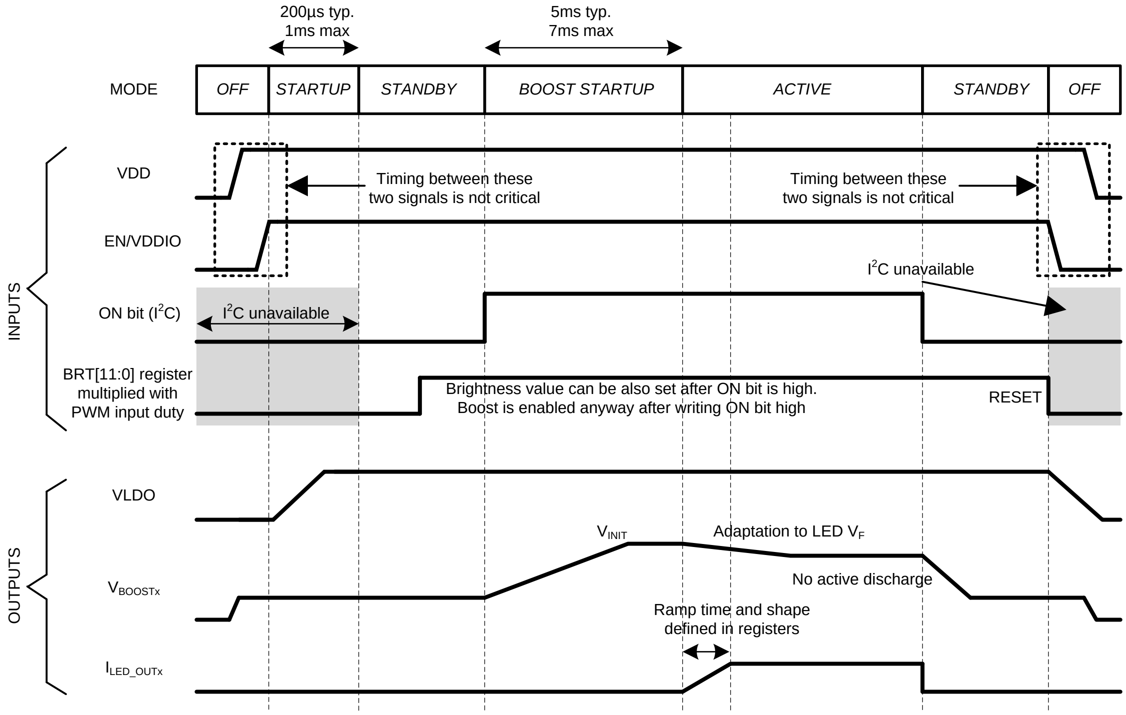


Figure 36. Start-up and Shutdown with I$^2$C + PWM Input Brightness Control (BRTMODE = 01b)

### 8.3.5 LED String Count Auto Detection

The LP8555 can be pre-configured to auto-detect the number of the LED strings attached. If the CONFIG.AUTO bit is set to 1, the LP8555 will automatically remove the unused current sink and adjust phasing of the remaining current sinks. The LED OPEN fault condition will not be set in this mode.

### 8.3.6 Fault Detection

The LP8555 has fault detection for LED OPEN, LED SHORT, UVLO, BST_OVP, BST_OCP, BST_UV and TSD. Faults are recorded in the STATUS register. Each time the STATUS register is read, it is automatically cleared. When BRTMODE is set to 01b any fault may be enabled to cause an interrupt on the PWM/INT terminal.

#### *8.3.6.1 LED Short Detection*

Voltages at the individual current sinks are constantly monitored for the LED SHORT fault. This fault may occur when some LEDs in a string are electrically bypassed making that LED string shorter than the other LED strings. The reduced forward voltage causes the current sink attached to that string to have a higher headroom voltage than the other current sinks. When the headroom voltage is higher than the fault comparator threshold (configured with the OV field in the LEDEN register) that current sink is disabled and the PWM phasing is automatically adjusted. The fault comparator threshold may be configured for 1 V, 2 V, 3 V or 4 V.

#### *8.3.6.2 LED Open Detection*

Each current sink is also monitored for an LED OPEN condition. The condition is set when the headroom voltage on one or more current sinks is below the LOW comparator threshold and the boost voltage is at the maximum. This fault condition may be caused by one or more OPEN LED strings or by one or more current sinks shorted to GND.

The AUTO bit of the CONFIG register determines how the LP8555 responds to an LED OPEN condition. If the CONFIG.AUTO bit is set to 1, the LP8555 will automatically adjust the phasing to remove the current sink with the LED OPEN condition. In this case the condition is normal and indicates an unpopulated LED string. If the CONFIG.AUTO bit is set to 0, the LP8555 will immediately shut down the backlight whenever an LED OPEN condition is detected on any enabled LED drivers. The backlight will not turn on again (regardless of the COMMAND.ON bit) until the STATUS register is read.

#### *8.3.6.3 Undervoltage Detection*

The LP8555 continuously monitors the voltage on the VDD terminal. When the VDD voltage drops below 2.5 V the backlight will be immediately shut down, and the UVLO bit will be set in the STATUS register. The backlight will automatically start again when the voltage has increased above 2.5 V + 50 mV hysteresis. Hysteresis is implemented to avoid continuously triggering undervoltage.

#### *8.3.6.4 Thermal Shutdown*

If the internal temperature reaches 150°C, the LP8555 will immediately shut down the backlight to protect it from damage. The TSD bit will also be set in the STATUS register. The device will re-activate the backlight again when the internal temperature drops below 137°C (typ).

#### *8.3.6.5 Boost Overcurrent Protection*

The LP8555 will automatically limit boost current to 3.1 A (EPROM programmable). When the 3.1-A limit is reached the BST_OCP bit is set in the STATUS register.

#### *8.3.6.6 Boost Overvoltage Protection*

The LP8555 will automatically limit boost voltage to VBOOST_MAX+1.6 V. When the limit is reached the BST_OVP bit is set in the STATUS register. It is possible to set the limit to four threshold levels programmable via EPROM bits.

#### *8.3.6.7 Boost Undervoltage Protection*

The LP8555 can detect when the boost voltage is below VBOOST – 2.5 V for longer than 6ms. When the threshold is reached the BST_UV bit is set in the STATUS register.

### 8.3.7 I$^2$C-Compatible Serial Bus Interface

#### *8.3.7.1 Interface Bus Overview*

The I$^2$C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol use a two-wire interface for bi-directional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (FSET/SDA), and the Serial Clock Line (ISET/SCL). These lines should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (ISET/SCL). The LP8555 is always a slave device.

See the LP8555EVM User Guide for full register map details and programming considerations.

#### *8.3.7.2 Data Transactions*

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

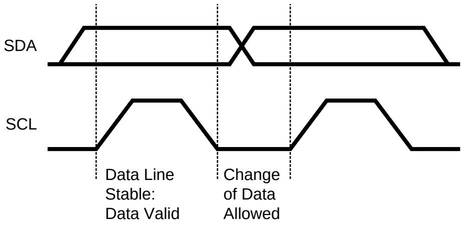


**Figure 37. Bit Transfer**

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

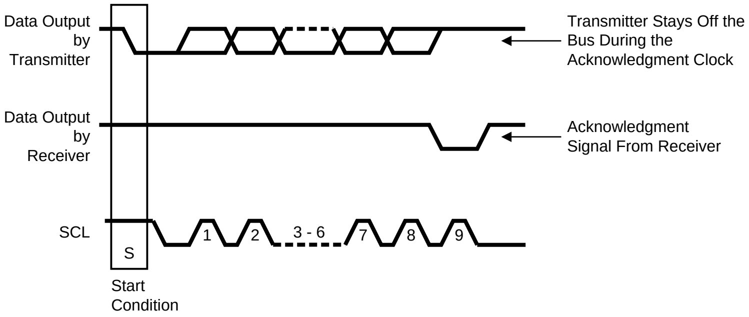


**Figure 38. Start And Stop**

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

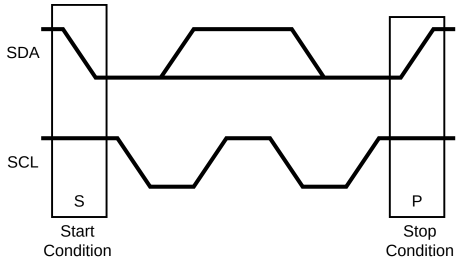


**Figure 39. Start And Stop Conditions**

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

### 8.3.7.3 Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

### 8.3.7.4 "Acknowledge After Every Byte" Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the "acknowledge after every byte" rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging ("negative acknowledge") the last byte clocked out of the slave. This "negative acknowledge" still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

### 8.3.7.5 Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP8555 operates as a slave device with 7-bit address combined with data direction bit. Slave address is 2Ch as 7-bit or 58h for write, and 59h for read in an 8-bit format.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address. The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

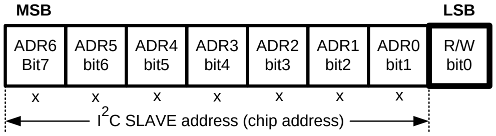


**Figure 40. I$^2$C Slave Address**

### *8.3.7.6 Control Register Write Cycle*

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes, the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

### *8.3.7.7 Control Register Read Cycle*

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

| | ADDRESS MODE |
|---|---|
| Data Read | <Start Condition><br><Slave Address><r/w = '0'>[Ack]<br><Register Addr.>[Ack]<br><Repeated Start Condition><br><Slave Address><r/w = '1'>[Ack]<br>[Register Data]<Ack or Nack>...additional reads from subsequent register address possible<br><Stop Condition> |
| Data Write | <Start Condition><br><Slave Address><r/w = '0'>[Ack]<br><Register Addr.>[Ack]<br><Register Data>[Ack]...additional writes to subsequent register address possible<br><Stop Condition> |

<> Data from master; [ ] Data from slave.

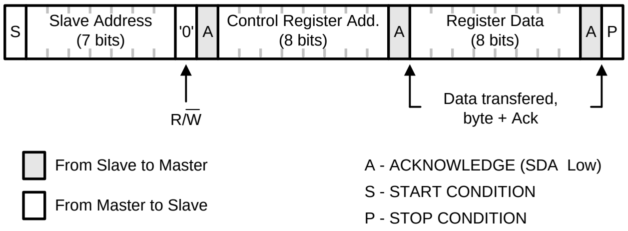


**Figure 41. Register Write Format**

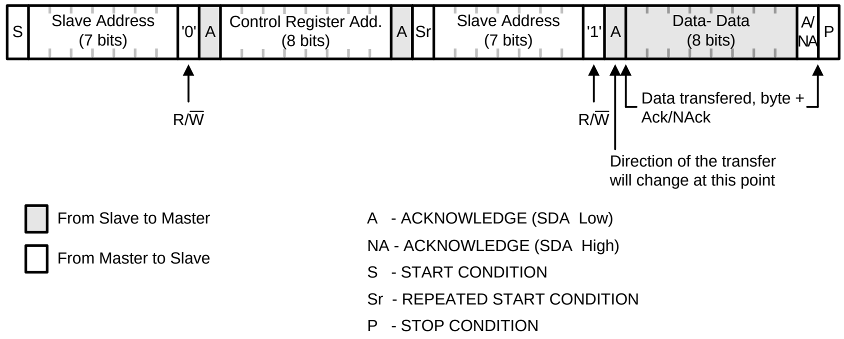


**Figure 42. Register Read Format**

## 8.4 Device Functional Modes

### 8.4.1 Operation Without I$^2$C Control

The device can operate without I$^2$C control in applications where I$^2$C bus is not available. Special EPROM configuration is needed for this setup. In this mode the EN/VDDIO terminal enables the device, and PWM input duty cycle adjusts the brightness. Slopes, PSPWM modes, different boost modes etc. are predefined in the EPROM which device loads at start-up. FSET/SDA and ISET/SCL terminals can be used to set the PWM frequency and LED current based on specific needs (see corresponding sections for setting the frequency and current), without needing separate EPROM configuration for each application. The backlight start-up happens when EN/VDDIO terminal is high and PWM input receives measurable duty cycle. If the PWMSB bit is set 1 in EPROM, the device enters standby mode automatically when PWM/INT is set low. If PWMSB is 0, the device is shut down setting EN/VDDIO low. See start-up and shutdown diagrams for more details.

### 8.4.2 Operation With I$^2$C Control

With I$^2$C control, user may set the device configuration more freely and have additional I$^2$C brightness control. The backlight brightness can be controlled with either PWM input, with I$^2$C, or a combination of both. Configuration for slopes, PSPWM, or different boost modes can be used from EPROM defaults, or user can set own configuration before backlight is turned on. Configuration setting is done when EN/VDDIO is high (I$^2$C is active) and the ON bit is low. $R_{FSET}$ and $R_{ISET}$ resistors cannot be used in I$^2$C control mode, because they are multiplexed as the I$^2$C bus terminals (SDA/SCL). The backlight is started by setting the ON bit high, and shutdown is done by setting ON bit low. See start-up and shutdown diagrams for more details. Details of the I$^2$C registers and programming considerations are seen in the LP8555EVM User Guide.

### 8.4.3 Shutdown Mode

The device is in shutdown mode when the EN/VDDIO terminal is low. the EN/VDDIO terminal enables an LDO, which is used for powering internal logic and analog blocks. Current consumption in this mode from VDD terminal is <1 µA.

### 8.4.4 Standby Mode

In standby mode the EN/VDDIO terminal is set high (with VDD power present), and logic is powered from an LDO. The device goes through the start-up sequence where NVM (EPROM) is loaded to the registers. I$^2$C is available in standby mode, and register settings can be changed. Current consumption is < 30 µA in this mode from VDD terminal.

### 8.4.5 Active Mode

In active mode the backlight is enabled either with setting the ON register bit high (I$^2$C control mode) or by activating PWM input. The EN/VDDIO terminal must be high, and VDD must be present. Brightness is controlled with I$^2$C writes to brightness registers or by changing PWM input duty cycle (operation without I$^2$C control). Configuration registers are not accessible in Active mode to prevent damage to the device by accidental writes. Current consumption from VDD terminal in this mode is typically 4.2 mA when LEDs are not drawing any current.

## 8.5 Register Maps

<table>
<tr><th>Register</th><th>Addr</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>COMMAND</td><td>00h</td><td>RESET</td><td></td><td></td><td></td><td></td><td>SREN</td><td>SSEN</td><td>ON</td></tr>
<tr><td>STATUS</td><td>01h</td><td>LED_OPEN</td><td>LED_OV</td><td></td><td>BST_UV</td><td>BST_OVP</td><td>BST_OCP</td><td>TSD</td><td>UVLO</td></tr>
<tr><td>MASK</td><td>02h</td><td>LED_OPEN</td><td>LED_OV</td><td></td><td>BST_UV</td><td>BST_OVP</td><td>BST_OCP</td><td>TSD</td><td>UVLO</td></tr>
<tr><td>BRTLO</td><td>03h</td><td colspan="4">BRT[3:0]</td><td colspan="4"></td></tr>
<tr><td>BRTHI</td><td>04h</td><td colspan="8">BRT[11:4]</td></tr>
<tr><td>CONFIG</td><td>10h</td><td>PWMSB</td><td>PWMFILT</td><td>EN_BPHASE180</td><td></td><td>RELOAD</td><td>AUTO</td><td colspan="2">BRTMODE</td></tr>
<tr><td>CURRENT</td><td>11h</td><td>ISET</td><td colspan="4"></td><td colspan="3">MAXCURR</td></tr>
<tr><td>PGEN</td><td>12h</td><td>PFSET</td><td></td><td colspan="3">THRESHOLD</td><td colspan="3">PFREQ</td></tr>
<tr><td>BOOST</td><td>13h</td><td></td><td></td><td colspan="2"></td><td colspan="2"></td><td>BIND</td><td>BFREQ</td></tr>
<tr><td>LEDEN_0</td><td>14h</td><td colspan="2">OV</td><td colspan="6">ENABLE_0</td></tr>
<tr><td>STEP</td><td>15h</td><td colspan="2">SMOOTH</td><td colspan="3">PWM_IN_HYST</td><td colspan="3">STEP</td></tr>
<tr><td>VOLTAGE_0</td><td>16h</td><td colspan="2">VMAX_0</td><td>ADAPT_0</td><td colspan="5">VINIT_0</td></tr>
<tr><td>LEDEN_1</td><td>19h</td><td colspan="2"></td><td colspan="6">ENABLE_1</td></tr>
<tr><td>VOLTAGE_1</td><td>1Ah</td><td colspan="2">VMAX_1</td><td>ADAPT_1</td><td colspan="5">VINIT_1</td></tr>
<tr><td>OPTION</td><td>1Ch</td><td colspan="4"></td><td colspan="4">OPTION</td></tr>
<tr><td>EXTRA</td><td>1Dh</td><td colspan="8">EXTRA</td></tr>
<tr><td>ID</td><td>1Eh</td><td colspan="4">ID_CUST</td><td colspan="4">ID_CFG</td></tr>
<tr><td>REVISION</td><td>1Fh</td><td colspan="4">MAJOR</td><td colspan="4">MINOR</td></tr>
<tr><td>CONF0</td><td>76h</td><td>BOOST_IS_DIV2</td><td colspan="2"></td><td>ALTID</td><td colspan="2">SRON</td><td colspan="2">CURR_LIMIT</td></tr>
<tr><td>CONF1</td><td>77h</td><td colspan="2">FMOD_DIV</td><td colspan="2"></td><td colspan="4"></td></tr>
<tr><td>VHR0</td><td>78h</td><td></td><td colspan="3">VHR_SLOPE</td><td></td><td colspan="3">VHR_VERT</td></tr>
<tr><td>VHR1</td><td>79h</td><td colspan="2"></td><td colspan="2">VHR_HYST</td><td colspan="2"></td><td colspan="2">VHR_HORZ</td></tr>
<tr><td>JUMP</td><td>7Ah</td><td>JEN</td><td colspan="3"></td><td colspan="2">JTHR</td><td colspan="2">JVOLT</td></tr>
</table>

Some register fields are loaded from an internal EPROM (shaded above). This EPROM is programmed by TI during final test. This allows default values to be assigned. This feature is intended for applications where the $I^2C$ interface is not used. With the exception of the ID fields, all EPROM based fields can be written via $I^2C$ writes like a normal register field. There are limitations on certain configuration bits, their operation and can they be changed "on-the-fly". It is noted in the description of corresponding bit.

### 8.5.1 COMMAND

Address: 0x00

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| RESET | — | | | | SREN | SSEN | ON |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7 | RESET | R/W | Write 1 to reset the device. This bit is self-cleaning and will always be 0 when read. |
| 6:3 | reserved | R/O | |
| 2 | SREN | R/W | 0 = Slew rate limited disabled<br>1 = Enable slower boost gate drive slew rate. Reduces EMI energy in high frequencies and reduces boost efficiency. |
| 1 | SSEN | R/W | 0 = Spread Spectrum Scheme disabled<br>1 = Enable spread-spectrum boost clocking. Spreads EMI spectrum spikes. |
| 0 | ON | R/W | Turn on the backlight.<br>0 = backlight off<br>1 = backlight on |

The COMMAND.ON bit must be programmed to 1 in the EPROM for applications without $I^2C$ access to the device. The COMMAND.SSEN bit may be updated at any time. It is not necessary for the backlight to be off when changing COMMAND.SSEN and/or COMMAND.SREN.

### 8.5.2 STATUS/MASK

Address: 0x01/0x02

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| DRV_FAULT | DRV_OV | — | BST_UV | BST_OVP | BST_OCP | TSD | UVLO |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7 | LED_OPEN | R/O | An open/short condition was detected on one or more LED strings. Once set this bit will stay set until the STATUS register is read. An LED open/short condition will turn off the backlight when CONFIG.AUTO is 0. |
| 6 | LED_OV | R/O | An overvoltage condition was detected on one or more LED strings. Once set this bit will stay set until the STATUS register is read. |
| 5 | reserved | R/O | |
| 4 | BST_UV | R/O | The boost reported an undervoltage condition. Once set this bit will stay set until the STATUS register is read. |
| 3 | BST_OVP | R/O | The boost reported an overvoltage protection condition when the maximum allowed voltage is requested. Once set this bit will stay set until the STATUS register is read. |
| 2 | BST_OCP | R/O | The boost reported an undervoltage condition longer than 50 ms in time when the backlight on. |
| 1 | TSD | R/O | A thermal shutdown condition was detected. Once set this bit will stay set until the STATUS register is read. A thermal shutdown condition will turn off the backlight. |
| 0 | UVLO | R/O | An undervoltage lockout condition was detected. Once set this bit will stay set until the STATUS register is read. An undervoltage lockout condition will turn off the backlight. |

Each fault bit of the STATUS register has a corresponding bit in the MASK register, which enables interrupts for the fault. For example, an interrupt will occur if the MASK.BST_UV and STATUS.BST_UV bits are both set. If a fault bit is cleared in the MASK register then that fault will not trigger an interrupt.

### 8.5.3 BRTLO

Address: 0x03

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| BRT[3:0] | | | | RESERVED | | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:4 | BRT[3:0] | R/W | Least significant bits of the brightness level. |
| 3:0 | reserved | R/O | |

### 8.5.4 BTHI

Address: 0x04

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| BRT[11:4] | | | | | | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:0 | BRT[11:4] | R/W | Most significant bits of the brightness level. |

The brightness level can be updated with 8-bit precision or 12-bit precision. To make brightness level updates effective the internal brightness level is only updated when the BRTHI register is written. If the BRTHI register is written without a previous write to the BRTLO register, then the lower 4 bits of the internal 12-bit brightness will be synthesized from the BRTHI register value.

| BRTLO | BRTHI | Brightness | Comments |
|---|---|---|---|
| write 0x95 | write 0xFC | 0xFC9 | BRTLO[3:0] is ignored |
| write 0x10 | write 0xDC | 0xDC1 | set to an exact 12-bit value |
| no write | write 0x8C | 0x8C8 | synthesize low order bits |
| no write | write 0x0C | 0x0C0 | synthesize low order bits |
| no write | write 0x00 | 0x000 | 0% brightness |
| no write | write 0xFF | 0xFFF | 100% brightness |

### 8.5.5 CONFIG

Address: 0x10

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| PWMSB | PWMFILT | EN_BPHASE180 | RESERVED | RELOAD | AUTO | BRTMODE | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7 | PWMSB | R/W | Enables PWM standby mode<br>0 = CONTROL.ON alone turns the backlight on/off<br>1 = turn off the backlight after 50 ms of PWM low |
| 6 | PWMFILT | R/W | 0 = PWM input filter disabled<br>1 = Enable 50 ns glitch filter on PWM input. |
| 5 | EN_BPHASE180 | R/W | 0 = Boosts operate in same phase<br>1 = Enable 180° phase shift between the 2 boost switchers. |
| 4 | reserved | R/O | |
| 3 | RELOAD | R/W | Automatically re-read the EPROM at each turn-on.<br>0 = only read the EPROM upon power-up<br>1 = re-read the EPROM when the backlight turns on |
| 2 | AUTO | R/W | Automatic LED string configuration<br>0 = enable LED strings using just LEDEN.ENABLE<br>1 = disable all open LED strings |
| 1:0 | BRTMODE | R/W | Brightness mode<br>00 = PWM<br>01 = BRTHI/BRTLO registers<br>10 = PWM × unshaped BRTHI/BRTLO registers<br>11 = BRTHI/BRTLO registers × unshaped PWM |

When the AUTO bit is set the LED configuration is done dynamically. When an OPEN/SHORT condition is detected on an LED string it will be removed, and PWM output phasing will be adjusted. Conversely, an LED string will be added back for operation if the LED string is not open.

The BRTMODE field selects how LED brightness is controlled. When BRTMODE is set to 00b the PWM/INT terminal duty cycle controls the LED brightness. When BRTMODE is set to 01b the BRTLO and BRTHI registers will control the LED brightness. When the backlight is turned on the brightness level is reset to 0% and will automatically transition to the brightness value programmed in the BRTLO and BRTHI registers.

When the BRTMODE field is set to 00b, and the PWMSB bit is set to 1, the backlight will be turned off whenever the PWM/INT terminal is held low for 50 ms. This will also put the device into its lowest power state. When the PWM/INT terminal becomes active the backlight will automatically turn back on.

A 50 ns glitch filter will be applied to the PWM input signal when the PWMFILT bit is set to 1. When BRTMODE is set to 10b or 11b the LED brightness is controlled by both the PWM/INT terminal duty cycle and the BRTLO and BRTHI registers.

When BRTMODE is set to 10b the PWM/INT terminal duty cycle is routed through the smoothing function (controlled via the STEP register). The smoothed duty cycle is multiplied with the value from the BRTLO/BRTHI registers. Updates to the BRTLO/BRTHI registers have an immediate effect on the LED brightness, while PWM/INT terminal duty cycle changes may be smoothed.

When BRTMODE is set to 11b the BRTLO/BRTHI register value is routed through the smoothing function. The smoothed brightness level is multiplied with the PWM/INT terminal duty cycle. In this configuration PWM/INT terminal duty cycle changes have an immediate effect on the LED brightness, while BRTLO/BRTHI register changes may be smoothed.

### 8.5.6 CURRENT

Address: 0x11

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| ISET | — | | | | MAXCURR | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7 | ISET | R/W | 0 = LED maximum current set with MAXCURR bits<br>1 = Set MAXCURR via the ISET/SCL terminal. This terminal should only set to 1 as an EPROM default, writing to this bit "on-the-fly" does not have effect. Resistor values and their corresponding LED current setting is seen in Full-Scale LED Current section. |
| 6:3 | reserved | R/O | |
| 2:0 | MAXCURR | R/W | Full-scale current, 100% brightness (typical).<br>000 = 5 mA<br>001 = 10 mA<br>010 = 15 mA<br>011 = 20 mA<br>100 = 23 mA<br>101 = 25 mA<br>110 = 30 mA<br>111 = 50 mA |

The full-scale current can be configured into two different ways: EPROM or ISET/SCL terminal. The ISET/SCL terminal resistor is automatically measured during start-up. The CURRENT.ISET bit is used to select between the maximum current value measured from the ISET/SCL terminal and the EPROM value. When the ISET bit is set to 1 the ISET/SCL terminal value is used; otherwise the EPROM value is used. Regardless of EPROM programming, the maximum current can always be configured from $I^2C$ by clearing the CURRENT.ISET bit and configuring the CURRENT.MAXCURR field as needed.

When the CURRENT register is read via $I^2C$ the MAXCURR field will contain the active full-scale current value. To read the EPROM value the ISET bit must be set to 0. To read the $R_{ISET}$ resistor value the ISET bit must be set to 1 during start-up, which means it must be set in EPROM.

If the ISET/SCL terminal is grounded or floating the MAXCURR value will be set to 23 mA if ISET = 1.

### 8.5.7 PGEN

Address: 0x12

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| PFSET | RESERVED | THRESHOLD | | | PFREQ | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7 | PFSET | R/W | 0 = PWM frequency is set with PFREQ register bits<br>1 = Set PFREQ via the FSET/SDA terminal. This bit should only be set to 1 as an EPROM default, writing to this bit "on-the-fly" does not have effect. Resistor values and their corresponding frequency settings are seen in Setting PWM Dimming Frequency section. |
| 6 | RESERVED | R/O | 0 |
| 5:3 | THRESHOLD | R/W | Adaptive dimming threshold. PWM dimming is used below the threshold and current dimming is used above the threshold.<br>000 = 100% current dimming<br>101 = PWM below 25% (10-bit PWM)<br>111 = 100% PWM (12-bit PWM) |
| 2:0 | PFREQ | R/W | PWM output frequency (typical)<br>000 = 4.9 kHz<br>001 = 9.8 kHz<br>011 = 19.5 kHz<br>111 = 39.1 kHz |

The output PWM frequency can be configured in two different ways: EPROM or FSET/SDA terminal. The FSET/SDA terminal is always automatically measured. The PGEN.PFSET bit is used to select between the PWM frequency value measured from the FSET/SDA terminal and the EPROM value. When the PFSET bit is set to 1 the FSET/SDA terminal value is used; otherwise the EPROM value is used. Regardless of EPROM programming, the PWM frequency can always be configured from I$^2$C by clearing the PGEN.PFSET bit and configuring the PGEN.PFREQ field as needed.

Full 12-bit precision is achieved in all adaptive dimming thresholds and PWM output frequencies. When the PGEN register is read via I$^2$C the PFREQ field will contain the active PWM output frequency value. To read the EPROM value the PFSET bit must be set to 0. To read the $R_{FSET}$ resistor value the PFSET bit must be set to 1.

If the FSET/SDA terminal is grounded or floating the PFREQ value will be set to 19.5 kHz.

### 8.5.8 BOOST

Address: 0x13

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | RESERVED | | RESERVED | | BIND | BFREQ |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:6 | RESERVED | R/W | |
| 5:4 | RESERVED | R/W | |
| 3:2 | RESERVED | R/W | |
| 1 | BIND | R/W | BIND bit is used to set boost inductor size.<br>0 = 4.7 µH … 6.8 µH<br>1 = 10 µH … 22 µH |
| 0 | BFREQ | R/W | Boost frequency (typical). This setting must be configured in EPROM, changing it with I2C register write does not have desired effect.<br>0 = 500 kHz<br>1 = 1 MHz |

### 8.5.9 LEDEN

Address: 0x14

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| OV | | ENABLE[6:1] | | | | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:6 | OV | R/W | Set LED overvoltage level (typical).<br>00 = 1V<br>01 = 2V<br>10 = 3V<br>11 = 4V |
| 5:0 | ENABLE | R/W | LED string enables for Bank A. |

The ENABLE field configures the enabled LED strings. If the CONFIG.AUTO bit is 0 these LED strings will stay active when the backlight is on. If the CONFIG.AUTO bit is set, then an LED open/short condition will cause that LED string to be removed. A given LED string will never be enabled if the corresponding bit of the ENABLE field is set to 0. The OV field configures the threshold for detecting an LED overvoltage condition; which may occur when one or more LEDs are bypassed (shorted) within an LED string.

### 8.5.10 STEP

Address: 0x15

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| SMOOTH | | PWM_IN_HYST | | | | STEP | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:6 | SMOOTH | R/W | Advanced Slope control. Filter strength for digital smoothing filter.<br>00 = no smoothing<br>01 = light smoothing<br>10 = medium smoothing<br>11 = heavy smoothing |
| 5:2 | PWM_IN_HYST | R/W | PWM input hysteresis<br>000 = None<br>001 = >1 LSB steps<br>010 = >2 LSB steps<br>011 = >4 LSB steps<br>100 = >8 LSB steps<br>101 = >16 LSB steps<br>110 = >32 LSB steps<br>111 = >64 LSB steps |
| 2:0 | STEP | R/W | Linear Sloping time (typical)<br>000 = 0 ms<br>001 = 8 ms<br>010 = 16 ms<br>011 = 24 ms<br>100 = 28 ms<br>101 = 32 ms (12.2 µs / 12-bit LSB)<br>110 = 100 ms (24.4 µs / 12-bit LSB)<br>111 = 200 ms (48.8 µs / 12-bit LSB) |

The STEP field controls the rate of brightness level changes. Brightness transitions have a fixed step time. The time required to complete a ramp between two levels is independent upon the difference between the starting and ending current levels. For example, when STEP is set to 110b a brightness transition between any brightness values will take 100 ms. The SMOOTH field controls the digital smoothing filter, Advanced Sloping. This filter behaves much like an RC filter. It can be used to remove the overshoot that appears to occur (for eye) on large brightness changes. The actual amount of smoothing is tailored for the STEP field setting. For example medium filter strength is higher for 100 ms ramp times than for 32 ms Linear Sloping times. This gives 32 possible brightness level ramping configurations.

The PWM detector over-samples the input PWM signal at 20 MHz. The accuracy of the duty-cycle measurement depends upon the frequency of the PWM signal. The maximum possible accuracy is 12-bit precision. To allow 12-bit precision the LP8555 must take at least 8192 samples.

$$\frac{20\ MHz}{2.44\ KHz} \approx 8192\ samples$$

| 0 | 2.4 kHz | 4.8 kHz | 9.6 kHz | 19.5 kHz | 39 kHz | 78 kHz | 156 kHz |
|---|---|---|---|---|---|---|---|
| 12-bit | 11-bit | 10-bit | 9-bit | 8-bit | 7-bit | 6-bit | |

When the PWM detector detects new PWM-value, it is effective only when it differs from previous value more than selected hysteresis. Hysteresis is selected with PWM_IN_HYST in register 0x15.

### 8.5.11 Brightness Transitions, Typical Times

| STEP | SMOOTH | RAMP TIME (0 to 100%) (ms) |
|---|---|---|
| 000 | 00 | 0.0 |
| 000 | 01 | 0.9 |
| 000 | 10 | 1.7 |
| 000 | 11 | 3.4 |
| 001 | 00 | **8.2** |
| 001 | 01 | 14.6 |
| 001 | 10 | 22.3 |
| 001 | 11 | 38.7 |
| 010 | 00 | **16.0** |
| 010 | 01 | 28.4 |
| 010 | 10 | 43.5 |
| 010 | 11 | 75.5 |
| 011 | 00 | **24.2** |
| 011 | 01 | 42.9 |
| 011 | 10 | 65.8 |
| 011 | 11 | 114.2 |
| 100 | 00 | **27.9** |
| 100 | 01 | 49.5 |
| 100 | 10 | 75.8 |
| 100 | 11 | 131.7 |
| 101 | 00 | **32.0** |
| 101 | 01 | 56.8 |
| 101 | 10 | 87.0 |
| 101 | 11 | 151.1 |
| 110 | 00 | **102.0** |
| 110 | 01 | 181.0 |
| 110 | 10 | 277.2 |
| 110 | 11 | 481.5 |
| 111 | 00 | **204.8** |
| 111 | 01 | 363.4 |
| 111 | 10 | 556.6 |
| 111 | 11 | 966.9 |

### 8.5.12 VOLTAGE_0

Address: 0x16

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| VMAX | | ADAPT | VINIT | | | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:6 | VMAX | R/W | Maximum boost voltage for Boost A (typical).<br>00 = 18V<br>01 = 22V<br>10 = 25V<br>11 = 28V |
| 5 | ADAPT | R/W | Enable adaptive headroom optimization. |
| 4:0 | VINIT | R/W | Initial boost voltage. When ADAPT is 0 the boost voltage will remain at the VINIT setting. The voltage range is from 7V to 28V; where 0x00 equals 7V and 0x3F equals 28V (typical). |

The VOLTAGE_0.VMAX bit sets the maximum allowed boost voltage for Boost A. The boost control loop will never request a higher voltage than the VMAX value. When the VOLTAGE.ADAPT bit is set to 1 the boost voltage may vary from 7V to the VMAX configured voltage.

| VINIT (DEC) | Voltage (V) | VINIT (DEC) | Voltage (V) | VINIT (DEC) | Voltage (V) |
|---|---|---|---|---|---|
| 0 | 7.00 | 11 | 14.45 | 22 | 21.91 |
| 1 | 7.68 | 12 | 15.13 | 23 | 22.58 |
| 2 | 8.35 | 13 | 15.8 | 24 | 23.26 |
| 3 | 9.03 | 14 | 16.48 | 25 | 23.94 |
| 4 | 9.71 | 15 | 17.16 | 26 | 24.61 |
| 5 | 10.39 | 16 | 17.84 | 27 | 25.29 |
| 6 | 11.06 | 17 | 18.52 | 28 | 25.97 |
| 7 | 11.74 | 18 | 19.2 | 29 | 26.65 |
| 8 | 12.42 | 19 | 19.87 | 30 | 27.32 |
| 9 | 13.09 | 20 | 20.55 | 31 | 28.00 |
| 10 | 13.77 | 21 | 21.23 | | |

Example: For system where is 7 LEDs in series with 2.9 V Vf. Target value for boost initial voltage would be: 7 x (2.9 V + 0.1 V) + 2 V = 23 V → VINIT = 24(DEC). 0.1 V represents Vf variation of single LED, and 2 V is worst case headroom. So it is desirable to set the initial voltage little higher than the actual Vf voltage to take the worst-case condition in consideration.

### 8.5.13 LEDEN1

Address: 0x19

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | ENABLE[6:1] | | | | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:6 | RESERVED | R/O | |
| 5:0 | ENABLE1 | R/W | LED string enables for Bank B. |

The ENABLE field configures the enabled LED strings. If the CONFIG.AUTO bit is 0 these LED strings will stay active when the backlight is on. If the CONFIG.AUTO bit is set, then an LED open/short condition will cause that LED string to be removed. A given LED string will never be enabled if the corresponding bit of the ENABLE field is set to 0. The OV field configures the threshold for detecting an LED overvoltage condition; which may occur when one or more LEDs are bypassed (shorted) within an LED string.

### 8.5.14 VOLTAGE1

Address: 0x1A

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| VMAX1 | | ADAPT1 | VINIT1 | | | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:6 | VMAX | R/W | Maximum boost voltage for Boost B (typical).<br>00 = 18 V<br>01 = 22 V<br>10 = 25 V<br>11 = 28 V |
| 5 | ADAPT | R/W | Enable adaptive headroom optimization. |
| 4:0 | VINIT1 | R/W | Initial boost voltage. When ADAPT is 0 the boost voltage will remain at the VINIT setting. The voltage range is from 7 V to 28 V; where 0x00 equals 7 V and 0x3F equals 28 V (typical). |

The VOLTAGE1.VMAX bit sets the maximum allowed boost voltage for Boost B. The boost control loop will never request a higher voltage than the VMAX value. When the VOLTAGE.ADAPT bit is set to 1 the boost voltage may vary from 7 V to the VMAX configured voltage.

| VINIT (DEC) | VOLTAGE (V) | VINIT (DEC) | VOLTAGE (V) | VINIT (DEC) | VOLTAGE (V) |
|---|---|---|---|---|---|
| 0 | 7.00 | 11 | 14.45 | 22 | 21.91 |
| 1 | 7.68 | 12 | 15.13 | 23 | 22.58 |
| 2 | 8.35 | 13 | 15.8 | 24 | 23.26 |
| 3 | 9.03 | 14 | 16.48 | 25 | 23.94 |
| 4 | 9.71 | 15 | 17.16 | 26 | 24.61 |
| 5 | 10.39 | 16 | 17.84 | 27 | 25.29 |
| 6 | 11.06 | 17 | 18.52 | 28 | 25.97 |
| 7 | 11.74 | 18 | 19.2 | 29 | 26.65 |
| 8 | 12.42 | 19 | 19.87 | 30 | 27.32 |
| 9 | 13.09 | 20 | 20.55 | 31 | 28.00 |
| 10 | 13.77 | 21 | 21.23 | | |

### 8.5.15 OPTION

Address: 0x1C

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | OPTION | | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:4 | reserved | R/O | |
| 3:0 | OPTION | R/O | Metal option identifier. |

### 8.5.16 EXTRA

Address: 0x1D

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| EXTRA | | | | | | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:0 | EXTRA | R/W | User accessible extra identifier register |

### 8.5.17 ID

Address: 0x0E

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| ID_CUST | | | | ID_CFG | | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:4 | ID_CUST | R/W | TI Customer ID code. |
| 3:0 | ID_CFG | R/W | TI Configuration ID code. |

The ID field is configured by TI when the EPROM is programmed.

### 8.5.18 REVISION

Address: 0x0F

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| MAJOR | | | | MINOR | | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:4 | MAJOR | R/O | Major silicon revision. |
| 3:0 | MINOR | R/O | Minor silicon revision. |

The REVISION register provides silicon revision information in case test SW needs to distinguish between different revisions of the device or later identification is needed. REVISION register content comes from read only metal register (connected at COM level).

### 8.5.19 CONF0

Address: 0x76

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| BOOST_IS_DIV2 | RESERVED | | ALTID | SRON | | CURR_LIMIT | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7 | BOOST_IS_DIV2 | R/W | Divide inductor peak current by 2<br>0 = Normal operation<br>1 = Inductor currents divided by 2 |
| 6:5 | RESERVED | R/W | |
| 4 | ALTID | R/W | $I^2C$ Slave ID selector<br>0 = 2Ch<br>1 = 2Eh |
| 3:2 | SRON | R/W | Slowed boost slew rate. When COMMAND.SREN is set to 1 boost slew rate is controlled with this value. |
| 1:0 | CURR_LIMIT | R/W | Boost inductor peak current limit (typical). BOOST_IS_DIV2 sets which of the limits is used.<br>00 = 0.9 A / 1.55 A<br>01 = 1.2 A / 2.1 A<br>10 = 1.5 A / 2.6 A<br>11 = 1.8 A / 3.1 A |

### 8.5.20 CONF1

Address: 0x77

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FMOD_DIV | | RESERVED | | RESERVED | | RESERVED | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:6 | FMOD_DIV | R/W | Spread spectrum modulation frequency divisor.<br>00 = 0.45%<br>01 = 0.27%<br>10 = 0.17%<br>11 = 0.12% |
| 5:0 | RESERVED | R/W | |

The FMOD_DIV field controls modulation frequency for spread spectrum clocking. The actual modulation frequency scales with the boost frequency.

| BOOST FREQUENCY (kHz) | FMOD_DIV = 00b (kHz) | FMOD_DIV = 01b (kHz) | FMOD_DIV = 10b (kHz) | FMOD_DIV = 11b (kHz) |
|---|---|---|---|---|
| 1000 | 4.17 | 2.78 | 1.67 | 1.19 |
| 500 | 2.08 | 1.39 | 0.83 | 0.64 |

### 8.5.21 VHR0

Address: 0x78

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| RESERVED | VHR_SLOPE | | | RESERVED | VHR_VERT | | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7 | RESERVED | R/O | |
| 6:4 | VHR_SLOPE | R/W | Typical headroom voltage at maximum current (50 mA)<br>000 = 210 mV<br>001 = 223 mV<br>010 = 235 mV<br>011 = 248 mV<br>100 = 260 mV<br>101 = 273 mV<br>110 = 285 mV<br>111 = 300 mV |
| 3 | RESERVED | | |
| 2:0 | VHR_VERT | R/W | Typical minimum headroom voltage<br>000 = 50 mV<br>001 = 80 mV<br>010 = 110 mV<br>011 = 140 mV<br>100 = 170 mV<br>101 = 200 mV<br>110 = 230 mV<br>111 = 260 mV |

### 8.5.22 VHR1

Address: 0x79

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | VHR_HYST | | RESERVED | | VHR_HORZ | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7:6 | RESERVED | R/O | |
| 5:4 | VHR_HYST | R/W | Typical hysteresis for the mid comparator threshold (above the low comparator threshold).<br>00 = 200 mV<br>01 = 233 mV<br>10 = 466 mV<br>11 = 600 mV |
| 3:2 | RESERVED | R/O | |
| 1:0 | VHR_HORZ | R/W | Percentage of full driver range (horizontal component)<br>00 = 1%<br>01 = 25%<br>10 = 37.5%<br>11 = 50% |

### 8.5.23 JUMP

Address: 0x7A

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| JEN | RESERVED | | | JTHR | | JVOLT | |

| Bits | Field | Type | Description |
|---|---|---|---|
| 7 | JEN | R/W | Enable boost voltage jumping on large brightness percentage increases. |
| 6:4 | RESERVED | R/W | |
| 3:2 | JTHR | R/W | Jump brightness percentage threshold.<br>00 = 6.25%<br>01 = 12.5%<br>10 = 25%<br>11 = 50% |
| 1:0 | JVOLT | R/W | Typical Boost voltage jump size (10.26 mV/step)<br>00 = 195 steps (2 V)<br>01 = 390 steps (4 V)<br>10 = 585 steps (6 V)<br>11 = 780 steps (8 V) |

The jump feature operates outside of the normal adaptive headroom loop. Whenever the brightness percentage instantaneously increases above the configured threshold the boost voltage is instructed to immediately jump up. This can be used in some rare cases where extremely fast boost reaction time to brightness changes is needed. The JTHR field configures the threshold and the JVOLT field configures the voltage increase. The requested boost voltage will never exceed the value set by the VOLTAGE.VMAX field.

# 9 Application and Implementation

## 9.1 Application Information

The LP8555 designed for LCD backlighting, especially for high-resolution tablet panels where more backlight power is needed due to smaller aperture ratio of the LCD. With single-boost configuration the inductor selection is difficult for height restricted applications; to overcome this LP8555 uses dual-boost configuration. This shares the total load to two boost inductors and allows using two smaller inductors instead of one large inductor while maintaining good efficiency. 12 LED current sinks allow driving up to 96 LEDs with high efficiency. Better efficiency is achieved with using lower conversion ratio for boost and driving more LEDs in parallel, compared to using fewer LED strings and higher boost conversion ratio. Main limiting factor for output power is inductor current limit, which is calculated in the Detailed Design Procedure. PCB thermal performance must be considered in high power applications where thermal dissipation of LP8555 can become limiting factor.

Due to a flexible input voltage configuration, the LP8555 can be used also in various other applications, such as laptop backlighting, as well as other LED lighting where high number of LEDs are needed and must be driven with highest possible efficiency. The following design procedure can be used to select component values for the LP8555. An example for default EPROM configuration is given with corresponding design parameters. LP8555EVM User Guide has reference bill of materials and example layout pictures.

## 9.2 Typical Applications

### 9.2.1 Application for Default LP8555YFQR EPROM Configuration

With the default EPROM configuration PWM input is used for brightness control. The backlight is enabled/disabled and also configuration can be changed before backlight turning on with I$^2$C writes. Up to 12 LED strings can be used with max 28-V boost output voltage. LED current is set to 25 mA by default. See detailed EPROM setup in LP8555YFQR EPROM Configuration.

#### 9.2.1.1 Schematic

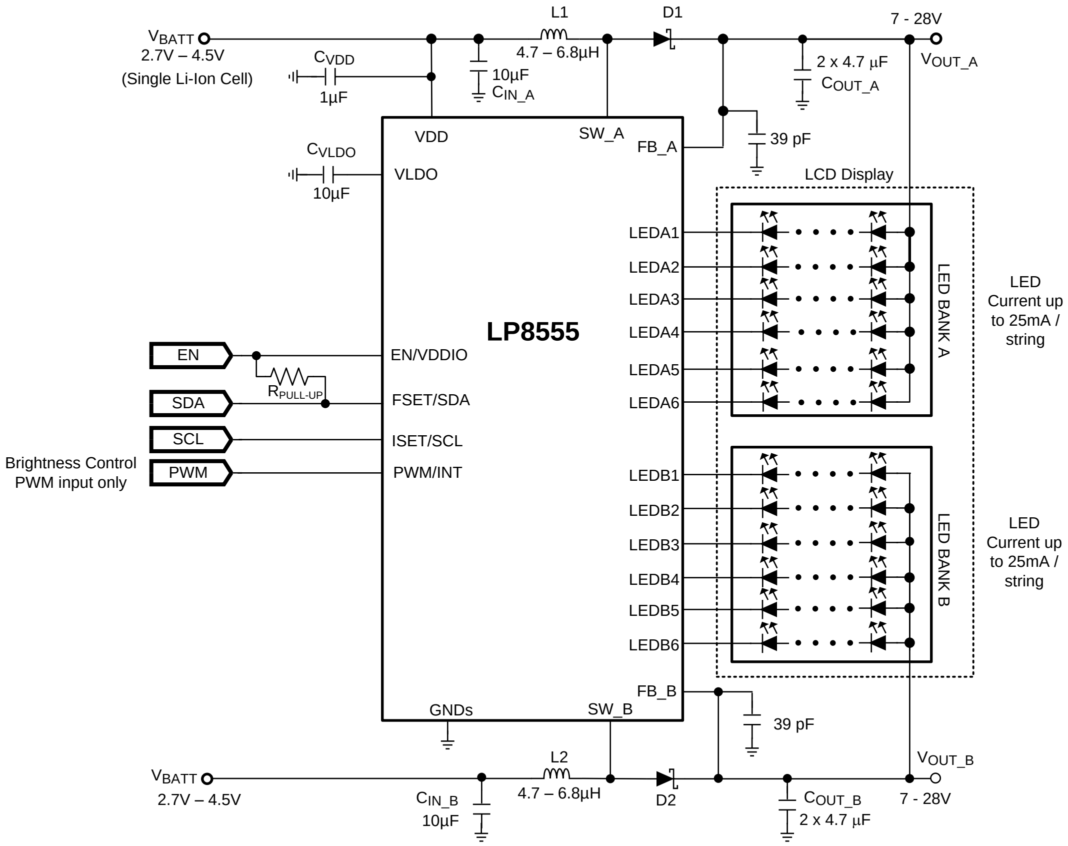


**Figure 43. Application Diagram for Default EPROM Setup**

## Typical Applications (continued)

### 9.2.1.2 LP8555YFQR EPROM Configuration

| ADDRESS (HEX) | BIT | BIT NAME | BIT DESCRIPTION | VALUE | MEANING | REG VALUE (HEX) |
|---|---|---|---|---|---|---|
| 00 | 2 | SREN | Boost slew rate limit enable | 0b | 0 = Boost slew rate not limited | 00 |
| | 1 | SSEN | Spread spectrum enable | 0b | 0 = Spread spectrum disabled | |
| | 0 | ON | Backlight enable | 0b | 0 = Backlight enabled only by writing this bit to 1 | |
| 10 | 7 | PWMSB | Enable automatic PWM input shutdown | 0b | 0 = Shutdown function disabled | 64 |
| | 6 | PWMFILT | Enable PWM input filtering | 1b | 1 = PWM input analog 50 ns filter enabled | |
| | 5 | EN_BPHASE180 | Enable boost 180° phase difference | 1b | 1 = Boosts clocks are 180° shifted | |
| | 4 | - | | 0b | | |
| | 3 | RELOAD | Enable EPROM read at every BL enable sequence | 0b | 0 = EPROM is read only at first start-up | |
| | 2 | AUTO | Enable auto detect for number of LEDs during start-up | 1b | 1 = LED string auto detection enabled | |
| | 1:0 | BRTMODE | Brightness control mode | 00b | 00 = PWM input duty control only | |
| 11 | 7 | ISET | Enable external resistor setting of LED string current | 0b | 0 = LED current set with registers | 05 |
| | 6:3 | - | | 0000b | | |
| | 2:0 | MAXCURR | Set maximum DC current per string | 101b | 101 = 25 mA | |
| 12 | 7 | PFSET | Enable external resistor PWM frequency setting | 0b | 0 = PWM frequency selected with registers | 2B |
| | 6 | - | | 0b | | |
| | 5:3 | THRESHOLD | Hybrid PMW and Current Control switch point control | 101b | 101 = 25% switch point | |
| | 2:0 | PFSET | PWM frequency selection | 011b | 011 = 19.5 kHz | |
| 13 | 7 | - | | 0b | | 01 |
| | 6 | - | | 0b | | |
| | 5:2 | - | | 0000b | | |
| | 1 | BIND | Boost inductor selection | 0b | 0 = 4.7 µH ... 6.8 µH inductor | |
| | 0 | BFREQ | Boost SW frequency | 1b | 1 = 1 MHz | |
| 14 | 7:6 | OV | Set LED high comparator detection level | 10b | 10 = 3 V | BF |
| | 5:0 | ENABLE_0 | LED bank A string enable | 111111b | 1 = Enabled (all six strings) | |
| 15 | 7:6 | SMOOTH | Advanced Sloping smoothing factor | 00b | 00 = No smoothing | 20 |
| | 5:3 | PWM_IN_HYST | PWM input hysteresis | 100b | 100 = >8 LSB steps | |
| | 2:0 | STEP | Linear Slope time | 000b | 000 = 0ms | |
| 16 | 7:6 | VMAX_0 | Bank A boost maximum voltage | 11b | 11 = 28 V | F8 |
| | 5 | ADAPT_0 | Enable boost adaptive control for bank A | 1b | 1 = Adaptive headroom enabled | |
| | 4:0 | VINIT_0 | Initial voltage for bank A boost | 11000b | 11000 = 23.26 V | |
| 19 | 5:0 | ENABLE_1 | LED bank B string enable | 111111b | 1 = Enabled (all six strings) | 3F |
| 1A | 7 | VMAX_1 | Bank B boost maximum voltage | 11b | 11 = 28 V | F8 |
| | 6 | ADAPT_1 | Enable boost adaptive control for bank B | 1b | 1 = Adaptive headroom enabled | |
| | 5 | VINIT_1 | Initial voltage for bank B boost | 11000b | 11000 = 23.26 V | |
| 1E | 7:4 | ID_CUST | ID register, Customer ID | 0000b | 0000 | 00 |
| | 3:0 | ID_CFG | ID register, EPROM config | 0000b | 0000 | |
| 76 | 7 | BOOST_IS_DIV2 | Option divide Imax peak current by 2 | 0b | 0 = Normal current limit | 0B |
| | 6:5 | - | | 00b | | |
| | 4 | ALTID | I2C slave ID selector | 0b | 0 = 2Ch (7-bit) | |
| | 3:2 | SRON | Slowed boost slew rate | 10b | When COMMAND.SREN is set to 1 this value is used.<br>10 = Second slowest | |
| | 1:0 | CURR_LIMIT | Inductor peak current limit | 11b | 11 = 3.1 A | |

## Typical Applications (continued)

| ADDRESS (HEX) | BIT | BIT NAME | BIT DESCRIPTION | VALUE | MEANING | REG VALUE (HEX) |
|---|---|---|---|---|---|---|
| 77 | 7:6 | FMOD_DIV | Spread spectrum modulation frequency divisor | 00b | When COMMAND.SSEN is set to 1 this value is used.<br>00 = 0.42% | 17 |
|  | 5:0 | - |  | 010111b |  |  |
| 78 | 6:4 | VHR_SLOPE | LED driver maximum headroom voltage at maximum current (50mA) | 110b | 110 = 285 mV | 60 |
|  | 3 | - |  | 0b |  |  |
|  | 2:0 | VHR_VERT | LED driver maximum headroom voltage at minimum current | 000b | 000 = 50 mV |  |
| 79 | 5:4 | VHR_HYST | LED driver hysteresis for mid comparator level | 01b | 01 = 233 mV | 11 |
|  | 3:2 | - |  | 00b |  |  |
|  | 1:0 | VHR_HORZ | LED driver headroom control knee percentage of full LED current | 01b | 01 = 25% |  |
| 7A | 7 | JEN | Enable boost voltage jumping on brightness change | 1b | 1 = Jump enabled | 88 |
|  | 6:4 | - |  | 000b |  |  |
|  | 3:2 | JTHR | Jump brightness threshold | 10b | 10 = 25% |  |
|  | 1:0 | JVOLT | Jump voltage | 00b | 00 = 2 V |  |

### *9.2.1.3 Design Requirements*

Example requirements based on default EPROM setup.

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 2.7 V to 4.5 V (Single Li-Ion cell battery) |
| Brightness Control | PWM input duty cycle |
| Backlight enabled | Writing ON bit 1 with I$^2$C |
| PWM output frequency | 19.2 kHz with PSPWM enabled |
| LED Current | 25 mA / channel |
| Number of Channels | Up to 12 with string auto detection enabled |
| Brightness slopes | Disabled |
| External set resistors | Disabled |
| Inductor | 4.7 µH to 6.8 µH, at least 3.1-A saturation current |
| Boost SW frequency | 1 MHz |
| Maximum output voltage | 28 V |
| SW current limit | 3.1 A |
| CABC | Jump enabled for >25% brightness changes |

### 9.2.1.4 Detailed Design Procedure

#### 9.2.1.4.1 Inductor

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and should be preferred.

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current.

Figure 44 shows the worst case conditions.

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \text{ x } L \text{ x } f)} \text{ x } \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \quad \text{and } D' = (1 - D)$$

**Figure 44. Calculating Inductor Maximum Current**

- $I_{RIPPLE}$: peak inductor current
- $I_{OUTMAX}$: maximum load current
- $V_{IN}$: minimum input voltage in application
- L : min inductor value including worst case tolerances
- f : minimum switching frequency
- $V_{OUT}$: output voltage
- D: Duty Cycle for CCM Operation
- $V_{OUT}$ : Output Voltage

As a result the inductor should be selected according to the $I_{SAT}$. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 3.1 A. A 4.7-µH to 6.8-µH inductor with a saturation current rating of at least 3.1 A is recommended for most applications. The inductor's resistance should be less than 300 mΩ for good efficiency.

#### 9.2.1.4.2 Output Capacitor

A ceramic capacitor with 50-V voltage rating is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80% especially with small package size capacitors, which needs to be considered in capacitance value and package selection. Typically one 10-µF or two 4.7-µF capacitors is sufficient. Effectively the capacitance should be at least 2 µF at boost maximum output voltage.

#### 9.2.1.4.3 LDO Capacitor

A ceramic capacitor with at least 10 V voltage rating is recommended for the output capacitor of the LDO. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Typically 10 µF capacitor is sufficient.

#### 9.2.1.4.4 VDD Capacitor

A ceramic capacitor with at least 10-V voltage rating is recommended for the VDD input capacitor. If input voltage is higher, then the rating should be selected accordingly. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Typically, a 1-µF capacitor is sufficient. X5R/X7R are recommended types.

#### 9.2.1.4.5 Boost Input Capacitor

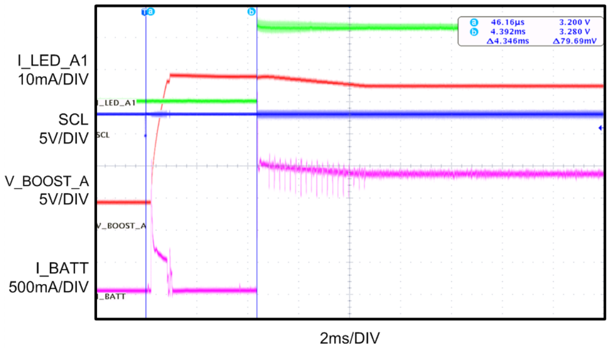
A ceramic capacitor with at least 10-V voltage rating is recommended for the boost input capacitor. If input voltage is higher, then the rating should be selected accordingly. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Typically, a 10-µF capacitor per boost is sufficient. X5R/X7R are recommended types.

#### 9.2.1.4.6 Diode

A Schottky diode should be used for the output diode. Peak repetitive current should be greater than inductor peak current (3.1 A) to ensure reliable operation. Average current rating should be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown voltage of the Schottky diode significantly larger (~40 V) than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

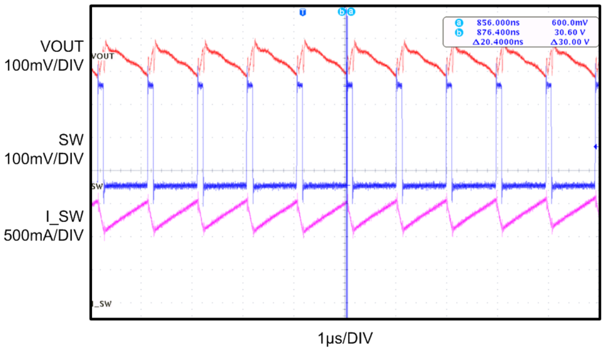
### 9.2.1.5 Application Performance Plots

Typical performance plots with default EPROM configuration. The LP8555EVM was used for taking the oscilloscope plots.



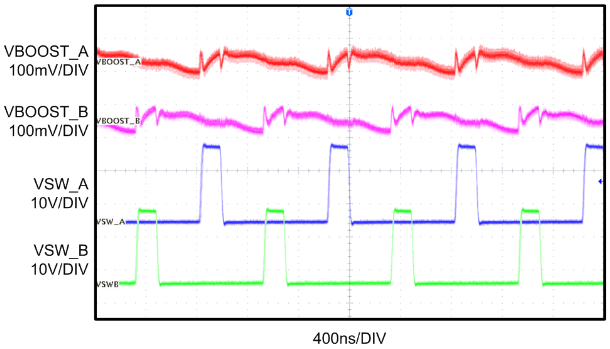
VDD = 3.7V $I_{LED}$ = 25 mA 12 x 7 LEDs

**Figure 45. Start-up Waveform with I$^2$C Write Full Brightness Slope Function Disabled.**



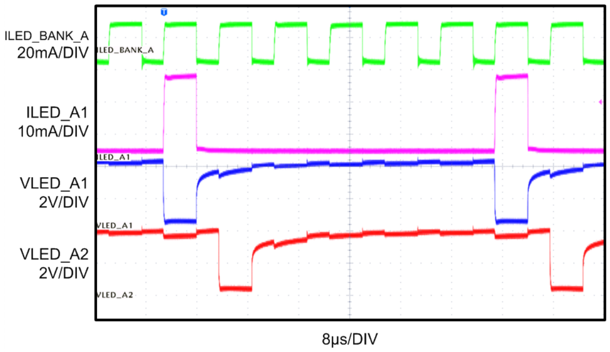
VDD = 3.7V $V_{BOOST}$ = 28V Load = 150 mA

**Figure 46. Typical Boost Waveform, Boost A**



VDD = 3.7V $f_{SW}$ = 1 MHz

**Figure 47. 180° Phase Difference Between Boost A and B**



$f_{PWM}$ = 19.5 kHz 6 Strings

**Figure 48. Typical LED Current and Voltage Waveforms.**

### 9.2.2 Application Example With Different LED Configuration for Each Bank

In the following example schematic it is shown how the LED banks can have different LED configuration. Bank A has 4 active LED outputs and Bank B has 5 active LED outputs. LP8555 will automatically detect open outputs and adjust phase shifting for both banks optimally. Control in this example is from I$^2$C bus and PWM/INT terminal is used for interrupt signal, notifying processor on possible fault conditions. Component selection and performance plots follow the examples shown in first application example with default EPROM configuration, but the PSPWM is adjusted based on the number of connected strings. Details on I$^2$C registers and EPROM settings are seen in the Register Map section. If custom EPROM is required, please contact TI Sales representative for availability.

#### *9.2.2.1 Schematic*

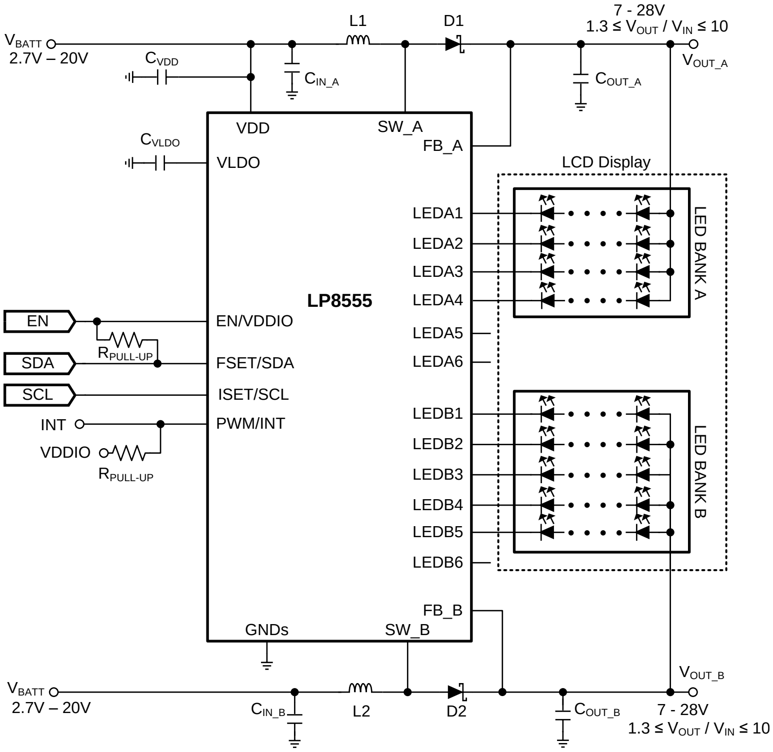


**Figure 49. Application Example With Different LED Configurations on Each Bank**

### 9.2.3 Application Example With 12 LED Strings and PWM Input Brightness Control

In the following example schematic it is shown how the LP8555 can be configured for operating without I$^2$C control. Only controls needed are PWM input for brightness control and EN for enabling and disabling device. PWM frequency is set with $R_{FSET}$ resistor and LED current is set with $I_{SET}$ resistor. Full 12 channels are used in this example, but other configurations can be used as well. Component selection and performance plots follow the examples shown in first application example with default EPROM configuration. Details on I$^2$C registers and EPROM settings are seen in the Register Map section. If custom EPROM is required, please contact TI Sales representative for availability. Since this configuration relies on pre-programmed EPROM for basic setup (although LED current and PWM frequency are set with resistors), special EPROM configuration is needed for this application.

#### *9.2.3.1 Schematic*

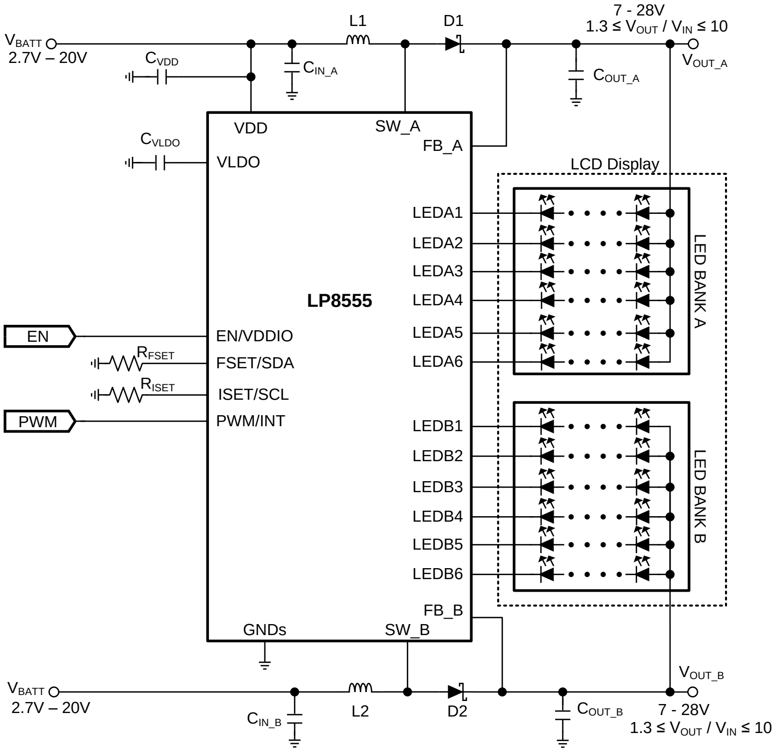


**Figure 50. Application Example with 12 LED Strings and PWM Input Brightness Control**

### 9.2.4 Application With 12 LED Strings, I$^2$C Brightness Control

In the following example full 12 channels are used with I$^2$C brightness control. PWM/INT terminal is used for interrupt signal, notifying processor on possible fault conditions. LED current and PWM frequency are set with I$^2$C writes, or default EPROM values can be used as well. Component selection and performance plots follow the examples shown in first application example with default EPROM configuration. Configuration registers can be set before backlight is enabled, so special pre-set EPROM is not necessarily needed. Details on I$^2$C registers and EPROM settings are seen in the Register Map section. If custom EPROM is required, please contact TI Sales representative for availability.

#### *9.2.4.1 Schematic*

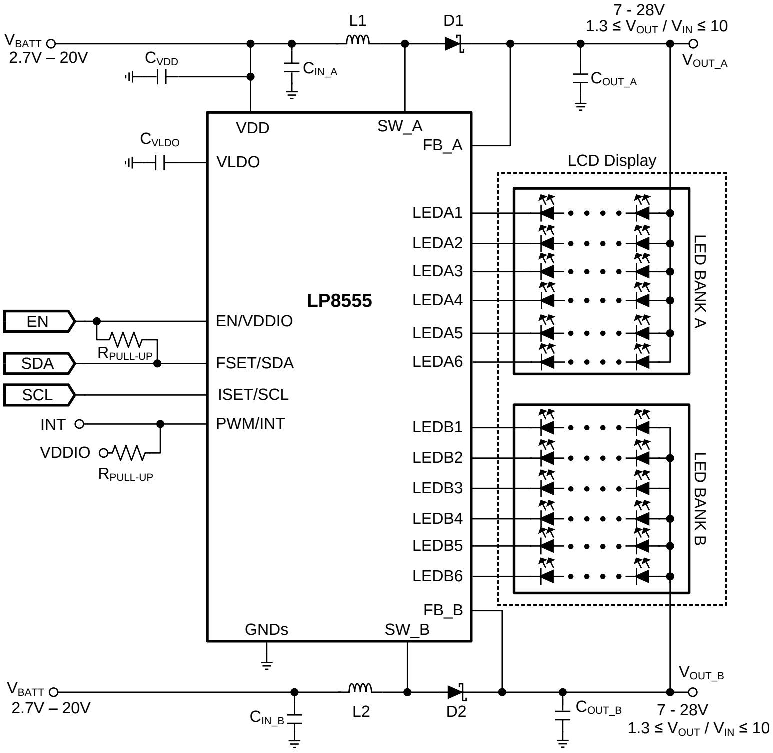


**Figure 51. Application Example With 12 LED Strings, I$^2$C Brightness Control**

# 10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V and 20 V. This input supply should be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition (start-up or rapid brightness change). The resistance of the input supply rail should be low enough that the input current transient does not cause drop high enough in the LP8555 supply voltage that can cause false UVLO fault triggering.

If the input supply is located more than a few inches from the LP8555 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. Depending on device EPROM configuration and usage case the boost converter is configured to operate optimally with certain input voltage range. Examples are seen in the Detailed Design Procedures. In uncertain cases, it is recommended to contact TI Sales Representative for confirmation of the compatibility of the use case, EPROM configuration and input voltage range.

# 11 Layout

## 11.1 Layout Guidelines

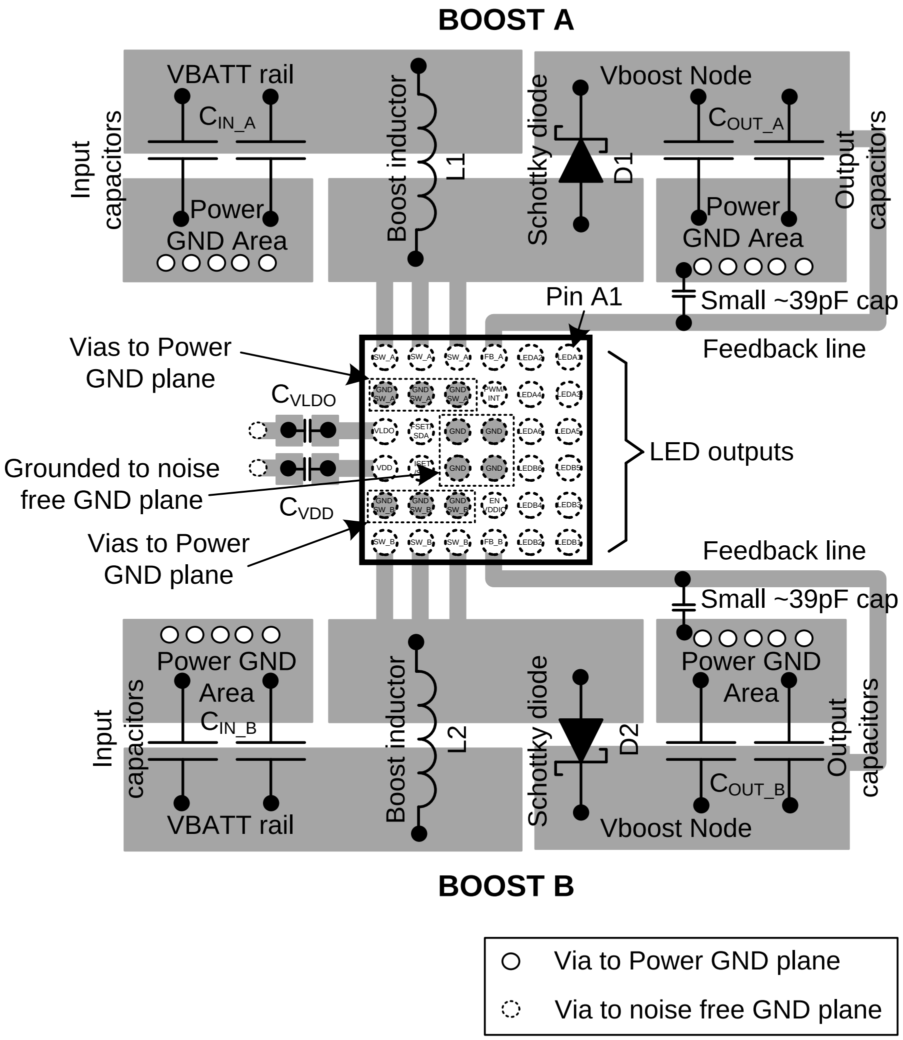
In Layout Example is a layout recommendation for LP8555. The figure is used for demonstrating the principle of good layout. This layout can be adapted to the actual application layout if/where possible.

It is important that all boost components are close to the chip and the high current traces should be wide enough. By placing one boost component on one side of the chip it is easy to keep the ground plane intact below the high current paths. This way other chip terminals can be routed more easily without splitting the ground plane. VDD and VLDO need to be as noise-free as possible. Place the bypass capacitors near the corresponding terminals and ground them to as noise-free ground as possible.

Here are some main points to help the PCB layout work:

- Current loops need to be minimized:
  - For low frequency the minimal current loop can be achieved by placing the boost components as close to the SW and SW_GND terminals as possible. Input and output capacitor grounds need to be close to each other to minimize current loop size.
  - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High frequency return currents try to find route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the “positive” current route in the ground plane, if the ground plane is intact under the route. Traces from inner pads of the LP8555 need to be routed from below the part in the inner layer so that traces do not split the ground plane under the boost traces or components.
- GND plane needs to be intact under the high current boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
- Current loops when the boost switch is conducting and not conducting needs to be on the same direction in optimal case.
- Inductor placement should be so that the current flows in the same direction as in the current loops. Rotating inductor 180° changes current direction.
- Use separate power and noise free grounds. Power ground is used for boost converter return current and noise free ground for more sensitive signals, like VDD and VLDO bypass capacitor grounding as well as grounding the GND terminals of LP8555 itself.
- Boost output feedback voltage to LEDs need to be taken out “after” the output capacitors, not straight from the diode cathode.
- A small (for example, 39 pF) bypass capacitor should be placed close to the FB terminal(s) to suppress high frequency noise
- VDD line should be separated from the high current supply path to the boost converter(s) to prevent high frequency ripple affecting the chip behavior. A separate 1-µF bypass capacitor is used for the VDD terminal, and it is grounded to noise-free ground.
- Input and output capacitors need strong grounding (wide traces, many vias to GND plane)
- If two output capacitors are used they need symmetrical layout to get both capacitors working ideally
- Output capacitors DC-bias effect. If the output capacitance is too low, it can cause boost to become instable on some loads and this increases EMI. DC bias characteristics need to be obtained from the component manufacturer; it is not taken into account on component tolerance. X5R/X7R capacitors are recommended.

## 11.2 Layout Example



# 12 Device and Documentation Support

## 12.1 Trademarks

All trademarks are the property of their respective owners.

## 12.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and revision of this document

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP8555YFQR | ACTIVE | DSBGA | YFQ | 36 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 8555 | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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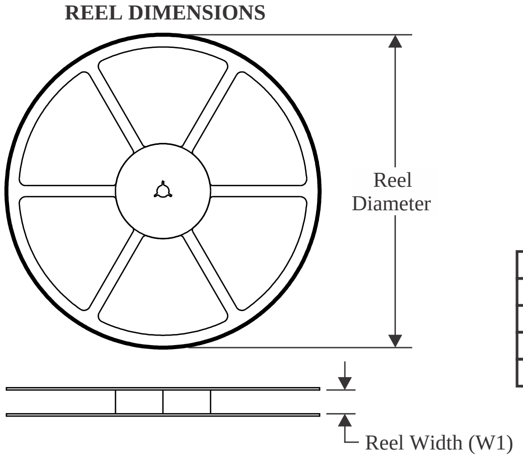
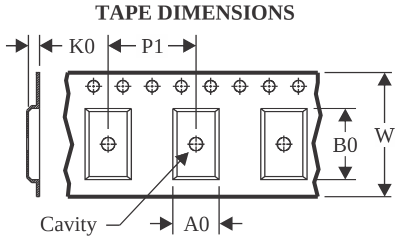
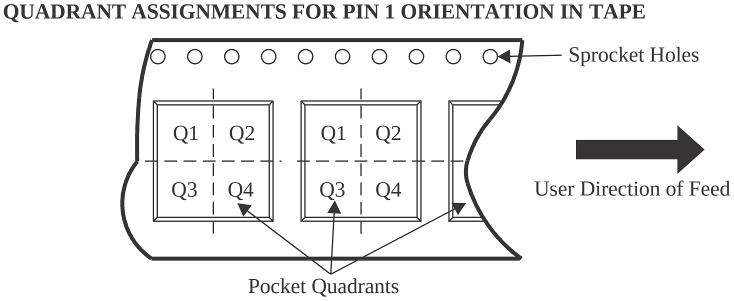
## TAPE AND REEL INFORMATION





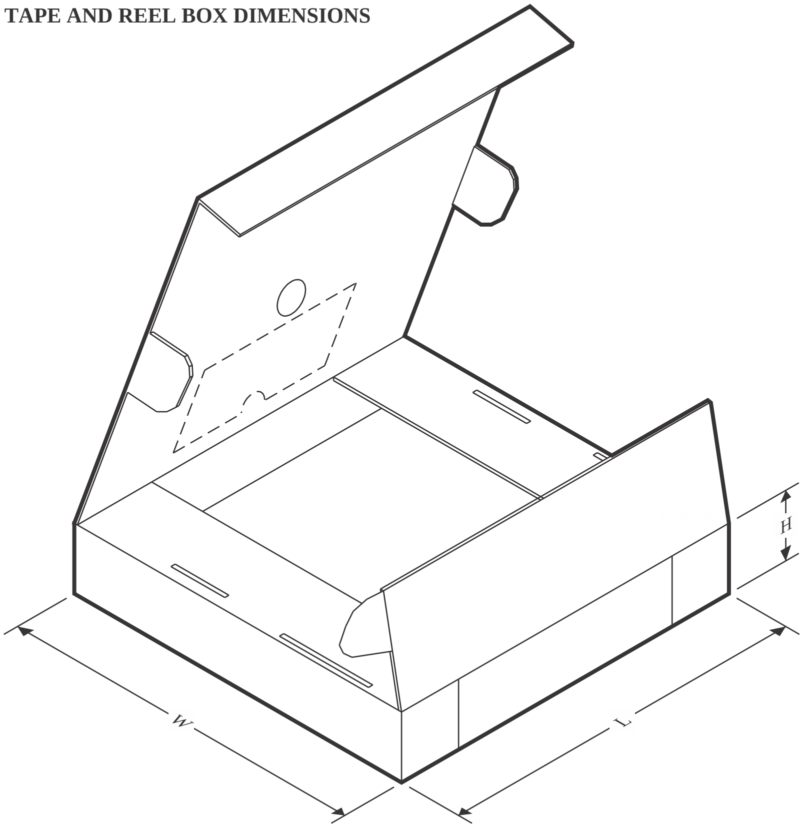
| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP8555YFQR | DSBGA | YFQ | 36 | 3000 | 178.0 | 8.4 | 2.69 | 2.69 | 0.76 | 4.0 | 8.0 | Q1 |

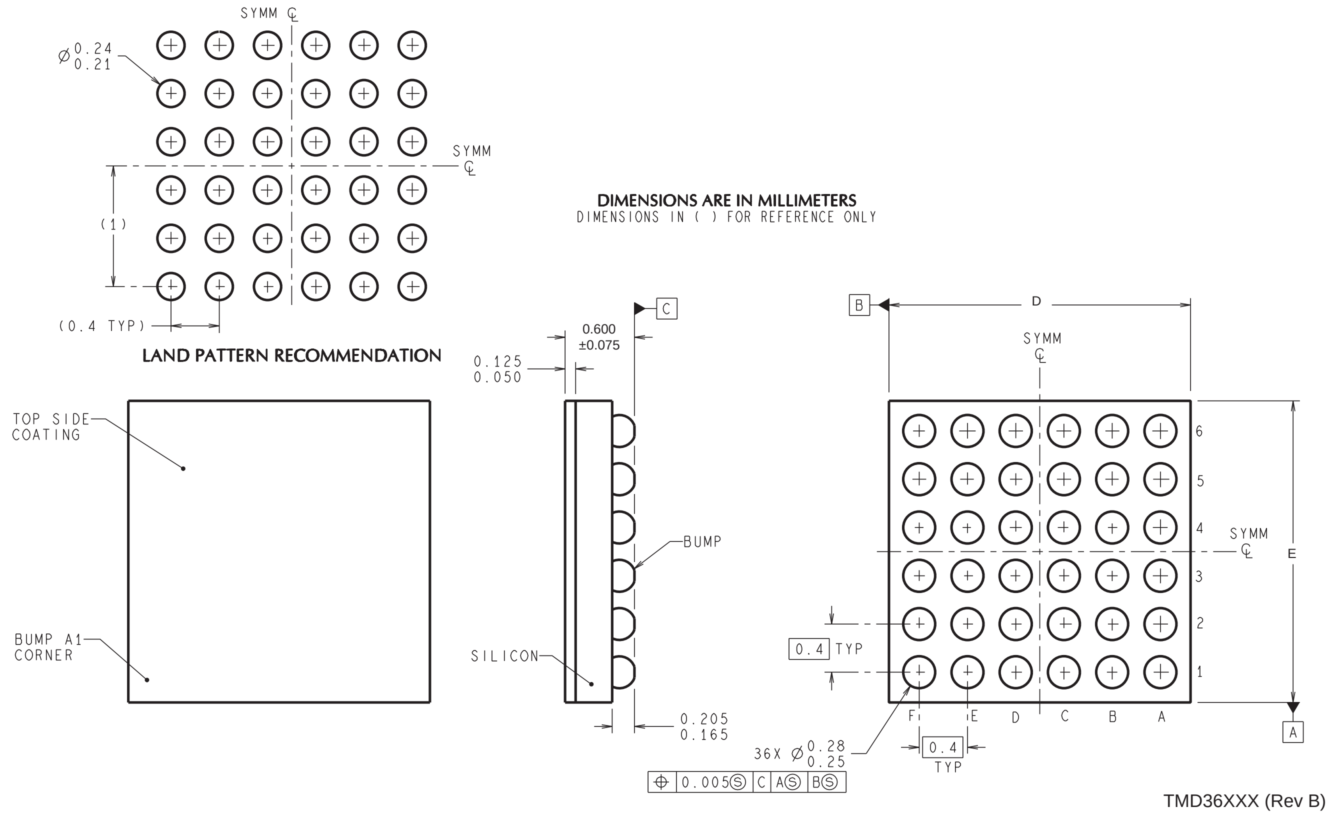
## TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP8555YFQR | DSBGA | YFQ | 36 | 3000 | 208.0 | 191.0 | 35.0 |

# YFQ0036



D: Max = 2.478 mm, Min =2.418 mm

E: Max = 2.478 mm, Min =2.418 mm

4215086/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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