

Integrated Power Supply Design for NXP i.MX8 QuadMax Processor



ABSTRACT

This application report describes a power solution and fully working development board integrating two TI PMICs, LP87564-Q1 (OPN LP87564TRNFRQ1) and TPS65917-Q1 (OPN O917A186TRGZRQ1), with the NXP™ i.MX 8QuadMax Application Processor. The hardware design also includes LPDDR4 SDRAM (6GB, x32-bit), Octal SPI NOR-Flash (64MB), 32GB eMMC, SD Card, and USB 2.0/CAN/M.2/Audio/Video interfaces. This design is intended for any project that is using the i.MX8QM processor.

Table of Contents

Features	2
Applications	2
1 Introduction	3
2 System Block Diagram	4
3 Board Components and Interfacing	5
3.1 Processor - i.MX8QuadMax.....	5
3.2 i.MX8QM - Memory Interfaces.....	7
3.3 LPDDR4 - MT53B768M32D4DT-062 AIT:B Interface.....	7
3.4 MT53B768M32D4DT-062 AIT:B 062.....	8
3.5 Ultra High Speed SD/SDIO/MMC Host Interface.....	10
3.6 SD Card Interface.....	10
3.7 Octal SPI flash - MT35XU512ABA1G12-0A Interface.....	10
3.8 USB Interfaces.....	11
3.9 Audio Codec - WM8960 Interface.....	12
3.10 1Gbps Ethernet Interface.....	13
3.11 USB Debug Interface.....	13
3.12 JTAG Interface.....	14
3.13 HDMI Port.....	15
3.14 LVDS, MIPI-CSI and MIPI-DSI Interface.....	15
3.15 M.2 E-Key for Wifi-Bluetooth Module.....	16
3.16 Processor I2C Interface.....	16
3.17 On-Board Sensors.....	17
3.18 Processor - UART Interfaces.....	18
3.19 Processor - I2S Interfaces.....	18
3.20 CAN Interface.....	18
3.21 Boot Device Selection.....	19
4 Reset Scheme	20
4.1 Reset Timing Parameters of i.MX8QM.....	20
4.2 WDOG Reset Timing Parameters of i.MX8QM.....	20
4.3 VCC_EXT_5V0 Generation.....	21
4.4 VCC_Buck_3V3 Generation.....	23
4.5 VCC_Buck_1V8 Generation.....	24
5 Power Scheme	26
5.1 Power Requirements for i.MX8QM.....	26
5.2 TI PMICs Interfacing.....	26
5.3 TI PMICs Power Tree and Sequencing.....	27
6 Clock Scheme	31
7 Design Files, Software, Documentation	32
7.1 Bill of Materials.....	32
8 Test Results	34

9 Summary	35
10 References	36

Trademarks

NXP™ is a trademark of NXP B.V.

ARM® and Cortex® are registered trademarks of Arm Limited.

All trademarks are the property of their respective owners.

Features

- Development of NXP i.MX8QM systems
- Low-power modes and DVFS supported
- Automated startup and shutdown sequencing for the PMIC power rails
- Flexible connectivity for memory, serial ports, ethernet, audio and video
- Selectable boot options (SD, eMMC, Octal SPI, Serial)

Applications

- [Automotive Infotainment and Cluster](#)
- [Engine Management](#)

1 Introduction

This document describes how to design and develop a hardware and software power solution for the i.MX8QM processor board. The main portion of the solution involves two TI PMICs (LP87564-Q1 and TPS65917-Q1) which support most of the features and interfacing. TI's load switch device TPS22965-Q1 is also used to source the 3.3V rail.

2 System Block Diagram

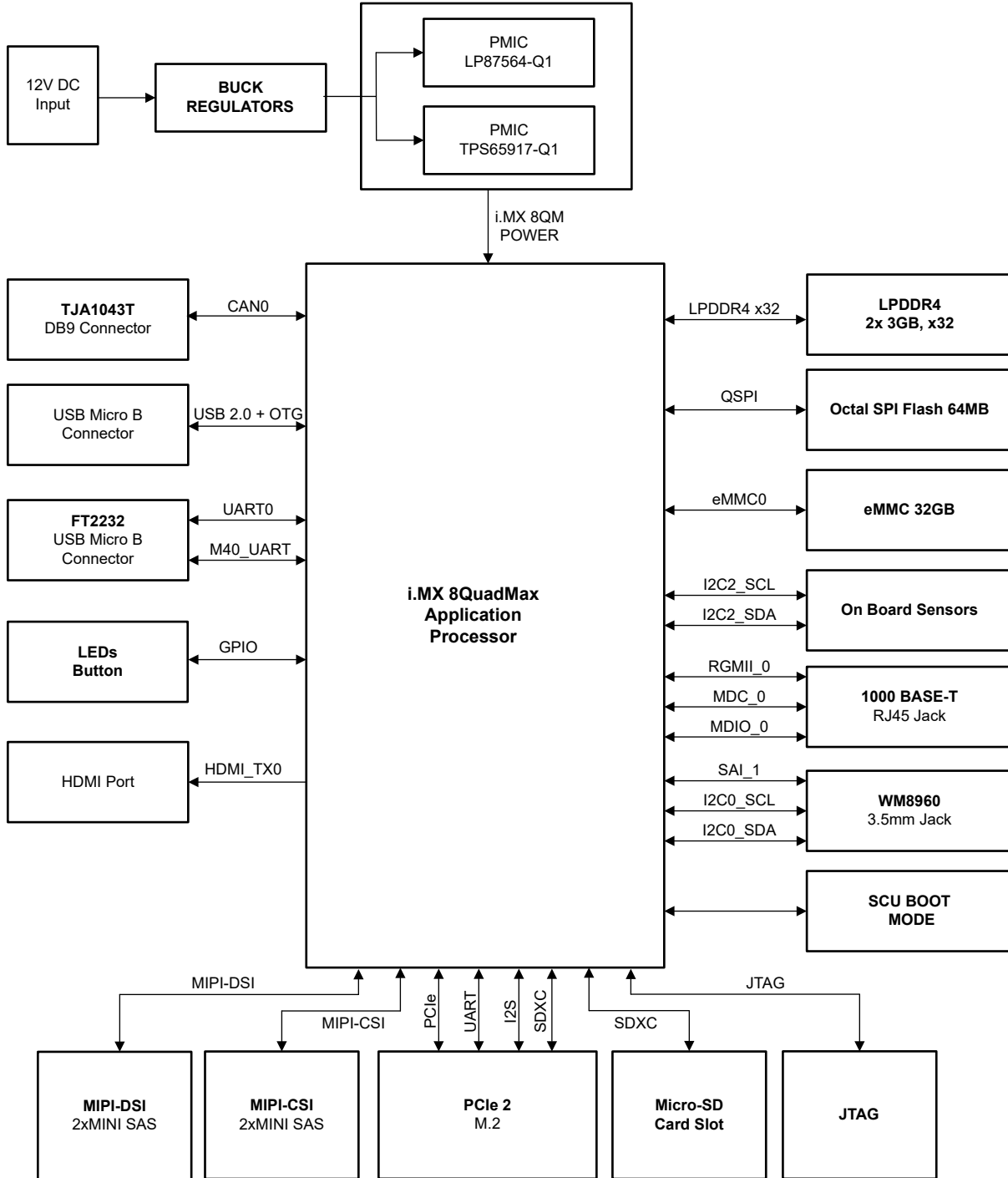


Figure 2-1. i.MX8QM Functional Block Diagram

3 Board Components and Interfacing

The i.MX8QM board consists of the following main components and their interfaces:

- Processor – i.MX8QM
- LPDDR4 - MT53B768M32D4DT-062 AIT:B
- eMMC - MTFC32GAKAEFF-AIT
- Octal SPI NOR flash – MT35XU512ABA1G12-0AATES
- Audio Codec – WM8960
- RGMII PHY – AR8031
- USB to serial converter – FT4232H
- M.2 Connector for WiFi and Bluetooth Module
- USB 2.0 OTG
- CAN Transceiver – TJA1043T

3.1 Processor - i.MX8QuadMax

The i.MX8 Family consists of three processors:

- i.MX8QuadMax
- i.MX8QuadPlus
- i.MX8Quad

The i.MX8QuadMax (i.MX8QM) processor consists of eight cores (4xARM® Cortex®-A53, 2xCortex-A72, 2xCortex-M4F), dual 32-core GPU subsystems, 4K H.265 capable VPU, and dual Failover-ready Display controllers. The i.MX8 family supports up to 2x4K display and includes multiple display output options such as MIPI-DSI, HDMI 2.0, eDP and LVDS. Memory interfaces supporting LPDDR-4, DDR4, Octal-SPI, eMMC, NAND and SD, and a wide range of peripheral I/Os such as PCIe 3.0 provide wide flexibility.

Description	Manufacturer	Part Number
IC, uP, i.MX8QM, ARM Cortex-A53, Cortex-A72, Cortex-M4F Processor, TFBGA-1313	NXP	PIMX8M6AVUDD1A

3.1.1 i.MX8QM - Features

Function	Features
1. Innovative multicore architecture	<ul style="list-style-type: none"> • Provides 4 Cortex-A53, 2 Cortex-A72 cores, and 2 Cortex-M4F cores • AArch64 for 64-bit support and new architectural features • AArch32 for full backward compatibility with ARMv7 • Integrated hardware virtualization capabilities • Cortex-M4F cores for real-time applications
2. Graphics processing unit (GPU)	<ul style="list-style-type: none"> • 16 Vec4 shaders with 64 execution units • Split GPU architecture allows for dual independent 8-Vec4 shader GPUs or a combined 16- Vec4 shader GPU. • Delivers up to 8x performance level of the i.MX 6 Series processors • Supports OpenGL 3.0, 2.1, OpenGL ES 3.2; Open GL ES 3.1 (with AEP); Open GL • ES 3.0, 2.0, and 1.1; OpenCL 1.2 FP and 1.1; OpenVG 1.1; and Vulkan • Supports OpenVX 1.0, 1.01, and 1.1 to provide enhanced vision image processing

Function	Features
3. Video processing unit (VPU)	<ul style="list-style-type: none"> • H.265 decode (4K) • H.264 decode (4K) • VP8 decode (1080p) • MPEG-2 decode (1080p) • RealVideo decode (1080p) • H.263 decode (1080p) • H.264 encode (1080p) • JPEG decoder and encoder (8×8 image size)
4. Memory	<ul style="list-style-type: none"> • 64-bit LPDDR4 @1600 MHz, DDR4 @1200 MHz • Dual Quad-SPI for fast boot from SPI NOR flash • SD 3.0 card interfaces • eMMC 5.1 • RAW NAND
5. Display controller	<ul style="list-style-type: none"> • Supports single Ultra HD 4K display or up to 4 independent Full HD 1080p displays • Up to 18 layer blending • Integrated failover path • Complementary 2D blitting engines and online warping functionality • SafeAssure Failover Capability to ensure display content stays valid even in event of a software failure
6. Display I/O	<ul style="list-style-type: none"> • 2 MIPI-DSI with 4-lanes each • HDMI 2.0a with HDCP 2.2 and 1.4 (Tx) • eDP 1.4/DP 1.2 (Tx) • 2 LVDS Tx with 2 channels each
7. Camera I/O and video	<ul style="list-style-type: none"> • 2 MIPI-CSI with 4-lanes each • HDMI 2.0 with HDCP 1.4 (Rx)1 • Imaging subsystem capable of bilinear scaling, color space conversion, and de-interlace
8. Security	<ul style="list-style-type: none"> • HABv4.2 secure and encrypted boot • NIST SP800-90A random number generator • RSA4096, ECDSA4096 • AES-128/256, DES, 3DES, ARC4, MD5, SHA-1, SHA-224/256 • Flashless SHE, Trustzone, RTIK • 4 tamper pins • DPA, voltage and temperature attacks • Zeroizable 32kB secure RAM

Function	Features
9. I/O	<ul style="list-style-type: none"> • PCIe 3.0 (2-lanes) can be used as two PCIe 3.0 controllers with one-lane, independent operation. • 1 USB3.0 with PHY • 2 USB2.0s (1 with PHY, 1 with HSIC) • SATA 3.0 • Controller • Dual Gb Ethernet with AVB • 8 UARTs: <ul style="list-style-type: none"> – 5 UARTs (2 with hardware flow control) – 2 UARTs tightly coupled with Cortex-M4Fcores (1 per Cortex-M4F core) • 19 I2C: <ul style="list-style-type: none"> – 2 primary I2C in MIPI-CSI (1 per instance) – 1 primary I2C in HDMI-RX • Dedicated I2C ports: • 4 SAI • ASRC • 1 SPDIF (Tx and Rx) • MPEG-2 Transport stream • Two 4-channel ADCs

3.2 i.MX8QM - Memory Interfaces

On the i.MX8QM processor board, the i.MX8QM processor is interfaced with the following memory devices:

- 6GB LPDDR4
- 32GB eMMC
- 64MB Octal SPI Flash
- SD interface

3.3 LPDDR4 - MT53B768M32D4DT-062 AIT:B Interface

The i.MX8QM has a dedicated DDR memory controller, which can support either DDR4 or LPDDR-4 memories. The i.MX8QM processor board is provided with 6GB (48Gb) DDR memory. MT53B768M32D4DT-062 LPDDR4 has 24Gb of memory and the board uses two LPDDR4 chips with each chip having a capacity of 3GB, thus, a total of 6GB SDRAM is available to the system. The memory interface consists of two channels, each having a 32 bit data bus.

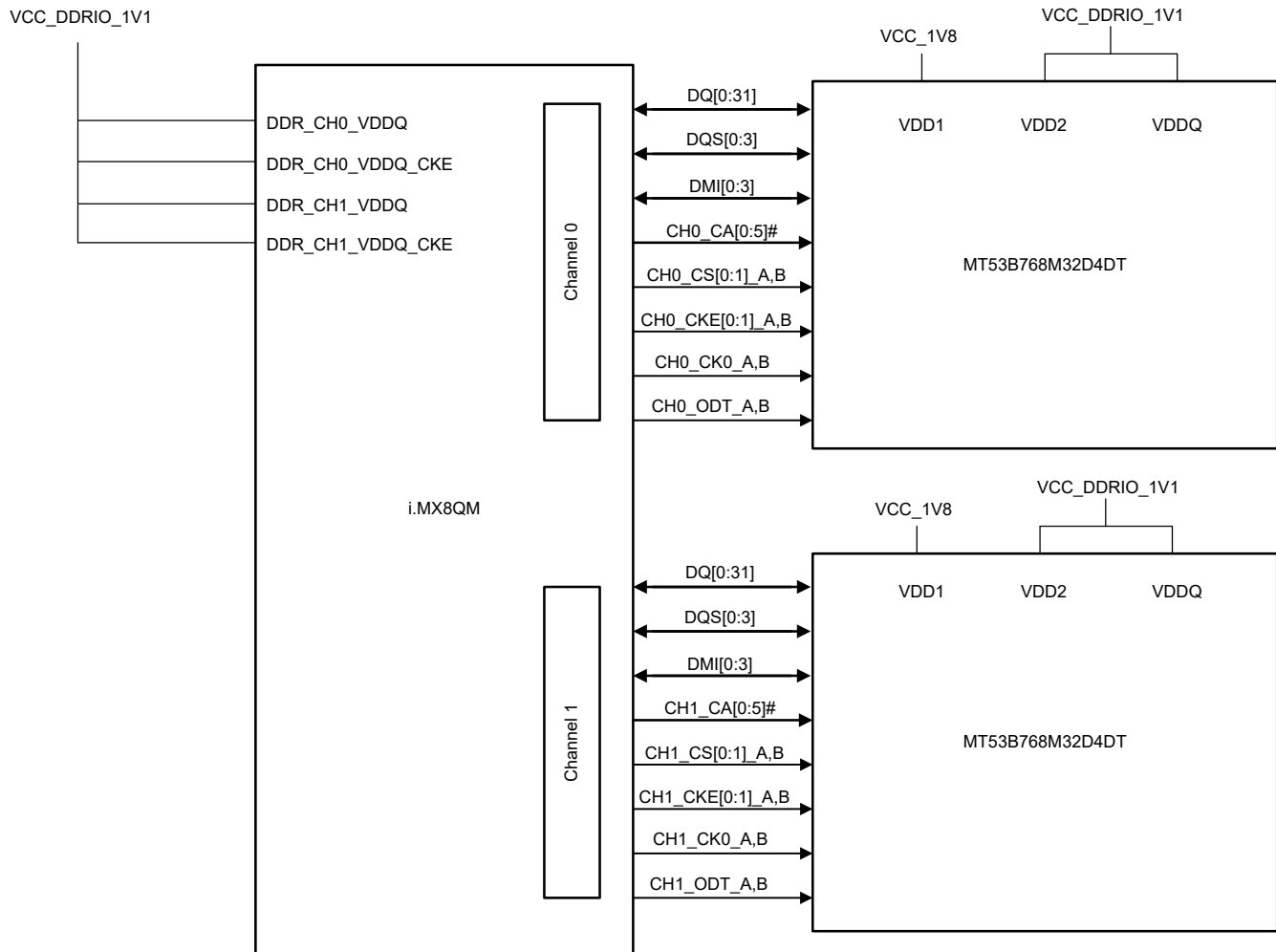


Figure 3-1. LPDDR4 Interface

Part Number	Density	Width	Package	Voltage
MT53B768M32D4DT-062 AIT:B	3GB	32-Bit	VFBGA-200	1V8

3.4 MT53B768M32D4DT-062 AIT:B 062

Features:

- Quad-Die, dual-channel package
- Ultra-low-voltage core and I/O power supplies
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Programmable READ and WRITE latencies (RL/WL)
- On-chip temperature sensor to control self-refresh rate
- Partial-array self-refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable VSS (ODT) termination

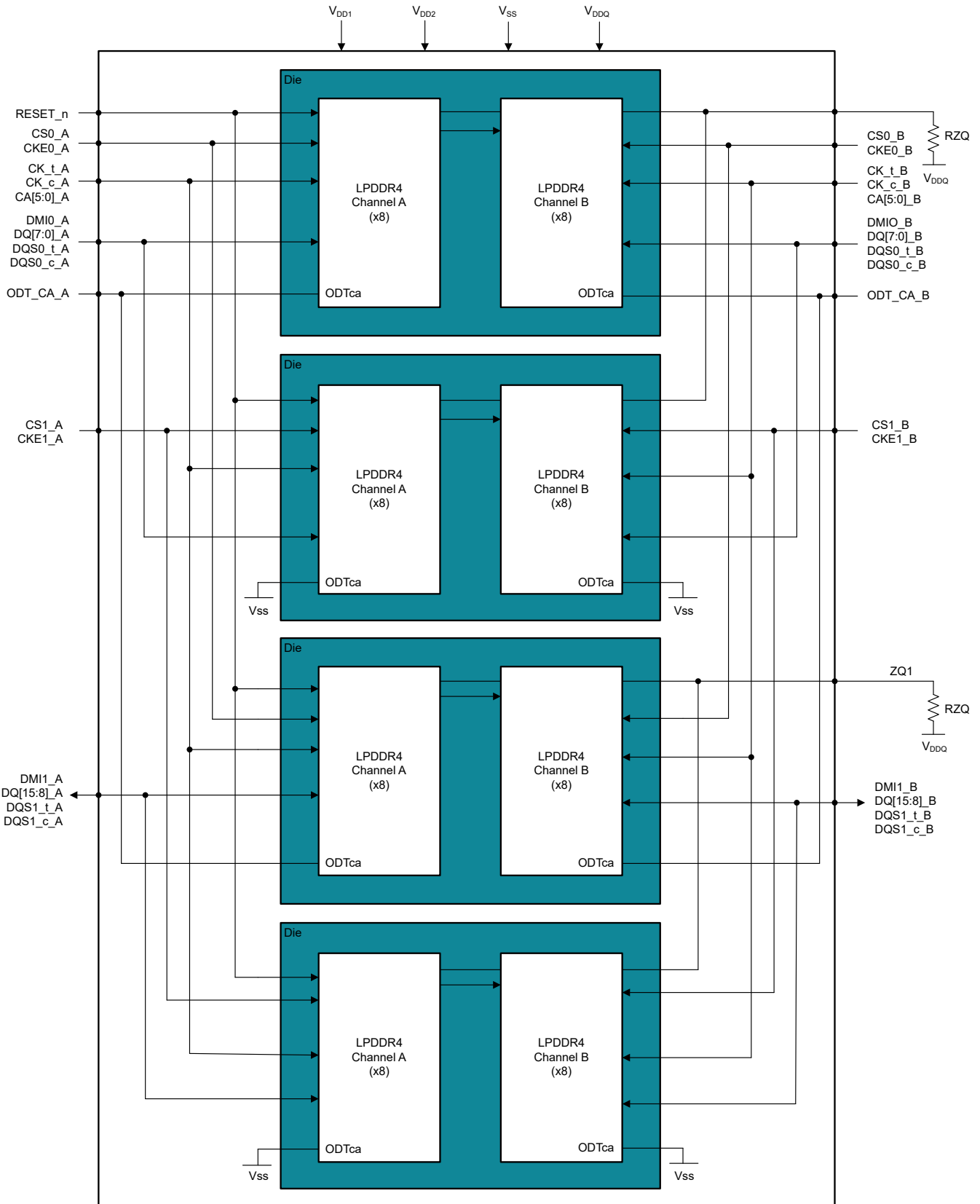


Figure 3-2. Quad-Die, Dual-Channel Package of LPDDR4

3.5 Ultra High Speed SD/SDIO/MMC Host Interface

This section describes the SD and eMMC5.0 interfaces. The board has one SDHC interface and one eMMC interface.

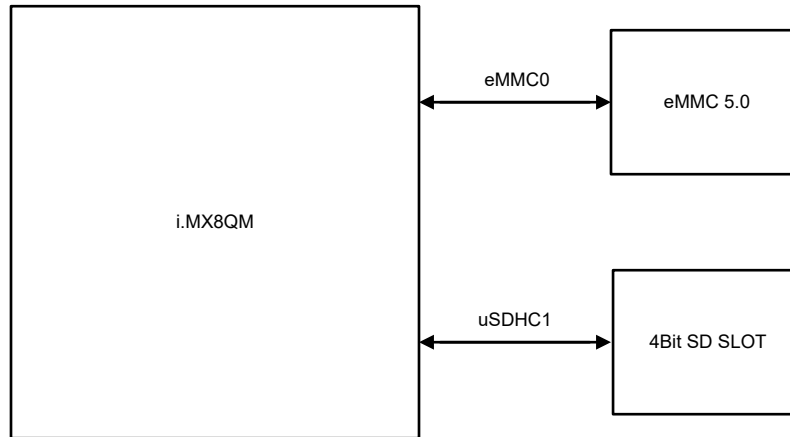


Figure 3-3. i.MX8QM uSDHC/MMC Interface

3.6 SD Card Interface

i.MX8QM processor board has an external SD slot which supports a 4 bit SDXC. The 4 bit SD card connector is interfaced with the USDHC2 port of iMX8. The interfacing of the SD card is shown in the below diagram:

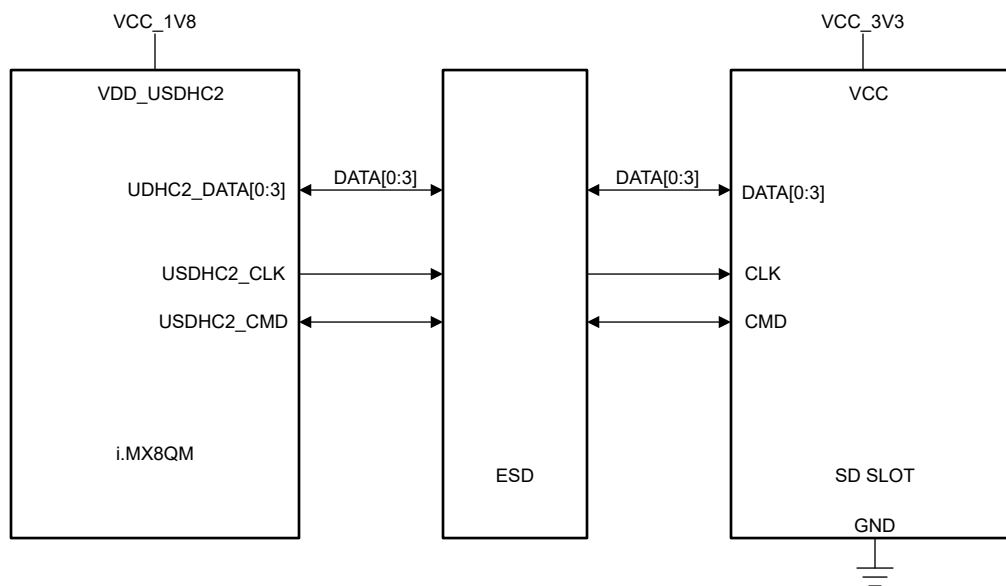


Figure 3-4. SD Card Interface

3.7 Octal SPI flash - MT35XU512ABA1G12-0A Interface

The i.MX8QM processor board has a 64MB Micron NOR flash memory (MT35XU512ABA1G12-0AATES) with an 8-bit data bus. The NOR flash memory is powered from a 1.8V power supply. The Octal SPI flash is connected to the QSPI0 interface of the i.MX8QM. The Micron MT35XU512ABA1G12 is a high-performance, multiple I/O, SPI-compatible flash memory device. This Micron memory device features a high-speed, low pin count Xccela bus interface with a DDR clock frequency of up to 200MHz for 1.8V parts and up to 133MHz for 3.0V parts. The Micron device also uses eight I/O signals and a data strobe (DQS pin). It is automotive grade but not AEC-Q100 qualified and has an operating temperature range from - 40°C to 105°C. The interfacing is shown below:

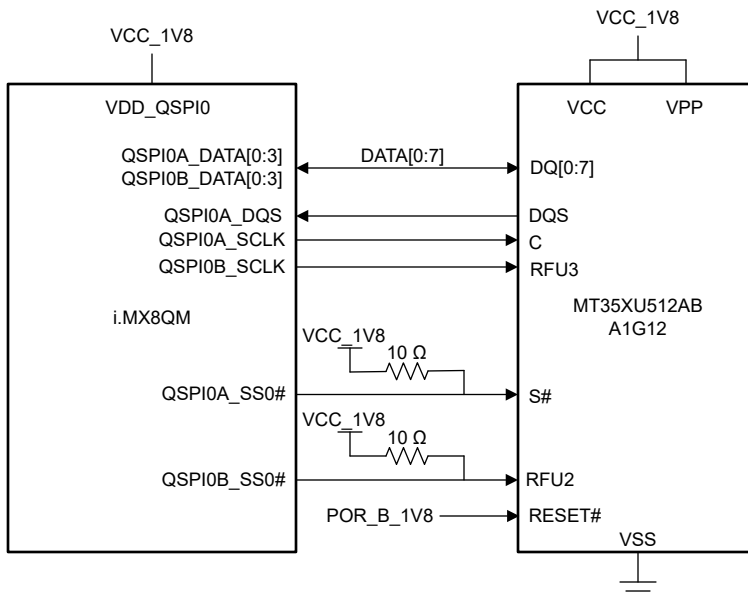


Figure 3-5. Octal SPI Flash Interface

Part Number	Density	Width	Package	Voltage
MT35XU512ABA1G12-0A	64MB	8-Bit	TPBGA-24	1.8

3.8 USB Interfaces

The i.MX8QM processor board has two USB 2.0 interfaces with OTG support. One of the USB 2.0 is terminated on a Micro USB connector and can be used to interface USB 2.0 devices. The other USB 2.0 lines are used in WIFI-BT M.2 E-Key interfacing.

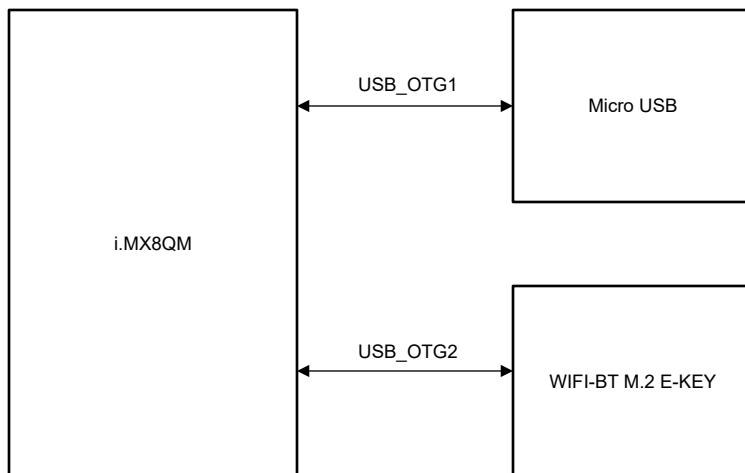
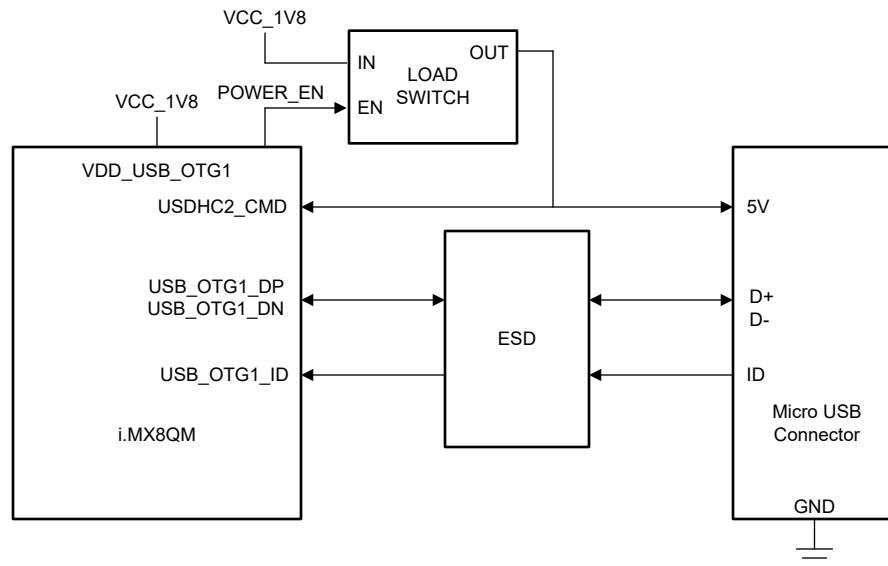


Figure 3-6. i.MX8 USB Interfaces

3.8.1 USB 2.0 OTG Interface

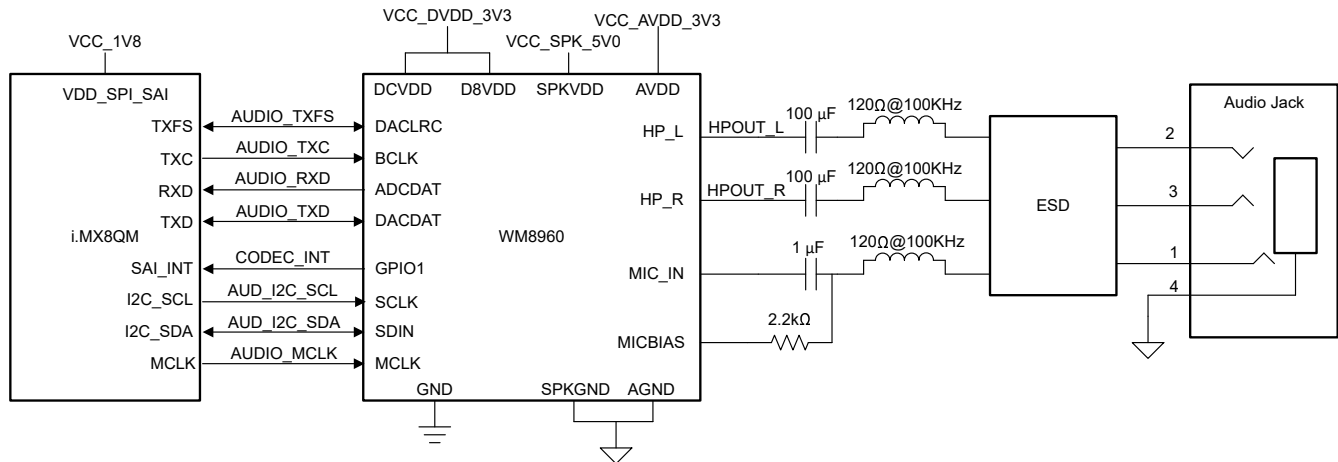
USB 2.0 signals are terminated to a Micro USB connector. The ID pin is connected to i.MX8QM for supporting OTG functionality. Common mode chokes and ESD protection diodes are provided in the USB signal path for better signal integrity. A load switch from Microchip Technology is used to deliver power to the connector with a current limit of 500mA in Host mode.


Figure 3-7. USB 2.0 OTG Interface

Description	Manufacturer	Part Number
Conn, USB Micro AB Receptacle, 1x1, RA, SMD	TBD	TBD
IC, MIC2026, 0.5A Current-Limited Power-Distribution Switch, SOIC-8	Microchip Technology	MIC2026-1YM
IC, PUSB3FR4, ESD Protection For USB Interface, WLCSP24	NXP	PUSB3FR4

3.9 Audio Codec - WM8960 Interface

The audio codec WM8960 is interfaced with the i.MX8QM using the serial audio interface, SAI1. The audio codec supports a headphone output and microphone input. The WM8960 is a low power, high quality stereo codec designed for portable digital audio applications.


Figure 3-8. Audio Codec Interface

Description	Manufacturer	Part Number
IC, WM8960, stereo audio codec, Class D, 1W,QFN-32	Cirrus Logic	WM8960CGEFL
TVS diode, bi-direction, 15kV, SMD	EPCOS	B72590D0050H160
Audio jack stereo, 3.5mm, 4 Pin, RA, SMD	CUI INC	SJ-43514-SMT

3.10 1Gbps Ethernet Interface

The i.MX8QM processor board is equipped with a RGMII PHY chip AR8031. The PHY chip is connected to the ENET0 interface of the i.MX8QM processor.

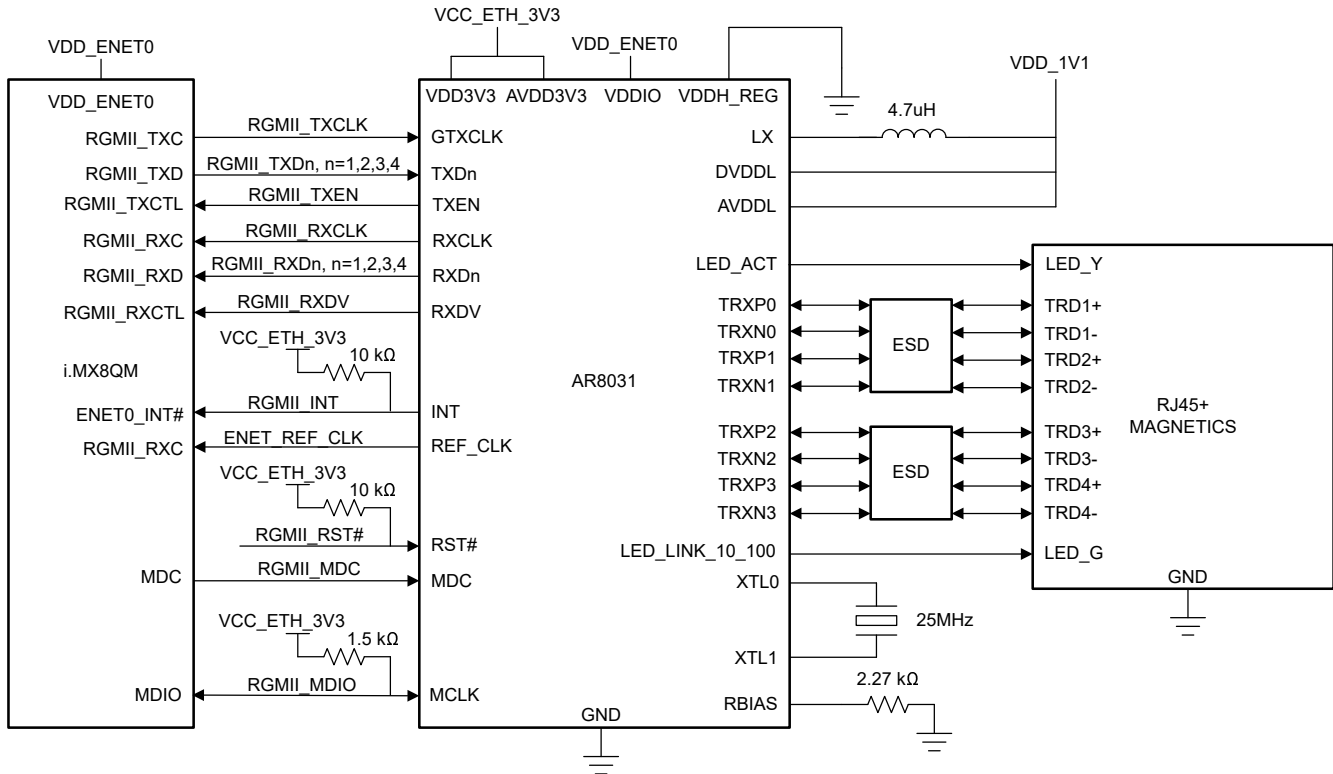


Figure 3-9. RGMII Interface

Description	Manufacturer	Part Number
IC, AR8031, Single Port, 1Gbps Ethernet PHY, QFN-48	ATHEROS	AR8031-AL1A
XTAL, 25MHz, 10pF, +/-10ppm, 5x3.2mm, SMD	ABRACON LLC	ABM3B25.000MHZ-10-1-U-T
Conn, RJ45 Jack with Magnetics, 1x1, Shielded, 1000 BaseT, LED(Y, G), RA, TH	STEWART CONNECTOR	SI-61001-F
TVS Diode, Uni-direction, 30kV, DFN-10	NXP	IP4238CZ10

3.11 USB Debug Interface

A micro USB connector is provided for debug. The USB serial converter IC, FT4232 from FTDI, is used to convert the i.MX8QM UART interface to USB. FT4232 is a single chip USB to four channel UART bridge IC and it is configured in bus powered mode.

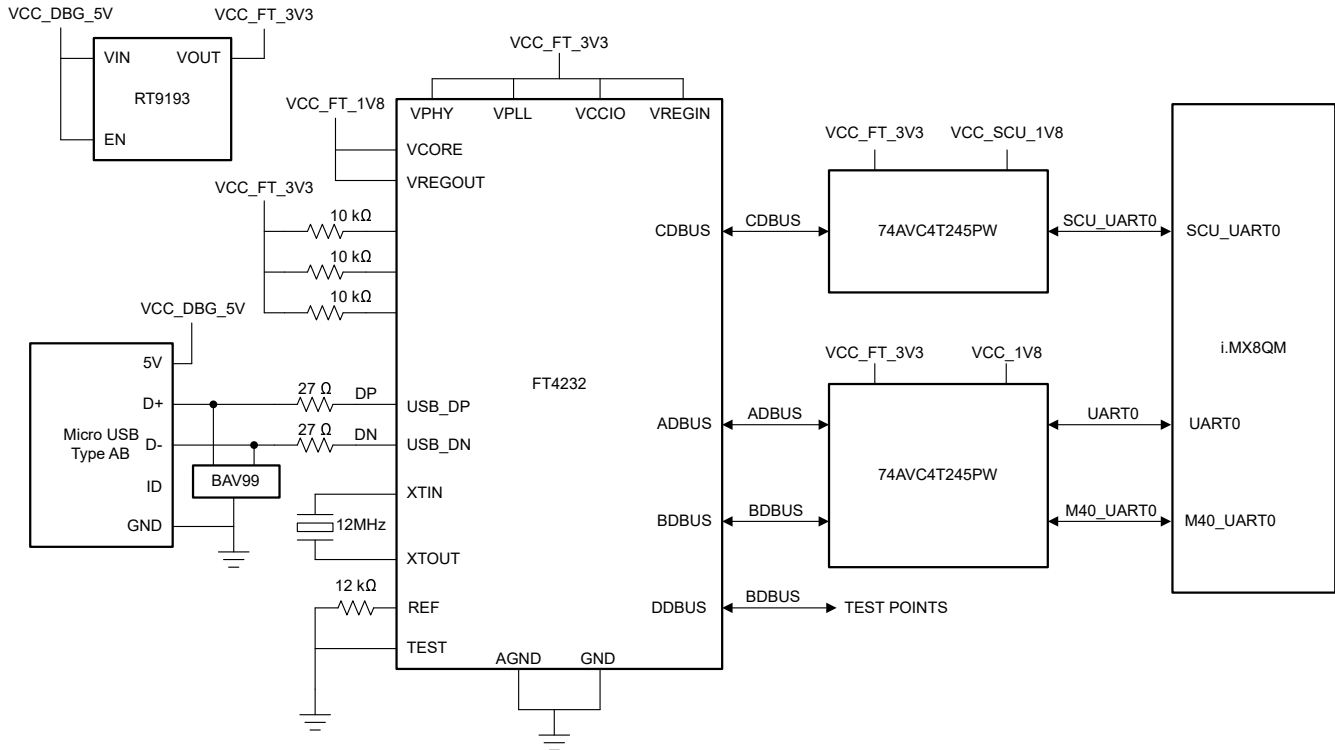


Figure 3-10. UART Debug Interface

Description	Manufacturer	Part Number
IC, FT4232H, quad port, USB to UART interface, QFN-64	FTDI CHIP	FT4232HQ
IC, 74LVC126A, quad buffer driver, 3 state O/P, TSSOP-14	NXP	74LVC126APW
IC, LDO, 2.5-5.5Vin, 3.3Vout/0.3A, SOT23-5	RICHTEK	RT9193-33GB
Diode, switching, 0.2A, 70V, 0.35W, SOT23-3	FAIRCHILD	BAV99
USB Micro AB receptacle, 1x1, shielded, RA, SMD	HIROSE	ZX62D-AB-5P8

3.12 JTAG Interface

A 2x5 header is provided in the board for i.MX8QM debug purposes. Connections are shown in the diagram below:

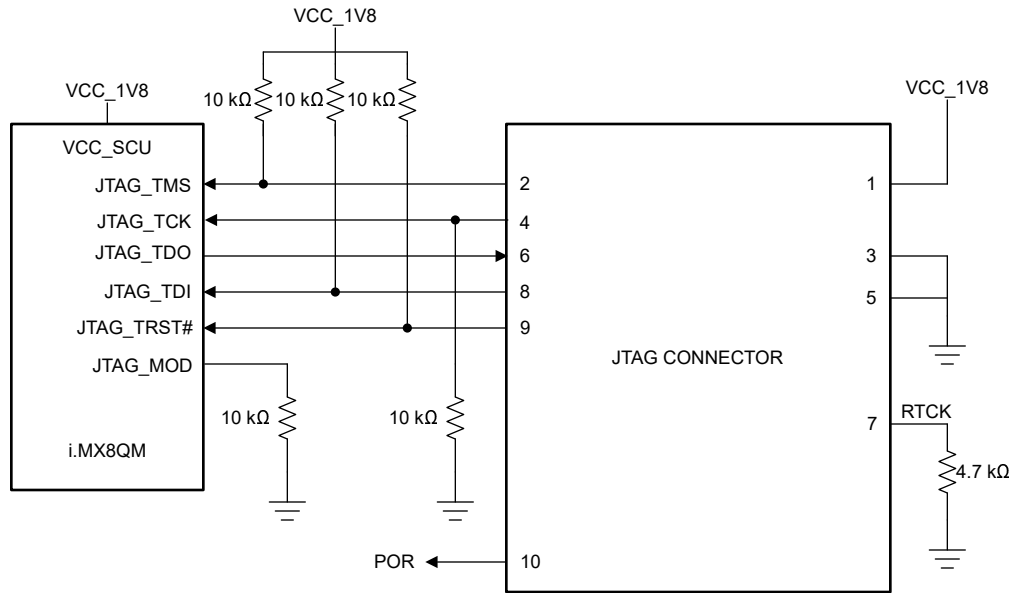


Figure 3-11. JTAG Interface

Description	Manufacturer	Part Number
B2C, male, 2X5, 1.27mm, 3.3A, shrouded, key, ST, SMD	SAMTECH	FTSH-105-01-L-DV-K

3.13 HDMI Port

The i.MX8QM processor board has one HDMI Out Port. HDMI acts as transmitter with the IP4292CZ10-TBR chip used for ESD protection. The interfacing is shown in the diagram below:

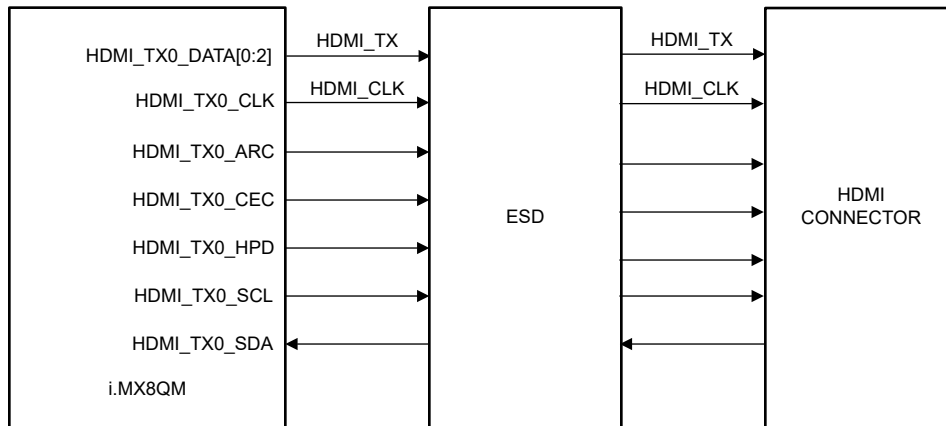


Figure 3-12. HDMI Port

Description	Manufacturer	Part Number
IC, IP4292CZ10, 4-Channel ESD Protection, DFN2510A-10	NEXPERIA	IP4292CZ10-TBR
Conn, HDMI, Type A, Receptacle, Shielded, ST, SMD	MOLEX	0476591000

3.14 LVDS, MIPI-CSI and MIPI-DSI Interface

The LVDS, MIPI (DSI and CSI) interfaces of i.MX8QM are terminated with 4 numbers of mini SAS connectors. The interfaces are shown in the diagram below:

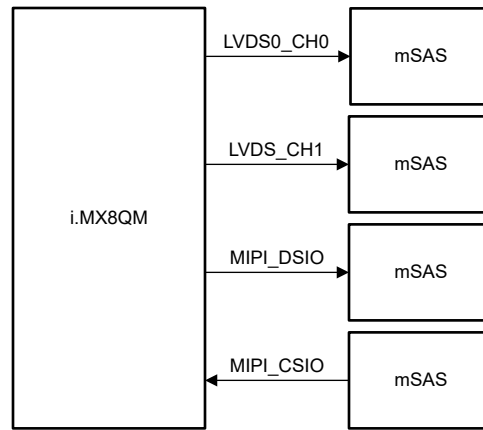


Figure 3-13. Mini SAS Connectors Interface

Description	Manufacturer	Part Number
IPass (Mini-SAS) internal, receptacle, 1x1, 0.8mm,0.5A, shielded, ST, SMD	MOLEX	75784-0136

3.15 M.2 E-Key for Wifi-Bluetooth Module

NGFF M.2 Cards can be interfaced with the i.MX8QM processor board using the M.2 E-Key connector. The interfaces required for WIFI and Bluetooth modules are provided within the M.2 connector.

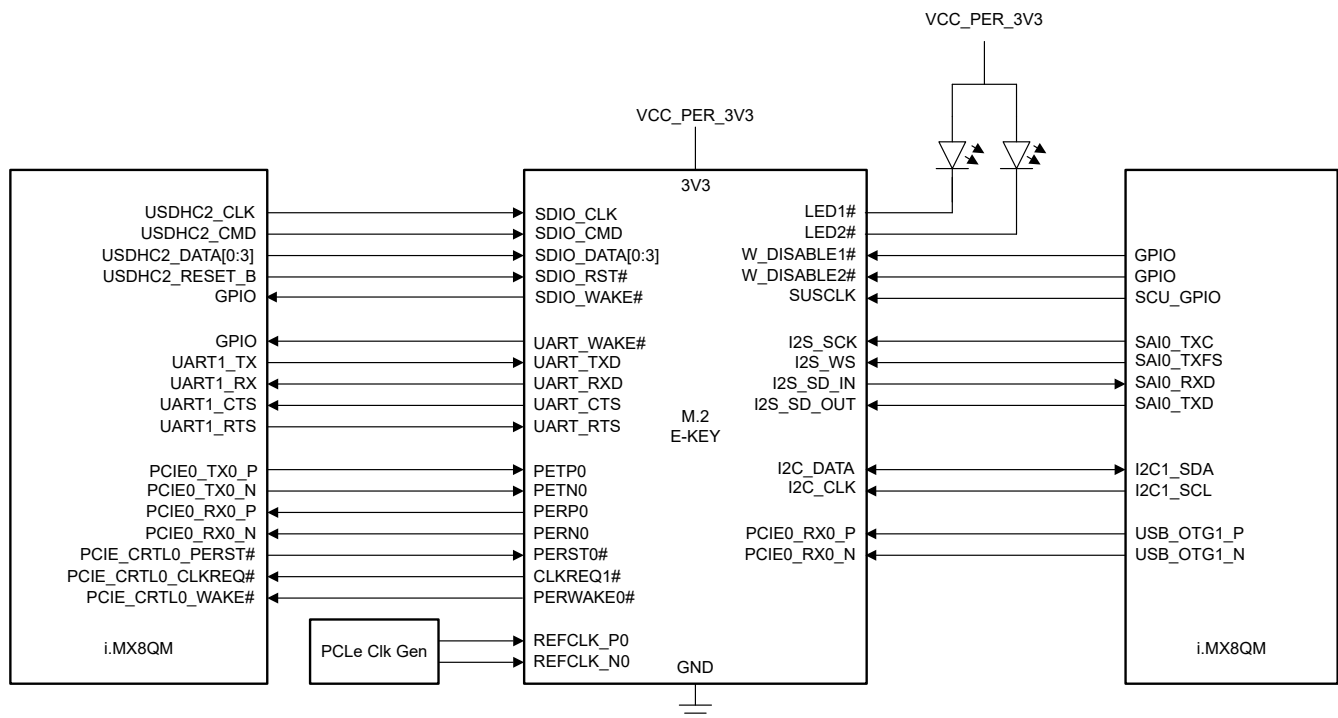


Figure 3-14. M.2 E-Key Interface in Processor Board

3.16 Processor I2C Interface

The LVDS0 CH0, LVDS0 CH1 interfaces are controlled with LVDS0_I2C1 lines that connect to the i.MX8QM processor. The MIPI interface also has individual I2C interfaces DSIO_I2C0 and CSIO_I2C0 which are used to configure and control the connected devices to these ports. The processor I2C interface diagram is shown below:

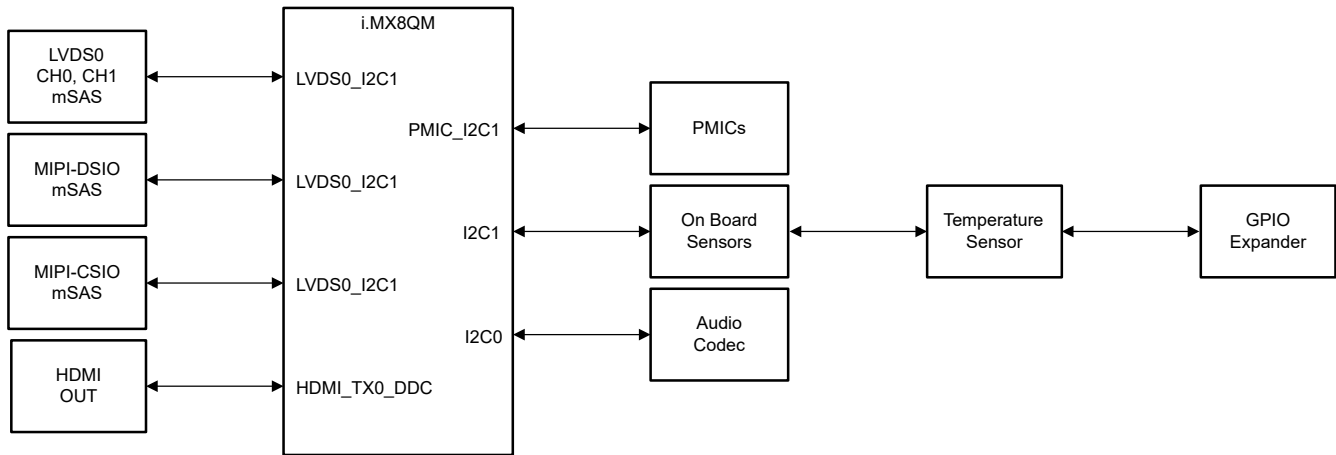


Figure 3-15. I2C Interface

All the on-board sensors are controlled by I2C1 lines of the i.MX8QM. There are dedicated I2C lines (PMIC_I2C) which configure and control PMICs. I2C0 is interfaced with the audio codec and there is also a dedicated HDMI_TX0_DDC I2C line for HDMI display control.

3.17 On-Board Sensors

The i.MX8QM processor board consists of the following on-board sensors:

- Combo accelerometer + magnetometer
- Gyroscope
- Pressure and temperature sensor
- Ambient light sensor

These sensors are interfaced with the i.MX8QM processor through I2C1 SDA and SCL lines. The interfacing is shown below:

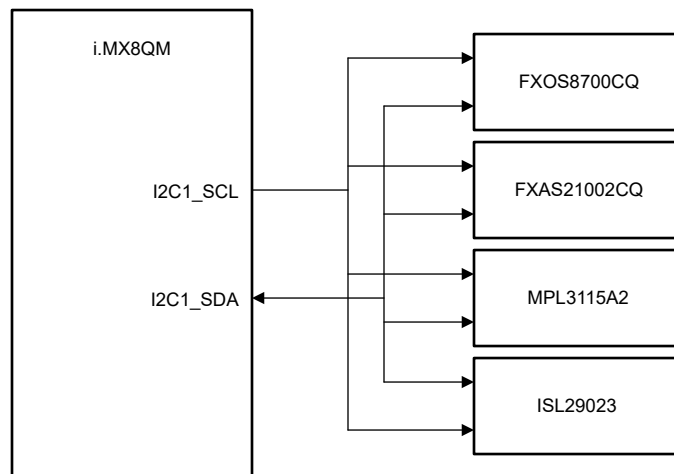


Figure 3-16. Sensors Interface

Description	Manufacturer	Part Number
Gyroscope, 3-Axis, 16-Bit, SPI/I2C, QFN-24	NXP SEMICONDUCTORS	FXAS21002CQR1
Barometric pressure and temperature Sensor, SPI/I2C, LGA-8	NXP SEMICONDUCTORS	MPL3115A2
Accelerometer and magnetometer, 6-Axis, 14/16-Bit, SPI/I2C, QFN-16	NXP SEMICONDUCTORS	FXOS8700CQ
Light sensor, I2C, 2.25-3.63Vin, ODFN-6	INTERSIL	ISL29023IROZ-T7

3.18 Processor - UART Interfaces

The i.MX8QM processor has eight UART interfaces, five of which support 5Mbps. Two UARTS (M40_UART0 and M41_UART0) are tightly coupled with Cortex-M4F cores. The SCU also has a dedicated UART (SCU_UART0) which is used for on-board debugging. The overall UART interface diagram is shown below:

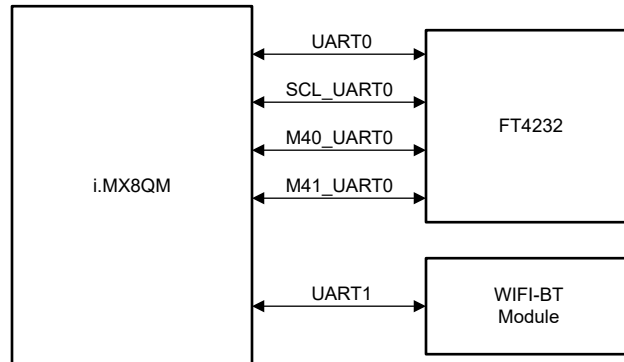


Figure 3-17. UART Interfaces

3.19 Processor - I2S Interfaces

The i.MX8QM processor board has I2S0 and I2S1 interfaces for audio communication in addition to two ESAI (enhanced serial audio interface). The I2S connection diagram is shown below:

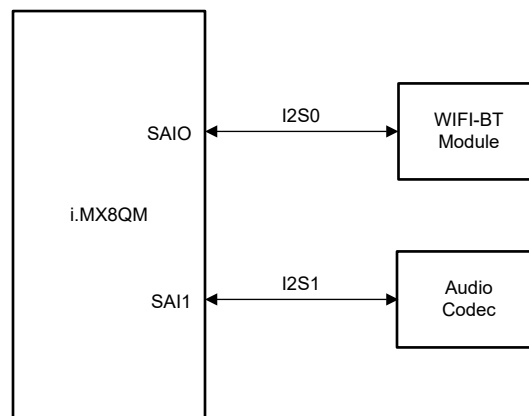


Figure 3-18. I2S Interfaces

3.20 CAN Interface

The i.MX8QM processor has three dedicated controller area network (CAN) interfaces for automotive application. One set of the CAN (CAN0) signals are terminated on a DB-9 connector. The CAN0 is interfaced with a high speed CAN transceiver TJA1043. The TJA1043, high-speed CAN transceiver provides an interface between a CAN protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing differential transmit and receive capability to a CAN protocol controller. Three different powers, VIO, VBAT and VCC, are required for CAN transceivers.

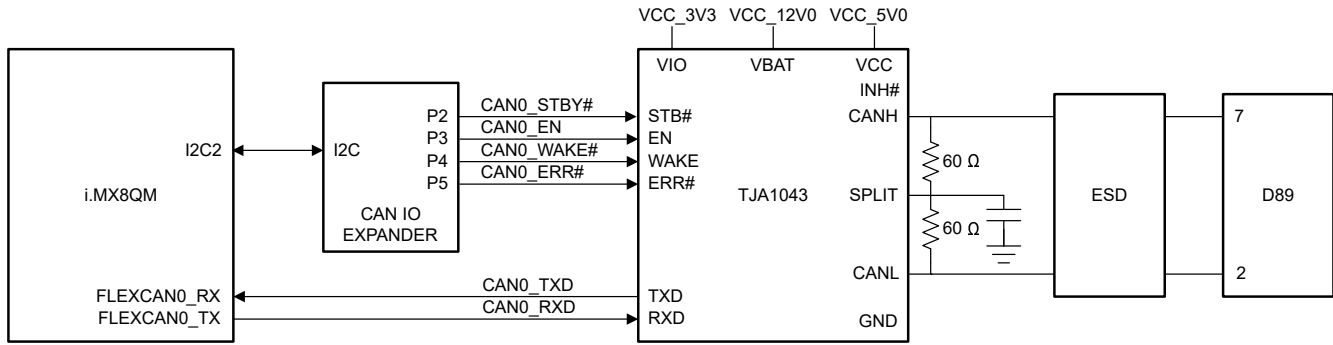


Figure 3-19. CAN Interface

Description	Manufacturer	Part Number
IC, TJA1043, high speed CAN transceiver, SO-14	NXP SEMICONDUCTORS	TJA1043T
TVS Diode, 41V, 230W, SOT-23	NXP SEMICONDUCTORS	PESD2CAN
Connector, DB9, receptacle, 1x1, 5A, shielded, ST, TH	TE CONNECTIVITY	5207826-4

3.21 Boot Device Selection

A four position DIP switch is provided in the board to select the interface that can be used by the boot process in accordance with the specific boot mode configurations. In SOM, the following devices can be used for the boot process:

- EMMC
- Octal SPI flash
- SD Card
- Serial Boot
- Fuse

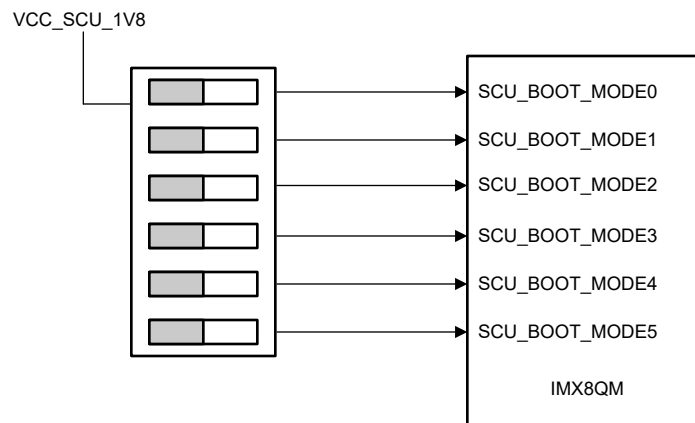


Figure 3-20. Boot Switch

BOOT MODE						
MODE	5	4	3	2	1	0
FUSE	0	0	0	0	0	0
SERIAL BOOT	0	0	0	1	0	0
eMMC0	0	0	1	0	0	0
SD1	0	0	1	1	0	0
OCTAL SPI	0	1	1	0	0	0

4 Reset Scheme

The power on reset input of the processor is generated from three sources:

- PMIC
- Manual reset switch
- SRST output of JTAG

A reset button (SW1) can trigger a reset event in the i.MX8QM processor board. Also SCU of the processor can initiate a SCU_WDOG_OUT signal that can trigger a watchdog reset. Both the resets are combined to generate a primary reset signal that controls the PMIC and thus initiating power down and power up sequences.

PMIC_POR is the power on reset signal that is connected to POR_B pin of the i.MX8QM processor that initiates the peripheral power on reset.

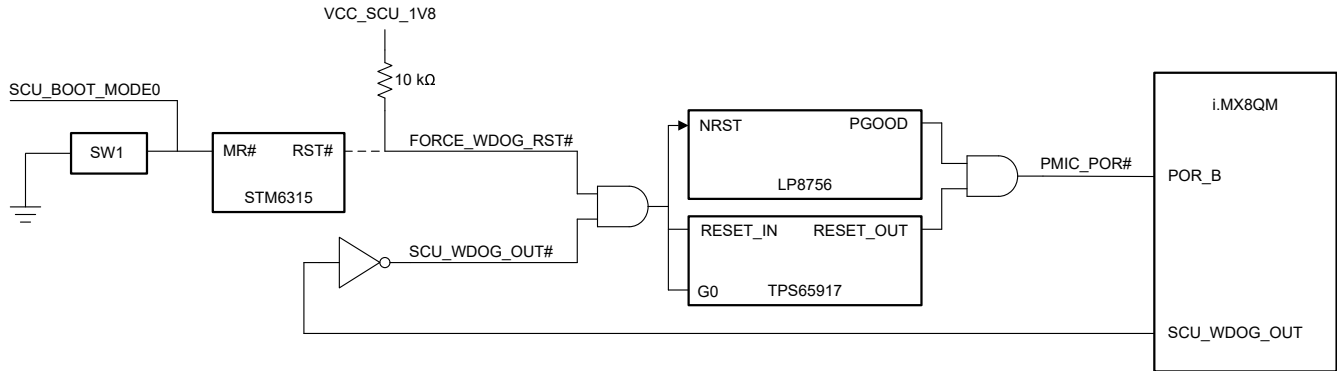


Figure 4-1. Reset Scheme

Note: Switch SW1 is provided for development purposes. If not used, an option is provided to mount a=or un-mount a 0Ω resistor to disable the switch section.

4.1 Reset Timing Parameters of i.MX8QM

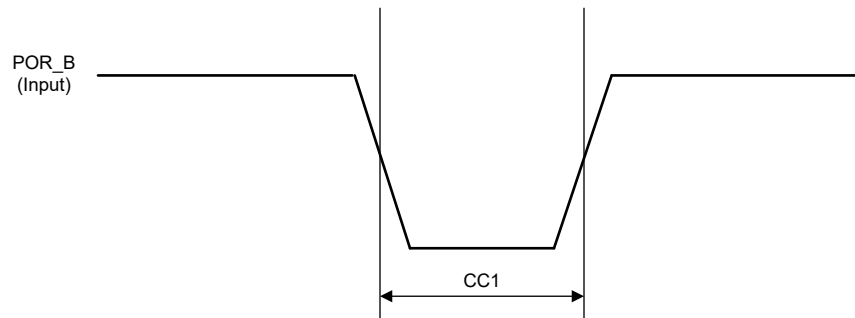


Figure 4-2. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of SRC_POR_B to be qualified as valid	1	—	XTALOSC_RTC_XTALI cycle

4.2 WDOG Reset Timing Parameters of i.MX8QM

The i.MX8QM processor consists of a watchdog timer in its SCU section. When the processor enters a hang state, the WDOG timer initiates a logic HI on the SCU_WDOG_OUT pin. The WDOG is also triggered when there is no boot media present on the board. The following figure shows the WDOG reset timing parameters of the i.MX8QM:

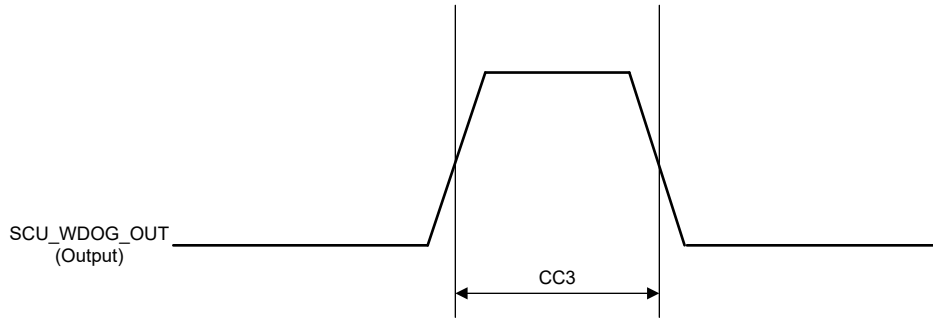


Figure 4-3. WDOG Reset Timing Diagram

ID	Description	Min	Max	Unit
CC3	Duration of SCU_WDOG_OUT assertion	1		XTALOSC_RTC_XTALI cycle

XTALOSC_RTC_XTALI is approximately 32kHz.

XTALOSC_RTC_XTALI cycle is one period or approximately 30us.

4.3 VCC_EXT_5V0 Generation

The main 5V is generated from the 12V input by using a buck converter, IR3895, from Invencon Technologies. A DIN connector is used in the board which connects to the main AC power adapter. The output of the adapter is 12V DC. This 12V DC is used as the inputs to the buck. The 5V output of the buck is used as the input voltage for the PMIC.

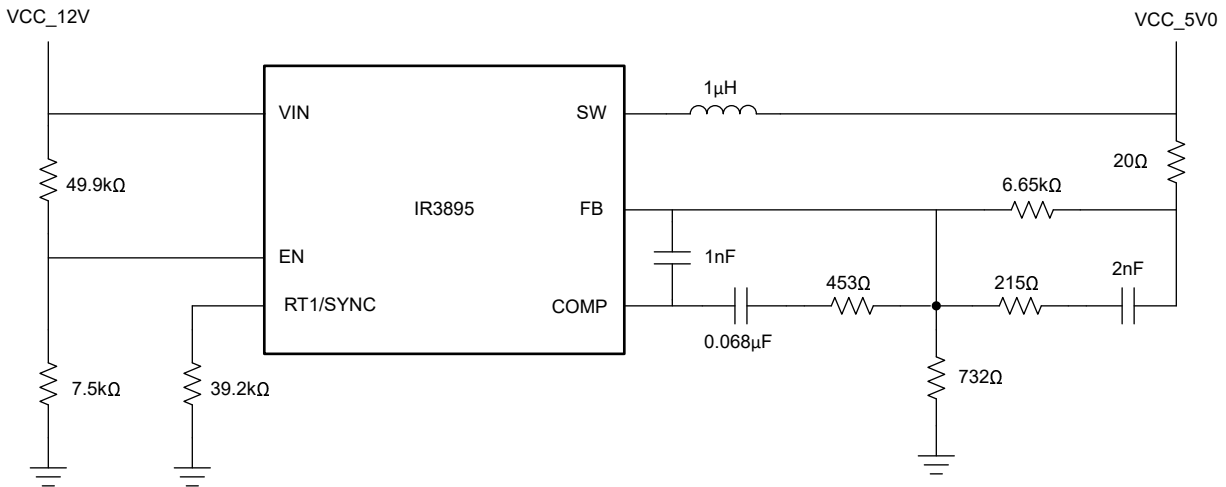


Figure 4-4. EXT_5V0 Generation

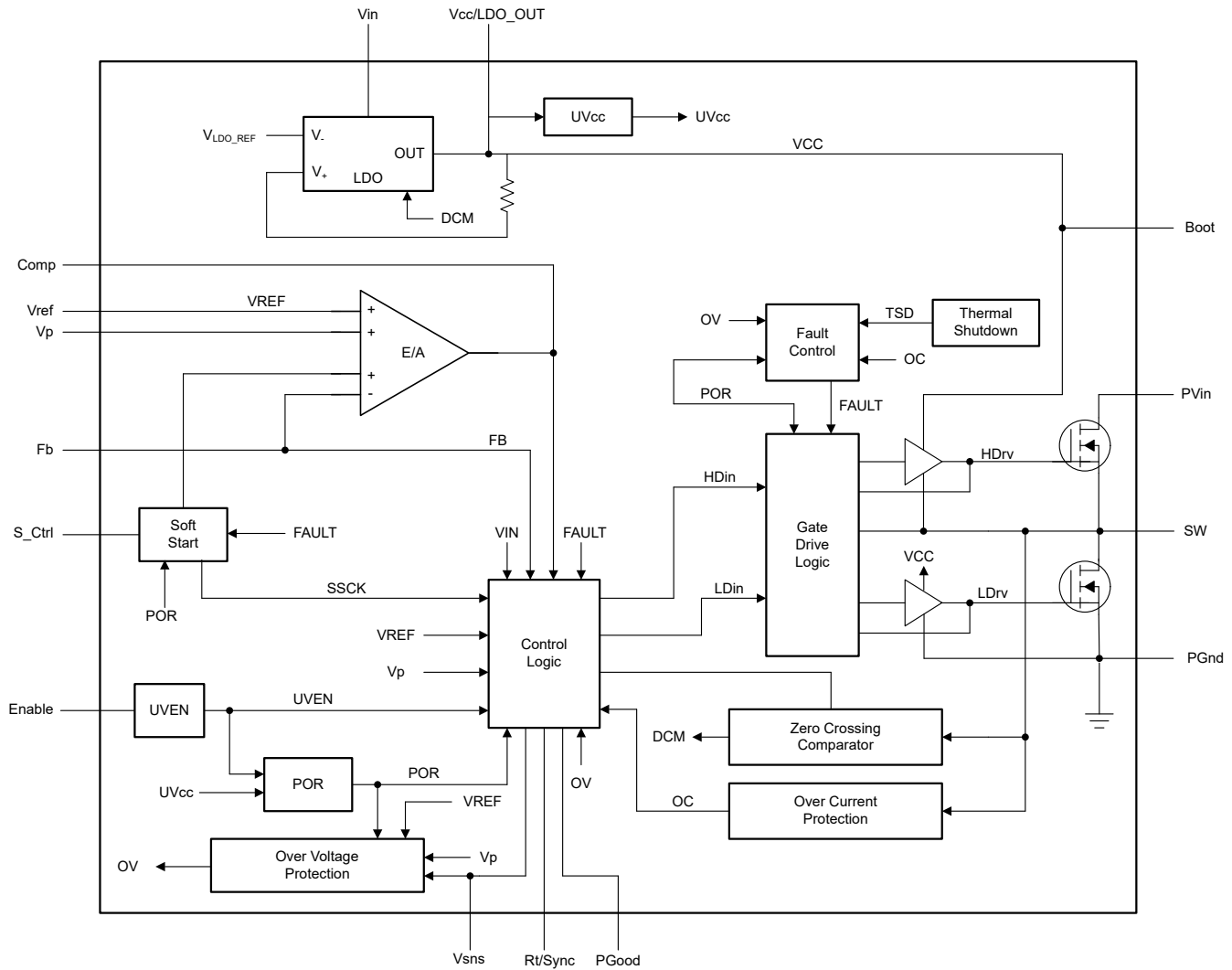


Figure 4-5. IR3895 Internal Block Diagram

Table 4-1.

Description	Manufacturer	Part Number
IC, switcher, 1-21V Vin, 0.5-18.06Vout/15A, sync buck, QFN-28	International Rectifier	IR3895MTRPBF

Design for the 5V Output

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. The resistor values can be chosen according to:

$$R1 = R2 \left[\frac{V_{REF}}{V_{OUT} - V_{REF}} \right]$$

Where $V_{OUT}=5V$, $V_{REF}=0.5V$ and $R2=6.85k\Omega$.

Therefore $R1 = 0.76k\Omega$

So the standard value $0.732k\Omega$ can be chosen.

Setting the Switching Frequency

In IR3895 the switching frequency can be programmed between 300kHz – 1500kHz by connecting an external resistor from Rt pin to ground. The switching frequency is set at 600kHz by connecting a 39.2kΩ from the RTI pin to ground.

Output Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in smaller size and faster response to a load transient. However, this also results in poor efficiency and high output noise so tradeoffs need to be accounted for properly. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor. For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$L = (VIN - VOUT) \left[\frac{VOUT}{VIN * \Delta I * Fs} \right]$$

Where ΔI = inductor peak-to-peak ripple current and Fs = switching frequency.

Now set $VIN=12V$, $VOUT=5V$, $\Delta I =5\%$ and $Fs=600kHz$.

Therefore $L=1\mu H$

4.4 VCC_Buck_3V3 Generation

The 3.3V for the PMIC input and peripheral devices is generated from the 12V main input by using the buck converter IR3895 from International Rectifier. The Enable input of the converter is given from the divider output of the 12V rail.

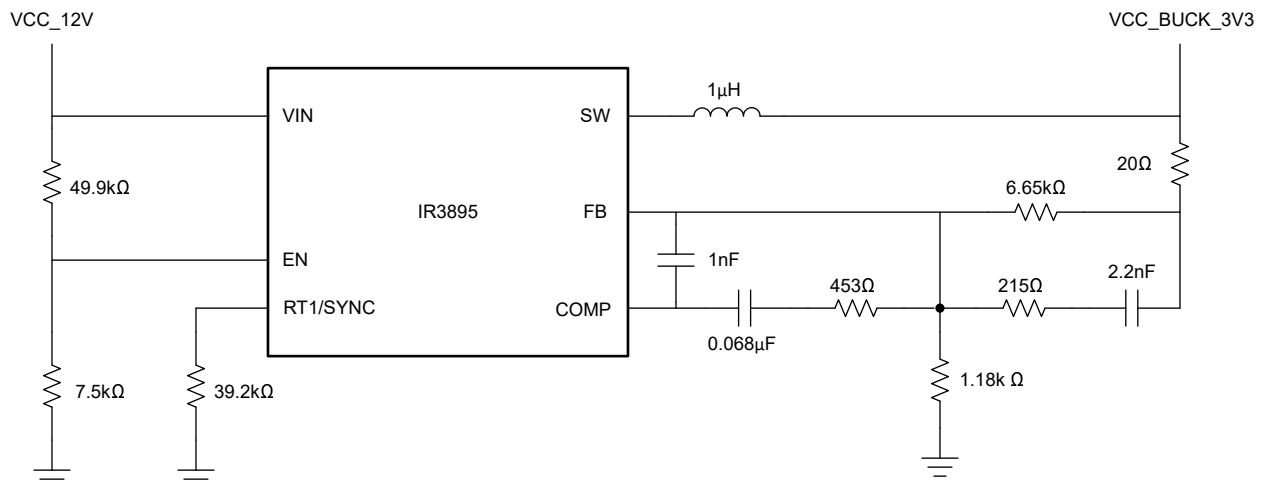


Figure 4-6. VCC_BUCK_3V3 Generation

Description	Manufacturer	Part Number
IC, switcher, 1-21V input voltage, 0.5-18.06Vout/15A, sync buck, QFN-28	International Rectifier	IR3895MTRPBF

Design for the 3V3 Output

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. The resistor values can be chosen according to:

$$R1 = R2 \left[\frac{VREF}{VOUT - VREF} \right]$$

Where $VOUT=3.3V$, $VREF=0.5V$ and $R2 =6.85k\Omega$.

Therefore $R1=1.18k\Omega$.

So the standard value 1.18kΩ can be chosen

Setting the Switching Frequency

In IR3895 the switching frequency can be programmed between 300kHz – 1500kHz by connecting an external resistor from Rt pin to ground. We set the switching frequency at 600kHz by connecting a 39kΩ from the RTI pin to ground.

Output Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in smaller size and faster response to a load transient. However, this also results in poor efficiency and high output noise so tradeoffs need to be accounted for properly. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor. For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$L = (VIN - VOUT) \left[\frac{VOUT}{VIN * \Delta I * Fs} \right]$$

Where VIN=12V, VOUT=5V, ΔI =5% and Fs=600kHz.

Therefore L=1μH

4.5 VCC_Buck_1V8 Generation

The 1.8V for the peripheral devices is generated from the 12V main input by using the buck converter IR3827 from International Rectifier. The Enable input of the converter is given from the 1.8V output from the PMIC so that the buck converter turns on only after the PMIC has turned on.

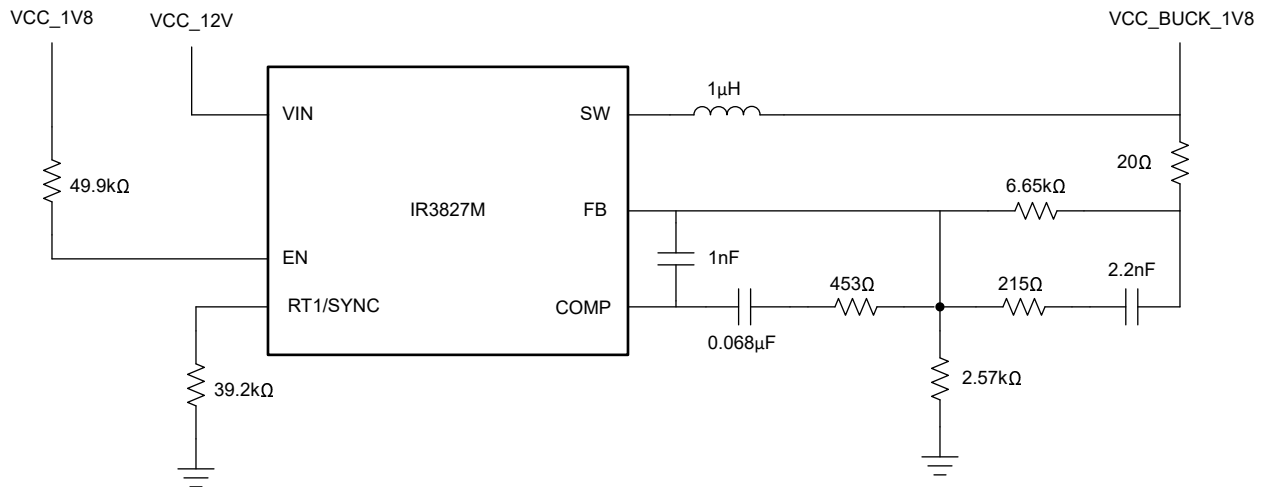


Figure 4-7. VCC_BUCK_1V8 Generation

Description	Manufacturer	Part Number
IC, Switcher, Positive, Adjustable 0.6V 1 Output 6A 17-PowerVQFN	International Rectifier	IR3895MTRPBF

Design for the 1V8 Output

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. The resistor values can be chosen according to:

$$R1 = R2 \left[\frac{VREF}{VOUT - VREF} \right]$$

Where VOUT=1.8V, VREF=0.5V and R2 =6.85kΩ.

Therefore $R1=2.57k\Omega$

So the standard value $2.57k\Omega$ can be chosen.

Setting the Switching Frequency

In IR3895 the switching frequency can be programmed between 300kHz – 1500kHz by connecting an external resistor from Rt pin to ground. We set the switching frequency at 600kHz by connecting a $39.2k\Omega$ from the RTI pin to ground.

Output Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in smaller size and faster response to a load transient. However, this also results in poor efficiency and high output noise so tradeoffs need to be accounted for properly. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor. For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$L = (VIN - VOUT) \left[\frac{VOUT}{VIN * \Delta I * Fs} \right]$$

Where $VIN=12V$, $VOUT=5V$, $\Delta I =5\%$ and $Fs=600kHz$.

Therefore $L=1\mu H$

5 Power Scheme

5.1 Power Requirements for i.MX8QM

The various voltage rails of the i.MX8QM Processor are shown below:

Power Rail	Voltage (V)	Max. Current (mA)
VCC_MAIN	1.0	4000
VCC_CPU1	1.1	4000
VCC_CPU0	1.1	3500
VCC_GPU1	1.1	4000
VCC_GPU0	1.1	4000
VCC-MEMC	1.1	3500
VCC_DDRIO1	1.1	3000
VCC_DDRIO0	1.1	2000
VCC_SCU_1V8	1.8	500 (Ext. LDO)
VCC_3V3	3.3	2500 (Not by PMICs)
VCC_1V8	1.8	1500
VCC_LDO_SD1	1.8	300
VCC_SNVS	3.0 - 4.2	100 (Ext. LDO)

5.2 TI PMICs Interfacing

BUCK_3V3 and EXT_5V0 are externally generated voltages. BUCK_3V3 is the main source for the PMICs. VCC_SNVS is sourced by TPS79133-Q1 (LDO) from TI. VCC_SNVS is expected to be always ON when the board is powered. VCC_3V3 is controlled through TPS22965-Q1 (Load Switch). VCC_SCU_1V8 is sourced by LP5912-Q1 (LDO). All the other power rails of i.MX8QM are sourced by LP87564-Q1 and TPS65917-Q1 PMICs.

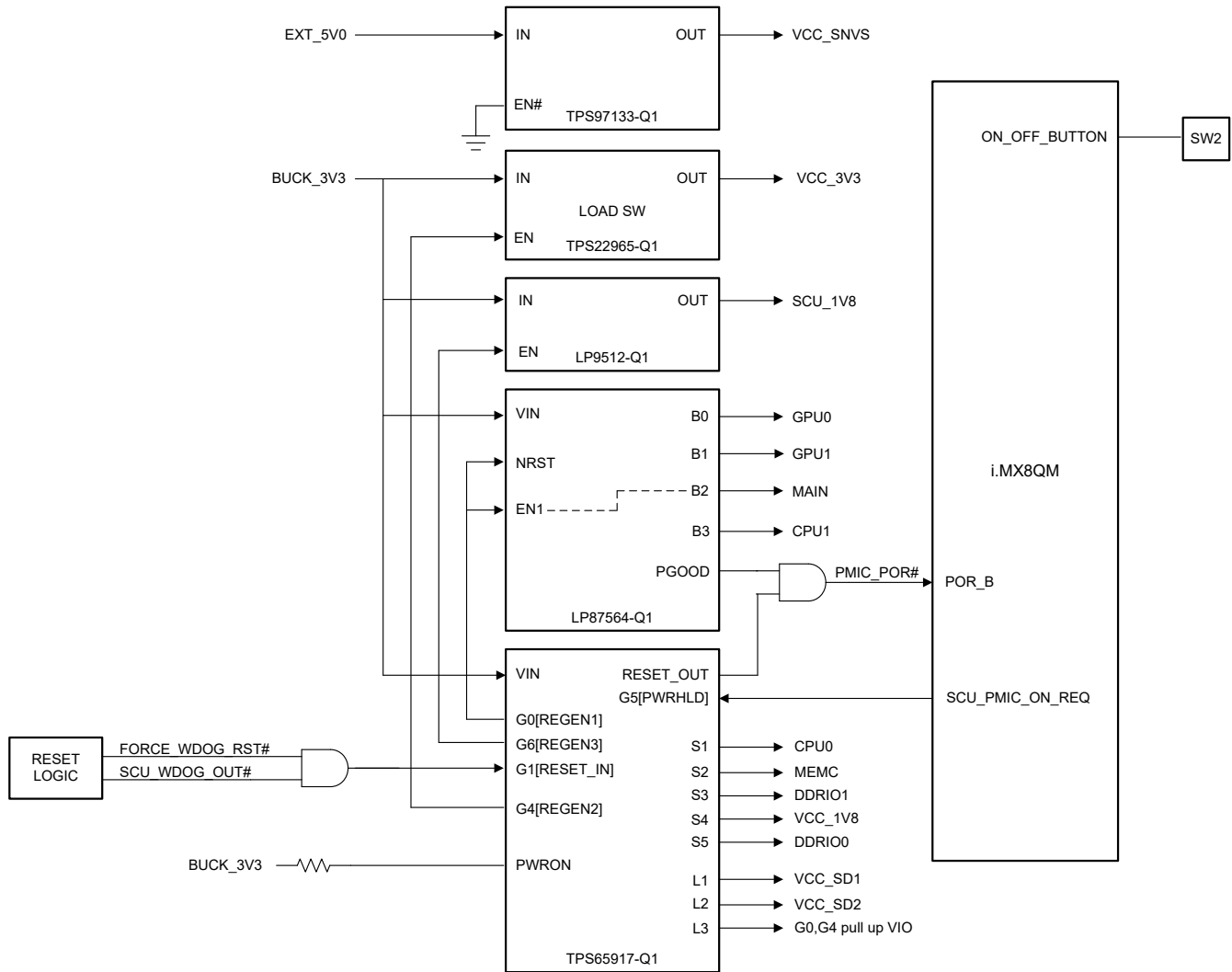


Figure 5-1. TI PMICs Interfacing with i.MX8QM

5.3 TI PMICs Power Tree and Sequencing

Power tree for i.MX8QM is shown in [Figure 5-2](#).

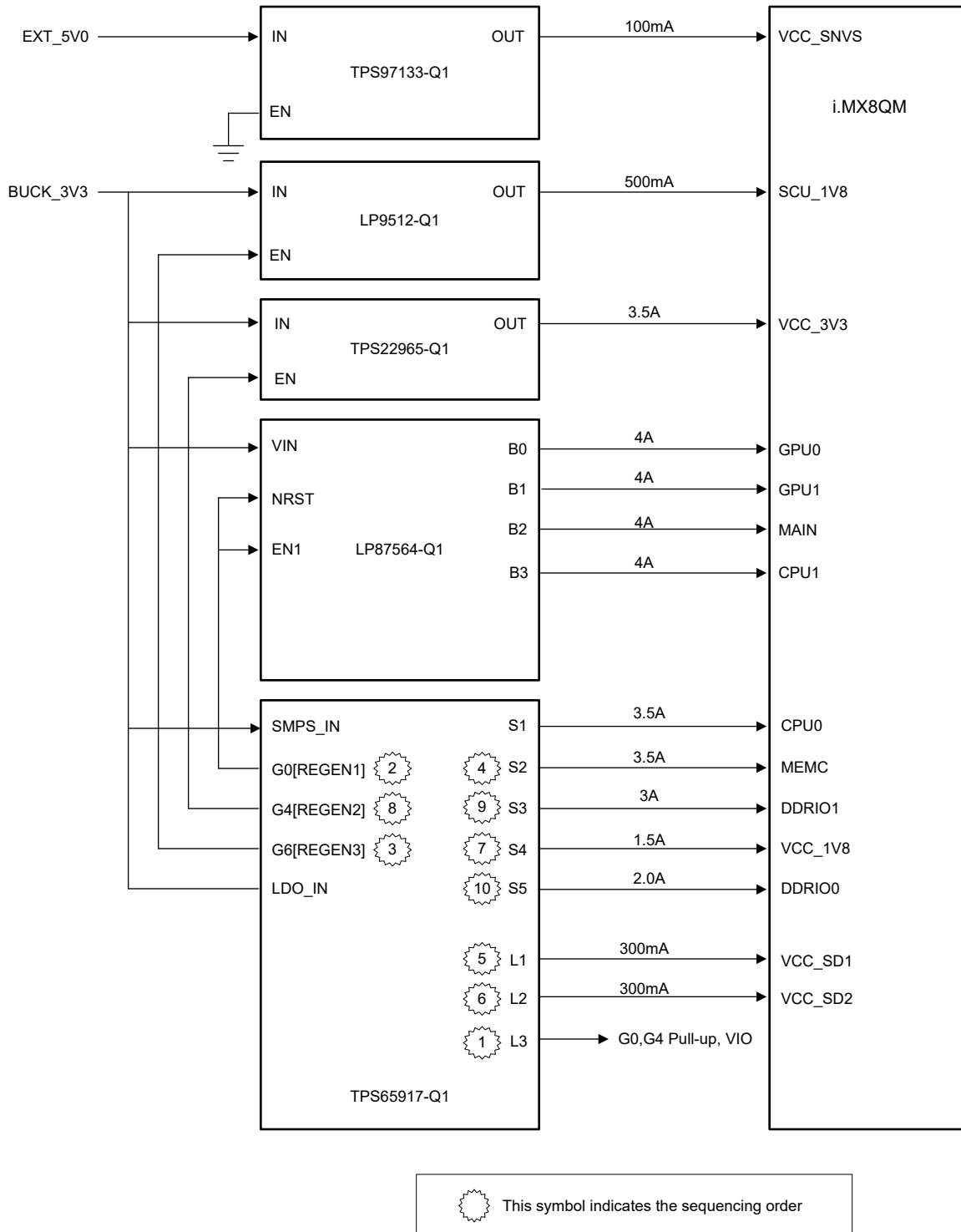


Figure 5-2. Power Tree for i.MX8QM

LDO L3 is used for the VIO supply for the TPS65917-Q1 device as well as the pull-up voltage for G0,G4,G6 and RESET_OUT.

The following images show the power-up sequencing and power-down sequencing along with the timing interval between the voltage rails. These timing intervals are programmed to the OTP configurations in the TPS65917-Q1 and LP87564-Q1.

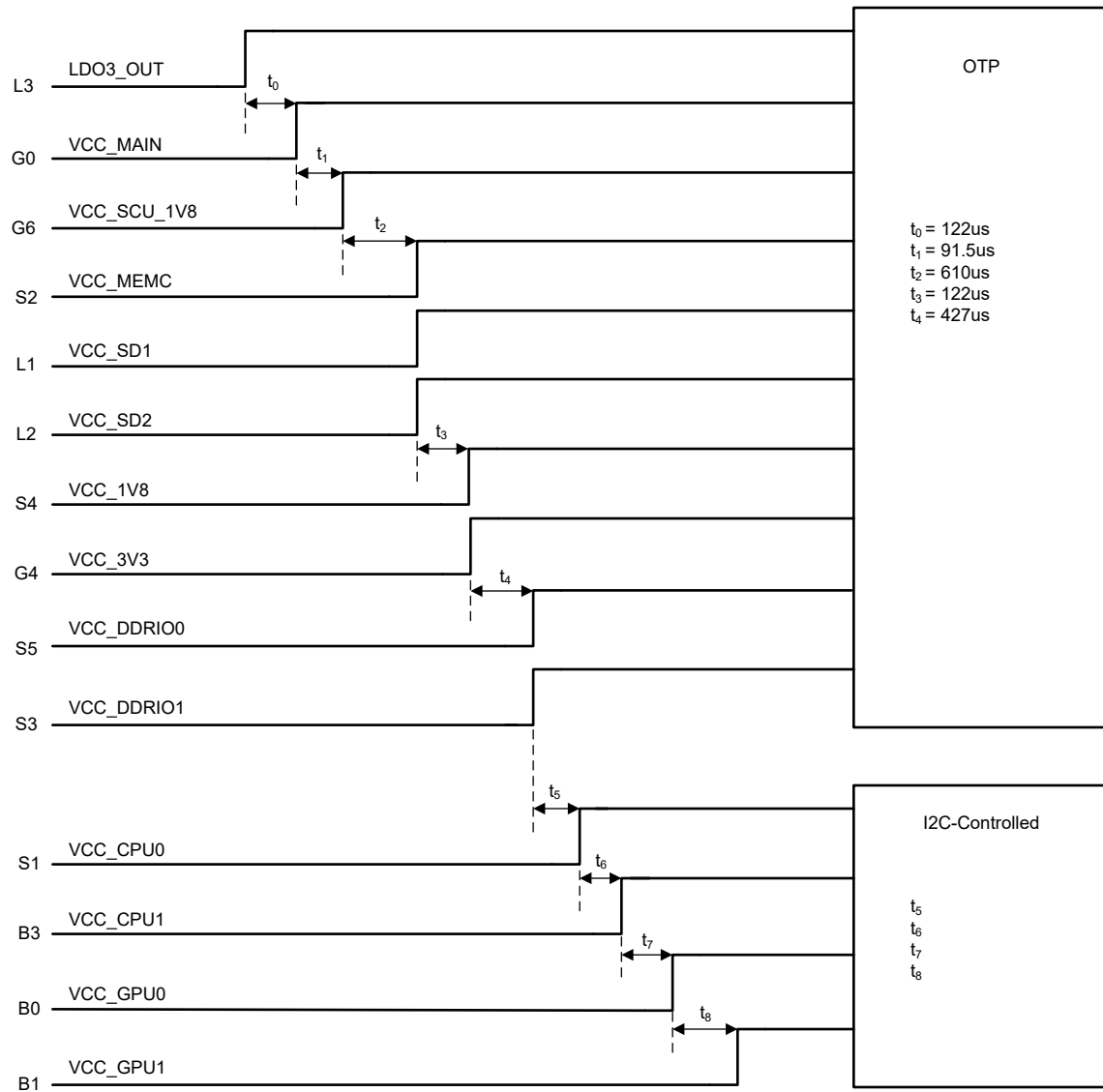


Figure 5-3. Power-up Timings

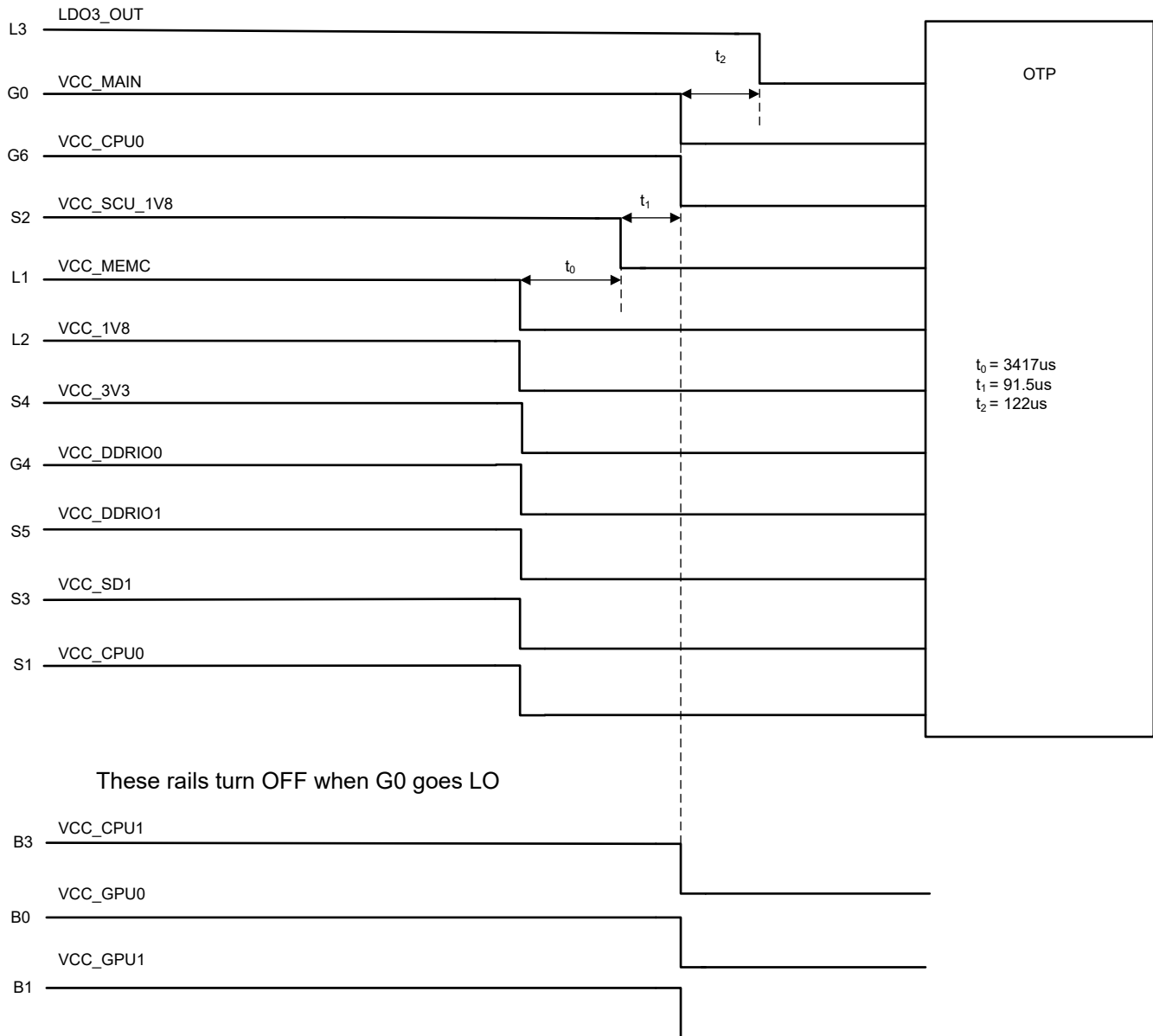


Figure 5-4. Power Down Timings

6 Clock Scheme

The i.MX8QM processor requires two crystal inputs with frequencies 24MHz and 32.768 KHz. The 32.768 KHz crystal is connected across the RTC_XTALI and RTC_XTALO balls. The 24MHz crystal is connected to XTALI and XTALO balls of the processor for PLL Reference.

The clock frequencies for the LPDDR and eMMC are provided by the processor itself. A separate clock oscillator is provided for the PCIe interface, the WiFi-BT module can get the reference clock directly from the processor or the oscillator.

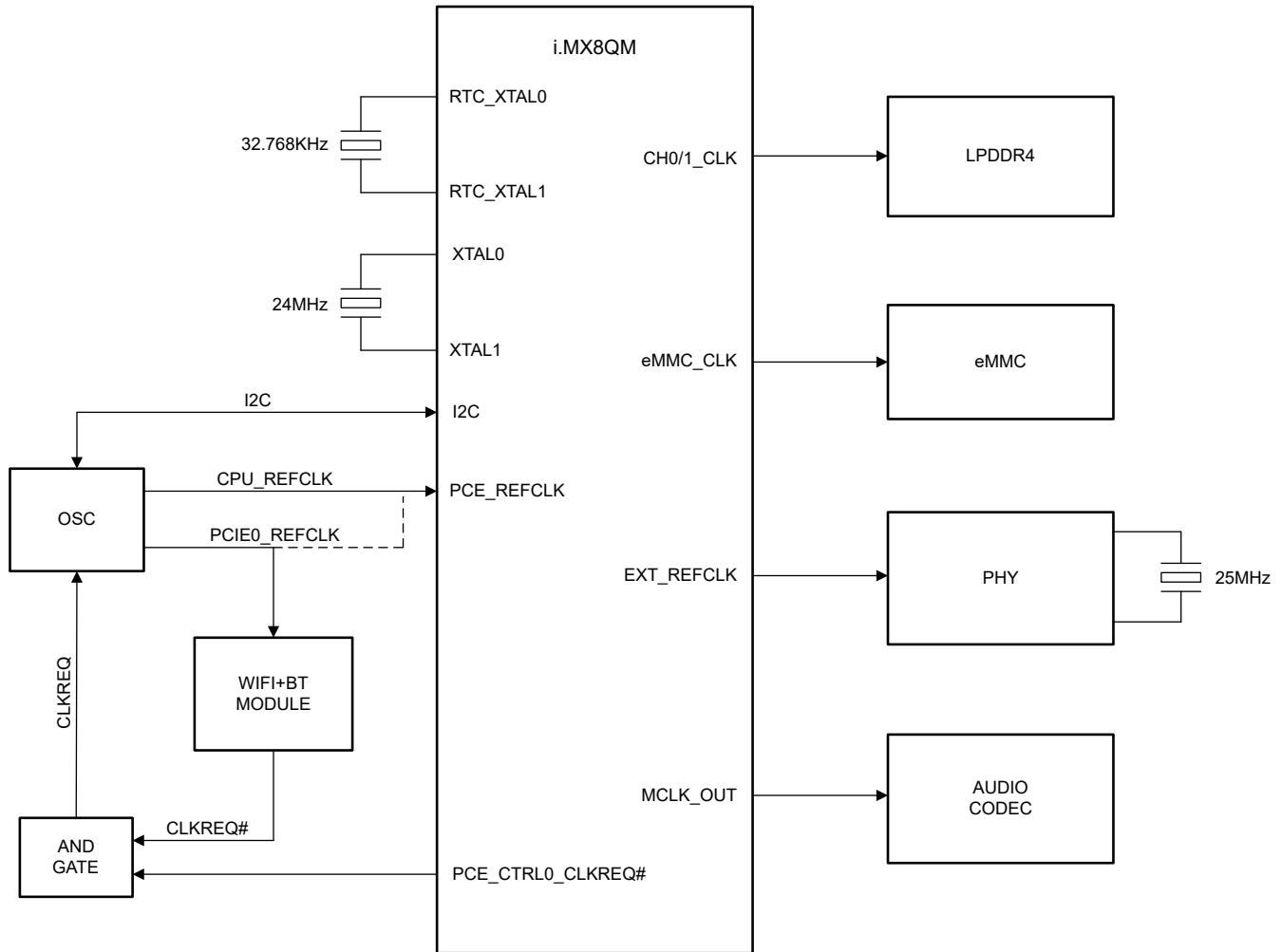


Figure 6-1. Clock Scheme

7 Design Files, Software, Documentation

Board Design

All design files (schematics, layout, gerbers, BOM and so on) are available on request. See links below:

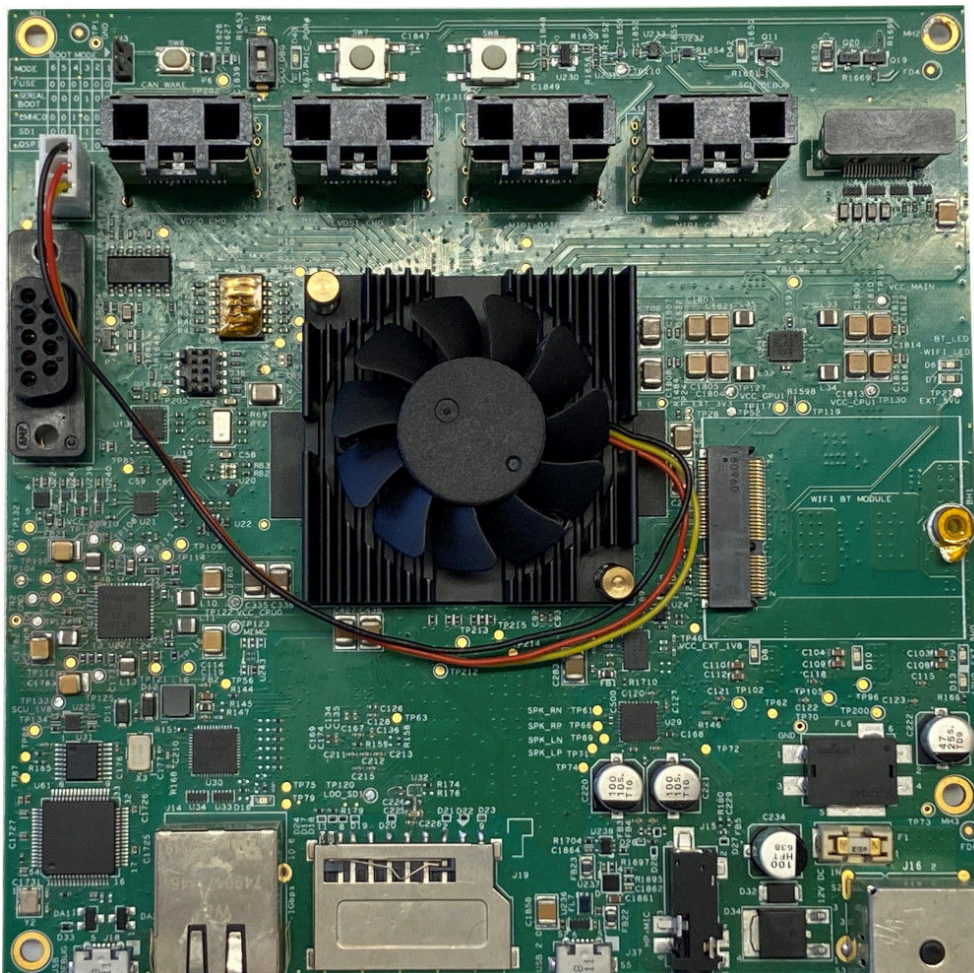


Figure 7-1. Fully Assembled iMX8QM Development Board with TI Power Solution

Software

Software for the board is based on embedded Linux. Full design files, details on the driver implementation, and more detailed documentation is available on request. See links below:

https://www.ti.com/licreg/docs/swlicexportcontrol.tsp?form_id=300248&prod_no=LP875X-Q1_LP873X-Q1_TPS65917-Q1_DESIGN_DOCS&ref_url=APP-BMC-IPM

Note: Users need an active ti.com account and must request access for the files. Once the request has been processed and approved, the files can be downloaded from <https://www.ti.com/mysecursoftware>.

7.1 Bill of Materials

Bill of materials for the power solution and also estimated area with keep out (1 mm) and routing factor (+30%) is shown in [Table 7-1](#).

Table 7-1. BOM and Area Summary

BOM and Area Summary								
QTY	Vendor	Part #	Description	W	L	H	Unit Area in mm ² (w/keep out)	Total Area (mm ²)
1	TI	LP87564TRNFRQ1	Configurable 4-phase Buck	4.00	4.50	0.90	27.50	27.50
4	Murata	DFE252012PD-R47M	LP8756x Inductor 0.47uH, I _{max} 4.0A, R _{dc} typ 21mOhm	2.50	2.00	1.20	10.50	42.00
4	Murata	GCM21BR71A106KE22	LP8756x SMPS Input Capacitor 10uF, 10V, 10%	2.00	1.25	1.25	6.75	27.00
8	Murata	GCM21BD70J226ME35	LP8756x SMPS Output Capacitor 22uF, 10V, 10%	2.00	1.25	1.25	6.75	54.00
1	Murata	GCM155R71C104KA55D	LP8756x Input Capacitor 0.1uF, 16V, 10%	1.00	0.50	0.50	3.00	3.00
1	TI	O917A186TRGZRQ1	PMIC	7.00	7.00	1.00	64.00	64.00
5	Murata	DFE252012PD-1R0M	1uH Inductor	2.50	2.00	1.20	10.50	52.50
5	Murata	GCM21BR71C475KA73	SMPS Input Capacitor 4.7uF	2.00	1.25	1.25	6.75	33.75
5	Murata	GCM32ER70J476KE19L	SMPS Output Capacitor 47uF	2.50	3.20	2.50	14.70	73.50
3	Murata	GCM188R70J225KE22	LDO Input Capacitor 2.2uF	1.60	0.80	0.90	4.68	14.04
5	Murata	GCM188R70J225KE22	LDO Output Capacitor 2.2uF	1.60	0.80	0.90	4.68	23.40
2	Murata	GCM155R71C104KA55D	Input Capacitor 0.1uF, 16V, 10%	1.00	0.50	0.50	3.00	6.00
1	Murata	GCM21BR70J106KE22	Input Capacitor 10uF	2.00	1.25	1.25	6.75	6.75
3	Murata	GCM188R70J225KE22	Input Capacitor 2.2uF	1.60	0.80	0.90	4.68	14.04
1	TI	LP5912-Q1	Low Dropout Regulator	2.00	2.00	0.80	9.00	9.00
1			Input Capacitor 1uF	1.00	0.50	0.50	3.00	3
1			Output Capacitor 1uF	1.00	0.50	0.50	3.00	3
1	TI	TPS22965-Q1		2.00	2.00	0.80	9.00	9
1			Input Capacitor 1uF	1.00	0.50	0.50	3.00	3
1	TI	TPS79133-Q1		3.00	3.00	1.00	16.00	16.00
1			Input Capacitor 1uF	1.00	0.50	0.50	3.00	3.00
1			Output Capacitor 1uF	1.00	0.50	0.50	3.00	3.00

Component area with keep out 490.48 mm²
 Routing area 210.21 mm²
 Total area 700.69 mm²

8 Test Results

DVFS

Dynamic voltage and frequency scaling (DVFS) is useful in reducing power, since lowering the voltage has a squared effect on active power consumption. DVFS techniques provide ways to reduce power consumption of chips on the fly by scaling down the voltage and frequency based on the targeted performance requirements of the application. Since DVFS optimizes both the frequency and the voltage, it is one of the techniques that is highly effective on both dynamic and static power.

Procedure:

1. Set the A53 cluster to a specific frequency of operation.
2. Measure the voltage at the A53 cluster rails for change in voltage with frequency.
3. Repeat the same steps for A72 cluster.
4. Note down the readings for frequency vs. voltage.

The following table shows the measurements for different frequencies in A53 CPU cluster:

Frequency	Voltage Rail			
	VCC_CPU0	VCC_CPU1	VCC_GPU0	VCC_GPU1
	TPI22	TPI30	TPI28	TPI27
CPU: A53				
600MHz	0.996V	0.991V	1.091V	1.092V
900MHz	0.996V	0.991V	1.091V	1.092V
1100MHz	1.097V	0.991V	1.091V	1.092V
1200MHz	1.096V	0.991V	1.091V	1.092V

The following table shows the measurements for different frequencies in A72 CPU cluster:

Frequency	Voltage Rail			
	VCC_CPU0	VCC_CPU1	VCC_GPU0	VCC_GPU1
	TPI22	TPI30	TPI28	TPI27
CPU: A72				
600MHz	1.096V	0.991V	1.090V	1.092V
1060MHz	1.096V	0.990V	1.090V	1.092V
1300MHz	1.096V	1.090V	1.090V	1.092V
1600MHz	1.096V	1.090V	1.090V	1.092V

9 Summary

With this presented solution using the LP87564-Q1 and TPS65917-Q1, it is possible to power the i.MX8QM. Sequencing is handled in the PMICs and the solution is compact due to minimum number of external components. Design files for the development platform including hardware, software, and detailed documentation are available on request.

10 References

See these references for additional information:

- Texas Instruments, [LP8756x-Q1 16A Buck Converter With Integrated Switches Data Sheet](#) (SNVSB22)
- Texas Instruments, [TPS65917-Q1 Power Management Unit \(PMU\) for Processor Data Sheet](#) (SLVSCO4)
- Texas Instruments, [LP87564T-Q1 Technical Reference Manual](#) (SNVU815)
- Texas Instruments, [TPS65917-Q1 Users Guide to Power i.MX8QM](#) (SLVUCD2)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated