Functional Safety Information

LM4132-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LM4132-Q1 (5-pin DBV package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

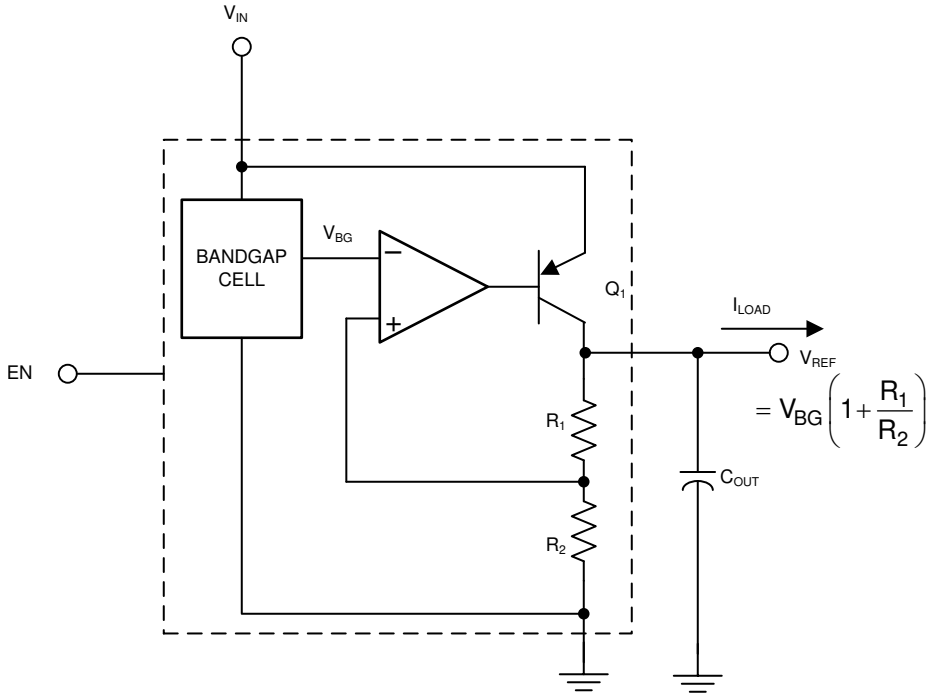

Figure 1-1. Functional Block Diagram

LM4132-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM4132-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM4132-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No OUTPUT (Output Low)	30%
OUTPUT High (Following Input)	25%
OUTPUT not in Specification	40%
EN False enable	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM4132-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LM4132-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM4132-Q1 data sheet.

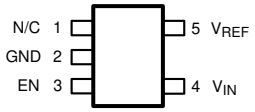

Figure 4-1. 5-Pin SOT-23 Package (Top View)

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Unless otherwise specified, the voltage applied to the VIN pin and EN pin is within the LM4132-Q1 Recommended Operating Range.
- The EN pin is driven from an external source.
- Device functionality indicates that the LM4132 status can be remotely changed between the two functional states (ENABLED and DISABLED) by the external control connected to the EN pin.

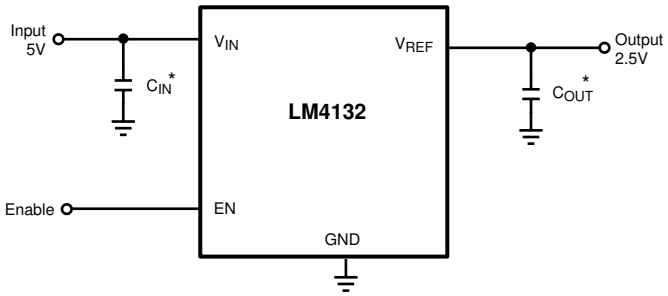

Figure 4-2. Typical LM4132-Q1 Schematic

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
N/C	1	In the actual application, make sure N/C pin is always floating.	D
GND	2	No effect.	D
EN	3	No output voltage. Output is forced OFF	B
VIN	4	No output voltage.	B
VREF	5	No, or low, output voltage. Output current is at short-circuit current limit; thermal shutdown may be activated.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
N/C	1	No effect.	D
GND	2	Output is not regulated.	B
EN	3	EN pin is floating and its state is indeterminable.	B
VIN	4	No output voltage.	B
VREF	5	No output voltage to load.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
N/C	1	GND	In the actual application, make sure N/C pin is always floating.	D
GND	2	EN	No output voltage. Output is forced OFF.	B
EN	3	VIN	Output forced ON.	B
VIN	4	VREF	No VREF regulation. Output voltage is same as input voltage.	B
VREF	5	N/C	In the actual application, make sure N/C pin is always floating.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
N/C	1	In the actual application, make sure N/C pin is always floating.	D
GND	2	No output voltage.	B
EN	3	Output forced ON.	B
VIN	4	No effect.	D
VREF	5	No VREF regulation. Output voltage is same as input voltage. Power supply might experience a current increase.	B

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