AN-2178 LM5118 Four Switch Conversion

ABSTRACT

This application note discusses the conversion of the LM5118 Buck-Boost Controller from a two-switch version to a fully synchronous four-switch version.

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1 Introduction

The LM5118 Buck-Boost Controller is a two switch implementation that means there are two switching MOSFETs and two diodes in the power path. See Figure 1 for a basic schematic. Although a converter based on the LM5118 is very efficient, there are applications where even greater efficiency is required. By replacing the two diodes with MOSFETs, a fully synchronous 4 switch version is realized, with corresponding increase in efficiency. This is shown in Figure 2, in its basic form. All of the unique mode transition capabilities of the LM5118 are preserved in the four switch version. For a complete discussion of the two switch converter, see the *LM5118/LM5118Q Wide Voltage Range Buck-Boost Controller* (SNVS566) data sheet.

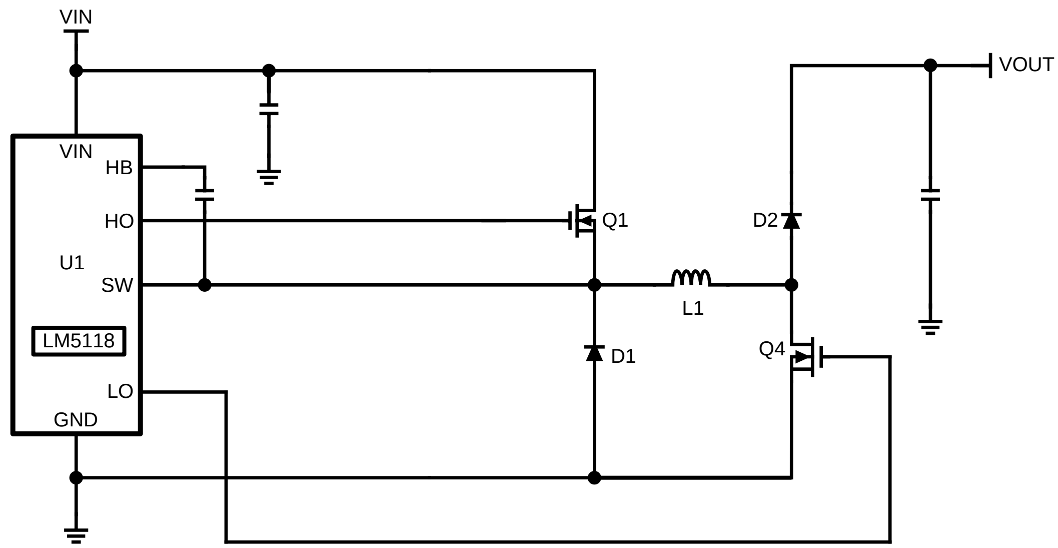

Figure 1. Two Switch Simplified Block Diagram

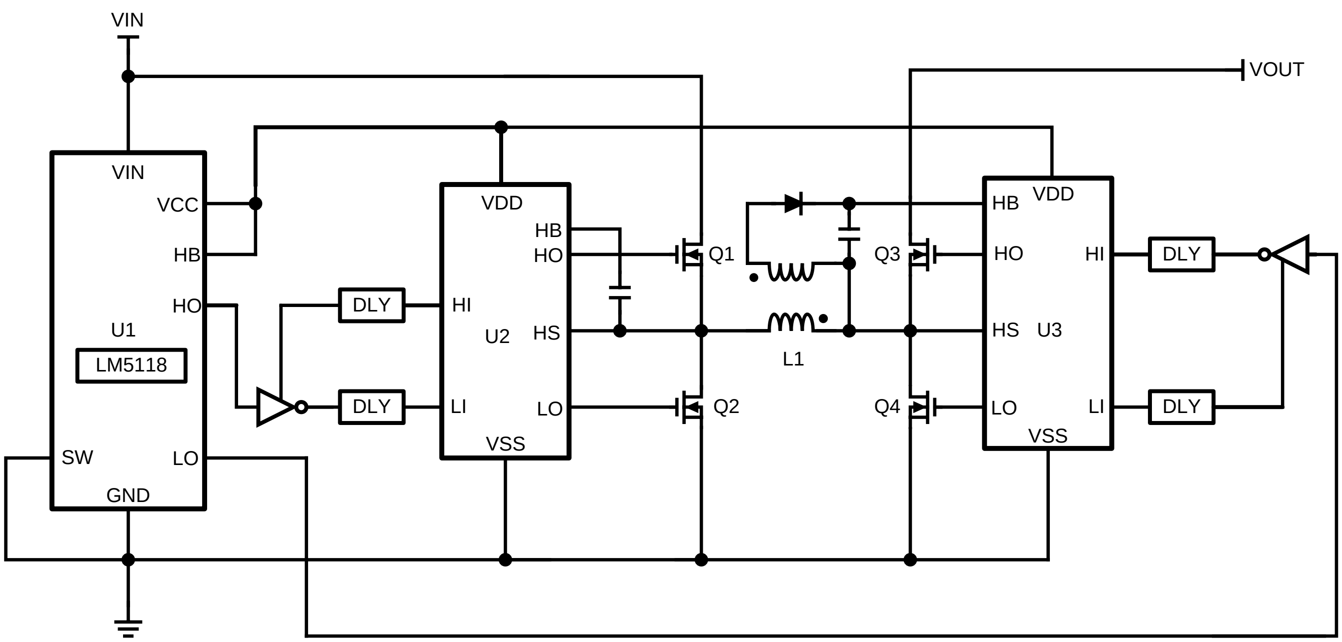

Figure 2. Four Switch Simplified Block Diagram

Referring to Figure 2, two gate drivers and two inverters/buffers are used to implement the logic required to drive the two synchronous MOSFETs, Q2 and Q3. The delay blocks composed of resistors, diodes, and capacitors are required to prevent shoot through. Because Q3 is required to be continuously on during buck operation, a simple voltage supply is generated by a second winding on the inductor, L1. The other high side drive is generated by its internal bootstrap circuitry.

2 Applications Information

The following are specifications are included:

- VIN: 6V to 60V
- VOUT: 12V
- IOUT: 3A
- Switching Frequency: 300 kHz
- Load Regulation: 1%
- Line Regulation: 0.1%
- Over Current Limiting
- Under Voltage Lockout

3 Air Flow

Prolonged operation without airflow at low input voltage and at full power will cause the MOSFETs to overheat. A fan should be used under these conditions.

4 Design Details

The starting point for this design is the LM5118 Applications Board. With the exception of the additional components, all of the standard demo board parts are the same. An inverter with an additional non-inverting output was chosen for the final design to balance the delays through the inverter and buffer. Please refer to Figure 10 for the following discussion.

Because the LM5118 is used as a driver for the inverters, both outputs are referenced to ground. This is accomplished by grounding the HS output of the LM5118 and connecting HB to VCC. Both outputs of the LM5118 are connected to two separate inverter/buffers. The inverter/buffer outputs are connected to the appropriate LI and HI inputs of the gate drivers. The gate driver outputs drive the switching MOSFETs to implement the four switch function. Note the delay circuits consist of a single resistor, diode, and capacitor on the input of the gate drivers. These inputs are high impedance, allowing the use of smaller components as opposed to the output side of the gate drivers. The delay is approximately 40ns with the components chosen. Since this is a wide input range design, some optimization of the delays would be possible with a dedicated design with an improvement in efficiency. If deviations from this design are required, start with a large delay and then tune the delay carefully to an optimum value. Otherwise, shoot through will destroy the MOSFETs.

The high side voltage for U2, which drives the output MOSFET, is derived from the inductor L1. The second winding is connected in a “flyback” or inverted configuration from L1. In the buck mode, the voltage across L1 during the off time (when the flyback winding conducts) is VOUT. During the buck-boost mode, the L1 winding voltage is also VOUT. Therefore, the voltage across the second winding when it conducts is also VOUT for a 1:1 turns ratio. This means the bias voltage for U2 is a constant 12 volts. If a different VOUT is required, adjust L1’s turns ratio accordingly.

5 Precautions

If this design is used at full current at low input conditions, an increase in input capacitance may be required depending on the impedance of the input supply and its associated input connections. During low VIN conditions, the VIN ripple current due to converter switching is relatively high. If the input impedance is high, the associated ripple voltage could either trigger the UVLO during its valley time, or could cause the loop to become unstable. Increasing the input capacitance will solve this possible problem. Make sure the additional capacitance is close to the LM5118 input.

If the converter is only used under lower VIN conditions, the MOSFETs could be optimized for low R_{DSON} and gate threshold. The gate drive voltage will decrease with VIN less than approximately 7.8 volts, so using low threshold MOSFETs for Q1, Q3, and Q4 will also increase efficiency.

In this evaluation board design, LM5113 gate driver was selected to demonstrate its minimum delay. In real application, the voltage limitation of the gate drivers should be carefully considered.

6 Results

A working PCB was constructed for the measurements of the five graphs below that illustrate the improvement in efficiency of the four switch conversion vs. the original two switch LM5118 demo board. Note that the efficiency increases are over 3% under the conditions of the 8V Input graph, and are generally over 2% for most of the operating range. The efficiency at the lower voltages can be improved with the changes suggested in the previous section, if the operating VIN is consistently low.

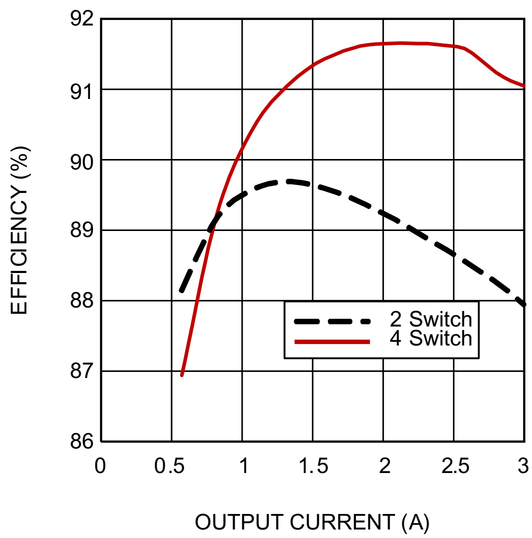

Figure 3. 8V Input

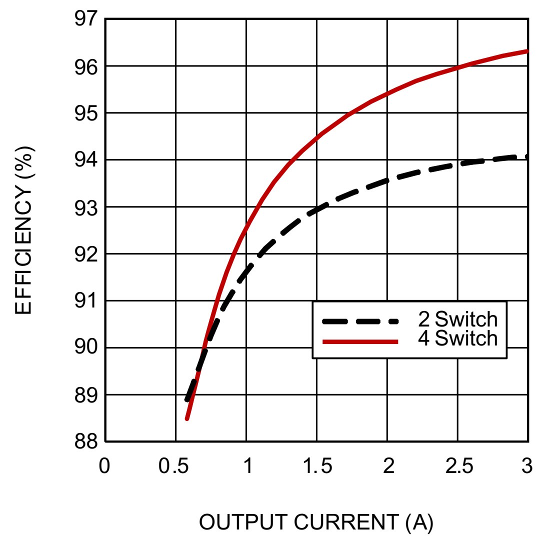

Figure 4. 18 V Input

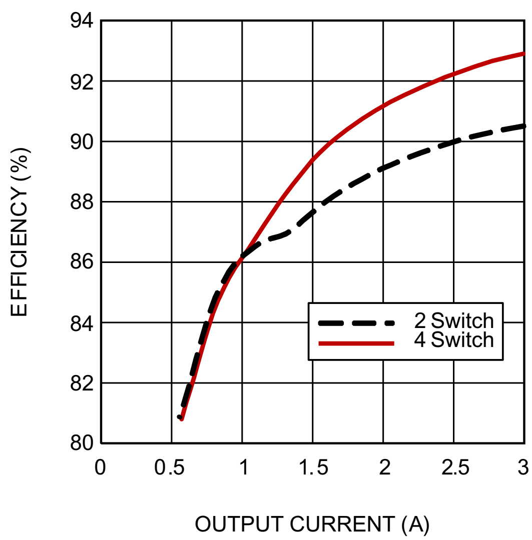

Figure 5. 36 V Input

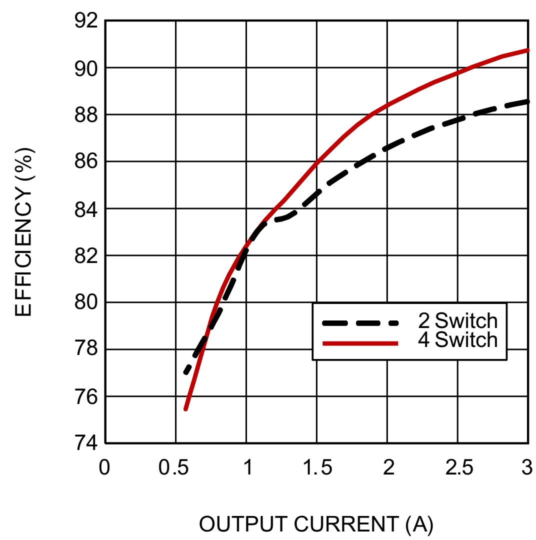

Figure 6. 48 V Input

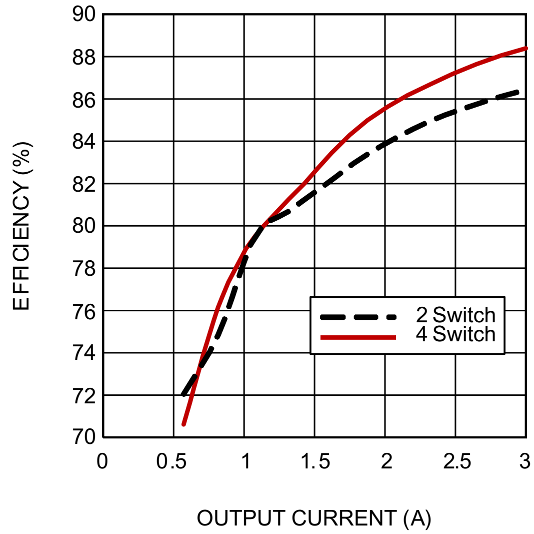

Figure 7. 60 V Input

7 PCB Layout

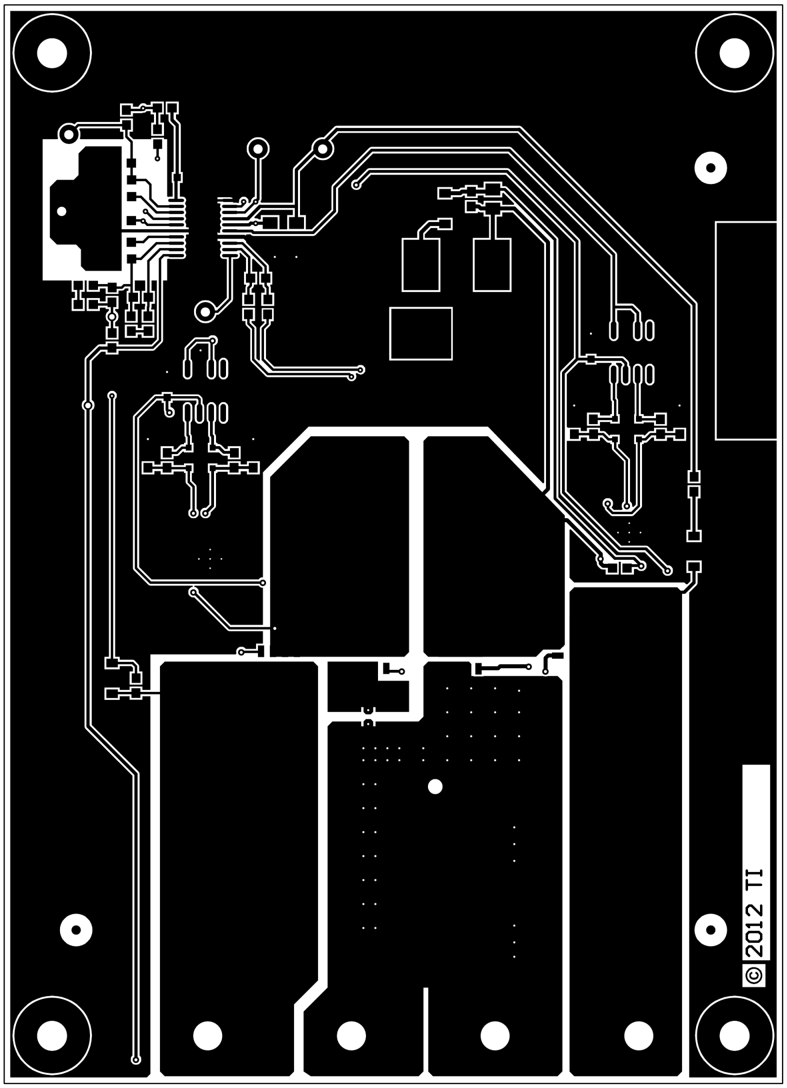

Figure 8. Top PCB Layer

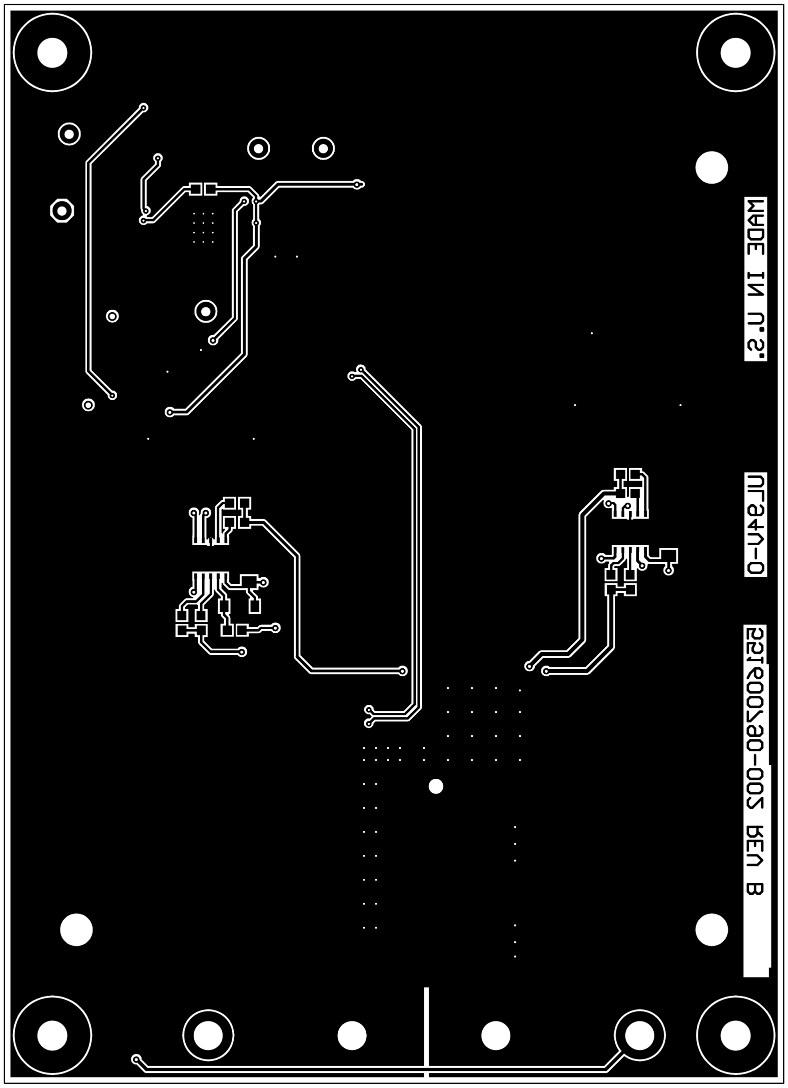

Figure 9. Bottom PCB Layer

The PCB is a two layer design with care taken to minimize high current loops and to separate small signal analog ground from the higher current power ground paths. Input and output capacitances are located to minimize path inductance. The board size is 4.3” X 3.55”. This input and output are located on the same end of the board and are on the “bottom” in Figure 9.

8 Schematic Diagram

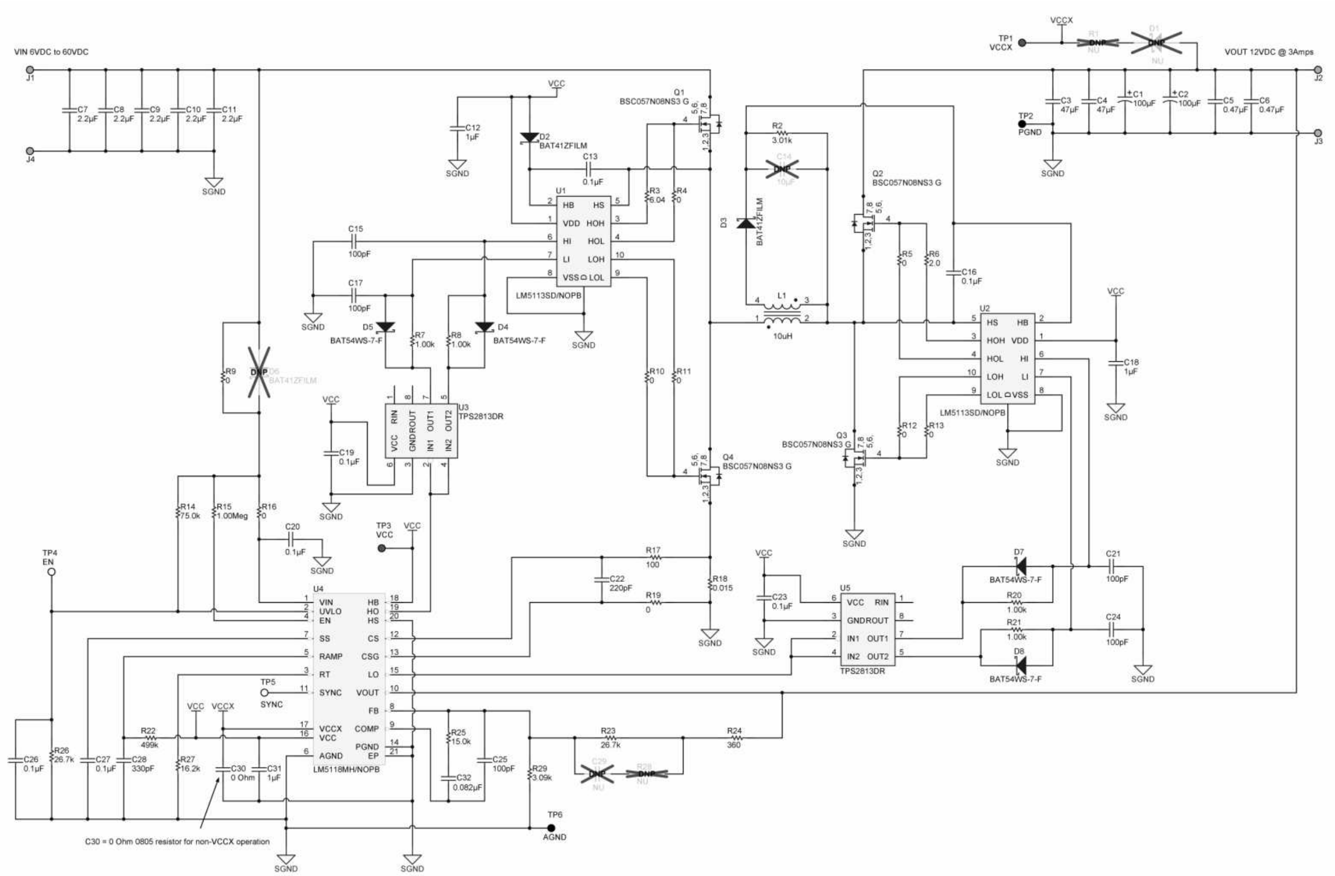

Figure 10. Schematic Diagram

9 Bill of Materials

Table 1. Bill of Materials

Designator	Description	Manufacturer	Part Number
C1, C2	CAP, AL, 100uF, 16V, +/-20%, 0.024 ohm, SMD	Nippon Chemi-Con	APXE160ARA101MF80G
C3, C4	CAP, CERM, 47uF, 16V, +/-10%, X5R, 1210	MuRata	GRM32ER61C476KE15L
C5, C6	CAP, CERM, 0.47uF, 25V, +/-10%, X7R, 1206	AVX	12063C474KAT2A
C7, C8, C9, C10, C11	CAP, CERM, 2.2uF, 100V, +/-10%, X7R, 1210	Taiyo Yuden	HMK325B7225KN-T
C12, C18, C31	CAP, CERM, 1uF, 25V, +/-10%, X7R, 0805	MuRata	GRM219R71E105KA88D
C13, C16, C19, C20, C23, C26, C27	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0603	MuRata	GRM188R72A104KA35D
C15, C17, C21, C24	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H101J
C22	CAP, CERM, 220pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H221J
C25	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C101J5GAC
C28	CAP, CERM, 330pF, 100V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C2A331JA01D
C30	RES, 0 ohm, 5%, 0.125W, 0805	Vishay-Dale	CRCW08050000Z0EA
C32	CAP, CERM, 0.082uF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H823KA93D
D2, D3	Diode, Schottky, 100V, 0.2A, SOD-123	ST Microelectronics	BAT41ZFILM
D4, D5, D7, D8	Diode, Schottky, 30V, 0.2A, SOD-323	Diodes Inc.	BAT54WS-7-F
J1, J2, J3, J4	Terminal, Turret, TH, Double	Keystone	1503-2
L1	Inductor, Coupled, 10uH, 15A	CoilCraft	NA5766-AL
Q1, Q2, Q3, Q4	MOSFET, N-CH, 80V, 100A, PG-TDSON-8	Infineon Technologies	BSC057N08NS3 G
R2	RES, 3.01k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06033K01FKEA
R3	RES, 6.04 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06036R04FKEA
R4, R5, R9, R10, R11, R12, R13, R16, R19	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA
R6	RES, 2.0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06032R00JNEA
R7, R8, R20, R21	RES, 1.00k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031K00FKEA
R14	RES, 75.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060375K0FKEA
R15	RES, 1.00Meg ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031M00FKEA
R17	RES, 100 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100RJNEA
R18	RES, 0.015 ohm, 1%, 3W, 3015	Susumu Co Ltd	KRL7638-C-R015-F-T1
R22	RES, 499k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603499KFKEA
R23, R26	RES, 26.7k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060326K7FKEA
R24	RES, 360 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-07360RL
R25	RES, 15.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060315K0FKEA
R27	RES, 16.2k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060316K2FKEA
R29	RES, 3.09k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06033K09FKEA
TP1, TP3	Test Point, TH, Miniature, Red	Keystone	5000
TP2	Test Point, TH, Multipurpose, Black	Keystone	5011
TP4, TP5	Test Point, TH, Miniature, White	Keystone	5002
TP6	Test Point, TH, Miniature, Black	Keystone	5001
U1, U2	IC GATE DVR HALF BRIDGE 4A 10LLP	TI	LM5113SD

Table 1. Bill of Materials (continued)

Designator	Description	Manufacturer	Part Number
U3, U5	IC DUAL HS MOSFET DRVR 8-SOIC	TI	TPS2813DR
U4	Wide Voltage Range Buck-Boost Controller, 20-pin TSSOP-EP, Pb-Free	TI	LM5118MH
C14, C29			NU
R1, R28			NU
D1, D6			NU

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7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS ANDCONDITIONS OR THE USE OF THE EVMS PROVIDED HEREUNDER, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY WARRANTY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS AND CONDITIONS, OR ANY USE OF ANY TI EVM PROVIDED HEREUNDER, EXCEED THE TOTAL AMOUNT PAID TO TI FOR THE PARTICULAR UNITS SOLD UNDER THESE TERMS AND CONDITIONS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM AGAINST THE PARTICULAR UNITS SOLD TO USER UNDER THESE TERMS AND CONDITIONS SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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