User's Guide

LMG342XEVM-04X User Guide

ABSTRACT

The LMG342XEVM-04X features two LMG342XR0X0 600-V GaN FETs with an integrated driver and protection in a half-bridge configuration with all the required bias circuit and logic/power level shifting. Essential power stage and gate-driving, high-frequency current loops are fully enclosed on the board to minimize power loop parasitic inductance for reducing voltage overshoots and improving performance. The LMG342XEVM-04X is configured for a socket style external connection for easy interface with external power stages to run the LMG342XR0X0 in various applications. Refer to the LMG342XR0X0 data sheet before using this EVM.

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Trademarks

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1 General TI High Voltage Evaluation User Safety Guidelines

Always follow TI's set-up and application instructions, including the use of all interface components within the recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and the safety of those working around you. Contact TI's Product Information Center at http://support/ti./com for further information.

Note

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and/or burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed PCB (printed circuit board) assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise, and knowledge of electrical safety risks in development and application of high-voltage electrical circuits. Any other use or application is strictly prohibited by Texas Instruments. If you are not suitably qualified, you must immediately stop from further use of the HV EVM.

- **Work Area Safety:**
  - Maintain a clean and orderly work area.
  - Qualified observer(s) must be present anytime circuits are energized.
  - Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized; indicating operation of accessible high voltages may be present for the purpose of protecting inadvertent access.
  - All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50 VRMS/75 VDC must be electrically located within a protected Emergency Power Off (EPO) power strip.
  - Use a stable and non-conductive work surface.
  - Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
- **Electrical Safety:**
  - As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
  - De-energize the TI HV EVM and all its inputs, outputs, and electrical loads before performing any electrical or other diagnostic measurements. Confirm that TI HV EVM power has been safely de-energized.
  - After confirming the EVM is de-energized, proceed with the required electrical circuit configurations, wiring, measurement equipment hook-ups, and other application needs while still assuming the EVM circuit and measuring instruments are electrically live.
  - When EVM readiness is complete, energize the EVM as intended.

    WARNING

    While the EVM is energized, never touch the EVM or its electrical circuits as they could be at high voltages capable of causing electrical shock hazard.
- **Personal Safety:**
  - Wear personal protective equipment like latex gloves and safety glasses with side shields, or protect the EVM from accidental touch in an adequate translucent plastic box with interlocks.
- **Limitation for Safe Use:**
  - EVMs are not to be used as all or part of a production unit.

1.1 Safety and Precautions

The EVM is designed for professionals who have received the appropriate technical training and is designed to operate from an AC power supply or a high-voltage DC supply. Read this user guide and the safety-related documents that come with the EVM package before operating this EVM.

CAUTION

Do not leave the EVM powered when unattended.

WARNING

Hot surface! Contact may cause burns. Do not touch!

WARNING

High Voltage! Electric shock is possible when connecting board to live wire. Board must be handled with care by a professional.

For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

2 Introduction

The LMG342XEVM-04X operates as a half-bridge daughter card that can be either part of a larger custom designed system or paired with the mother board. TI provides two mother boards (LMG342X-BB-EVM and LMG34XX-BB-EVM) to interface with LMG342XEVM-04X. LMG342X-BB-EVM can support up to 4-kW, and LMG34XX-BB-EVM can provide up to 1.7-kW. The mother boards are designed to operate LMG342XR0X0 in an open-loop synchronous buck or boost converters. Probe locations are provided to measure the logic and power stage voltages. This board assembly is not suitable for Double Pulse Testing (DPT).

Note

TI provides a custom interposer board that must be used when the LMG342XEVM-04X is paried with the LMG34XX-BB-EVM. The interposer board is not needed with LMG342x-BB-EVM.

2.1 LMG342XEVM-04X Daughter Card

The LMG342XEVM-04X has two LMG342XR0X0 GaN FETs in a half-bridge configuration. All the bias and level shifting components are included, which allows low-side referenced signals to control both FETs. High-frequency decoupling capacitors are included on the power stage in an optimized layout to minimize parasitic inductance and reduce voltage overshoot.

The layout of the board is critical to device's performance and functionality. TI prefers a four-layer or higher layer count board to reduce the parasitic inductance of the layout to achieve suitable performance. Layout guidelines are provided in the *LMG342xR030 600-V 30-mΩ GaN FET With Integrated Driver, Protection, and Temperature Reporting* data sheet to optimize the solder-joint reliability, power loop inductance, signal to ground connection, switched-node capacitance and thermal heat dissipation.

Table 2-1. EVM Version Lookup Table

EVM NAME	FEATURED GaN FET WITH INTEGRATED DRIVER AND PROTECTION
LMG3422EVM-041	LMG3422R050
LMG3422EVM-043	LMG3422R030
LMG3425EVM-041	LMG3422R050
LMG3425EVM-043	LMG3425R030

There are 12 logic pins on the LMG342XEVM-04X.

Table 2-2. Logic Pin Function Description

PIN	PIN DESIGNATION	DESCRIPTION
LS PWM	1	Logic gate signal input for low-side LMG342XR0X0. Compatible with both 3.3-V and 5-V logic. Referenced to AGND.
HS TEMP	2	PWM TEMP output for high-side LMG342XR0X0. Referenced to AGND.
LS Fault	3	FAULT output signal for low-side LMG342XR0X0. Referenced to AGND.
HS OC	4	OC output signal for high-side LMG342XR0X0. Referenced to AGND.
LS OC	5	OC output signal for low-side LMG342XR0X0. Referenced to AGND.
HS Fault	6	FAULT output signal for high-side LMG342XR0X0. Referenced to AGND.
LS Temp	7	PWM TEMP output for low-side LMG342XR0X0 . Referenced to AGND.
HS PWM	8	Logic gate signal input for high-side LMG342XR0X0. Compatible with both 3.3-V and 5-V logic. Referenced to AGND.
12V	9	Auxiliary power input for when the LMG342XEVM-04X is configured in bootstrap mode. Pin is not used when configured in isolated power mode.
5V	10	Auxiliary power input for the LMG342XEVM-04X. Used to power logic isolators. Used as input bias power of LMG342XR0X0 devices when configured in isolated power mode.
AGND	11,12	Logic and bias power ground return pin. Functionally isolated from PGND.

There are six power pins on the LMG342XEVM-04X.

Table 2-3. Power Pin Function Description

PIN	DESCRIPTION
SW	Switch node of the half-bridge configuration
HV	Input DC voltage of the half-bridge configuration
PGND	Power ground of the half-bridge configuration. Functionally isolated from AGND.

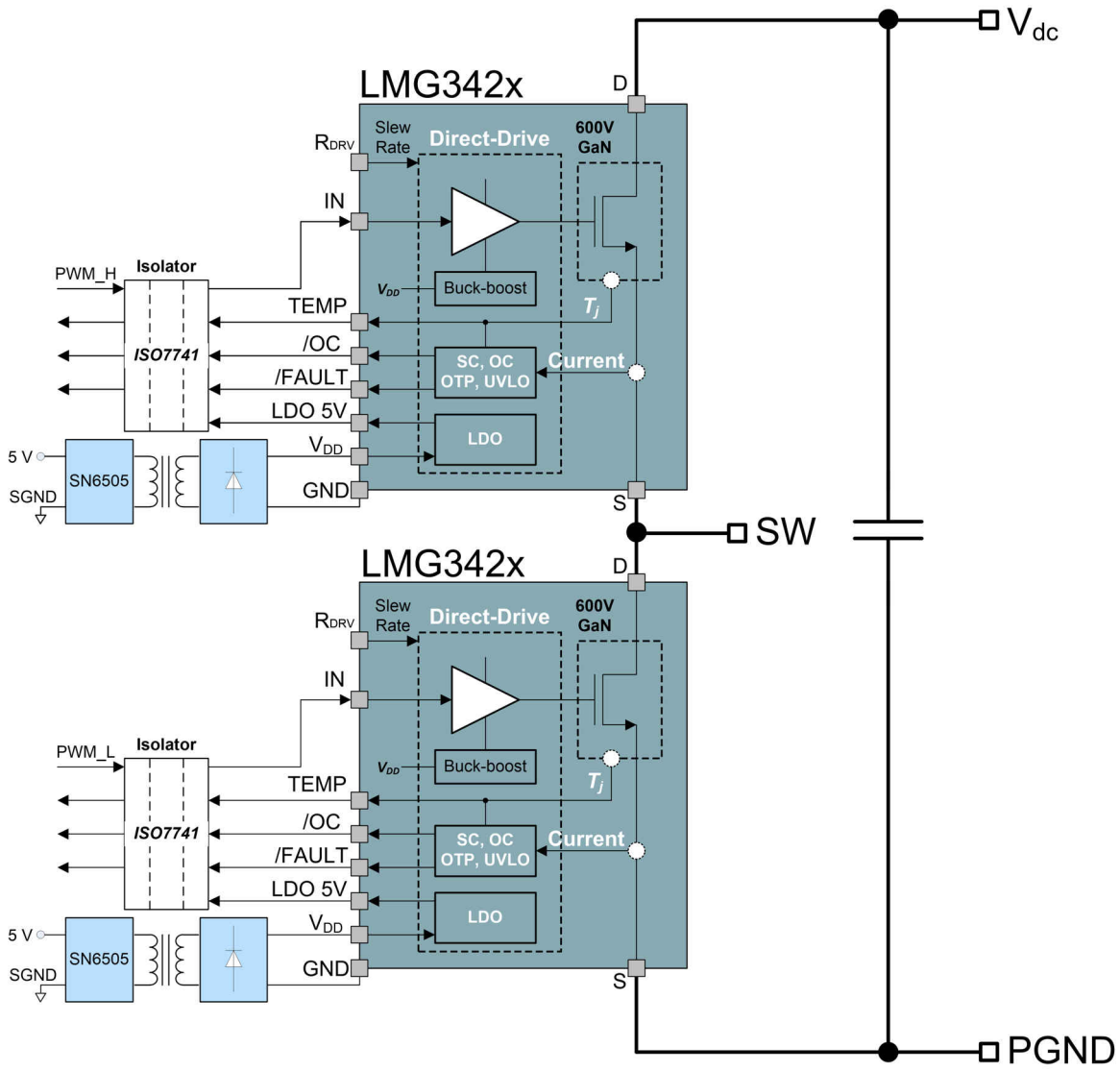

Figure 2-1. LMG342XEVM-04X Block Diagram

CAUTION

High-voltage levels are present on the evaluation module whenever it is energized. Take proper precautions when working with the EVM.

2.1.1 FAULT and OC

The FAULT and OC pins of the LMG342XEVM-04X are active low when an undervoltage lockout occurs on an auxiliary voltage rail, when an overtemperature event occurs, or when an overcurrent/short-circuit event occurs on the LMG342XR0X0. The signals are level-shifted to AGND. Refer to the LMG342XR0X0 data sheet for operation details.

CAUTION

Do NOT ignore a FAULT signal when using the LMG342XEVM-04X. Turn off both top and bottom devices if any device generates a FAULT signal. The device under a fault condition may operate in the undesired third-quadrant mode and can overheat or become damaged due to the high source-drain voltage drop if the other device is still switching.

2.1.2 Power Pins

There are some high frequency decoupling capacitors on the LMG342XEVM-04X from VDC to PGND to minimize voltage overshoot during switching, but more bulk capacitance is required to hold up the DC voltage during operation. TI recommends preventing any overlap and parasitic capacitance from VSW to VDC, PGND, and any logic pins. The two ground PGND and AGND pins are functionally isolated from each other on the LMG342XEVM-04X.

2.1.3 Bootstrap Mode

The LMG342XEVM-04X card can be modified to operate in bootstrap mode, where the 12-V bias voltage is used to power both LMG342XR0X0 devices. This mode can be achieved by the following modifications to the EVM:

1. Remove R1.
2. Place a 2-Ω resistor on R2.
3. Place a 600-V SOD-123 diode on D1, such as UFM15PL-TP.
4. Adjust Rdrv resistor for the low side to be above 70 kΩ, which corresponds to a slew rate below 60 V/ns for the low side. During starup, FAULT signal from the top GaN device is used to control Q1 on the bottom GaN device to operate it at lower slew rate. Once the bootstrap power supply is ready, the bottom GaN, U2 switch to normal operation which is higher slew rate.

2.1.4 Heat Sink

The heat sink is installed to help with heat dissipation of the LMG342XR0X0. Exposed copper pads are attached to the die attach pad (DAP) on the high-side and low-side devices to provide a low thermal impedance point for the heat sink. The two copper pads have a high-voltage potential difference between them, therefore an electrically isolated thermal interface material (TIM) is required.

For optimal thermal dissipation and board level reliability, recommendation for thermal via pattern and solder paste example are provided in the *LMG342xR030 600-V 30-mΩ GaN FET With Integrated Driver, Protection, and Temperature Reporting* data sheet. Pin numbers 1, 16, 17 and 54 are NC (no connection) which are used to anchor QFN package to PCB. These pins must be soldered to PCB landing pads which have to be non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally, pins 1 and 16 are connected to DRAIN and pins 17 and 54 are connected to SOURCE/GND and THERMAL PAD. All pads must be NSMD for mechanical performance, refer to the device datasheet for trace connection recommendations to the pads. Filling the thermal pad with thermal vias is recommended for thermal performance. Vias must be filled and planarized.

In this daughter card design, 'S05MZZ12-A' heatsink and 'GR80A-0H-50GY' (thermal conductivity of 8 W/m·K and thickness of 0.5 mm), thermal interface material has been used. More details on thermal performance and comparison between different TIM are shown in *Thermal Performance of QFN 12x12 Package for 600-V GaN Power Stage* application note.

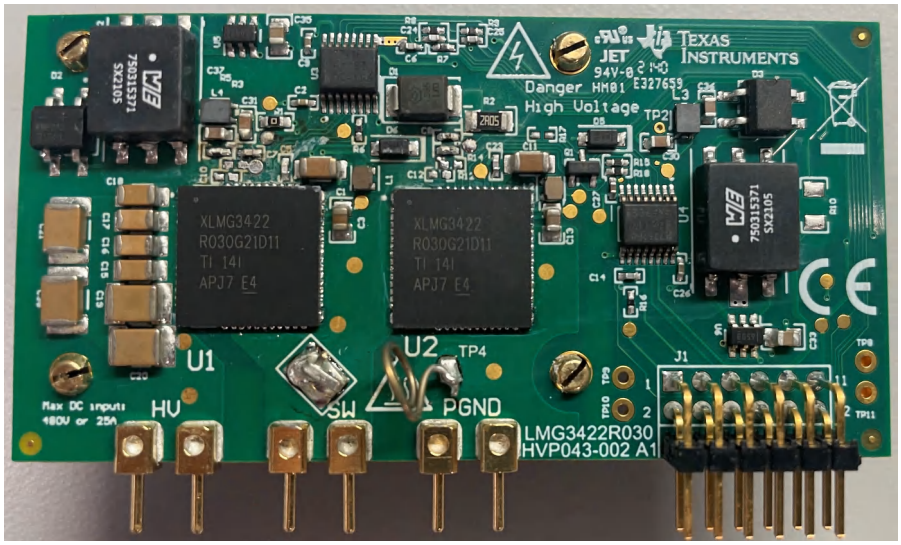

Figure 2-2. Front Side View of the EVM

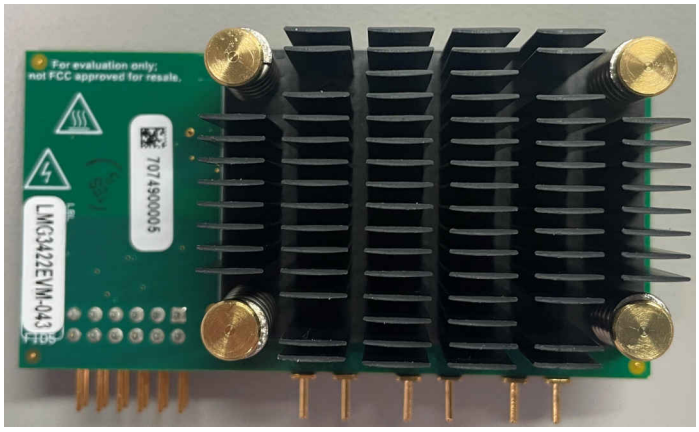

Figure 2-3. Back Side View of the EVM

2.2 Mother Boards

Two mother boards are available from TI: LMG342X-BB-EVM and LMG34XX-BB-EVM.

Note

TI provides a custom interposer board that must be used when the LMG342XEVM-04X is paried with the LMG34XX-BB-EVM. The interposer board is not needed with LMG342x-BB-EVM.

2.2.1 Bias Supply

The motherboard requires one 12-V bias supply. A linear dropout regulator (in LMG34XX-BB-EVM) or buck regulator (in LMG342X-BB-EVM) steps the voltage down to a tightly regulated 5-V for the logic and auxiliary power of the LMG342XR0X0 when the LMG342XEVM-04X is configured in isolated power mode.

2.2.2 PWM Input

Both LMG342X-BB-EVM and LMG34XX-BB-EVM mother boards have on-board complementary PWM generation circuits that create a pair of complimentary PWM signals out of a single PWM input. A 0-V to 5-V square wave input is recommended. In LMG34XX-BB-EVM, the default dead time is 50ns, and other values are achievable by changing the resistance values (R1 and R5). In LMG342X-BB-EVM mother boards, the dead time can be easily adjusted by tuning the trimmer resistance values (R3 and R15).

2.2.3 Fault Protection

There is an option to disable the PWM input to the daughter card in the event of a fault signal from the LMG342XEVM-04X. When the FAULT Protect jumper is placed in the EN mode, PWM is disabled when either LMG342XR0X0 has an active fault. This disable is not latching, so PWM immediately resumes when the fault clears. If the FAULT Protect mode is not desired, that mode can be disabled by placing the jumper in the DIS position. The FAULT LED will still illuminate when either LMG342XR0X0 has an active fault, regardless of the position of FAULT Protect jumper.

2.3 Typical Applications

The LMG342XEVM-04X is designed for use in AC/DC, DC/DC and DC/AC applications:

- Totem-Pole PFC Converters
- Phase-Shifted Full Bridge or LLC Converters
- Inverters
- Buck or Boost Converters

2.4 Features

The LMG342XEVM-04X has the following features and specifications:

- Overtemperature, overcurrent, short-circuit, and undervoltage lockout protection with FAULT and OC indication that is level-shifted to an AGND referenced signal
- A real-time digital output with its duty cycle indicating the device's junction temperature
- Cycle-by-cycle overcurrent protection and latched short-circuit protection
- Gate logic input support of either 3.3-V or 5-V logic
- Maximum recommended operating voltage of 480-V and absolute maximum voltage of 600-V

The mother boards have the following features and specifications:

- Requires only a single 12-V bias supply
- Requires only a single 0-V to 5-V PWM input to generate a gate drive signal
- PWM disables in the event of a fault from the LMG342XEVM-04X
- Maximum recommended operating voltage of 480-V and absolute maximum voltage of 600-V

3 LMG342XEVM-04X Schematic

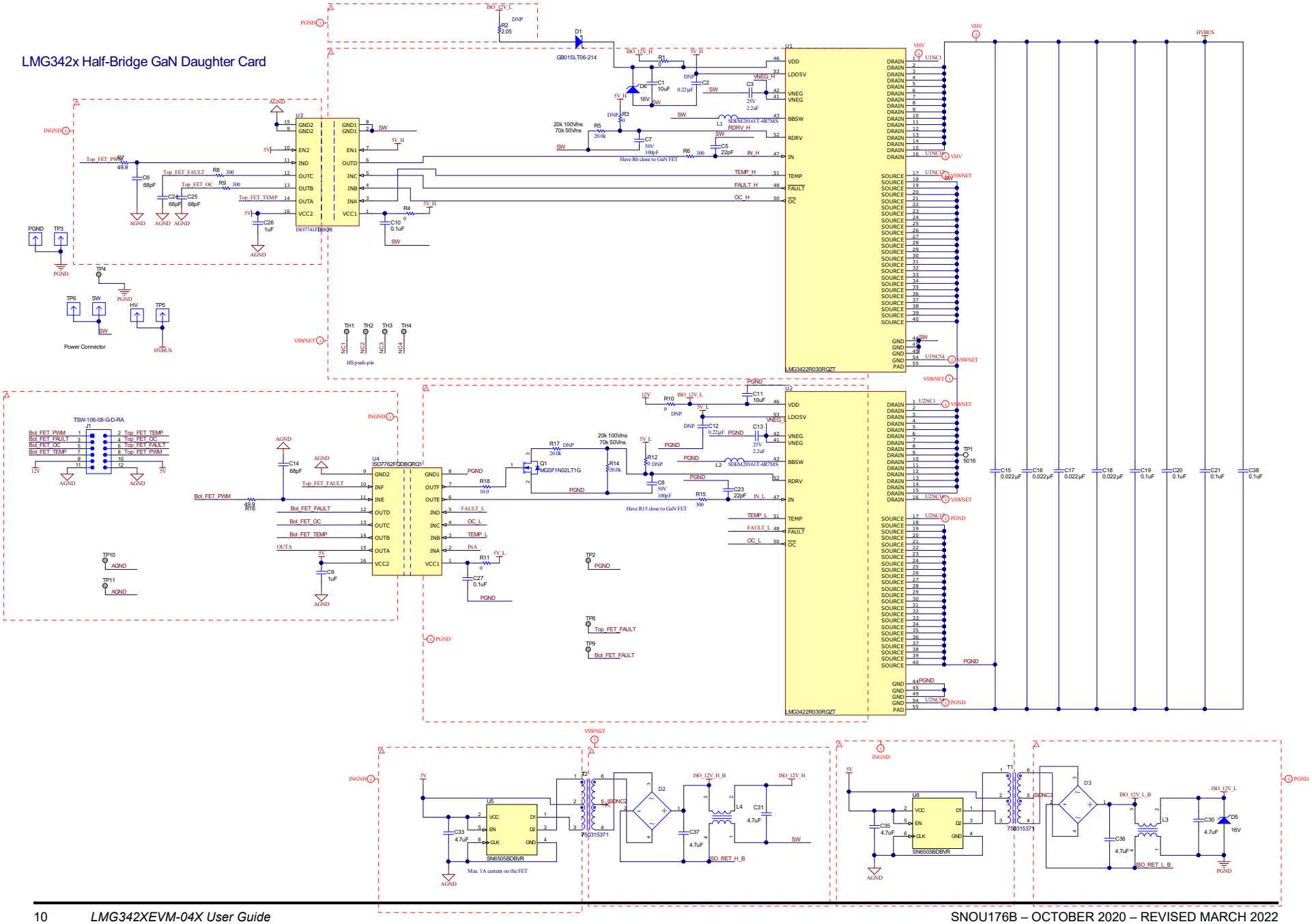

Figure 3-1. LMG342XEVM-04X Schematic

Here are some of the guidelines while designing with LMG342x.

The ISO77xx series provides the best common-mode transient immunity capability. It is highly recommended to use ISO77xxF series which has default output as LOW in the case of carrier signal is affected by the common-mode noises, helping to avoid any shoot throughs for PWM signals. An RC filter is recommended on the isolator output for FAULT signal and OC signal in order to reduce teh CMTI noises. A 100 pF capacitor is recommended in parallel to the Rdrv resistors (R5 and R14) to mitigate the high-frequency noises coupled to slew-rate setting circuit.

Slew rate of the GaN device can be adjusted by changing the resistor connection at the RDRV pin. At very high slew rate operation (such as RDRV connected to GND), LDO5V pin may get overstressed due to ground bouncing. During such condition, it is recommended to remove capacitor closer to LDO5V (C2 and C12) and add a small resistor of 10 ohm (R4 and R11) between this pin and VCC of digital isolators. This helps in mitigating the over voltage stress on the LDO5V.

For the bootstrap power supply operation, a SiC Schottky diode (GB01SLT06-214) is recommended. The bootstrap resistance is suggested to be 2 Ω for high-frequency and low-duty cycle operations. Also, a large footprint SMD resistors with copper vias is preferred for thermal management. A 16V Zener diode needs to be placed close to the high-side Vdd pin. When bootstrap is used, the low-side GaN device's slew rate needs to be controlled during the start-up. When the high-side power supply is fully charged, the low-side device can shift back to a higher slew rate in normal operation. This is realized using Q1 and R18. R14 of 100 kΩ is used to control the slew rate.

4 Mother Board Schematic

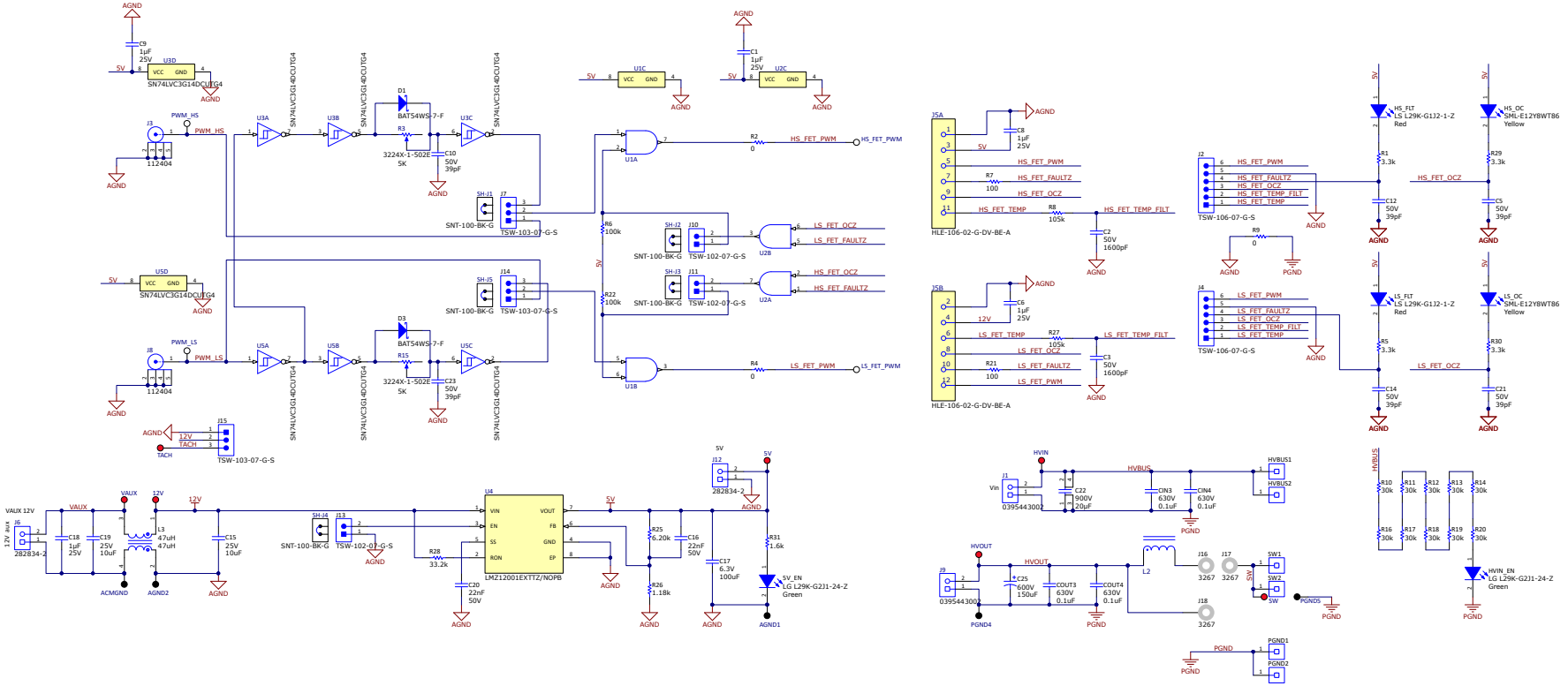

Figure 4-1. LMG342X-BB-EVM Schematic

TI HV Synchronous Buck Motherboard

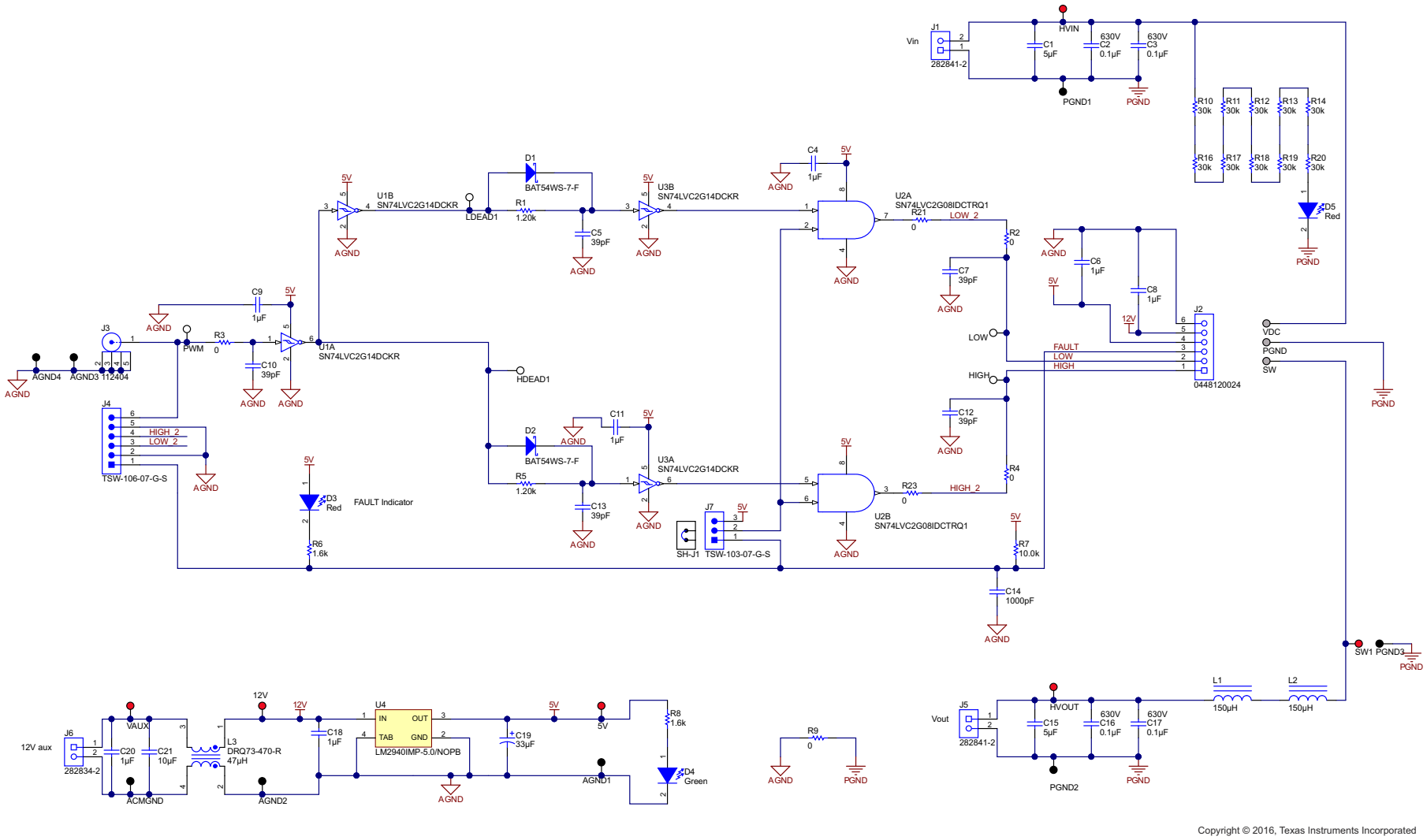

Figure 4-2. LMG34XX-BB-EVM Schematic

5 Recommended Footprint

When the EVM daughter card is used in a custom design system, the recommended footprint to interface with the LMG342XEVM-04X daughter card is shown below.

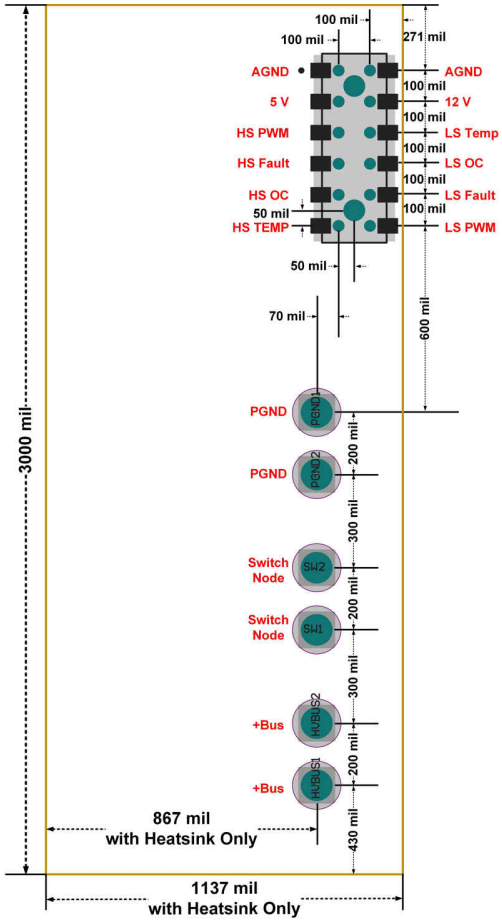

Figure 5-1. Recommended Footprint for LMG342XEVM-04X

6 Test Equipment

DC Voltage Source: Capable of supplying the input of the EVM up to 480 V.

DC Bias Source: Capable of 12-V output up to 1.5-A.

Function Generator: Capable of 0-V to 5-V square wave output with adjustable duty cycle and frequency in the operating range. TI recommends operating the LMG342XEVM-04X and mother boards with a switching frequency between 50 kHz to 200 kHz in hard-switching converters.

Note

TI provides a custom interposer board that must be used when the LMG342XEVM-04X is paried with the LMG34XX-BB-EVM. The interposer board is not needed with LMG342x-BB-EVM.

Oscilloscope: Capable of at least 200 MHz operation. A 1 GHz or greater oscilloscope and probes with short ground springs are required for accurate measurements.

DC Multimeter(s): Capable of 600-V measurement, suitable for determining operation and efficiency (if desired).

DC Load: Capable of 600-V operation at up to 20-A in current-mode operation.

Fan: For the heatsink-version EVM daughter card, a dedicated cooling fan is attached on the back side of the heatsink. Please make sure the fan is powered by the 12-V power supply before test.

7 Test Procedure When Paired With LMG342X-BB-EVM

7.1 Setup

The inductor on LMG342X-BB-EVM is capable of around 3-kW operation. For higher power levels, use an external inductor.

TI recommends the following procedure to set up the LMG342X-BB-EVM with the LMG342XEVM-04X:

1. Connect the LMG342XEVM-04X to LMG342X-BB-EVM as shown in Figure 7-1. The area for connection on the mother board is shown in Figure 7-2.
2. Install the LMG342X-BB-EVM inside a ventilated HV safety box.
3. Disconnect jumper J13 to enable the 12-V to 5-V onboard power conversion.
4. Disconnect jumper J12.
5. If the onboard complementary PWM generation circuits are used to generate the dead time, please connect Pin 2 to Pin 3 for header J7 and J14 with jumpers. Under this configuration, only one PWM signal is required and it can be connected to either J3 or J8.
6. If two complementary PWM signals with dead time are provided to J3 (high-side PWM) and J8 (low-side PWM), then please connect Pin 1 to Pin 2 for header J7 and J14 (Pin1 of J7 and J14 are indicated in Figure 7-2). This action allows the two PWM signals to directly control the high-side and low-side devices.
7. If fault interlock feature is desired, please connect jumper J10 and J11. Otherwise, disconnect them and the PWM signals can always pass through to the devices.
8. Set the signal generator to a desired frequency and duty cycle (that is, 100 kHz, and 50% duty cycle). 5 V for high input and 0 V for low input.
9. Connect the signal generator output to the LMG342X-BB-EVM PWM input as shown in Figure 7-2.
10. Connect 12-V, 2-A DC power supply to the LMG342X-BB-EVM 12-V bias supply as shown in Figure 7-2.
11. Connect the high voltage power supply to the LMG342X-BB-EVM high voltage input for buck mode (High Voltage) as shown in Figure 7-2.
12. Provide 12-V bias supply to fan by connecting the 3-pin power cord from fan to J15.

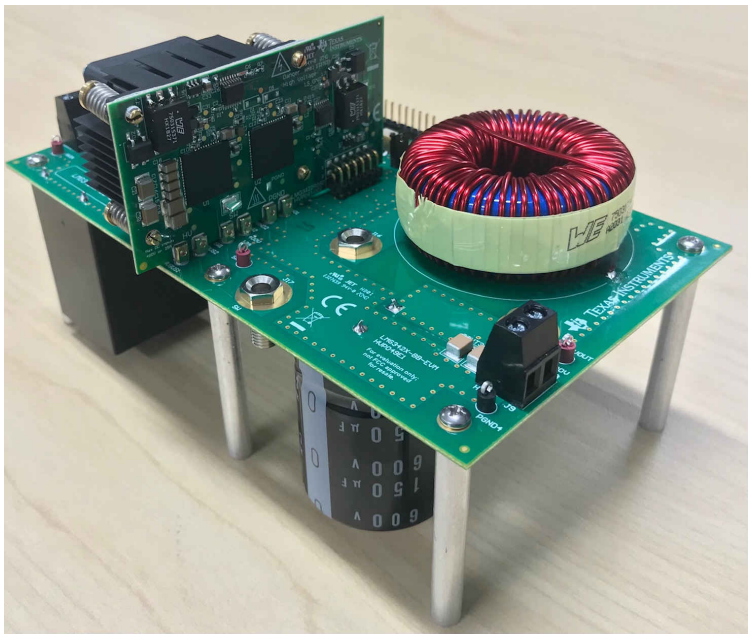

Figure 7-1. LMG342X-BB-EVM Motherboard With LMG342XEVM-04X

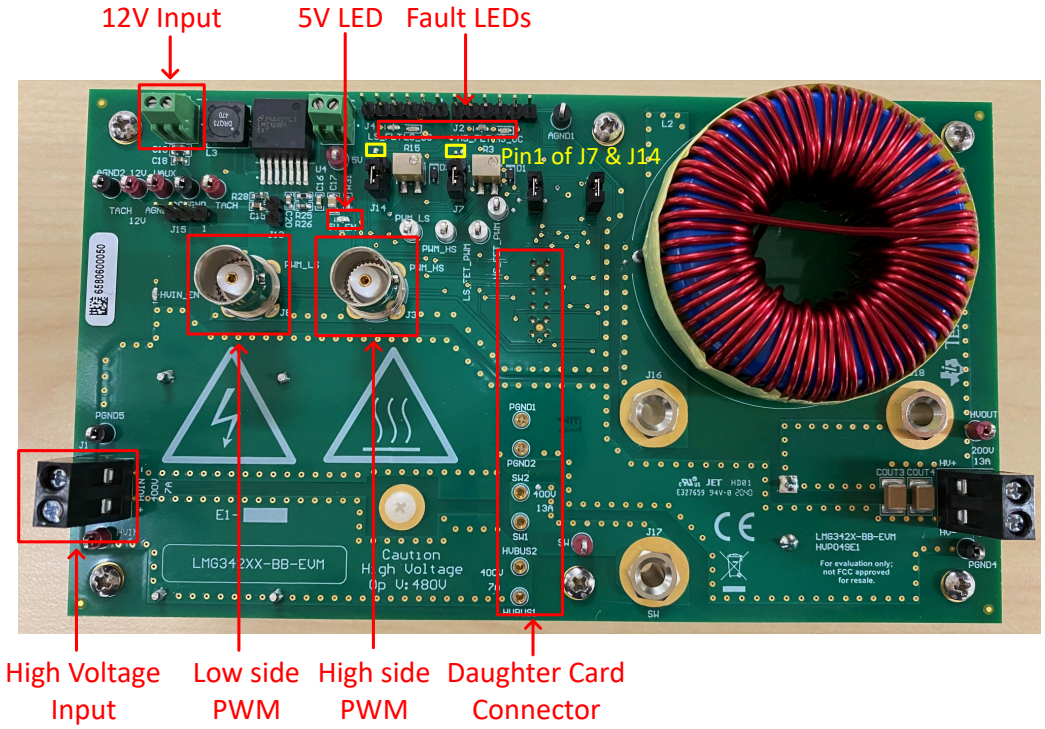

Figure 7-2. Connector and LEDs on the LMG342X-BB-EVM

7.2 Start-Up and Operating Procedure

1. Turn on +12VDC to the LMG342X-BB-EVM. Watch the power supply for the DC current to settle down after approximately 3 to 5 seconds.
2. Make sure all the fault LEDs are off and the 5-V LED is on.
3. Turn on +12VDC to enable the fan.
4. Turn on the function generator to output the continuous pulse, and check the deadtime of the PWM signals.
5. User proper probes for measurement. To measure the fast switching transient in the switch-node, it is recommended to use the high-bandwidth high-voltage passive probes with minimized ground loop connections.
6. It is recommended to add common-mode chokes to the measurement signals and to the power input/output connections.
7. Enable the high voltage power supply and make sure to ramp the voltage up gradually from 0V to the desired bus voltage (up to 480V). As the voltage is ramping up, the HV LED will turn on and become brighter.

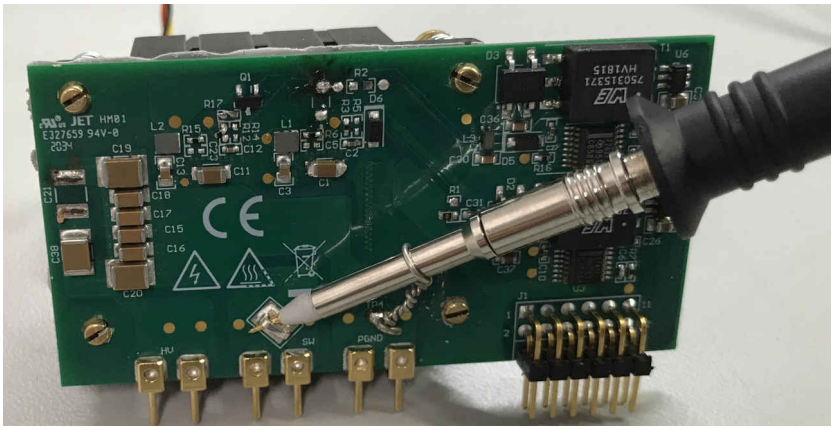

Figure 7-3. Switch-Node Voltage Measurement with High-Bandwidth Probe and Pigtail Ground Connection

WARNING

Do NOT turn on the device at the absolute maximum voltage. TI recommends to start the device at or below 480 V. Slowly increase the input voltage and monitor the VSW to ensure the peak voltage does not exceed the absolute maximum rating of 600 V.

7.3 Test Results

In this test example, a synchronous buck converter operation is implemented. The input voltage is 400 V, and the output voltage is 200 V with 50% duty cycle. With the heatsink-version EVM, the inductor current goes to 20 A in this test, and an output power of 4 kW is achieved. The waveform for continuous operation is shown in Figure 7-4 . The slew rate is set to 85 V/ns by connecting 20 kohm between Rdrv and ground. From this waveform, a turn-on voltage slew rate of 85 V/ns is observed at 400 V/20 A switching conditions.

The turn-on slew-rate of the device can be easily adjusted from 30V/ns to 150V/ns by changing the Rdrv resistor values. This is also verified from the test results shown in Figure 7-7. The adjustable slew-rate feature provides a flexibility to adapt the device's switching speed in different applications.

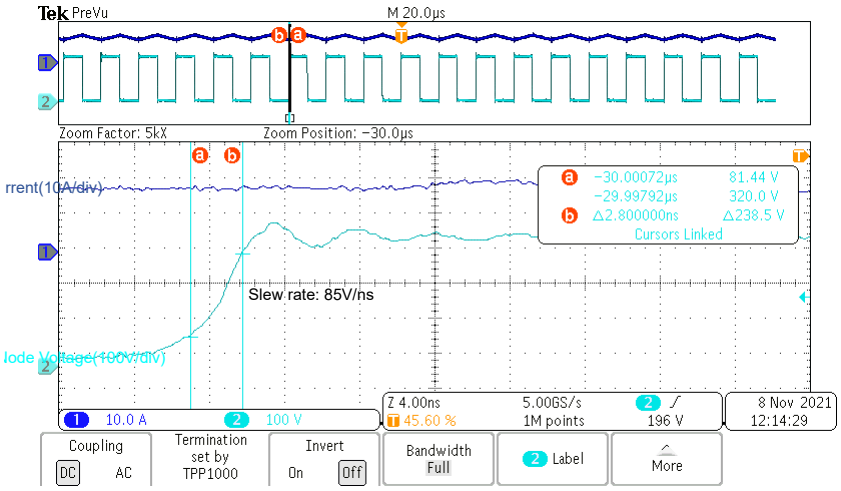

Figure 7-4. 85 V/ns at 400 V/20 A

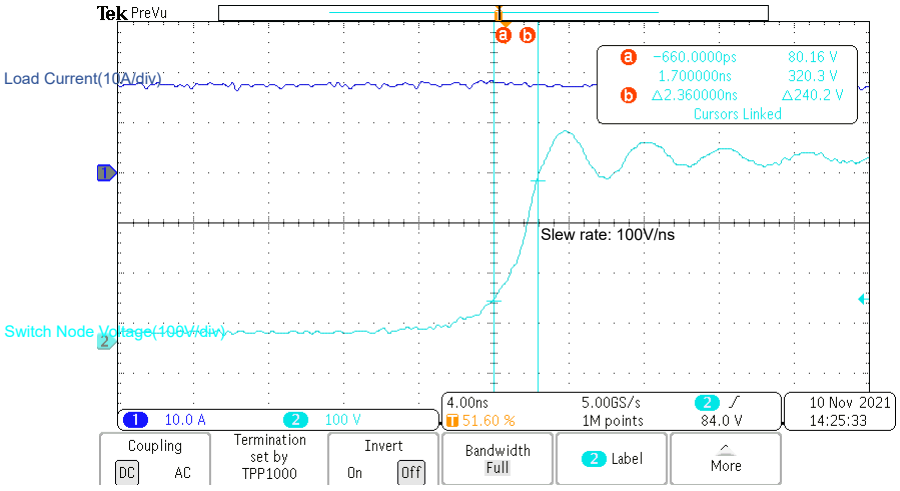

Figure 7-5. 100 V/ns at 400 V/20 A

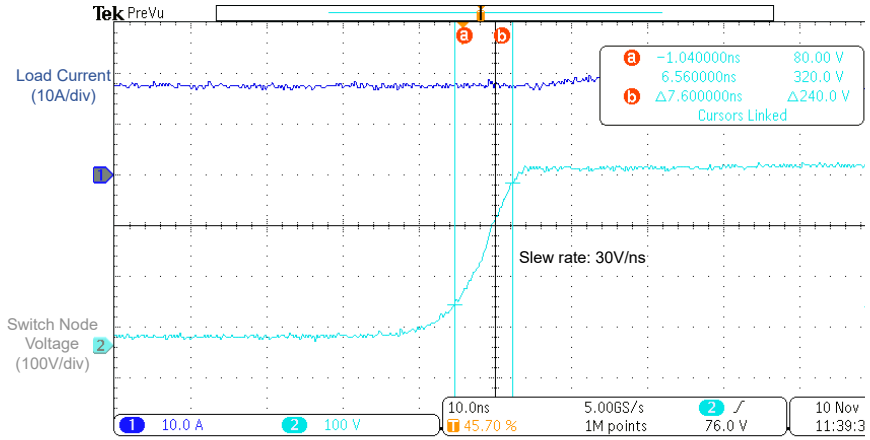

Figure 7-6. 30 V/ns at 400 V/20 A

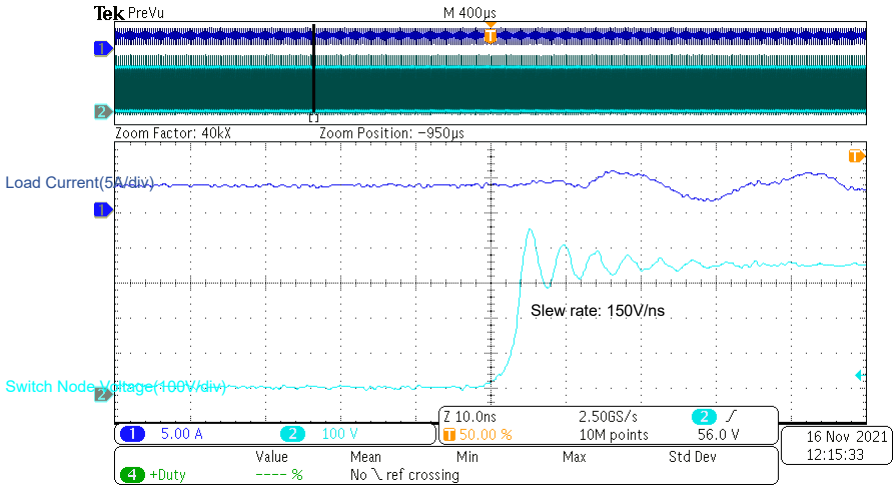

Figure 7-7. 150 V/ns at 400 V/5 A

7.4 Shutdown Procedure

1. Turn off the high voltage power supply then PWM. Wait until red “HV Enable” LED turns off.
2. Disable the 12-V bias supply.

7.5 Additional Operating Notes

- Fault protection on the LMG342X-BB-EVM is not latching, therefore PWM will resume if a fault clears and the LMG342X-BB- EVM is still operational.

8 Test Procedure When Paired With LMG34XX-BB-EVM

8.1 Setup

The following procedure is recommended to set up the LMG34XX-BB-EVM with the LMG342XEVM-04X. The inductor on the LMG34XX-BB-EVM is capable of up to 1.7-kW operation. For a higher power level, use an external inductor.

Figure 8-1 shows the LMG342XEVM-04X connected to the LMG34XX-BB-EVM.

Note

TI provides a custom interposer board that must be used when the LMG342XEVM-04X is paired with the LMG34XX-BB-EVM. The interposer board is not needed with LMG342x-BB-EVM.

Figure 8-1. LMG342XEVM-04X Connected to the LMG34XX-BB-EVM

Figure 8-2 shows the LMG34XX-BB-EVM power and probe connection points.

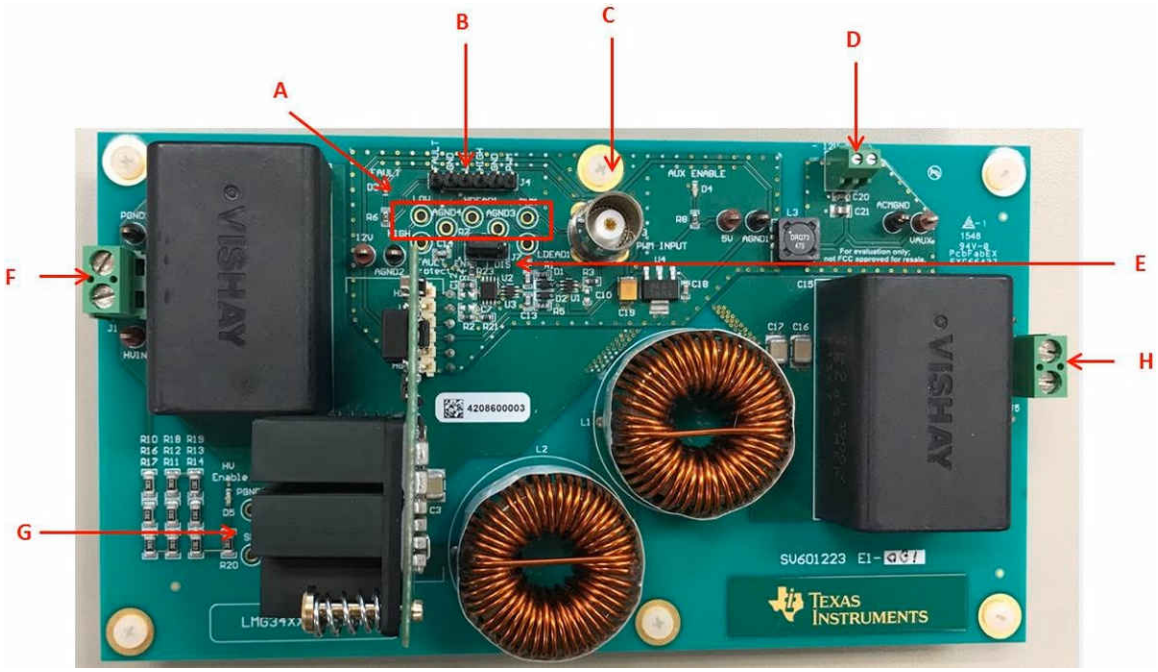

Figure 8-2. Recommended Connection Points

PCB Notes:

- A: Probe points for gate drive logic
- B: 100-mil header for PWM input, PWM signals to LMG342XEVM-04X and FAULT output
- C: BNC connector for PWM input
- D: 12-V bias supply input
- E: FAULT protection option header
- F: Power stage high voltage input
- G: Probe point for power stage switch node
- H: Power stage high voltage output

To connect the LMG342XEVM-04X to the LMG34XX-BB-EVM:

1. Connect the oscilloscope or multimeter probes to the desired test points in A or G.
2. Connect the 12-V bias supply, connect load to output, and connect the input supply to input.
3. Connect the function generator to either the BNC connector PWM input at C or 100-mil header connector input at pin 6 (PWM) and pin 5 (GND) at B.
4. Connect 12-V bias supply to the fan attached on the EVM, or enable an external fan to direct airflow across the heat sink attached to the LMG342XEVM-04X.

8.1.1 List of Test Points

Key test points on this EVM are designed for oscilloscope probes with short ground springs. Using short ground springs instead of alligator ground leads will minimize measurement error and produce a cleaner signal with the fast switching GaN devices used on this EVM. The data in this user guide uses this measurement method.

Table 8-1. Test Point Functional Description

NAME	DESCRIPTION
VAUX	12-V bias input connection before filter
ACMGND	Ground for 12-V bias input before filter
5V	5-V bias
AGND1	Analog ground for logic
PWM	Single input PWM signal
LDEAD1	Low-side PWM signal before dead time generation
AGND3	Analog ground for logic
HDEAD1	High-side PWM signal before dead time generation
AGND4	Analog ground for logic
LOW	Low-side PWM signal with dead time
HIGH	High-side PWM signal with dead time
AGND2	Analog ground for logic
12V	12-V bias after filter
PGND1	Power ground
HVIN	DC input voltage
PGND2	Power ground
HVOUT	DC output voltage
PGND3	Power ground
SW1	Switch node voltage

For this EVM version, not all the test points are available on the motherboard due to the size of the daughter card. To probe the switching node, TI recommends using a pigtail on the daughter card on PGND pin. A probe could use the PGND pigtail and SW test point on the daughter card to complete the measurement.

8.1.2 List of Terminals

Table 8-2. List of Terminals

TERMINAL	NAME	DESCRIPTION
J1	VIN	Input DC voltage input
J5	VOUT	Output DC voltage output
J6	12V AUX	12-V bias voltage input
J3	PWM INPUT	Single 0-V to 5-V PWM input for gate
J4	LOGIC	Header to connect PWM, FAULT logic
J2	HB Card PIN	Connector to interface LMG342XEVM-04X board

8.2 Start-Up and Operating Procedure

The following procedure is recommended to enable the LMG342XEVM-04X with the LMG342XEVM-04X:

1. Power up the 12-V bias supply. Ensure the top right green “Aux Enable” LED is illuminated.
2. Enable PWM on the function generator.
3. Power up the high voltage input supply. Ensure the red “HV Enable” LED is illuminated when the input supply is above 20 V.

WARNING

Do NOT turn on device at absolute maximum voltage. TI recommends starting at voltages at or below 480 V, and then increase the input voltage slowly while monitoring VSW to insure the peak voltage does not exceed the absolute maximum rating of 600 V.

8.3 Shutdown Procedure

1. Turn off the high voltage power supply then PWM. Wait until the red “HV Enable” LED turns off.
2. Disable the 12-V bias supply.

8.4 Additional Operation Notes

- Fault protection on the LMG34XX-BB-EVM is not latching, therefore PWM will resume if a fault clears and the LMG34XX-BB- EVM is still operational.

9 Bill of Materials

Table 9-1. Bill of Materials for LMG342XEVM-04X

DESIGNATOR	QTY	DESCRIPTION	PART NUMBER
C1, C11	2	CAP, CERM, 10 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 1206	TMK316AB7106KLHT
C2, C12	2	CAP, CERM, 0.22 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D
C3, C13	2	CAP, CERM, 2.2 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	CGA4J3X7R1E225K125AB
C5, C23	2	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	GCM1555C1H220JA16D
C6, C14	2	CAP, CERM, 68 pF, 50 V, +/- 5%, C0G/NP0, 0402	GCM1555C1H680JA16D
C9, C26	2	CAP, CERM, 1 µF, 35 V,+/- 10%, X5R, AEC-Q200 Grade 3, 0402	GRT155R6YA105KE13D
C10, C27	2	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71H104KE02D
C15, C16, C17, C18	4	CAP, CERM, 0.022 µF, 1000 V,+/- 10%, X7R, AEC-Q200 Grade 1, 1206	C1206C223KDRACTU
C19, C20, C21, C38	4	CAP, CERM, 0.1 uF, 1000 V, +/- 10%, X7R, 1812	C1812X104KDRACAUTO
C30, C41	2	Cap Ceramic 10uF 25V X7S 10% Pad SMD 0805 +125°C Automotive T/R	CGA4J1X7S1E106K125AC
C31, C36, C37	3	CAP, CERM, 4.7 µF, 25 V,+/- 10%, X6S, AEC-Q200 Grade 2, 0603	GRT188C81E475KE13D
C33, C35	2	CAP, CERM, 4.7 uF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	GCM21BR71C475KA73L
C39, C40	2	CAP, CERM, 43 pF, 50 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	GCQ1555C1H430JB01D
C42, C43	2	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	CGA2B2C0G1H101J050BA
D1	1	Diode, Schottky, 650 V, 1 A, SMB	GB01SLT06-214
D2, D3	2	Bridge Rectifier Single Phase Schottky 40V Surface Mount MBS	KMB24STR
D5, D6	2	Diode, Zener, 16 V, 500 mW, AEC-Q101, SOD-123	BZT52C16-7-F
H1, H2	2	Heat Sink, Black Anodized, 35 x 50 mm, 20 mm high, with Push Pin and Spring, [NoValue]	S05MZZ14
HV, PGND, SW, TP3, TP5, TP6	6		3621-0-32-15-00-00-08-0
J1	1	Header, 100mil, 6x2, Gold, R/A, TH	TSW-106-08-G-D-RA
L1, L2	2	4.7µH Shielded Molded Inductor 1.22A 262mOhm Max 1008 (2520 Metric)	MPIA2510V2-4R7-R
L3, L4	2	2 Line Common Mode Choke Surface Mount 90 Ohms @ 100MHz 400mA DCR 190mOhm	ACM2012-900-2P-T001
LBL1	1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10
Q1	1	MOSFET, N-CH, 20 V, 2.8 A, AEC-Q101, SOT-23	DMG2302UK-7
R1	1	RES, 0, 5%, 0.333 W, AEC-Q200 Grade 0, 0805	CRCW08050000Z0EAHP

Table 9-1. Bill of Materials for LMG342XEVM-04X (continued)

DESIGNATOR	QTY	DESCRIPTION	PART NUMBER
R2	1	RES, 2.05, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	CRCW12062R05FKEA
R3, R12, R18	3	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GE0R00X
R5, R14, R17	3	RES, 20 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GEJ203X
R6, R15, R19, R20	4	RES, 300, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402300RJNED
R7, R16	2	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040249R9FKED
R10	1	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	ERJ-8GEY0R00V
R21	1	RES, 10, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040210R0JNED
T1, T2	2	Transformer, 105uH, TH	750315371
TP1	1	Test Point, Compact, SMT	5016
TP2	1	Test Point, SMT	S2751-46R
U1, U2	2	650-V 30-mΩ GaN FET with Integrated Driver and Protection	LMG342xR030Q
U3	1	Automotive, high-speed, robust-EMC quad-channel digital isolators 16-SSOP -40 to 125	ISO7741FQDBQQ1
U4	1	Automotive, robust EMC, six-channel, 4/2, reinforced digital isolator 16-SSOP -40 to 125	ISO7762FQDBQRQ1
U5, U6	2	Transformer Driver PMIC SOT-23-6	SN6505BQDBVTQ1

Table 9-2. Bill of Materials for LMG342X-BB-EVM

DESIGNATOR	QTY	DESCRIPTION	PART NUMBER
5V, 12V, HVIN, HVOUT, SW, TACH, VAUX	7	Test Point, Compact, Red, TH	5005
5V_EN, HVIN_EN	2	LED, Green, SMD	LG L29K-G2J1-24-Z
ACMGND, AGND1, AGND2, PGND4, PGND5	5	Test Point, Compact, Black, TH	5006
C1, C6, C8, C9, C18	5	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E1X7R1E105K080AD
C2, C3	2	CAP, CERM, 1600 pF, 50 V, +/- 5%, C0G/NP0, 0603	GRM1885C1H162JA01D
C5, C10, C12, C14, C21, C23	6	CAP, CERM, 39 pF, 50 V, +/- 5%, C0G/NP0, 0603	GRM1885C1H390JA01D
C15	1	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603	GRT188R61E106ME13D
C16, C20	2	CAP, CERM, 0.022 uF, 50 V, +/- 10%, X7R, 0603	885012206091
C17	1	CAP, CERM, 100 uF, 6.3 V, +/- 20%, X5R, 0805	GRM21BR60J107M
C19	1	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805	CL21A106KAFN3NE
C22	1	CAP, Film, 20 µF, 900 V,+/- 10%, 0.0055 ohm, TH	FE37M6C0206KB
C25	1	CAP, AL, 150 uF, 600 V, +/- 20%, TH	LGN2X151MELB50
CIN3, CIN4, COUT3, COUT4	4	CAP, CERM, 0.1 uF, 630 V, +/- 10%, X7R, 1812	GRM43DR72J104KW01L
D1, D3	2	Diode, Schottky, 30 V, 0.2 A, SOD-323	BAT54WS-7-F
H1, H8, H9, H10, H11, H12	6		3484

Table 9-2. Bill of Materials for LMG342X-BB-EVM (continued)

DESIGNATOR	QTY	DESCRIPTION	PART NUMBER
H2, H3, H4, H5, H6, H7	6	MACHINE SCREW PAN PHILLIPS 4-40	PMSSS 440 0025 PH
H13	1	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH
H14	1		1902C
HS_FET_PWM, LS_FET_PWM, PWM_HS, PWM_LS	4	Test Point, Compact, White, TH	5007
HS_FLT, LS_FLT	2	LED, Red, SMD	LS L29K-G1J2-1-Z
HS_OC, LS_OC	2	LED, Yellow, SMD	SML-E12Y8WT86
HVBUS1, HVBUS2, PGND1, PGND2, SW1, SW2	6	Receptacle, 1 Pos, Gold, TH	0435-0-15-15-03-27-10-0
J1, J9	2	Terminal Block, 5.08mm, 2x1, TH	0395443002
J2, J4	2	Header, 100mil, 6x1, Gold, TH	TSW-106-07-G-S
J3, J8	2	Connector, TH, BNC	112404
J5	1	12 Position Receptacle, Bottom Entry Connector Surface Mount	HLE-106-02-G-DV-BE-A
J6, J12	2	Terminal Block, 2x1, 2.54mm, TH	282834-2
J7, J14, J15	3	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S
J10, J11, J13	3	Header, 100mil, 2x1, Gold, TH	TSW-102-07-G-S
J16, J17, J18	3	Standard Banana Jack, Uninsulated	3267
L2	1	INDUCTOR 570uH 13A	750317345
L3	1	Coupled inductor, 47 uH, 1.14 A, 0.4825 ohm, SMD	DRQ73-470-R
LBL1	1	Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	THT-13-457-10
R1, R5, R29, R30	4	RES, 3.3 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06033K30JNEA
R2, R4, R9	3	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0EA
R3, R15	2	Trimmer, 5 K, 0.25 W, SMD	3224X-1-502E
R6, R22	2	RES, 100 k, 5%, 0.1 W, 0603	CRCW0603100KJNEAC
R7, R21	2	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100RJNEA
R8, R27	2	RES, 105 k, 1%, 0.1 W, 0603	RC0603FR-07105KL
R10, R11, R12, R13, R14, R16, R17, R18, R19, R20	10	RES, 30 k, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	CRCW120630K0JNEA
R25	1	RES, 6.20 k, 1%, 0.1 W, 0603	RC0603FR-076K2L
R26	1	RES, 1.18 k, 1%, 0.1 W, 0603	RC0603FR-071K18L
R28	1	RES, 33.2 k, 0.1%, 0.1 W, 0603	RT0603BRD0733K2L
R31	1	RES, 1.6 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K60JNEA
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5	5	Shunt, 100mil, Gold plated, Black	SNT-100-BK-G
U1, U2	2	Automotive Catalog Dual 2-Input Positive-AND Gate, DCT0008A, LARGE T&R	
U3, U5	2	Triple Schmitt-Trigger Inverter, DCU0008A (VSSOP-8)	SN74LVC3G14DCUTG4
U4	1	1A SIMPLE SWITCHER® Power Module with 20V Maximum Input Voltage for Military and Rugged Applications, 7 pin TO-PMOD	LMZ12001EXTTZ/NOPB

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2020) to Revision B (March 2022)	Page
• Revised the *Heat Sink* section	7
• Updated Figure 3-1	10

Changes from Revision * (October 2020) to Revision A (January 2022)	Page
• Revised the *LMG342XEVM-04X Daughter Card* section	5
• Revised the *Bootstrap Mode* section	7
• Updated Figure 2-2 and Figure 2-3	7
• Revised the *Heat Sink* section	7
• Revised the *Mother Boards* section	9
• Updated Figure 3-1	10
• Added Figure 4-2	12
• Revised the *Test Equipment* section	15
• Revised the *Test Procedure When Paired With LMG342X-BB-EVM* section	16
• Revised the *Setup* section	16
• Added the *Test Results* section	18
• Revised the *Test Procedure When Paired With LMG34XX-BB-EVM* section	20
• Updated Table 9-1	24

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