LM709

Application Note 24 A Simplified Test Set for Op Amp Characterization

Literature Number: SNOA637

A Simplified Test Set for Op Amp Characterization

National Semiconductor
Application Note 24
M. Yamatake
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INTRODUCTION

The test set described in this paper allows complete quantitative characterization of all dc operational amplifier parameters quickly and with a minimum of additional equipment. The method used is accurate and is equally suitable for laboratory or production test — for quantitative readout or for limit testing. As embodied here, the test set is conditioned for testing the LM709 and LM101 amplifiers; however, simple changes discussed in the text will allow testing of any of the generally available operational amplifiers.

Amplifier parameters are tested over the full range of common mode and power supply voltages with either of two output loads. Test set sensitivity and stability are adequate for testing all presently available integrated amplifiers.

The paper will be divided into two sections, i.e., a functional description, and a discussion of circuit operation. Complete construction information will be given including a layout for the tester circuit boards.

FUNCTIONAL DESCRIPTION

The test set operates in one of three basic modes. These are: (1) Bias Current Test; (2) Offset Voltage, Offset Current Test; and (3) Transfer Function Test. In the first two of these tests, the amplifier under test is exercised throughout its full common mode range. In all three tests, power supply voltages for the circuit under test may be set at ±5V, ±10V, ±15V, or ±20V.

POWER SUPPLY

Basic waveforms and dc operating voltages for the test set are derived from a power supply section comprising a positive and a negative rectifier and filter, a test set voltage regulator, a test circuit voltage regulator, and a function generator. The dc supplies will be discussed in the section dealing with detailed circuit description.

The waveform generator provides three output functions, a ±19V square wave, a −19V to +19V pulse with a 1% duty cycle, and a ±5V triangular wave. The square wave is the basic waveform from which both the pulse and triangular wave outputs are derived.

The square wave generator is an operational amplifier connected as an astable multivibrator. This amplifier provides an output of approximately ±19V at 16 Hz. This square wave is used to drive junction FET switches in the test set and to generate the pulse and triangular waveforms.

The pulse generator is a monostable multivibrator driven by the output of the square wave generator. This multivibrator is allowed to swing from negative saturation to positive saturation on the positive going edge of the square wave input and has a time constant which will provide a duty cycle of approximately 1%. The output is approximately −19V to +19V.

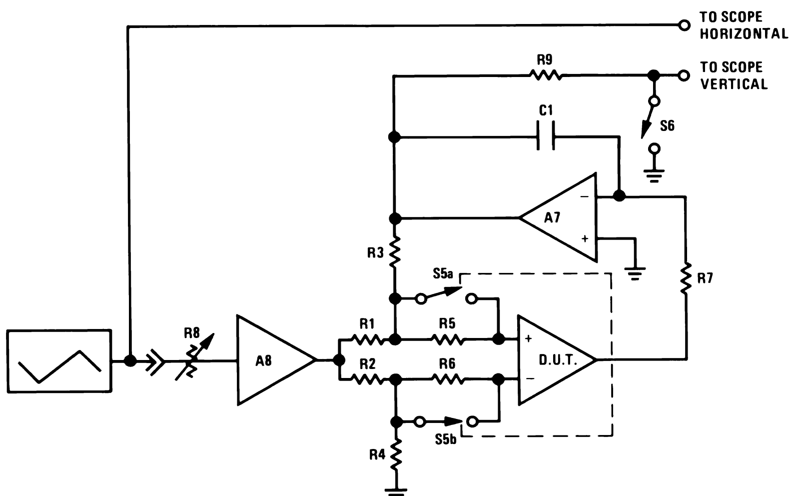

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FIGURE 1. Functional Diagram of Bias Current Test Circuit

The triangular wave generator is a dc stabilized integrator driven by the output of the square wave generator and provides a ±5V output at the square wave frequency, inverted with respect to the square wave.

The purpose of these various outputs from the power supply section will be discussed in the functional description.

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BIAS CURRENT TEST

A functional diagram of the bias current test circuit is shown in *Figure 1.* The output of the triangular wave generator and the output of the test circuit, respectively, drive the horizontal and vertical deflection of an oscilloscope.

The device under test, (cascaded with the integrator, A_7), is connected in a differential amplifier configuration by R_1, R_2, R_3, and R_4. The inputs of this differential amplifier are driven in common from the output of the triangular wave generator through attenuator R_8 and amplifier A_8. The inputs of the device under test are connected to the feedback network through resistors R_5 and R_6, shunted by the switch S_{5a} and S_{5b}.

The feedback network provides a closed loop gain of 1,000 and the integrator time constant serves to reduce noise at the output of the test circuit as well as allowing the output of the device under test to remain near zero volts.

The bias current test is accomplished by allowing the device under test to draw input current to one of its inputs through the corresponding input resistor on positive going or negative going halves of the triangular wave generator output. This is accomplished by closing S_{5a} or S_{5b} on alternate halves of the triangular wave input. The voltage appearing across the input resistor is equal to input current times the input resistor. This voltage is multiplied by 1,000 by the feedback loop and appears at the integrator output and the vertical input of the oscilloscope. The vertical separaton of the traces representing the two input currents of the amplifier under test is equivalent to the total bias current of the amplifier under test.

The bias current over the entire common mode range may be examined by setting the output of A_8 equal to the amplifier common mode range. A photograph of the bias current oscilloscope display is given as *Figure 2.* In this figure, the total input current of an amplifier is displayed over a ±10V common mode range with a sensitivity of 100 nA per vertical division.

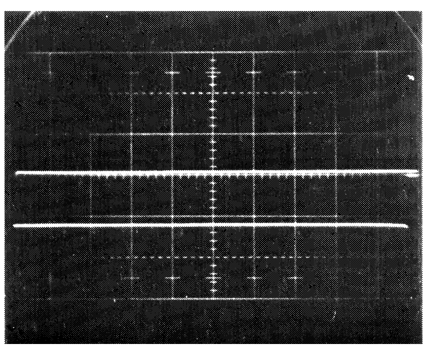

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FIGURE 2. Bias Current and Common Mode Rejection Display

The bias current display of *Figure 2* has the added advantage that incipient breakdown of the input stage of the device under test at the extremes of the common mode range is easily detected.

If either or both the upper or lower trace in the bias current display exhibits curvature near the horizontal ends of the oscilloscope face, then the bias current of that input of the amplifier is shown to be dependent on common mode voltage. The usual causes of this dependency are low breakdown voltage of the differential input stage or current sink.

OFFSET VOLTAGE, OFFSET CURRENT TEST

The offset voltage and offset current tests are performed in the same general way as the bias current test. The only difference is that the switches S_{5a} and S_{5b} are closed on the same half-cycle of the triangular wave input.

The synchronous operation of S_{5a} and S_{5b} forces the amplifier under test to draw its input currents through matched high and low input resistors on alternate halves of the input triangular wave. The difference between the voltage drop across the two values of input resistors is proportional to the difference in input current to the two inputs of the amplifier under test and may be measured as the vertical spacing between the two traces appearing on the face of the oscilloscope.

Offset voltage is measured as the vertical spacing between the trace corresponding to one of the two values of source resistance and the zero volt baseline. Switch S_6 and Resistor R_9 are a base line chopper whose purpose is to provide a baseline reference which is independent of test set and oscilloscope drift. S_6 is driven from the pulse output of the function generator and has a duty cycle of approximately 1% of the triangular wave.

Figure 3 is a photograph of the various waveforms presented during this test. Offset voltage and offset current are displayed at a sensitivity of 1 mV and 100 nA per division, respectively, and both parameters are displayed over a common mode range of ±10V.

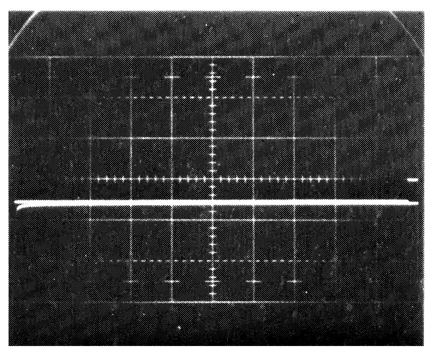

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FIGURE 3. Offset Voltage, Offset Current and Common Mode Rejection Display

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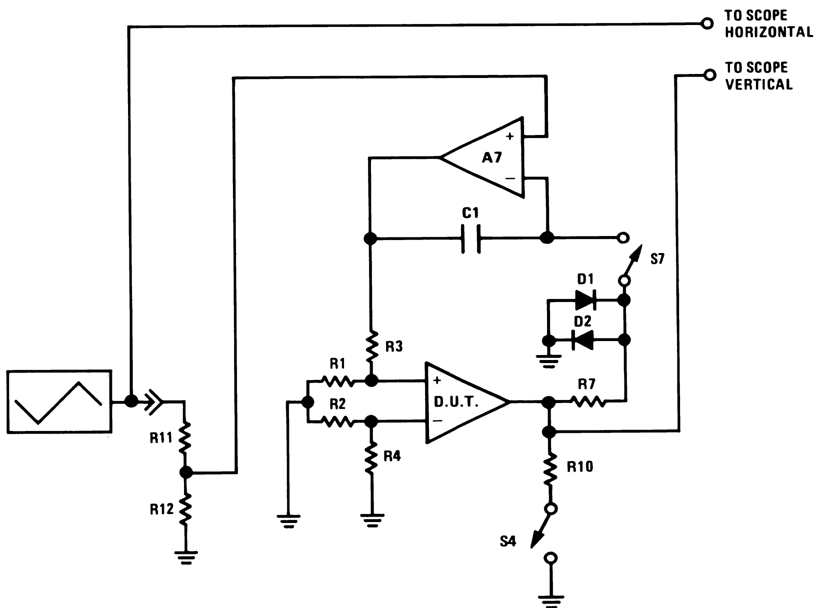

FIGURE 4. Functional Diagram of Transfer Function Circuit

TRANSFER FUNCTION TEST

A functional diagram of the transfer function test is shown in *Figure 4*. The output of the triangular wave generator and the output of the circuit under test, respectively, drive the horizontal and vertical inputs of an oscilloscope.

The device under test is driven by a ±2.5 mV triangular wave derived from the ±5V output of the triangular wave generator through the attenuators R_{11}, R_{12}, and R_1, R_3 and through the voltage follower, A_7. The output of the device under test is fed to the vertical input of an oscilloscope.

Amplifier A_7 performs a dual function in this test. When S_7 is closed during the bias current test, a voltage is developed across C_1 equal to the amplifier offset voltage multiplied by the gain of the feedback loop. When S_7 is opened in the transfer function test, the charge stored in C_1 continues to provide this offset correction voltage. In addition, A_7 sums the triangular wave test signal with the offset correction voltage and applies this sum to the input of the amplifier under test through the attenuator R_1, R_3. This input sweeps the input of the amplifier under test ±2.5 mV around its offset voltage.

Figure 5 is a photograph of the output of the test set during the transfer function test. This figure illustrates the function of amplifier A_7 in adjusting the dc input of the test device so that its transfer function is displayed on the center of the oscilloscope face.

The transfer function display is a plot of V_{IN} vs V_{OUT} for an amplifier. This display provides information about three amplifier parameters: gain, gain linearity, and output swing.

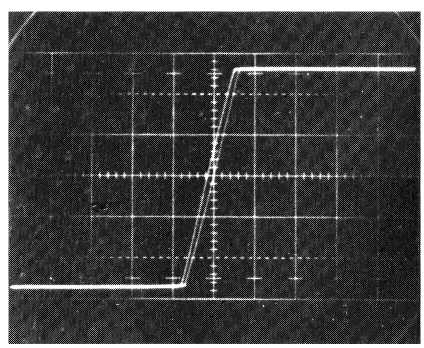

FIGURE 5. Transfer Function Display

Gain is displayed as the slope, $\Delta V_{OUT}/\Delta V_{IN}$ of the transfer function. Gain linearity is indicated change in slope of the V_{OUT}/V_{IN} display as a function of output voltage. This display is particularly useful in detecting crossover distortion in a Class B output stage. Output swing is measured as the vertical deflection of the transfer function at the horizontal extremes of the display.

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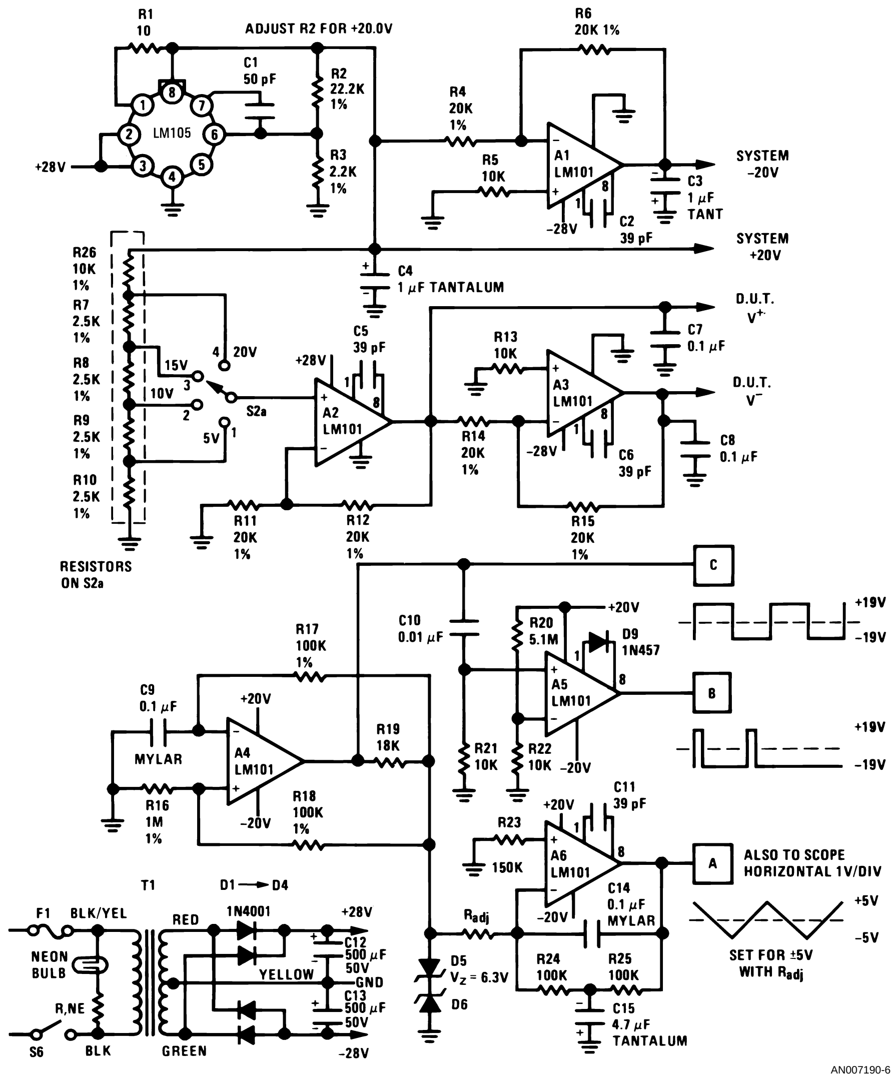

NOTE: All resistor valves in ohms.
All resistors ¼W, 5% unless specified otherwise.

FIGURE 6. Power Supply and Function Generator

DETAILED CIRCUIT DESCRIPTION

POWER SUPPLIES

As shown in *Figure 6*, which is a complete schematic of the power supply and function generator, two power supplies are provided in the test set. One supply provides a fixed ±20V to power the circuitry in the test set; the other provides ±5V to ±20V to power the circuit under test.

The test set power supply regulator accepts +28V from the positive rectifier and filter and provides +20V through the LM100 positive regulator. Amplifier A_1 is powered from the negative rectifier and filter and operates as a unity gain inverter whose input is +20V from the positive regulator, and whose output is −20V.

The test circuit power supply is referenced to the +20V output of the positive regulator through the variable divider comprising R_7, R_8, R_9, R_{10}, and R_{26}. The output of this divider is +10V to +2.5V according to the position of S_{2a} and is fed to the non-inverting, gain-of-two amplifier, A_2. A_2 is powered from +28V and provides +20V to +5V at its output. A_3 is a

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unity gain inverter whose input is the output of A_2 and which is powered from −28V. The complementary outputs of amplifiers A_2 and A_3 provide dc power to the circuit under test.

LM101 amplifiers are used as A_2 and A_3 to allow operation from one ground referenced voltage each and to provide protective current limiting for the device under test.

FUNCTION GENERATOR

The function generator provides three outputs, a ±19V square wave, a −19V to +19V pulse having a 1% duty cycle, and a ±5V triangular wave. The square wave is the basic function from which the pulse and triangular wave are derived, the pulse is referenced to the leading edge of the square wave, and the triangular wave is the inverted and integrated square wave.

Amplifier A_4 is an astable multivibrator generating a square wave from positive to negative saturation. The amplitude of this square wave is approximately ±19V. The square wave frequency is determined by the ratio of R_{18} to R_{16} and by the time constant, $R_{17}C_9$. The operating frequency is stabilized against temperature and power regulation effects by regulating the feedback signal with the divider R_{19}, D_5 and D_6.

Amplifier A_5 is a monostable multivibrator triggered by the positive going output of A_4. The pulse width of A_5 is determined by the ratio of R_{20} to R_{22} and by the time constant $R_{21}C_{10}$. The output pulse of A_5 is an approximately 1% duty cycle pulse from approximately −19V to +19V.

Amplifier A_6 is a dc stabilized integrator driven from the amplitude-regulated output of A_4. Its output is a ±5V triangular wave. The amplitude of the output of A_6 is determined by the square wave voltage developed across D_5 and D_6 and the time constant R_{adj} C_{14}. DC stabilization is accomplished by the feedback network R_{24}, R_{25}, and C_{15}. The ac attenuation of this feedback network is high enough so that the integrator action at the square wave frequency is not degraded.

Operating frequency of the function generator may be varied by adjusting the time constants associated with A_4, A_5, and A_6 in the same ratio.

TEST CIRCUIT

A complete schematic diagram of the test circuit is shown in *Figure 7*. The test circuit accepts the outputs of the power supplies and function generator and provides horizontal and vertical outputs for an X-Y oscilloscope, which is used as the measurement system.

The primary elements of the test circuit are the feedback buffer and integrator, comprising amplifier A_7 and its feedback network C_{16}, R_{31}, R_{32}, and C_{17}, and the differential amplifier network, comprising the device under test and the feedback network R_{40}, R_{43}, R_{44}, and R_{52}. The remainder of the test circuit provides the proper conditioning for the device under test and scaling for the oscilloscope, on which the test results are displayed.

The amplifier A_8 provides a variable amplitude source of common mode signal to exercise the amplifier under test over its common mode range. This amplifier is connected as a non-inverting gain-of-3.6 amplifier and receives its input from the triangular wave generator. Potentiometer R_{37} allows the output of this amplifier to be varied from ±0 volts to ±18 volts. The output of this amplifier drives the differential input resistors, R_{43} and R_{44}, for the device under test.

The resistors R_{46} and R_{47} are current sensing resistors which sense the input current of the device under test. These resistors are switched into the circuit in the proper sequence by the field effect transistors Q_6 and Q_7. Q_6 and Q_7 are driven from the square wave output of the function generator by the PNP pair, Q_{10} and Q_{11}, and the NPN pair, Q_8 and Q_9. Switch sections S_{1b} and S_{1c} select the switching sequence for Q_8 and Q_9 and hence for Q_6 and Q_7. In the bias current test, the FET drivers, Q_8 and Q_9, are switched by out of phase signals from Q_{10} and Q_{11}. This opens the FET switches Q_6 and Q_7 on alternate half cycles of the square wave output of the function generator. During the offset voltage, offset current test, the FET drivers are operated synchronously from the output of Q_{11}. During the transfer function test, Q_6 and Q_7 are switched on continuously by turning off Q_{11}. R_{42} and R_{45} maintain the gates of the FET switches at zero gate to source voltage for maximum conductance during their on cycle. Since the sources of these switches are at the common mode input voltage of the device under test, these resistors are connected to the output of the common mode driver amplifier, A_8.

The input for the integrator-feedback buffer, A_7, is selected by the FET switches Q_4 and Q_5. During the bias current and offset voltage offset current tests, A_7 is connected as an integrator and receives its input from the output of the device under test. The output of A_7 drives the feedback resistor, R_{40}. In this connection, the integrator holds the output of the device under test near ground and serves to amplify the voltages corresponding to bias current, offset current, and offset voltage by a factor of 1,000 before presenting them to the measurement system. FET switches Q_4 and Q_5 are turned on by switch section S_{1b} during these tests.

FET switches Q_4 and Q_5 are turned off during the transfer function test. This disconnects A_7 from the output of the device under test and changes it from an integrator to a non-inverting unity gain amplifier driven from the triangular wave output of the function generator through the attenuator R_{33} and R_{34} and switch section S_{1a}. In this connection, amplifier A_7 serves two functions; first, to provide an offset voltage correction to the input of the device under test and, second, to drive the input of the device under test with a ±2.5 mV triangular wave centered about the offset voltage. During this test, the common mode driver amplifier is disabled by switch section S_{1a} and the vertical input of the measurement oscilloscope is transferred from the output of the integrator-buffer, A_7, to the output of the device under test by switch section S_{1d}. S_{2a} allows supply voltages for the device under test to be set at ±5, ±10, ±15, or ±20V. S_{2b} changes the vertical scale factor for the measurement oscilloscope to maintain optimum vertical deflection for the particular power supply voltage used. S_4 is a momentary contact pushbutton switch which is used to change the load on the device under test from 10 kΩ to 2 kΩ.

A delay must be provided when switching from the input tests to the transfer function tests. The purpose of this delay is to disable the integrator function of A_7 before driving it with the triangular wave. If this is not done, the offset correction voltage, stored on C_{16}, will be lost. This delay between opening FET switch Q_4, and switch Q_5, is provided by the RC filter, R_{35} and C_{19}.

Resistor R_{41} and diodes D_7 and D_8 are provided to control the integrator when no test device is present, or when a faulty test device is inserted. R_{41} provides a dc feedback path in the absence of a test device and resets the integrator to zero. Diodes D_7 and D_8 clamp the input to the integrator to approximately ±0.7 volts when a faulty device is inserted.

FET switch Q_1 and resistor R_{28} provide a ground reference at the beginning of the 50-ohm-source, offset-voltage trace. This trace provides a ground reference which is independent of instrument or oscilloscope calibration. The gate of Q_1 is

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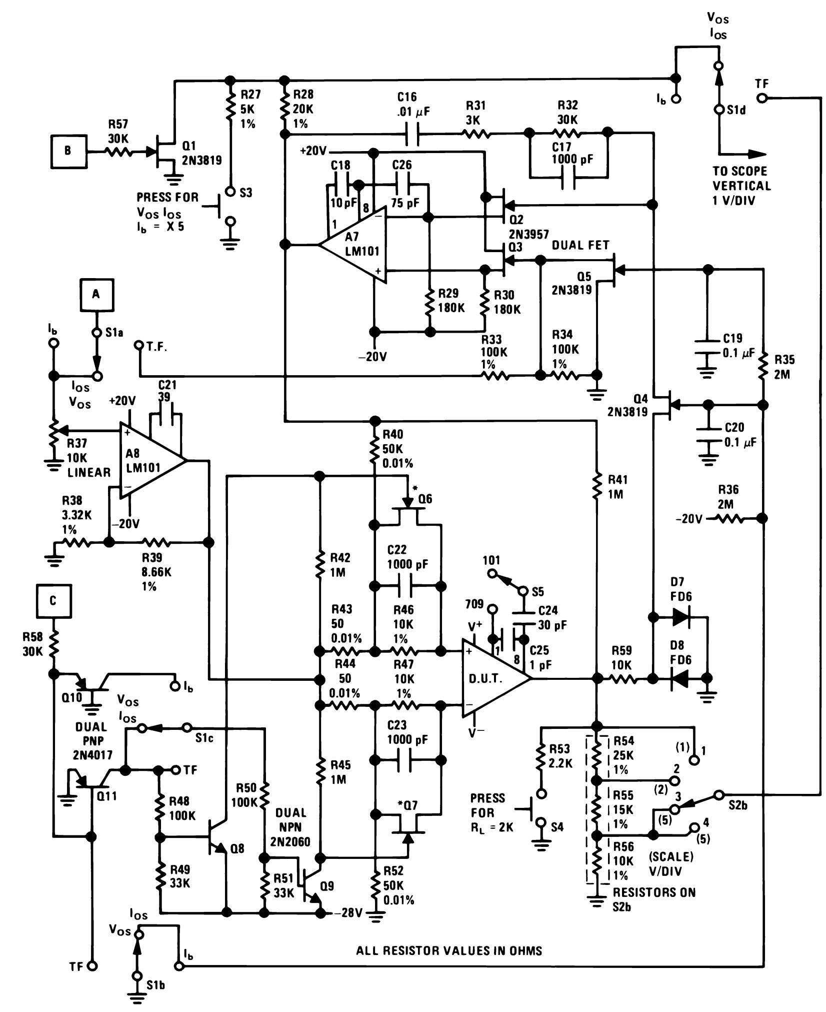
driven by the output of monostable multivibrator A_5, and shorts the vertical oscilloscope drive signal to ground during the time that A_5 output is positive.

Switch S_3, R_{27}, and R_{28} provide a 5X scale increase during input parameter tests to allow measurement of amplifiers with large offset voltage, offset current, or bias current.

Switch S_5 allows amplifier compensation to be changed for 101 or 709 type amplifiers.



Note: All resistors 1/4W, 5% unless specified otherwise *2N3819 matched for on resistance within 200Ω Select for $BV_{GS} > 45V$

FIGURE 7. Test Circuit

CALIBRATION

Calibration of the test system is relatively simple and requires only two adjustments. First, the output of the main regulator is set up for 20V. Then, the triangular wave generator is adjusted to provide ±5V output by selecting R_{adj}. This sets the horizontal sweep for the X-Y oscilloscope used as the measurement system. The oscilloscope is then set up for 1V/division vertical and for a full 10 division horizontal sweep.

Scale factors for the three test positions are:

1. **Bias Current Display** (*Figure 2*)

I_{bias} total	100 nA/div. vertical
Common Mode Voltage	Variable horizontal

2. **Offset Voltage-Offset Current** (*Figure 3*)

I_{offset}	100 nA/div. vertical
V_{offset}	1 mV/div. vertical
Common Mode Voltage	Variable horizontal

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3. **Transfer Function** (*Figure 5*)

V_{IN}	0.5 mV/div.
V_{OUT}	5V/div. @ V_s ±20V
	5V/div. @ V_s ±15V
	2V/div. @ V_s ±10V
	1V/div. @ V_s ±5V

$$\text{Gain} = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$$

CONSTRUCTION

Test set construction is simplified through the use of integrated circuits and etched circuit layout.

Figures 8, 9, 10 give photographs of the completed tester. *Figure 11* shows the parts location for the components on the circuit board layout of *Figure 12*. An attempt should be made to adhere to this layout to insure that parasitic coupling between elements will not cause oscillations or give calibration problems.

Table 1 is a listing of special components which are needed to fit the physical layout given for the tester.

TABLE 1. Partial Parts List

T_1	Triad F-90X
S_1	Centralab PA2003 non-shorting
S_2	Centralab PA2015 non-shorting
S_3, S_4	Grayhill 30-1 Series 30 subminiature pushbutton switch
S_5, S_6	Alcoswitch MST-105D SPDT

CONCLUSIONS

A semi-automatic test system has been described which will completely test the important operational amplifier parameters over the full power supply and common mode ranges. The system is simple, inexpensive, easily calibrated, and is equally suitable for engineering or quality assurance usage.

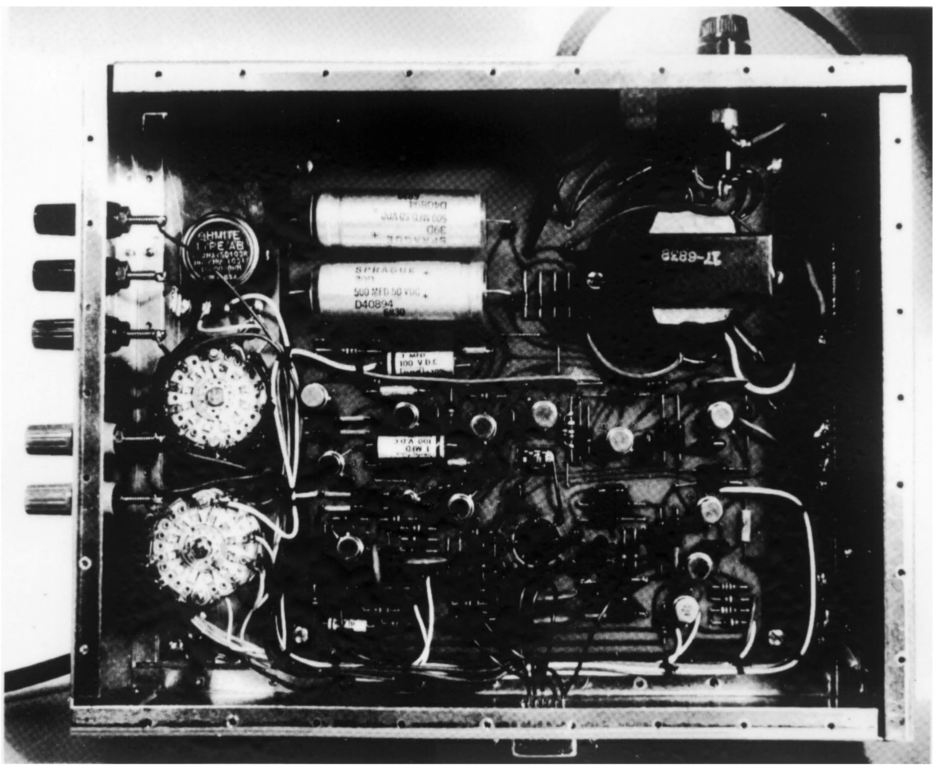

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FIGURE 8. Bottom of Test Set

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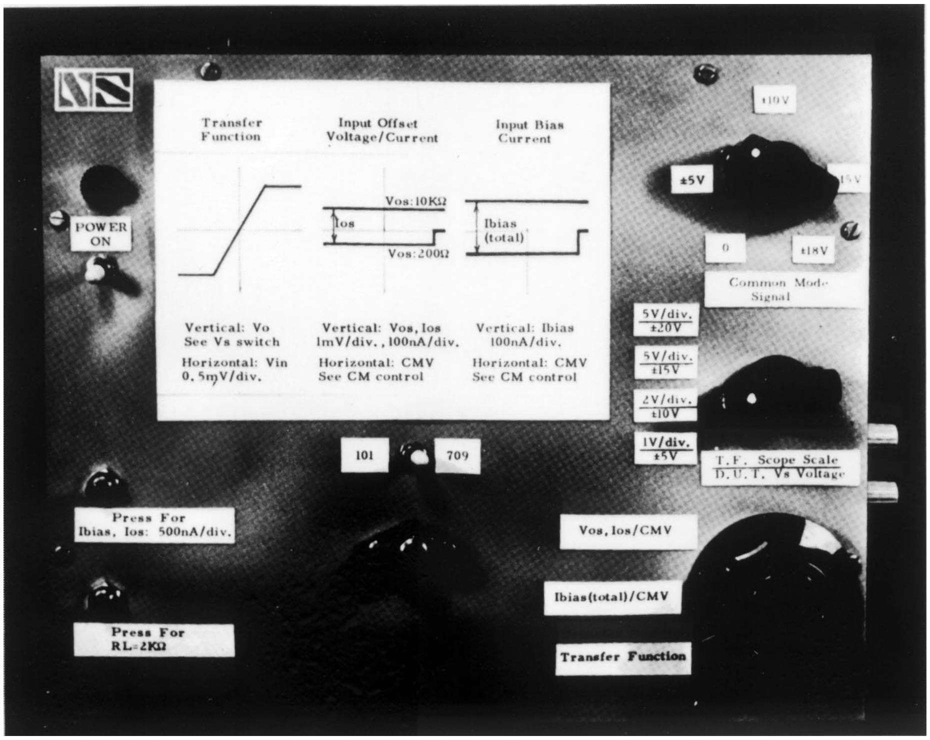

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FIGURE 9. Front Panel

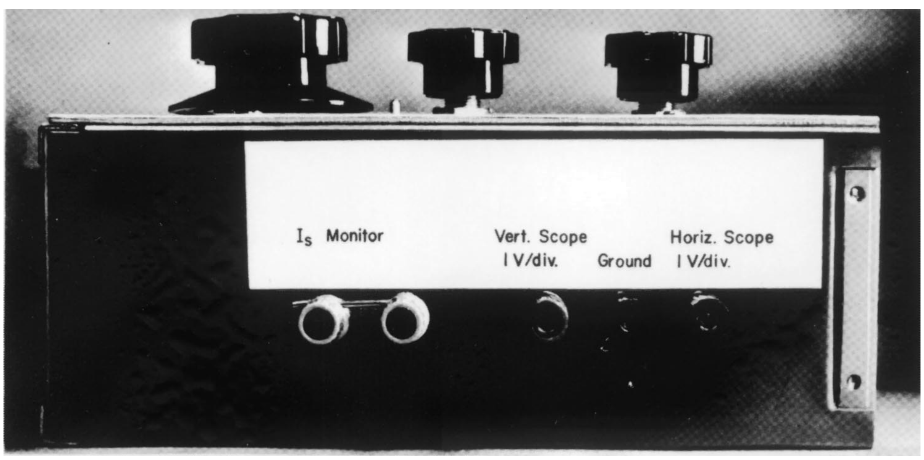

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FIGURE 10. Jacks

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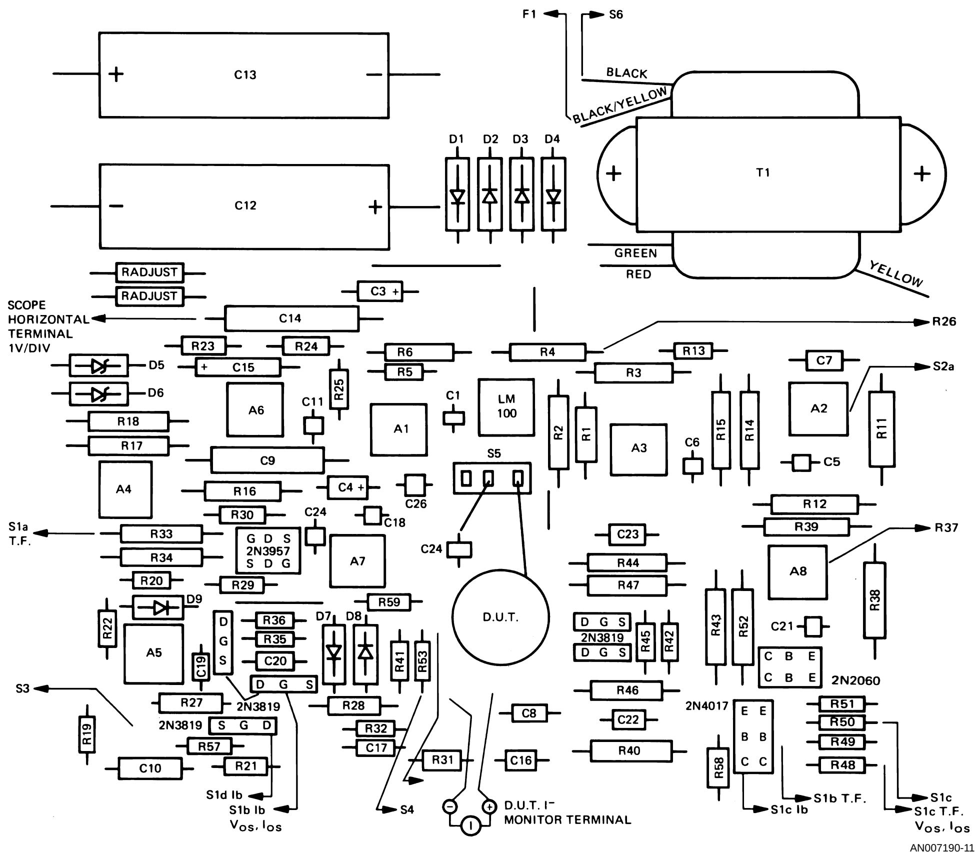

FIGURE 11. Component Location, Top View

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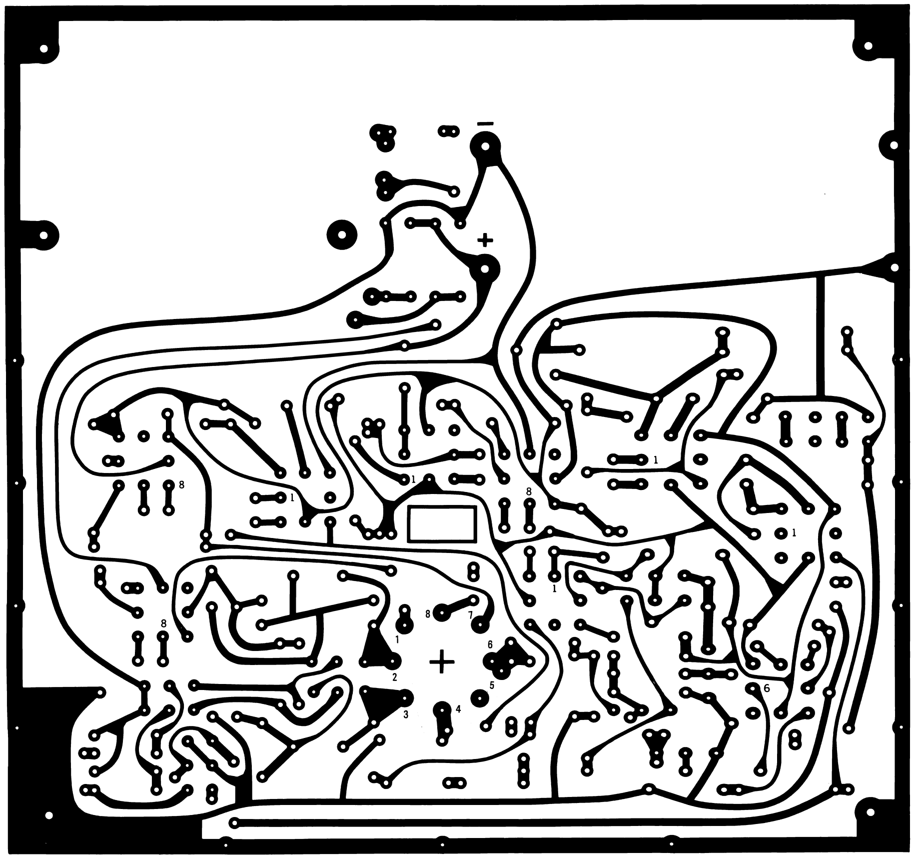

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FIGURE 12. Circuit Board Layout

Book Extract End

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Americas
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Fax: 1-800-737-7018
Email: support@nsc.com

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Deutsch Tel: +49 (0) 1 80-530 85 85
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Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

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