AN-2113 Applying I^2C Compatible Temperature Sensors in Systems with Slow Clock Edges

ABSTRACT

This Application Note describes a method of interfacing a given microcontroller with a Texas Instruments digital temperature sensor.

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1 Overview

Occasionally, there is a question about interfacing a particular microcontroller to one of the Texas Instruments digital temperature sensors. Problems most often occur when the microcontroller has extremely slow falling edges on the clock line, where “extremely slow” means close to the I2C Standard Mode maximum for T_f, or 300ns. When using the Texas Instruments I2C-compatible temperature sensors in your system, keep in mind that only the timing parameters specifically listed in the data sheet are guaranteed. Those data have either been extensively characterized or are tested on each and every part before it leaves the factory. For example, some Texas Instruments digital temperature sensors with Two-Wire Interface do not specify the I2C-Standard timing parameter $t_{HD;DAT}$. T3, which is the time for data out to be stable after SCL falls, is the closest specification to $t_{HD;DAT}$ (see Figure 1). There is a footnote in the I2C specification that essentially says the device sending the SDA signal has to wait 300ns before it sends SDA out “to bridge the undefined region of the falling edge of SCL”. Let’s take a look at what the concern is with bridging the undefined region of SCL.

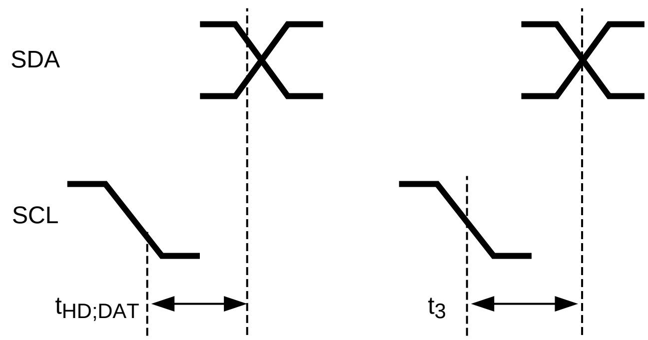

Figure 1. $T_{HD;DAT}$ and T_3 Definitions

Begin by examining the specification for what makes up a logic ‘1’ and what makes up a logic ‘0’ in I^2C. Figure 2 shows, as an example, a falling edge of SCL. The region that is assured to be a logic ‘1’ is from 70% of the signal and up to a little bit above the supply. The region that is assured to be a logic ‘0’ is from 30% of the signal down to a little bit below ground. The definition of logic ‘1’ and logic ‘0’ leaves a big part of the signal as undefined: the part from 30% to 70%. This is what the specification refers to when it mentions the undefined region. Due to the difficulty of manufacturing, an input buffer that will have a 30% to 70% hysteresis over all process, temperature and supply, most buffers will actually switch from an input ‘1’ to an input ‘0’ somewhere in the undefined region, although this will not be specified. Therefore, it is not unreasonable to suggest that in a system you could have an input buffer (input A, Figure 2) that has the transition from a ‘0’ to a ‘1’ at the 30% level and another input buffer (input B, Figure 2) that has the transition from a ‘0’ to a ‘1’ at the 70% level. In some cases, this difference in logic transition can cause system problems that are shown in Figure 2.

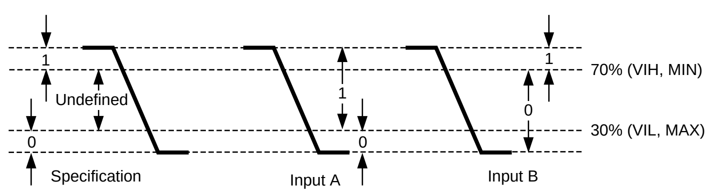

Figure 2. I^2C Switching Points and Logic Levels

The end of a typical bus transaction is shown in Figure 3. In this case, the master has sent information to the slave and the slave sends an ACK back to the master. The master in this example has a very slow fall time on the falling edge of its SCL and SDA signals, on the order of the 300 ns maximum allowed in the specification. The slave ACK bit, however, has a very fast falling edge, on the order of 5 ns, without a 300 ns delay. In most cases, this will not cause problems in the system. However, assume that the master has bus arbitration enabled. In bus arbitration, the master monitors the SCL line and the SDA line as it is sending out information. If the master sees data different from what it sent out, it assumes that another master is attempting to use the bus. At this point, the master typically stops sending data and sets an error flag to alert the program that it has lost control of the bus. If this happens with only a single master, the system will hang waiting for the bus to be released by another master that doesn't exist. A lost arbitration situation can occur if the SCL input to the slave is like input B, the input to the master that is monitoring the bus is like input A and the fall time of the ACK signal from the slave is much faster than the fall time of the SCL from the master. If those three conditions are met, your master may lose arbitration.

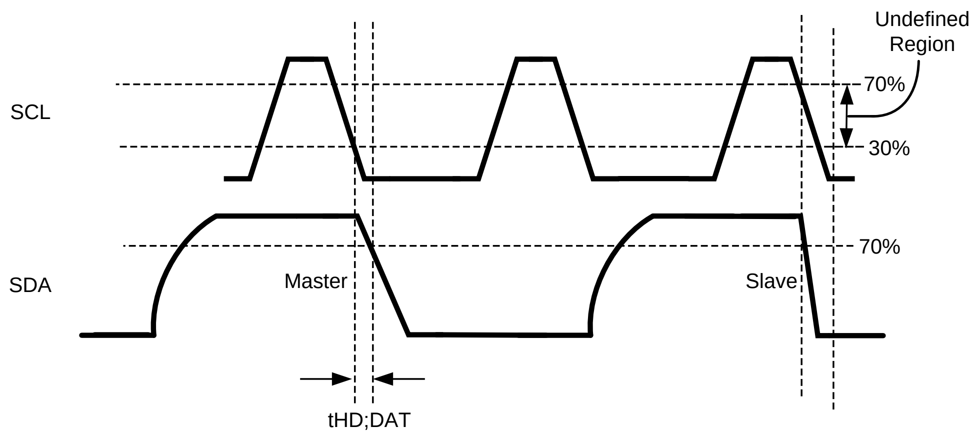

Figure 3. I²C Bus Signals

To determine if your system is at risk for this problem, compare the fall times of the SCL output from the master with the fall times of the slave. There will be two components to the fall time of the ACK: one is the propagation delay through the part (the delay from reading a ‘0’ on SCL to putting out a ‘0’ on SDA) and the other is the actual fall time of the ACK (the 10-90% time). These two components together make up the timing parameter T_3.The propagation delay is an order of magnitude larger than the fall time in many temperature sensors, so if the fall times are approximately the same (within a few 10s of ns) there will be plenty of margin to avoid unnecessarily losing arbitration. When probing, make sure to follow established probing practices for fast edges to avoid getting erroneous results.

One solution in systems that are having arbitration problems is adding capacitance from the SDA line to ground. That will resolve the problem in all but the most pathological cases. The exact amount of capacitance will depend on the size of the SDA line pull-ups (so as not degrade the rising edge too much), how much capacitance is already on the board and how much capacitance the other devices on the board are able to drive.

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