Programmer's Guide

DS320PR410 Programming Guide

ABSTRACT

This document provides a programming reference for the D320PR410 Four-Channel PCI-Express Gen-5 Linear Redriver. This document contains detailed information related to the DS320PR410 advanced configuration options. The intended audience includes software engineers working on system diagnostics and control software.

TI recommends that the reader be familiar with the *DS320PR410 Four-Channel Linear Redriver for PCIe 5.0, CXL 2.0* data sheet. This document and all other collateral data related to the DS320PR410 redriver (application notes, models, and so forth) are available for download from the TI website from the DS320PR410 product page. Alternatively, contact your local Texas Instruments field sales representative.

Table of Contents

List of Tables

Trademarks

1 Access Methods

There are two ways to access the DS320PR410 registers. The two methods are:

- Register control through the Serial Management Bus (SMBus/I^{2}C)
- Automatic configuration through an external EEPROM

1.1 Register Programming Through SMBus

The DS320PR410 internal registers can be accessed through the standard SMBus protocol. The SMBus secondary address is determined at power up based on the configuration of the EQ1 / ADDR1 and EQ0 / ADDR0 pins. The pin state is read on power up, after the internal power-on reset signal is deasserted.

The EQ1 / ADDR1 and EQ0 / ADDR0 pins along with GAIN, MODE, and RX_DET pins are 5-level input pins that are used to control the configuration of the device. These 5-level inputs use a resistor divider to help set the four valid levels as provided in Table 1-1.

Table 1-1. DS320PR410 5-Level Control Pin Settings

Pin Level	Pin Setting
L0	1 kΩ to GND
L1	8.25 kΩ to GND
L2	24.9 kΩ to GND
L3	75 kΩ to GND
L3	F (Float)

There are 16 unique SMBus secondary addresses that can be assigned to the device by placing external resistor straps on the EQ0 / ADDR0 and EQ1 / ADDR1 pins as provided in Table 1-2. When multiple DS320PR410 devices are on the same SMBus interface bus, each device must be configured with a unique SMBus secondary address.

Table 1-2. DS320PR410 SMBus Address Map

EQ1 / ADDR1 Pin Level	EQ0 / ADDR0 Pin Level	7-Bit Address [HEX]
L0	L0	0x18
L0	L1	0x1A
L0	L2	0x1C
L0	L3	0x1E
L0	L4	Reserved
L1	L0	0x20
L1	L1	0x22
L1	L2	0x24
L1	L3	0x26
L1	L4	Reserved
L2	L0	0x28
L2	L1	0x2A
L2	L2	0x2C
L2	L3	0x2E
L2	L4	Reserved
L3	L0	0x30
L3	L1	0x32
L3	L2	0x34
L3	L3	0x36
L3	L4	Reserved

1.2 Device Configuration Through External EEPROM

The DS320PR410 can automatically read initial configuration from the EEPROM at power up. Detailed information on EEPROM HEX file generation for this device is available in the *Understanding EEPROM Programming for PCI-Express Gen-4 Redrivers* application note

2 Register Mapping

The DS320PR410 has two types of registers:

- **Share Registers** – These registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers** – These registers are used to control and configure specific features for each individual channel. All channels have the same register set and can be configured independent of each other or configured as a group via broadcast writes to bank 0 (channels 0-3).

2.1 Share Registers

Table 2-1. General Register (Offset = 0xE2) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	rst_i2c_regs	R/W/SC	0x0	Device Reset Control: Reset all I^2C registers to default values (self- clearing).
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	frc_eeprm_rd	R/W/SC	0x0	Override MODE and READ_EN_N status to force manual EEPROM Configuration Load.

Table 2-2. DEVICE_ID0 Register (Offset = 0xF0) [reset = 0x02]

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	device_id0_3	R	0x0	Device ID0 [3:1]: 011
2	device_id0_2	R	0x0	see MSB
1	device_id0_1	R	0x1	see MSB
0	RESERVED	R	X	Reserved

Table 2-3. DEVICE_ID1 Register (Offset = 0xF1) [reset = 0x29]

Bit	Field	Type	Reset	Description
7	device_id[7]	R	0x0	Device ID 0010 1001: DS320PR410
6	device_id[6]	R	0x0	see MSB
5	device_id[5]	R	0x1	see MSB
4	device_id[4]	R	0x0	see MSB
3	device_id[3]	R	0x1	see MSB
2	device_id[2]	R	0x0	see MSB
1	device_id[1]	R	0x0	see MSB
0	device_id[0]	R	0x1	see MSB

2.2 Channel Registers

The DS320PR410 features one bank of channels (Bank 0) consisting of Channels 0-3, which features one register set and requires one SMBus Address.

Table 2-4. Channel Register Base Address Mapping

Channel Registers Base Address	Channel Bank 0 Access
0x00	Channel 0 registers
0x20	Channel 1 registers
0x40	Channel 2 registers
0x60	Channel 3 registers
0x80	Broadcast write channel bank 0 registers, read channel 0 registers
0xA0	Broadcast write channel 0-1 registers, read channel 0 registers
0xC0	Broadcast write channel 2-3 registers, read channel 2 registers
0xE0	Channel 0-3 share registers

Table 2-5. RX Detect Status Register (Channel register base + Offset = 0x00) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	rx_det_comp_p	R	0x0	Rx Detect Positive Polarity Status: 0: Not detected 1: Detected - the value is latched.
6	rx_det_comp_n	R	0x0	Rx Detect Negative Polarity Status: 0: Not detected 1: Detected - the value is latched.
5:0	RESERVED	R	0x0	Reserved

Table 2-6. EQ Control Register (Channel register base + Offset = 0x01) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	eq_stage1_bypass	R/W	0x0	Enable EQ Stage 1 Bypass: 0: Bypass disabled 1: Bypass enabled
6	eq_stage1_3	R/W	0x0	EQ Boost Stage 1 Control. For details, see the DS320PR410 data sheet.
5	eq_stage1_2	R/W	0x0	
4	eq_stage1_1	R/W	0x0	
3	eq_stage1_0	R/W	0x0	
2	eq_stage2_2	R/W	0x0	EQ Boost Stage 2 Control. For details, see the DS320PR410 data sheet.
1	eq_stage2_1	R/W	0x0	
0	eq_stage2_0	R/W	0x0	

Table 2-7. Mute EQ Control Register (Channel register base + Offset = 0x02) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R/W	0x0	Reserved
3	mute_eq	R/W	0x0	Mute EQ output
2:0	RESERVED	R	0x0	Reserved

Table 2-8. EQ Gain / Flat Gain Control Register (Channel register base + Offset = 0x03) [reset = 0x5]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	eq_profile_3	R/W	0x0	EQ mid-frequency boost profile For details, see the DS320PR410 data sheet.
5	eq_profile_2	R/W	0x0	
4	eq_profile_1	R/W	0x0	
3	eq_profile_0	R/W	0x0	
2	flat_gain_2	R/W	0x1	Flat Gain Select. For details, see the DS320PR410 data sheet.
1	flat_gain_1	R/W	0x0	
0	flat_gain_0	R/W	0x1	

Table 2-9. RX Detect Control Register (Channel register base + Offset = 0x04) [reset = 0x0]

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	mr_rx_det_man	R/W	0x0	Manual override of rx_detect_p/n decision: 0: Rx Detect state machine is enabled 1: Rx Detect state machine is overridden – always valid Rx termination detected
1	en_rx_det_count	R/W	0x0	Enable additional RX detect polling: 0: Additional Rx Detect Polling disabled 1: Additional Rx Detect Polling enabled
0	sel_rx_det_count	R/W	0x0	Select number of Valid Rx detect polls - gated by en_rx_det_count = 1. 0: 2x consecutive valid detections 1: 3x consecutive valid detections

Table 2-10. PD Override Register (Channel register base + Offset = 0x05) [reset = 0x3F]

Bit	Field	Type	Reset	Description
7	device_en_override	R/W	0x0	Enable power down overrides through SMBus/I^2C 0: Manual override disabled 1: Manual override enabled
6:0	device_en	R/W	0x3F	Manual power down of redriver various blocks – gated by device_en_override = 1 0x00: All blocks are disabled 0x3F: All blocks are enabled

Table 2-11. Bias Register (Channel register base + Offset = 0x06) [reset = 0x20]

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	bias_current_2	R/W	0x1	Control bias current
4	bias_current_1	R/W	0x0	See MSB.
3	bias_current_0	R/W	0x0	See MSB.
2:0	RESERVED	R	0x0	Reserved

3 Equalization Control Settings

Table 3-1. CTLE Index Equalization Settings

Equalization Setting					Typical EQ Boost (dB)	
	SMBus/I²C Mode					
EQ Index	EQ Control Register Eq_stage1_3:0	EQ Control Register Eq_stage2_2:0	EQ GAIN / Flat Gain Control Register Eq_profile_3:0	EQ Control Register Eq_stage1_bypass	@ 8 GHz	@ 16 GHz
0	0	0	0	1	For values, see the DS320PR410 data sheet	For values, see the DS320PR410 data sheet
1	1	0	0	1		
2	3	0	0	1		
Default	0	0	0	0		
5	0	0	1	0		
6	1	0	1	0		
7	2	0	1	0		
8	3	0	3	0		
9	4	0	3	0		
10	5	1	7	0		
11	6	1	7	0		
12	8	1	7	0		
13	10	1	7	0		
14	10	2	15	0		
15	11	3	15	0		
16	12	4	15	0		
17	13	5	15	0		
18	14	6	15	0		
19	15	7	15	0		

4 CTLE Index and Flat Gain Selection Matrix

Table 4-1. CTLE Index/Flat Gain Setting Matrix

CTLE Index	Flat Gain	Reg. Range Offset 0x01	Reg. Range Offset 0x03
0	-6 dB	0x80	0x00
0	-4 dB	0x80	0x01
0	-2 dB	0x80	0x03
0	0 dB (Default)	0x80	0x05
0	2 dB	0x80	0x07
1	-6 dB	0x88	0x00
1	-4 dB	0x88	0x01
1	-2 dB	0x88	0x03
1	0 dB (Default)	0x88	0x05
1	2 dB	0x88	0x07
2	-6 dB	0x98	0x00
2	-4 dB	0x98	0x01
2	-2 dB	0x98	0x03
2	0 dB (Default)	0x98	0x05
2	2 dB	0x98	0x07
Default	-6 dB	0x00	0x00
Default	-4 dB	0x00	0x01
Default	-2 dB	0x00	0x03

Table 4-1. CTLE Index/Flat Gain Setting Matrix (continued)

CTLE Index	Flat Gain	Reg. Range Offset 0x01	Reg. Range Offset 0x03
Default	0 dB (Default)	0x00	0x05
Default	2 dB	0x00	0x07
5	-6 dB	0x00	0x08
5	-4 dB	0x00	0x09
5	-2 dB	0x00	0x0B
5	0 dB (Default)	0x00	0x0D
5	2 dB	0x00	0x0F
6	-6 dB	0x08	0x08
6	-4 dB	0x08	0x09
6	-2 dB	0x08	0x0B
6	0 dB (Default)	0x08	0x0D
6	2 dB	0x08	0x0F
7	-6 dB	0x10	0x08
7	-4 dB	0x10	0x09
7	-2 dB	0x10	0x0B
7	0 dB (Default)	0x10	0x0D
7	2 dB	0x10	0x0F
8	-6 dB	0x18	0x18
8	-4 dB	0x18	0x19
8	-2 dB	0x18	0x1B
8	0 dB (Default)	0x18	0x1D
8	2 dB	0x18	0x1F
9	-6 dB	0x20	0x18
9	-4 dB	0x20	0x19
9	-2 dB	0x20	0x1B
9	0 dB (Default)	0x20	0x1D
9	2 dB	0x20	0x1F
10	-6 dB	0x29	0x38
10	-4 dB	0x29	0x39
10	-2 dB	0x29	0x3B
10	0 dB (Default)	0x29	0x3D
10	2 dB	0x29	0x3F
11	-6 dB	0x31	0x38
11	-4 dB	0x31	0x39
11	-2 dB	0x31	0x3B
11	0 dB (Default)	0x31	0x3D
11	2 dB	0x31	0x3F
12	-6 dB	0x41	0x38
12	-4 dB	0x41	0x39
12	-2 dB	0x41	0x3B
12	0 dB (Default)	0x41	0x3D
12	2 dB	0x41	0x3F
13	-6 dB	0x51	0x38
13	-4 dB	0x51	0x39
13	-2 dB	0x51	0x3B
13	0 dB (Default)	0x51	0x3D
13	2 dB	0x51	0x3F

Table 4-1. CTLE Index/Flat Gain Setting Matrix (continued)

CTLE Index	Flat Gain	Reg. Range Offset 0x01	Reg. Range Offset 0x03
14	-6 dB	0x52	0x78
14	-4 dB	0x52	0x79
14	-2 dB	0x52	0x7B
14	0 dB (Default)	0x52	0x7D
14	2 dB	0x52	0x7F
15	-6 dB	0x5B	0x78
15	-4 dB	0x5B	0x79
15	-2 dB	0x5B	0x7B
15	0 dB (Default)	0x5B	0x7D
15	2 dB	0x5B	0x7F
16	-6 dB	0x64	0x78
16	-4 dB	0x64	0x79
16	-2 dB	0x64	0x7B
16	0 dB (Default)	0x64	0x7D
16	2 dB	0x64	0x7F
17	-6 dB	0x6D	0x78
17	-4 dB	0x6D	0x79
17	-2 dB	0x6D	0x7B
17	0 dB (Default)	0x6D	0x7D
17	2 dB	0x6D	0x7F
18	-6 dB	0x76	0x78
18	-4 dB	0x76	0x79
18	-2 dB	0x76	0x7B
18	0 dB (Default)	0x76	0x7D
18	2 dB	0x76	0x7F
19	-6 dB	0x7F	0x78
19	-4 dB	0x7F	0x79
19	-2 dB	0x7F	0x7B
19	0 dB (Default)	0x7F	0x7D
19	2 dB	0x7F	0x7F

5 Programming Examples

In the examples below, assume that SMBus secondary address 0x18 is used for Device 0 (Channels 0-3) and SMBus secondary address 0x1A is used for Device 1 (Channels 0-3). Example code using TotalPhase Aardvark I2C controller.

- ***PD control through register programming***
  - Broadcast write to Device 0 and Device 1 Bank 0 registers at Channel register 0x85 (Channel base register 0x80 + PD Override register 0ffset 0x05) with a value of 0x80 to **power down** all channels.
    - <i2c_write addr="0x18" count="0" radix"16">85 80</i2c_write>
    - <i2c_write addr="0x1A" count="0" radix"16">85 80</i2c_write>
  - Broadcast write to Device 0 and Device 1 Bank 0 registers at Channel register 0x85 (Channel base register 0x80 + PD Override register 0ffset 0x05) with a value of 0x7F to **power on** all channels.
    - <i2c_write addr="0x18" count="0" radix"16">85 7F</i2c_write>
    - <i2c_write addr="0x1A" count="0" radix"16">85 7F</i2c_write>

- ***Broadcast Channel CTLE Index/Flat Gain Selection through register programming (CTLE Index 2, FlatGain 0dB)***

  To select CTLE Index 2 with Flat Gain of 0 dB on all channels:

  – Broadcast write to Device 0 and Device 1 Bank 0 registers at Channel register 0x81 (Channel base register 0x80 + EQ Control register 0ffset 0x01) with a value of 0x98.
  – Broadcast write to Device 0 and Device 1 Bank 0 registers at Channel register 0x83 (Channel base register 0x80 + EQ/Gain Control register 0ffset 0x03) with a value of 0x05
    - <i2c_write addr="0x18" count="0" radix"16">81 98</i2c_write>
    - <i2c_write addr="0x18" count="0" radix"16">83 05</i2c_write>
    - <i2c_write addr="0x1A" count="0" radix"16">81 98</i2c_write>
    - <i2c_write addr="0x1A" count="0" radix"16">83 05</i2c_write>
- ***Individual Channel CTLE Index / Flat Gain Selection via register programming (CTLE Index 2, FlatGain 0dB)***

  To select CTLE Index 2 with Flat Gain of 0 dB on a single channel (Channel 0):

  – Write to Channel 0 register on Device 0 Bank 0 and Device 1 Bank 0 registers at Channel register 0x01 (Channel 0 base register 0x00 + EQ Control register 0ffset 0x01) with a value of 0x98.
  – Write to Channel 0 register on Device 0 Bank 0 and Device 1 Bank 0 registers at Channel register 0x03 (Channel 0 base register 0x00 + EQ/Gain Control register 0ffset 0x03) with a value of 0x05
    - <i2c_write addr="0x18" count="0" radix"16">01 98</i2c_write>
    - <i2c_write addr="0x18" count="0" radix"16">03 05</i2c_write>
    - <i2c_write addr="0x1A" count="0" radix"16">01 98</i2c_write>
    - <i2c_write addr="0x1A" count="0" radix"16">03 05</i2c_write>

6 References

- Texas Instruments: *DS320PR410 Four-Channel Linear Redriver for PCIe 5.0, CXL 2.0 Data Sheet* (SNLS739)
- Texas Instruments: *Understanding EEPROM Programming for PCI-Express Gen-4 Redrivers*

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2023	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265