

LMH0318 Programming Guide

This document provides a reference for the LMH0318 Reclocker from a programming model perspective. It contains detailed information relating to programming and different configuration options. The intended audience includes software as well as hardware engineers working on the system diagnostics and control software.

The reader should be familiar with the LMH0318 datasheet ([SNLS508](#)). In addition to the LMH0318 datasheet, all other collateral data related to the LMH0318 Reclocker (application notes, models, etc.), are available on the TI website. Alternatively, contact your local Texas Instruments field sales representative.

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1 Access Methods

Two methods are provided for accessing the LMH0318 Registers:

- Register control via the Serial Management Bus (SMBus)
- Register control via the Serial Parallel Interface (SPI)

In a typical system, either SMBus or SPI access is used to configure and monitor the device status. Unless specified, the register configurations for SPI and SMBus are the same.

1.1 Register Programming via SMBus and SPI Interface

The LMH0318 internal registers can be accessed through standard SMBus or SPI protocol. The SMBUS Mode is enabled by setting MODE_SEL pin = LOW (1 k Ω to GND). Pins associated with SMBus interface are:

- * ADDR0 (pin #2): Strap pin used to set the SMBus address
- * ADDR1 (pin #15): Strap pin used to set the SMBus address
- * SDA (pin #14): SMBus data pin
- * SCL (pin #3): SMBus clock pin

The SMBus slave address is strapped at power up based on the configuration of the ADDR0 and ADDR1 pins. The state of these two pins are read on power up - after the internal power-on reset signal is de-asserted. The maximum operating speed supported on the SMBus is 400 kHz.

There are 16 unique SMBus addresses that can be assigned to each device by placing external Resistor straps on the ADDR0 and ADDR1 pins (pin #2 and #15).

1.1.1 SMBus Slave Address

ADDR0	ADDR1	ADDR0 Binary	ADDR1 Binary	7-bit SMBus Address ⁽¹⁾	8-bit SMBus Write Address
1 k Ω to GND	1 k Ω to GND	00	00	0D	1A
1 k Ω to GND	20 k Ω to GND	00	01	0E	1C
1 k Ω to GND	Float	00	10	0F	1E
1 k Ω to GND	1 k Ω to VDD	00	11	10	20
20 k Ω to GND	1 k Ω to GND	01	00	11	22
20 k Ω to GND	20 k Ω to GND	01	01	12	24
20 k Ω to GND	Float	01	10	13	26
20 k Ω to GND	1 k Ω to VDD	01	11	14	28
Float	1 k Ω to GND	10	00	15	2A
Float	20 k Ω to GND	10	01	16	2C
Float	Float	10	10	17	2E ⁽²⁾
Float	1 k Ω to VDD	10	11	18	30
1 k Ω to VDD	1 k Ω to GND	11	00	19	32
1 k Ω to VDD	20 k Ω to GND	11	01	1A	34
1 k Ω to VDD	Float	11	10	1B	36
1 k Ω to VDD	1 k Ω to VDD	11	11	1C	38

⁽¹⁾ Seven (7) bit SMBus addresses need to include LSB equal to zero for write and 1 for read operation. For example, for 7 bit hex address 0x0D, the controlling program should use I2C hex address 0x1A to write and 0x1B to read. This is true for other addresses as well.

⁽²⁾ Default SMBus Address

1.2 Register Programming via SPI

Alternatively, when MODE_Sel is pulled high with 1 k Ω -resistor, the SPI interface is used for device configuration. Pins associated with the SPI interface are:

- * MOSI: Master Output, Slave input (pin#4)
- * MISO: Master Input, Slave Output (pin#15)
- * SS_N: Slave Select active low (pin#2)
- * SPI_SCK: Serial clock output from master (pin#3)

The maximum operating speed supported on the SPI bus is 20 MHz.

1.3 Register Types

The LMH0318 register set is divided into four groups:

- Global Registers- These registers are divided into share and channel registers. Share register define LMH0318 ID, revision, enabling shared registers. Channels registers are feature specific such as interrupt status or interrupt mask
- Receiver Registers- These registers are associated with input stage of the device - equalizer boost setting, signal detect levels and input mux selection.
- Clock Data Recovery (CDR) Registers- These registers control CDR state machine, Eye Opening Monitor (EOM), and configuration.
- Transmitter Registers- These registers configure output multiplexers and output parameters for OUT0 and OUT1.

2 Initialization Set Up

After power up or register reset write the initialization sequences:

Table 1. LMH0318 Register Initialization

DESCRIPTION	ADDRESS [Hex]	VALUE [Hex]
Enable Channel Registers	0xFF	0x04
Enable Full Temperature Range	0x16	0x25
Initialize CDR State Machine Control	0x3E	0x00
	0x55	0x02
	0x6A	0x00
Restore media CTLE Setting	0x03	xx
Reset CDR	0x0A	0x5C
Release Reset	0x0A	0x50

See [LMH0318 Register Initialization](#) for detailed register programming

3 Register Command Syntax

Unless otherwise specified, the settings below apply to both SMBus and SPI register programming. Operations are read-modify-write. This requires the register to be read first and modified by applying the specific bit mask.

Command Syntax:

RAW	Register Address	Register Content	Register Mask	//Comments
-----	------------------	------------------	---------------	------------

RAW: This defines a Read/Write command
Register Address: Specifies the register address in hex
Register Content Specifies the value in hex that is going to be written
Register Mask: Defines bits within the register content that will be modified
//: Text comment
Example: RAW In this example, we are setting reg 0x80[0] = 1'b to power down OUT0.
 80 01 01 0x80[7:1] are not modified since mask = 0x01

RAR	Register Address	Register Content	Register Mask	//Comments
-----	------------------	------------------	---------------	------------

RAR: Read Only Command
Register Address: Specifies the register address in hex format
Register Content Specifies the register content that is being read
Register Mask: Defines the mask for register content. For example, 1 in a mask defines bits being read
//: Characters following // are text comments
Example: RAR Read 0xE2[4] and check if bit 4 is set
 E2 10 10

- When using SMBus or SPI interface, the host controller may need to set over-ride bit prior to setting the control bits of a register
- It is recommended to issue CDR Reset and Release after changing register settings that alters CDR state machine
- See [Register Tables](#) for further details on register bit definitions

4 Device Configuration

The following sections provide guidance for programming the LMH0318 for certain common applications.

Throughout the rest of the document, macro examples are given to setup the device for different configurations and settings.

4.1 Common Device Configuration

The LMH0318 supports SMPTE data rates. Once configured for SMPTE application, the LMH0318 can be optioned to lock to a selection of data rates and report lock status. The following is an example of common register settings for the LMH0318 initialization followed by possible settings to support SMPTE data rates.

Table 2. LMH0318 SMPTE Configuration

COMMAND	REGISTER	VALUE	MASK	//Comments
				//Initialization sequence
RAW	FF	04	07	//Select Channel Registers
RAW	16	25	FF	//Enable Full Temperature Range
RAW	3E	00	80	//Initialize CDR State Machine Control
RAW	55	02	02	
RAW	6A	00	FF	
RAW	03	XX	FF	//Use the desired CTLE settings. See CTLE Test Mode to determine the CTLE setting
RAW	0A	0C	0C	//Reset CDR
RAW	0A	00	0C	//Release CDR reset
				//In default mode, the LMH0318 automatically locks to different SMPTE and ST-2082/1 data rates
RAR	1	1	1	//Read LOS of IN0
RAW	31	1	3	//Assuming signal is present on IN0, enable IN0 to 75 Ω OUT0 and power down 50 Ω OUT1
RAW	2F	00	C0	//Default SMPTE is enabled
RAW	0A	0C	0C	//Reset CDR
RAW	0A	00	0C	//Release CDR Reset
RAR	02	18	18	//If reg 0x02[4:3] = 11'b, CDR locked
RAW	0C	30	F0	//Setup register 0x0C to enable reg 0x02 to read the VCO divider settings
RAR	02	38	38	//0x02[5:3] Indicates lock rates
RAW	0C	00	F0	//Setup register 0x0C to enable reg 0x02 to read lock indication

4.2 Common Register Commands

The followings macros specify register settings for common operations.

4.2.1 Enable Channel Control

In default mode, the shared registers are enabled. To change any channel specific parameter, input selection, Eye Opening Monitor, Horizontal Eye Opening (HEO), or Vertical Eye Opening (VEO), channel control must first be enabled as follows:

RAW	FF	04	07	//Select Channel Registers
-----	----	----	----	----------------------------

Note: Share register 0xFF can be written/read all the time and does not require selection of share register bank.

4.2.2 LMH0318 Reset Registers

The LMH0318 has two reset functions: CDR State Machine Reset and Register Reset.

4.2.2.1 LMH0318 CDR State Machine Reset

This operation should be done after changing any of the channel registers.

RAW	FF	04	07	//Select Channel Registers
RAW	0A	0C	0C	//Reset for the new settings to take place
RAW	0A	00	0C	//Release CDR Reset

4.2.2.2 LMH0318 Register Reset

Restore registers default settings:

RAW	FF	04	07	//Select Channel Registers
RAW	00	04	04	//Reset Channel Registers
RAW	FF	00	07	//Select shared registers
RAW	E2	01	0F	//Enable Clock Data Recovery (CDR) State Machine
RAR	E2	10	10	//Wait until bit 4 set
RAW	FF	04	07	//Select Channel Register

Note: [LMH0318 Register Initialization](#) must be done after issuing Register Reset

4.2.2.3 LMH0318 Register Initialization

After power up, ENABLE pin transition from low to high, or [LMH0318 Register Reset](#) write the following register initialization.

RAW	FF	04	07	//Select Channel Registers
RAW	16	25	FF	//Enable Full Temperature Range
RAW	3E	00	80	//Initialize CDR State Machine Control
RAW	55	02	02	
RAW	6A	00	FF	
RAW	03	XX	FF	//Use the desired CTLE settings. See CTLE Test Mode to determine the CTLE setting
RAW	0A	0C	0C	//Reset CDR
RAW	0A	00	0C	//Release CDR reset

4.2.3 Force Power Down

The ENABLE pin (#6) can be used to force the LMH0318 in power down. Additionally, the LMH0318 powers down when there is loss of signal (selected channel Signal Detect is not asserted). There could be a need to power down the device even when there is active signal. This could be achieved either by disabling ENABLE pin or forcing the signal detect de-asserted and thus powering down the selected channel.

To force IN0 signal detect off:

RAW	FF	04	07	//Select Channel Registers
RAW	14	40	C0	//Force Signal Detect Off for IN0

To force IN1 signal detect off:

RAW	FF	04	07	//Select Channel Registers
RAW	15	40	C0	//Force Signal Detect Off for IN1

After forcing signal detect off, the controlling program may need to enable the signal detect on IN0 or IN1 (normal operation):

RAW	FF	04	07	//Select Channel Registers
RAW	14	00	C0	//IN0 Signal Detect Normal Operation
RAW	FF	04	07	//Initialize CDR State Machine Control
RAW	15	00	C0	//IN1 Signal Detect Normal Operation

4.2.4 Selective Data Rate Lock

In default mode, the LMH0318 is configured to automatically lock to all SMPTE data rates. The LMH0318 can be configured to lock to certain data rate or restricts the dividers so the CDR can only lock to the desired data rate. This enables faster lock time.

Table 3. SMPTE Data Rate Selection

REGISTER	FUNCTION
Reg 0xA0[4]	1: Enable CDR Lock to 270Mbps
	0: Disable CDR Lock to 270Mbps
Reg 0xA0[3]	1: Enable CDR Lock to 1.485/1.4835 Gbps
	0: Disable CDR Lock to 1.485/1.4835 Gbps
Reg 0xA0[2]	1: Enable CDR Lock to 2.97/2.967 Gbps
	0: Disable CDR Lock to 2.97/2.967 Gbps

For example, to enable lock to 3G, HD, and 270 Mbps, the following script can be used:

RAW	FF	04	07	//Select Channel Registers
RAW	A0	1C	1F	//Enable Lock to ST 424, ST 292, and ST 259 only
RAW	0A	0C	0C	//Initialize CDR State Machine Control
RAW	0A	00	0C	//Release CDR Reset

Alternatively, the following sequence can be used to disable lock to certain data rates (for example 3G):

RAW	FF	04	07	//Select Channel Registers
RAW	A0	00	04	//Disable Lock to 3G
RAW	0A	0C	0C	//Reset CDR
RAW	0A	00	0C	//Release CDR Reset

4.2.5 Check Status of LOS (Loss Of Signal) on Input 1 or Input 0

The LMH0318 has two inputs and each input has its own signal detector. Based on signal detect status and input channel selected, the device automatically goes into power down. For example, if IN0 is selected and there is no signal on IN0 then the device, CDR and output drivers go into power down. The following macro checks the status of the signal detects on IN0 or IN1:

RAW	FF	04	07	//Select Channel Registers
RAW	1	01	01	//Read LOS of IN0
RAW	1	02	02	//Read LOS of IN1

4.2.6 Input/Output Selection

The LMH0318 has 2:1 Mux on the Input and 1:2 Fan out on the output. Different input and output configuration can be selected. The following settings allow these different configurations:

RAW	FF	04	07	//Select Channel Registers
RAW	31	00	03	//Set to 00: Enable IN0 to OUT0 and OUT1
//				
RAW	FF	04	07	//Select Channel Registers
RAW	31	01	03	//Set to 01: Enable IN0 to OUT0 (OUT1 is powered down)
//				
RAW	FF	04	07	//Select Channel Registers
RAW	31	02	03	//Set to 10: Enable IN1 to OUT1 (OUT0 is powered down)
//				
RAW	FF	04	07	//Select Channel Registers
RAW	31	03	03	//Set to 11: Enable IN1 to OUT0 and OUT1

4.2.7 CTLE Test Mode

The LMH0318 Continuous Time Linear Equalizer compensates for the high frequency loss caused by the transmission media. Deterministic jitter due to the ISI (Inter Symbol Interference) caused by the media can be equalized by the LMH0318 CTLE.

In the default mode, the CTLE boost is determined by register 0x03. The default value of 0x80'h equalizes 10-15 inches PCB FR4 trace loss. The user may change register 0x03 to enable different boost settings for different media loss characteristics . [Table 4](#) shows recommended CTLE boost settings vs different media trace length.

Table 4. CTLE Boost Setting vs Media Trace Length

FR4 TRACE LENGTH (Inches)	SDD21 (dB) @ 6 GHz	REGISTER	WRITE VALUE	BOOST SETTING @ 3 GHz (dB)	BOOST SETTING @ 6 GHz (dB)
1	-1.5	0x03	0x00	4.9	5.8
5	-7.5	0x03	0x00	4.9	5.8
10	-10.5	0x03	0x10	7.7	10.2
15	-15.5	0x03	0x50	10.9	15.3
20	-19.5	0x03	0x50	10.9	15.3
25	-24.5	0x03	0x60	13.2	17
30	-27.5	0x03	0x94	16.2	21.8

For test purpose only, the register sequence below determines the correct CTLE setting. Note, the selected CTLE setting produced by the test mode works for all of the data rates; therefore, this test should be done at the highest data rate. The CTLE compensates for the media not the data rate. Additionally, for 3 Gbps or lower, register 0x55 specifies the fixed CTLE setting when operating in CTLE test mode.

RAW	FF	04	07	//Select Channel Registers
RAW	2D	00	08	//Disable EQ over-ride
RAW	2C	40	40	//Enable VEO scaling
RAW	3E	80	80	//Enable HEO/VEO
RAW	6A	44	FF	
RAW	31	20	60	//Enable CTLE Test Mode to optimize eye opening
RAW	0A	0C	0C	//Reset CDR for the new settings to take place
RAW	0A	00	0C	//Release CDR Reset
RAW	0C	00	F0	//Setup register 0x0C to read lock indication
RAW	02	18	18	//Wait until bits [4:3] = 11'b to indicate CDR locked
RAR	52	xx	FF	//Read EQ Boost setting and store in xx for normal mode of operation
RAW	03	xx	FF	//Save EQ Boost setting in reg 0x03
RAW	2D	08	08	//Enable the device to force EQ Setting from Reg 0x03
RAW	31	00	60	//Allow register 0x03 to control CTLE setting
RAW	3E	00	80	//Restore initialization settings
RAW	6A	00	FF	//Restore initialization settings
RAW	2C	00	40	//Disable VEO scale

4.2.8 Eye Opening Monitoring Operation

The LMH0318 has an on-chip eye opening monitor (EOM) which can be used to analyze, monitor, and diagnose the performance of the link. The EOM operates on the post-equalized waveform, just prior to the data sampler. Therefore, it captures the effects of all the equalization circuits within the receiver.

The EOM monitors the post-equalized waveform in a time window that spans one unit intervals and a configurable voltage range that spans up to ± 400 mV differential. The time window and voltage range are divided into 64 steps, so the result of the eye capture is a 64×64 matrix of "hits," where each point represents a specific voltage and phase offset relative to the main data sampler. The number of "hits" registered at each point needs to be put into context with the total number of bits observed at that voltage and phase offset in order to determine the corresponding probability for that point. The number of bits observed at each point is configurable.

A common measurement performed by the EOM is the horizontal and vertical eye opening. The Horizontal Eye Opening (HEO) represents the width of the post-equalized eye at 0-V differential amplitude, typically measured in unit intervals or pico-seconds. The Vertical Eye Opening (VEO) represents the height of the post-equalized eye, measured midway between the mean zero crossing of the eye. This position in time approximates that of the CDR sampling phase. The followings are the steps required to read eye hits for 64×64 cells or total 4096 cells.

RAW	FF	04	07	//Select Channel Registers
RAW	11	00	20	//Enable EOM
RAW	24	80	80	// Start Fast EOM
RAR	24	00	01	//Wait until EOM samples ready (0x24[0]= 0'b)
RAW	26	xx	00	//Read Reg 0x26 and discard the content
RAR	24	00	01	//Wait until EOM Samples Ready
RAW	26	xx	00	//Read Reg 0x26
RAR	24	00	01	//Wait until EOM Samples Ready
RAW	25	xx	FF	//Read Reg 0x25 and save number of eye hits
RAW	26	xx	FF	//Read Reg 0x26 and save number of eye hits
				//Execute the above three commands for 4095 times (total 4096 times for 64X64 cells)
RAW	24	00	80	//Disable fast EOM
RAW	11	20	20	//Power down EOM

4.2.9 Lock Data Rate Indication

There could be a need to realize the data rate the device has locked to. In this case, register 0x02[4] is read to make sure the device is locked. Then VCO divisor setting indicates the data rate.

RAW	FF	04	07	//Select Channel Registers
RAW	0C	00	F0	//Setup register 0x0c to read lock indication bit 4
RAW	02	18	18	//Wait until bit 4 is set indicating device is locked
RAW	0C	30	F0	//Setup register 0x0C to read the VCO divider setting
RAR	02	38	38	//Read divider settings
				// 02[5-3] = 010'b 2.97 Gbps
				// 02[5-3] = 011'b 1.485 Gbps
				// 02[5-3] = 100'b 270Mbps
RAW	0C	00	F0	//Setup the default value for Reg 0x0C

4.2.10 Read Horizontal and Vertical Eye Opening

The LMH0318 produces two readings to indicate line signal quality: The Horizontal Eye Opening (HEO) and the Vertical Eye Opening (VEO) are indications of signal quality. These parameters can be read by the host processor or the LMH0318 can be optioned to cause interrupt if HEO/VEO reach a threshold.

To convert the HEO reading to Unit Interval (UI) eye opening, we need to divide the HEO reading, in decimal, to 64.

$$\text{HEO} = (\text{Decimal Reg0x27})/64$$

For example, if the HEO reading is 0x31 (49 decimal) then the HEO UI eye opening would be $49/64=0.77\text{UI}$. This means the HEO is about 77% open.

Similarly, VEO has 64 steps as well. The chip automatically covers differential peak to peak value from +/-100mV to +/-400mV and reports the value adjusted to +/-100 mV. Thus, each step is $200/64$ or 3.125 mV. Therefore VEO in mV = (Decimal VEO value) \times 3.125. For example, if we read 0xC8 (200 decimal) for the VEO reading, this corresponds to $200 \times 3.125 \text{ mV} = 625 \text{ mV}$ vertical eye opening.

RAW	FF	04	07	//Select Channel Registers
RAW	11	00	20	//Enable EOM
RAW	3E	80	80	//Enable HEO/VEO
RAR	27	xx	FF	//Read HEO, convert hex to dec, then divide by 64 for value in UI
RAR	28	xx	FF	//Read VEO, convert hex to decimal and Multiply by 3.125mV
RAW	3E	00	80	//Restore initialization setting
RAW	11	20	20	//Power down EOM

4.2.11 OUT0 and OUT1 Mode Selection

The LMH0318 75-Ω OUT0 and 50-Ω OUT1 can be configured to drive out the reclocked data, raw data (i.e non reclocked), clock, or these outputs to be muted (common mode voltage on both positive and negative output signal).

4.2.11.1 OUT0 and OUT1 Default Mode of Operation

In default mode, register 0x1C[3:2] determine the output configuration for both outputs per following table.

0x1C[3:2]	OUT0	OUT1
00	Mute	Mute
01	Locked: Reclocked Data Unlocked: Raw Data	Full data rate clock Unlocked: Mute
10	Locked: Reclocked Data Unlocked: Raw Data	Locked: Reclocked Data Unlocked: Raw Data
11	Forced Raw Data	Forced Raw Data

The following can be used to set OUT0 and OUT1 configuration:

RAW	FF	04	07	//Select Channel Registers
RAW	09	00	20	//Allow register 0x1C to control OUT0 and OUT1 configuration
RAW	1C	00	0C	//Mute OUT0 and OUT1
RAW	1C	04	0C	//Locked: OUT0 Reclocked Data OUT1 Recovered Clock Un-Locked: OUT0 Raw Data OUT1 Mute
RAW	1C	80	0C	//Locked: OUT0: Reclocked Data OUT1: Reclocked Data Un-Locked: OUT0 Raw Data OUT1 Raw data
RAW	1C	0C	0C	//OUT0 Raw Data OUT1 Raw Data

4.2.11.2 **OUT0 and OUT1 Independent Control:**

The LMH0318 allows independent control of OUT0 and OUT1. Note: 0x09[5] over-ride effects both OUT0 and OUT1.

4.2.11.2.1 **OUT0 10 MHz Clock**

RAW	FF	04	07	//Select Channel Registers
RAW	09	20	20	//Enable Over-ride
RAW	1C	20	F0	//10MHz on OUT0

4.2.11.2.2 **OUT0 RAW Data**

RAW	FF	04	07	//Select Channel Registers
RAW	09	20	20	//Enable over-ride
RAW	1C	40	E0	//OUT0 Raw Data

4.2.11.2.3 **OUT0 Mute**

RAW	FF	04	07	//Select Channel Registers
RAW	09	20	20	//Enable Over-ride
RAW	1C	00	E0	//Set to 0: Mute OUT0

4.2.11.2.4 **OUT0 Reclocked Data**

RAW	FF	04	07	//Select Channel Registers
RAW	09	20	20	//Enable Over-ride
RAW	1C	80	E0	//OUT0 Reclocked Data (valid only in locked condition)

4.2.11.2.5 **OUT1 RAW Data**

RAW	FF	04	07	//Select Channel Registers
RAW	09	20	20	//Enable Over-ride to control this setting with registers
RAW	1E	00	E0	//OUT1 RAW Data

4.2.11.2.6 **OUT1 Mute**

When OUT1 is muted, the differential peak-to-peak output voltage is approximately 0 V.

RAW	FF	04	07	//Select Channel Registers
RAW	09	20	20	//Enable over-ride to control with registers
RAW	1E	E0	E0	//Set to 0: Mute OUT1

4.2.11.2.7 OUT1 Reclocked Data

RAW	FF	04	07	//Select Channel Registers
RAW	09	20	20	//Enable over-ride
RAW	1E	20	E0	//Locked: OUT1 Reclocked Data (valid only in locked condition)

4.2.11.2.8 OUT1 Full Rate Clock

The following sequence enables full rate or line recovered clock.

RAW	FF	04	07	//Select Channel Registers
RAW	09	20	20	//Enable over-ride
RAW	1E	40	E0	//OUT1 full rate clock

4.2.11.2.9 OUT1 10 MHz Clock

RAW	FF	04	07	//Select Channel Registers
RAW	09	20	20	//Enable over-ride
RAW	1E	A0	E0	//Enable 10 MHz on OUT1

4.2.12 Invert OUT1 Data Polarity

For ease of layout, there may be a need to invert the polarity of the OUT1 differential pair.

RAW	FF	04	07	//Select Channel Registers
RAW	1E	80	80	//Invert OUT1 Polarity

4.2.13 OUT0 and OUT1 Settings

The LMH0318 has programmable VOD (Voltage Output Differential), Pre-Emphasis (OUT0), PW (Pulse Width OUT0 settings), De-Emphasis Settings, and individual power-down settings

4.2.13.1 OUT0 VOD Settings

75-Ω OUT0 has programmable peak to peak setting from 720 mV to 880 mV. In default mode, output voltage setting is expected to be 800mV ±15 mV. To increase or decrease the output voltage swing, the content of Reg 0x80[7:4] has to be read first and then increased or decreased respectively. Note: In raw mode, the VOD setting would use register setting -3 (irrespective of the data rate).

RAW	FF	04	07	//Select Channel Registers
RAR	80	XX	F0	//Read Register 0x80[7:4]
RAW	80	XX	F0	//Adjust by 1, 2, or 3 to get the desired output voltage swing

4.2.13.2 OUT0 Power Down or Power Up

The LMH0318 OUT0 75 Ω current mode output draws high current and can be powered down to save power.

RAW	FF	04	07	//Select Channel Registers
RAW	80	03	03	//Power Down OUT0
RAW	FF	04	07	//Select Channel
RAW	80	02	03	//Power up OUT0

4.2.13.3 OUT1 VOD Settings

OUT1 VOD settings can have a range of 600 mv to 1300 mv:

RAW	FF	04	07	//Select Channel Registers
RAW	84	00	70	//Set drv_1_sel_vod to 0 (570 mVp-p)
RAW	84	20	70	//Set drv_1_sel_vod to 2 (730 mVp-p)
RAW	84	40	70	//Set drv_1_sel_vod to 4 (900 mVp-p)
RAW	84	60	70	//Set drv_1_sel_vod to 6 (1035 mVp-p)

4.2.13.4 OUT1 De-Emphasis Settings

There are 15 output de-emphasis settings for the LMH0318 OUT1, ranging from 0 dB to -11 dB. The de-emphasis values come from register 0x85, bits 2:0 and 0x85 bit 3, which is the de-emphasis range bit.

RAW	FF	04	07	//Select Channel Registers
RAW	85	00	0F	//OUT1 DE Setting set to 0 dB
RAW	85	02	0F	//OUT1 DE Setting set to -2 dB
RAW	85	07	0F	//OUT1 DE Setting set to -11 dB

4.2.13.5 OUT1 Power Down

If needed the OUT1 output can be powered down:

RAW	FF	04	07	//Select Channel Registers
RAW	84	03	03	//Power Down out1
RAW	84	02	03	//Power Up OUT1 (normal operating State)

4.2.14 Signal Quality Alert HEO Interrupt Threshold

The LMH0318 can be optioned to cause interrupt if HEO goes below certain threshold and reg 0x56[3] = 1'b. The LMH0318 compares HEO value, reg 0x27[7:0], vs threshold setting of reg 0x32[7:4]*4. Note: Register 0x54[7:0] indicates source of interrupt. Also, reg 0x FF[5] needs to be set to enable interrupt on to LOS pin.

RAW	FF	04	07	//Select Channel Registers
RAW	11	00	20	//Enable EOM
RAW	32	60	F0	//Set HEO interrupt threshold level: $6*4 = 24/64 = .37$ If HEO drops below 0.37UI enable interrupt
RAW	56	08	08	//Enable HEO/VEO Signal Quality Alert interrupt
RAW	FF	20	20	//Enable interrupt onto LOS pin
RAW	0A	0C	0C	//Reset CDR
RAW	0A	00	0C	//Release CDR Reset so changes will go into effect

4.2.15 Signal Quality Alert VEO Threshold Settings

Similar to HEO setting, the VEO can also be programmed to cause if VEO drops below a threshold.

RAW	FF	04	07	//Select Channel Registers
RAW	11	00	20	//Enable EOM
RAW	32	06	0F	//Set VEO interrupt threshold level: $6*4*3.125 = 75\text{mV}$ If VEO drops below 75 mV enable interrupt
RAW	56	04	08	//Enable HEO/VEO Signal Quality Alert interrupt
RAW	FF	80	20	//Enable interrupt onto LOS pin
RAW	0A	0C	0C	//Reset CDR
RAW	0A	00	0C	//Release CDR Reset so changes will go into effect

5 Register Tables

Register Maps

The LMH0318 register set definition is organized into four groups:

1. Global Registers: Chip ID, Interrupt status, LOS registers
2. Receiver Registers: Equalizer boost settings and signal detect setting
3. CDR Registers: PLL control
4. Transmitter Registers: OUT0 and OUT1 parameter setting

The typical device initialization sequence for the LMH0318 includes the followings. For detailed register settings See *LMH0318 Programming Guide* ([SNLU183](#)).

1. Shared Register Configuration
 - (a) Reading device ID
 - (b) Selecting interrupt on to LOS pin
 - (c) Settings up the register to access the channel registers
2. Channel Register Configuration
 - (a) CDR Reset
 - (b) Interrupt register configuration
 - (c) Optional Input/Output selection
 - (d) Optional VOD selection
 - (e) CDR Reset and Release

5.1 Global Registers

Table 5. Global Registers

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
SMBus Observation		Reg_0x00 Share	0x00		SMBus Address Observation
	7	SMBUS_addr3	0	R	SMBus strap observation
	6	SMBUS_addr2	0	R	
	5	SMBUS_addr1	0	R	
	4	SMBUS_addr0	0	R	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
Reset Shared Regs		Reg 0x04 Share	0x01		Shared Register Reset
	7	Reserved	0	RW	
	6	rst_i2c_regs	0	RW	1: Reset Shared Registers 0: Normal operation
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	1	RW	
Enable SMBus Strap		Reg 0x06 Share	0x00		Allow SMBus strap observation
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	

Table 5. Global Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
	4	Reserved	0	RW	
	3	Test control[3]	0	RW	Set to >9 to allow strap observation on share reg 0x00
	2	Test control[2]	0	RW	
	1	Test control[1]	0	RW	
	0	Test control[0]	0	RW	
Device Version		Reg 0xF0 Share	0x01		Device Version
	7	VERSION[7]	0	RW	Device revision
	6	VERSION[6]	0	RW	
	5	VERSION[5]	0	RW	
	4	VERSION[4]	0	RW	
	3	VERSION[3]	0	RW	
	2	VERSION[2]	0	RW	
	1	VERSION[1]	0	RW	
	0	VERSION[0]	1	RW	
Channel Control		Reg 0xFF Control	0x00		Enable Channel Control
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	los_int_bus_sel	0	RW	1: Selects interrupt onto LOS pin 0: Selects signal detect onto LOS pin
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	en_ch_Access	0	RW	1: Enables access to channel registers 0: Enables access to share registers
	1	Reserved	0	RW	
	0	Reserved	0	RW	
Reset_Channel_Regs		Reg_0x00 Channel	0x00		Reset all Channel Registers to Default Values
	7	Reserved	0		
	6	Reserved	0		
	5	Reserved	0		
	4	Reserved	0		
	3	Reserved	0		
	2	Rst_regs	0		1: Reset Channel Registers (self clearing) 0: Normal operation
	1	Reserved	0		
	0	Reserved	0		
LOS_status		Reg_0x01 Channel	0x00		Signal Detect Status
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	LOS1	0	R	1: Loss of signal on IN1 0: Signal present on IN1
	0	LOS0	0	R	1: Loss of signal on IN0 0: Signal present on IN0

Table 5. Global Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
CDR_Status_1		Reg_0x02 Channel	0x00		CDR Status
	7	Reserved	0	R	
	6	Reserved	0	R	
	5	Reserved	0	R	
	4	cdr_status[4]	0	R	11: CDR locked 00: CDR not locked
	3	cdr_status[3]	0	R	
	2	Reserved	0	R	
	1	Reserved	0	R	
	0	Reserved	0	R	
Interrupt Status Register		Reg_0x54 Channel	0x00		Interrupt Status (clears upon read)
	7	Sigdet	0	R	1: Signal Detect from the selected input asserted 0: Signal Detect from the selected input de-asserted
	6	cdr_lock_int	0	R	1: CDR Lock interrupt 0: No interrupt from CDR Lock
	5	signal_det1_int	0	R	1: IN1 Signal Detect interrupt 0: No interrupt from IN1 Signal Detect
	4	signal_det0_int	0	R	1: IN0 Signal Detect interrupt 0: No interrupt from IN0 Signal Detect
	3	heo_veo_int	0	R	1: HEO_VEO Threshold reached interrupt 0: No interrupt from HEO_VEO
	2	cdr_lock_loss_int	0	R	1: CDR loss of lock interrupt 0: No interrupt from CDR lock
	1	signal_det1_loss_int	0	R	1: IN1 Signal Detect loss interrupt 0: No interrupt from IN1 Signal Detect
	0	signal_det0_loss_int	0	R	1: IN0 Signal Detect loss interrupt 0: No interrupt from IN0 Signal Detect

Table 5. Global Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
Interrupt Control		Reg 0x56 Channel	0x00		Interrupt Mask
	7	Reserved	0	RW	
	6	cdr_lock_int_en	0	RW	1: Enable Interrupt if CDR lock is achieved 0: Disable interrupt if CDR lock is achieved
	5	signal_det1_int_en	0	RW	1: Enable interrupt if IN1 Signal Detect is asserted 0: Disable interrupt if IN1 Signal Detect is asserted
	4	signal_det0_int_en	0	RW	1: Enable interrupt if IN0 Signal Detect is asserted 0: Disable interrupt if IN0 Signal Detect is asserted
	3	heo_veo_int_en	0	RW	1: Enable interrupt if HEO-VEO threshold is reached 0: Disable interrupt due to HEO-VEO threshold
	2	cdr_lock_loss_int_en	0	RW	1: Enable interrupt if CDR loses lock 0: Disable interrupt if CDR loses lock
	1	signal_det1_loss_int_en	0	RW	1: Enable interrupt if there is loss of signal on IN1 0: Disable interrupt if there is loss of signal on IN1
	0	signal_det0_loss_int_en	0	RW	1: Enable interrupt if there is loss of signal on IN0 0: Disable interrupt if there is loss of signal on IN0

5.2 Receiver Registers

Table 6. Receiver Registers

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
EQ_Boost		Reg 0x03 Channel	0x80		4 Stage EQ Boost Levels. Read-back value going to CTLE in reg_0x52. Used for setting EQ value when reg_0x2D[3] is high
	7	eq_BST0[1]	1	RW	2 Bits control for stage 0 of the CTLE. Adapts during CTLE adaptation
	6	eq_BST0[0]	0	RW	
	5	eq_BST1[1]	0	RW	2 Bits control for stage 1 of the CTLE. Adapts during CTLE adaptation
	4	eq_BST1[0]	0	RW	
	3	eq_BST2[1]	0	RW	2 Bits control for stage 2 of the CTLE. Adapts during CTLE adaptation
	2	eq_BST2[0]	0	RW	
	1	eq_BST3[1]	0	RW	2 Bits control for stage 3 of the CTLE. Adapts during CTLE adaptation
	0	eq_BST3[0]	0	RW	
SD_EQ		Reg_0x0D Channel	0x00		270 Mbps EQ Boost Setting
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Mr_auto_eq_en_bypass	0	RW	1: EQ Bypass for 270 Mbps 0: Use EQ Settings in reg0x03[7:0] for 270 Mbps Note: If 0x13[1] mr_eq_en_bypass is set, bypass would be set and auto-bypass has no significance.
EQ_SD_CONFIG		Reg 0x13 Channel	0x90		Channel EQ Bypass and Power Down
	7	Reserved	1	RW	
	6	sd_0_PD	0	RW	1: Power Down IN0 Signal Detect 0: IN0 Signal Detect normal operation
	5	sd_1_PD	0	RW	1: Power Down IN1 Signal Detect 0: IN1 Signal Detect normal operation
	4	Reserved	1	RW	
	3	eq_PD_EQ	0	RW	Controls the power-state of the selected channel. The un-selected channel is always powered-down 1: Powers down selected channel EQ stage 0: Powers up EQ of the selected channel
	2	Reserved	0	RW	
	1	eq_en_bypass	0	RW	1: Bypass stage 3 and 4 of CTLE 0: Enable Stage 3 and 4 of CTLE
	0	Reserved	0	RW	

Table 6. Receiver Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
SD0_CONFIG		Reg 0x14 Channel	0x00		IN0 Signal Detect Threshold Setting
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	sd_0_refa_sel[1]	0	RW	Controls signal detect S _{DH} ⁻ Assert [5:4], S _{D_L} ⁻ De-Assert [3:2], thresholds for IN0 0000: Default levels (nominal) 0101: Nominal -2 mV 1010: Nominal +5 mV 1111: Nominal +3 mV
	4	sd_0_refa_sel[0]	0	RW	
	3	sd_0_refd_sel[1]	0	RW	
	2	sd_0_refd_sel[0]	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
SD1_CONFIG		Reg_0x15 Channel	0x00		IN1 Signal Detect Threshold Setting
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	sd_1_refa_sel[1]	0	RW	Controls signal detect S _{DH} ⁻ Assert [5:4], S _{D_L} ⁻ De-Assert [3:2], thresholds for IN1 0000: Default levels (nominal) 0101: Nominal -2 mV 1010: Nominal +5 mV 1111: Nominal +3 mV
	4	sd_1_refa_sel[0]	0	RW	
	3	sd_1_refd_sel[1]	0	RW	
	2	sd_1_refd_sel[0]	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
EQ_BOOST_OV		Reg_0x2D Channel	0x88		EQ Boost Override
	7	Reserved	1	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	reg_eq_bst_ov	1	RW	1: Enable EQ boost over ride See LMH0318 Programming Guide (SNLU183) 0: Disable EQ boost over ride
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
CTLE Setting		Reg_0x31 Channel	0x00		CTLE Mode of Operation and Input/Output Mux Selection
	7	Reserved	0	RW	
	6	adapt_mode[1]	00	RW	00: Normal Operation - Manual CTLE Setting 01: Test Mode - See the LMH0318 Programming Guide (SNLU183) for details Other Settings - Invalid
	5	adapt_mode[0]			
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	input_mux_ch_sel[1]	0	RW	IN0/1 and OUT0/1 selection 00: selects IN0 and OUT0/1 01: selects IN0 and OUT0 10: selects IN1 and OUT1 11: selects IN1 and OUT0/1
	0	input_mux_ch_sel[0]	0	RW	

Table 6. Receiver Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
LOW_RATE_EQ_BST		Reg 0x3A Channel	0x00		HD and SD EQ Level
	7	fixed_eq_BST0[1]	0	RW	When CTLE is operating in test mode, Reg 0x3A[7:0] forces fixed EQ setting. In normal operating manual mode Reg_0x03 forces EQ boost. See LMH0318 Programming Guide (SNLU183) for details
	6	fixed_eq_BST0[0]	0	RW	
	5	fixed_eq_BST1[1]	0	RW	
	4	fixed_eq_BST1[0]	0	RW	
	3	fixed_eq_BST2[1]	0	RW	
	2	fixed_eq_BST2[0]	0	RW	
	1	fixed_eq_BST3[1]	0	RW	
	0	fixed_eq_BST3[0]	0	RW	
BST_Indx0		Reg_0x40 Channel	0x00		Index0 4 Stage EQ Boost. See LMH0318 Programming Guide (SNLU183)
	7	I0_BST0[1]	0	RW	Index 0 Boost Stage 0 bit 1
	6	I0_BST0[0]	0	RW	Index 0 Boost Stage 0 bit 0
	5	I0_BST1[1]	0	RW	Index 0 Boost Stage 1 bit 1
	4	I0_BST1[0]	0	RW	Index 0 Boost Stage 1 bit 0
	3	I0_BST2[1]	0	RW	Index 0 Boost Stage 2 bit 1
	2	I0_BST2[0]	0	RW	Index 0 Boost Stage 2 bit 0
	1	I0_BST3[1]	0	RW	Index 0 Boost Stage 3 bit 1
	0	I0_BST3[0]	0	RW	Index 0 Boost Stage 3 bit 0
BST_Indx1		Reg 0x41 Channel	0x40		Index1 4 Stage EQ Boost.
	7	I1_BST0[1]	0	RW	Index 1 Boost Stage 0 bit 1
	6	I1_BST0[0]	1	RW	Index 1 Boost Stage 0 bit 0
	5	I1_BST1[1]	0	RW	Index 1 Boost Stage 1 bit 1
	4	I1_BST1[0]	0	RW	Index 1 Boost Stage 1 bit 0
	3	I1_BST2[1]	0	RW	Index 1 Boost Stage 2 bit 1
	2	I1_BST2[0]	0	RW	Index 1 Boost Stage 2 bit 0
	1	I1_BST3[1]	0	RW	Index 1 Boost Stage 3 bit 1
	0	I1_BST3[0]	0	RW	Index 1 Boost Stage 3 bit 0
BST_Indx2		Reg 0x42 Channel	0x80		Index2 4 Stage EQ Boost.
	7	I2_BST0[1]	1	RW	Index 2 Boost Stage 0 bit 1
	6	I2_BST0[0]	0	RW	Index 2 Boost Stage 0 bit 0
	5	I2_BST1[1]	0	RW	Index 2 Boost Stage 1 bit 1
	4	I2_BST1[0]	0	RW	Index 2 Boost Stage 1 bit 0
	3	I2_BST2[1]	0	RW	Index 2 Boost Stage 2 bit 1
	2	I2_BST2[0]	0	RW	Index 2 Boost Stage 2 bit 0
	1	I2_BST3[1]	0	RW	Index 2 Boost Stage 3 bit 1
	0	I2_BST3[0]	0	RW	Index 2 Boost Stage 3 bit 0

Table 6. Receiver Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
BST_Idx3		Reg 0x43 Channel	0x50		Index3 4 Stage EQ Boost.
	7	I3_BST0[1]	0	RW	Index 3 Boost Stage 0 bit 1
	6	I3_BST0[0]	1	RW	Index 3 Boost Stage 0 bit 0
	5	I3_BST1[1]	0	RW	Index 3 Boost Stage 1 bit 1
	4	I3_BST1[0]	1	RW	Index 3 Boost Stage 1 bit 0
	3	I3_BST2[1]	0	RW	Index 3 Boost Stage 2 bit 1
	2	I3_BST2[0]	0	RW	Index 3 Boost Stage 2 bit 0
	1	I3_BST3[1]	0	RW	Index 3 Boost Stage 3 bit 1
	0	I3_BST3[0]	0	RW	Index 3 Boost Stage 3 bit 0
BST_Idx4		Reg 0x44 Channel	0xC0		Index4 4 Stage EQ Boost.
	7	I4_BST0[1]	1	RW	Index 4 Boost Stage 0 bit 1
	6	I4_BST0[0]	1	RW	Index 4 Boost Stage 0 bit 0
	5	I4_BST1[1]	0	RW	Index 4 Boost Stage 1 bit 1
	4	I4_BST1[0]	0	RW	Index 4 Boost Stage 1 bit 0
	3	I4_BST2[1]	0	RW	Index 4 Boost Stage 2 bit 1
	2	I4_BST2[0]	0	RW	Index 4 Boost Stage 2 bit 0
	1	I4_BST3[1]	0	RW	Index 4 Boost Stage 3 bit 1
	0	I4_BST3[0]	0	RW	Index 4 Boost Stage 3 bit 0
BST_Idx5		Reg 0x45 Channel	0x90		Index5 4 Stage EQ Boost.
	7	I5_BST0[1]	1	RW	Index 5 Boost Stage 0 bit 1
	6	I5_BST0[0]	0	RW	Index 5 Boost Stage 0 bit 0
	5	I5_BST1[1]	0	RW	Index 5 Boost Stage 1 bit 1
	4	I5_BST1[0]	1	RW	Index 5 Boost Stage 1 bit 0
	3	I5_BST2[1]	0	RW	Index 5 Boost Stage 2 bit 1
	2	I5_BST2[0]	0	RW	Index 5 Boost Stage 2 bit 0
	1	I5_BST3[1]	0	RW	Index 5 Boost Stage 3 bit 1
	0	I5_BST3[0]	0	RW	Index 5 Boost Stage 3 bit 0
BST_Idx6		Reg 0x46 Channel	0x54		Index6 4 Stage EQ Boost.
	7	I6_BST0[1]	0	RW	Index 6 Boost Stage 0 bit 1
	6	I6_BST0[0]	1	RW	Index 6 Boost Stage 0 bit 0
	5	I6_BST1[1]	0	RW	Index 6 Boost Stage 1 bit 1
	4	I6_BST1[0]	1	RW	Index 6 Boost Stage 1 bit 0
	3	I6_BST2[1]	0	RW	Index 6 Boost Stage 2 bit 1
	2	I6_BST2[0]	1	RW	Index 6 Boost Stage 2 bit 0
	1	I6_BST3[1]	0	RW	Index 6 Boost Stage 3 bit 1
	0	I6_BST3[0]	0	RW	Index 6 Boost Stage 3 bit 0
BST_Idx7		Reg 0x47 Channel	0xA0		Index7 4 Stage EQ Boost.
	7	I7_BST0[1]	1	RW	Index 7 Boost Stage 0 bit 1
	6	I7_BST0[0]	0	RW	Index 7 Boost Stage 0 bit 0
	5	I7_BST1[1]	1	RW	Index 7 Boost Stage 1 bit 1
	4	I7_BST1[0]	0	RW	Index 7 Boost Stage 1 bit 0
	3	I7_BST2[1]	0	RW	Index 7 Boost Stage 2 bit 1
	2	I7_BST2[0]	0	RW	Index 7 Boost Stage 2 bit 0
	1	I7_BST3[1]	0	RW	Index 7 Boost Stage 3 bit 1
	0	I7_BST3[0]	0	RW	Index 7 Boost Stage 3 bit 0

Table 6. Receiver Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
BST_Indx8		Reg 0x48 Channel	0xB0		Index8 4 Stage EQ Boost.
	7	I8_BST0[1]	1	RW	Index 8 Boost Stage 0 bit 1
	6	I8_BST0[0]	0	RW	Index 8 Boost Stage 0 bit 0
	5	I8_BST1[1]	1	RW	Index 8 Boost Stage 1 bit 1
	4	I8_BST1[0]	1	RW	Index 8 Boost Stage 1 bit 0
	3	I8_BST2[1]	0	RW	Index 8 Boost Stage 2 bit 1
	2	I8_BST2[0]	0	RW	Index 8 Boost Stage 2 bit 0
	1	I8_BST3[1]	0	RW	Index 8 Boost Stage 3 bit 1
	0	I8_BST3[0]	0	RW	Index 8 Boost Stage 3 bit 0
BST_Indx9		Reg 0x49 Channel	0X95	0x95	Index9 4 Stage EQ Boost.
	7	I9_BST0[1]	1	RW	Index 9 Boost Stage 0 bit 1
	6	I9_BST0[0]	0	RW	Index 9 Boost Stage 0 bit 0
	5	I9_BST1[1]	0	RW	Index 9 Boost Stage 1 bit 1
	4	I9_BST1[0]	1	RW	Index 9 Boost Stage 1 bit 0
	3	I9_BST2[1]	0	RW	Index 9 Boost Stage 2 bit 1
	2	I9_BST2[0]	1	RW	Index 9 Boost Stage 2 bit 0
	1	I9_BST3[1]	0	RW	Index 9 Boost Stage 3 bit 1
	0	I9_BST3[0]	1	RW	Index 9 Boost Stage 3 bit 0
BST_Indx10		Reg 0x4A Channel	0x69		Index10 4 Stage EQ Boost.
	7	I10_BST0[1]	0	RW	Index 10 Boost Stage 0 bit 1
	6	I10_BST0[0]	1	RW	Index 10 Boost Stage 0 bit 0
	5	I10_BST1[1]	1	RW	Index 10 Boost Stage 1 bit 1
	4	I10_BST1[0]	0	RW	Index 10 Boost Stage 1 bit 0
	3	I10_BST2[1]	1	RW	Index 10 Boost Stage 2 bit 1
	2	I10_BST2[0]	0	RW	Index 10 Boost Stage 2 bit 0
	1	I10_BST3[1]	0	RW	Index 10 Boost Stage 3 bit 1
	0	I10_BST3[0]	1	RW	Index 10 Boost Stage 3 bit 0
BST_Indx11		Reg 0x4B Channel	0xD5		Index11 4 Stage EQ Boost.
	7	I11_BST0[1]	1	RW	Index 11 Boost Stage 0 bit 1
	6	I11_BST0[0]	1	RW	Index 11 Boost Stage 0 bit 0
	5	I11_BST1[1]	0	RW	Index 11 Boost Stage 1 bit 1
	4	I11_BST1[0]	1	RW	Index 11 Boost Stage 1 bit 0
	3	I11_BST2[1]	0	RW	Index 11 Boost Stage 2 bit 1
	2	I11_BST2[0]	1	RW	Index 11 Boost Stage 2 bit 0
	1	I11_BST3[1]	0	RW	Index 11 Boost Stage 3 bit 1
	0	I11_BST3[0]	1	RW	Index 11 Boost Stage 3 bit 0
BSTIndx12		Reg 0x4C Channel	0x99		Index12 4 Stage EQ Boost.
	7	I12_BST0[1]	1	RW	Index 12 Boost Stage 0 bit 1
	6	I12_BST0[0]	0	RW	Index 12 Boost Stage 0 bit 0
	5	I12_BST1[1]	0	RW	Index 12 Boost Stage 1 bit 1
	4	I12_BST1[0]	1	RW	Index 12 Boost Stage 1 bit 0
	3	I12_BST2[1]	1	RW	Index 12 Boost Stage 2 bit 1
	2	I12_BST2[0]	0	RW	Index 12 Boost Stage 2 bit 0
	1	I12_BST3[1]	0	RW	Index 12 Boost Stage 3 bit 1
	0	I12_BST3[0]	1	RW	Index 12 Boost Stage 3 bit 0

Table 6. Receiver Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
BST_Idx13		Reg 0x4D Channel	0xA5		Index13 4 Stage EQ Boost.
	7	I13_BST0[1]	1	RW	Index 13 Boost Stage 0 bit 1
	6	I13_BST0[0]	0	RW	Index 13 Boost Stage 0 bit 0
	5	I13_BST1[1]	1	RW	Index 13 Boost Stage 1 bit 1
	4	I13_BST1[0]	0	RW	Index 13 Boost Stage 1 bit 0
	3	I13_BST2[1]	0	RW	Index 13 Boost Stage 2 bit 1
	2	I13_BST2[0]	1	RW	Index 13 Boost Stage 2 bit 0
	1	I13_BST3[1]	0	RW	Index 13 Boost Stage 3 bit 1
	0	I13_BST3[0]	1	RW	Index 13 Boost Stage 3 bit 0
BST_Idx14		Reg 0x4E Channel	0xE6		Index14 4 Stage EQ Boost.
	7	I14_BST0[1]	1	RW	Index 14 Boost Stage 0 bit 1
	6	I14_BST0[0]	1	RW	Index 14 Boost Stage 0 bit 0
	5	I14_BST1[1]	1	RW	Index 14 Boost Stage 1 bit 1
	4	I14_BST1[0]	0	RW	Index 14 Boost Stage 1 bit 0
	3	I14_BST2[1]	0	RW	Index 14 Boost Stage 2 bit 1
	2	I14_BST2[0]	1	RW	Index 14 Boost Stage 2 bit 0
	1	I14_BST3[1]	1	RW	Index 14 Boost Stage 3 bit 1
	0	I14_BST3[0]	0	RW	Index 14 Boost Stage 3 bit 0
BST_Idx15		Reg 0x4F Channel	0xF9		Index15 4 Stage EQ Boost.
	7	I15_BST0[1]	1	RW	Index 15 Boost Stage 0 bit 1
	6	I15_BST0[0]	1	RW	Index 15 Boost Stage 0 bit 0
	5	I15_BST1[1]	1	RW	Index 15 Boost Stage 1 bit 1
	4	I15_BST1[0]	1	RW	Index 15 Boost Stage 1 bit 0
	3	I15_BST2[1]	1	RW	Index 15 Boost Stage 2 bit 1
	2	I15_BST2[0]	0	RW	Index 15 Boost Stage 2 bit 0
	1	I15_BST3[1]	0	RW	Index 15 Boost Stage 3 bit 1
	0	I15_BST3[0]	1	RW	Index 15 Boost Stage 3 bit 0
Active_EQ		Reg 0x52 Channel	0x00		Active CTLE Boost Setting Read Back
	7	eq_bst_to_ana[7]	0	R	Read-back returns CTLE boost settings
	6	eq_bst_to_ana[6]	0	R	
	5	eq_bst_to_ana[5]	0	R	
	4	eq_bst_to_ana[4]	0	R	
	3	eq_bst_to_ana[3]	0	R	
	2	eq_bst_to_ana[2]	0	R	
	1	eq_bst_to_ana[1]	0	R	
	0	eq_bst_to_ana[0]	0	R	
EQ_Control		Reg 0x55 Channel	0x00		EQ Adaptation Control
	7	Reserved	0	R	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	INIT_CDR_SM_4	0	RW	At power-up, this bit needs to be set to 1'b. See initialization set up
	0	Reserved	0	RW	

5.3 CDR Registers

Table 7. CDR Registers

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
Output_Mux_OV		Reg 0x09 Channel	0x00		Output Data Mux Override
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reg_bypass_pfd_ovd	0	RW	1: Enable values from 0x1E[7:5] & 0x1C[7:5] to control output mux 0: Register 0x1C[3:2] determines the output selection
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
CDR_Reset		Reg 0x0A Channel	0x50		CDR State Machine Reset
	7	Reserved	0	RW	
	6	Reserved	1	RW	
	5	Reserved	0	RW	
	4	Reserved	1	RW	
	3	reg_cdr_reset_ov	0	RW	1: Enable 0x0A[2] to control CDR Reset 0: Disable CDR Reset
	2	reg_cdr_reset_sm	0	RW	1: Enable CDR Reset if 0x0A[3] = 1'b 0: Disable CDR Reset if 0x0A[3] = 1'b
	1	Reserved	0	RW	
	0	Reserved	0	RW	
CDR_Status		Reg 0x0C Channel	0x08		CDR Status Control
	7	reg_sh_status_control[3]	0	RW	Determines what is shown in Reg 0x02. See LMH0318 Programming Guide (SNLU183)
	6	reg_sh_status_control[2]	0	RW	
	5	reg_sh_status_control[1]	0	RW	
	4	reg_sh_status_control[0]	0	RW	
	3	Reserved	1	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
EOM_Vrange		Reg 0x11 Channel	0xE0		EOM Vrange Setting and EOM Power Down Control
	7	eom_sel_vrange[1]	11	RW	Sets eye monitor ADC granularity if 0x2C[6] = 0'b 00: 3.125 mV 01: 6.25 mV 10: 9.375 mV 11: 12.5 mV
	6	eom_sel_vrange[0]			
	5	eom_PD	1	RW	0: EOM Operational 1: Power down EOM
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	

Table 7. CDR Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
Full Temperature Range		Reg 0x16 Channel	0x7A		Temperature Range Setting
	7	INIT_CDR_SM_27	0	RW	At power-up, this register needs to be set to 0x25. See initialization set up
	6	INIT_CDR_SM_26	1	RW	
	5	INIT_CDR_SM_25	1	RW	
	4	INIT_CDR_SM_24	1	RW	
	3	INIT_CDR_SM_23	1	RW	
	2	INIT_CDR_SM_22	0	RW	
	1	INIT_CDR_SM_21	1	RW	
	0	INIT_CDR_SM_20	0	RW	
HEO_VEO_OV		Reg 0x23 Channel	0x40		
	7	eom_get_heo_veo_ov	0	RW	1: Enable reg 0x24[1] to acquire HEO/VEO 0: Disable reg 0x24[1] to acquire HEO/VEO
	6	Reserved	1	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
EOM_CNTL		Reg 0x24 Channel	0x00	0x00	Eye Opening Monitor Control Register
	7	fast_eom	0	R	1: Enable Fast EOM mode 0: Disable fast EOM mode
	6	Reserved	0	R	
	5	get_heo_veo_error_no_hits	0	R	1: No zero crossing in the eye diagram observed 0: Zero crossing in the eye diagram detected
	4	get_heo_veo_error_no_opening	0	R	1: Eye diagram is completely closed 0: Open eye diagram detected
	3	Reserved	0	R	
	2	Reserved	0	R	
	1	eom_get_heo_veo	0	RW	1: Acquire HEO & VEO(self-clearing) 0: Normal operation
	0	eom_start	0	R	1: Starts EOM counter(self-clearing) 0: Normal operation
EOM_MSB		Reg 0x25 Channel	0x00		Eye opening monitor hits(MSB)
	7	eom_count[15]	0	RW	MSBs of EOM counter
	6	eom_count[14]	0	RW	
	5	eom_count[13]	0	RW	
	4	eom_count[12]	0	RW	
	3	eom_count[11]	0	RW	
	2	eom_count[10]	0	RW	
	1	eom_count[9]	0	RW	
	0	eom_count[8]	0	RW	

Table 7. CDR Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
EOM_LSB		Reg 0x26 Channel	0x00		Eye opening monitor hits(LSB)
	7	eom_count[7]	0	RW	LSBs of EOM counter
	6	eom_count[6]	0	RW	
	5	eom_count[5]	0	RW	
	4	eom_count[4]	0	RW	
	3	eom_count[3]	0	RW	
	2	eom_count[2]	0	RW	
	1	eom_count[1]	0	RW	
	0	eom_count[0]	0	RW	
HEO		Reg 0x27 Channel	0x00		Horizontal Eye Opening
	7	heo[7]	0	R	HEO value. This is measured in 0-63 phase settings. To get HEO in UI, read HEO, convert hex to dec, then divide by 64.
	6	heo[6]	0	R	
	5	heo[5]	0	R	
	4	heo[4]	0	R	
	3	heo[3]	0	R	
	2	heo[2]	0	R	
	1	heo[1]	0	R	
	0	heo[0]	0	R	
VEO		Reg 0x28 Channel	0x00		Vertical Eye Opening
	7	veo[7]	0	R	This is measured in 0-63 vertical steps. To get VEO in mV, read VEO, convert hex to dec, then multiply by 3.125mV
	6	veo[6]	0	R	
	5	veo[5]	0	R	
	4	veo[4]	0	R	
	3	veo[3]	0	R	
	2	veo[2]	0	R	
	1	veo[1]	0	R	
	0	veo[0]	0	R	
Auto_EOM_Vrange		Reg 0x29 Channel	0x00		EOM Vrange Readback
	7	Reserved	0	RW	Auto Vrange readback of eye monitor granularity 00: 3.125mV 01: 6.25mV 10: 9.375mV 11: 12.5mV
	6	eom_vrange_setting[1]	00	R	
	5	eom_vrange_setting[0]			
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	

Table 7. CDR Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
EOM_Timer_Thr		Reg 0x2A Channel	0x30		EOM Hit Timer
	7	eom_timer_thr[7]	0	RW	EOM timer for how long to check each phase/voltage setting
	6	eom_timer_thr[6]	0	RW	
	5	eom_timer_thr[5]	1	RW	
	4	eom_timer_thr[4]	1	RW	
	3	eom_timer_thr[3]	0	RW	
	2	eom_timer_thr[2]	0	RW	
	1	eom_timer_thr[1]	0	RW	
	0	eom_timer_thr[0]	0	RW	
VEO_Scale		Reg 0x2C Channel	0x32		VEO_Scale
	7	Reserved	0	RW	
	6	veo_scale	0	RW	1: Enable Auto VEO scaling 0: VEO scaling based on Vrange Setting (0x11[7:6])
	5	Reserved	1	RW	
	4	Reserved	1	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	1	RW	
	0	Reserved	0	RW	
HEO VEO Threshold		Reg 0x32 Channel	0x11		HEO/VEO Interrupt Threshold
	7	heo_int_thresh[3]	0	RW	Compares HEO value, 0x27[7:0], vs threshold 0x32[7:4] * 4
	6	heo_int_thresh[2]	0	RW	
	5	heo_int_thresh[1]	0	RW	
	4	heo_int_thresh[0]	1	RW	
	3	veo_int_thresh[3]	0	RW	Compares VEO value, 0x28[7:0], vs threshold 0x32[3:0] * 4
	2	veo_int_thresh[2]	0	RW	
	1	veo_int_thresh[1]	0	RW	
	0	veo_int_thresh[0]	1	RW	

Table 7. CDR Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
CDR State Machine Control		Reg 0x3E Channel	0x80		CDR State Machine Setting
	7	INIT_CDR_SM_3	1	RW	At power-up, this bit needs to be set to 0'b. See initialization set up
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
HEO_VEO_Lock		Reg 0x69 Channel	0x0A		HEO/VEO Interval Monitoring
	7	Reserved	0	RW	While monitoring lock, this sets the interval time. Each interval is 6.5 ms. At default condition, HEO_VEO Lock Monitor occurs once every 65 ms.
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	hv_lckmon_cnt_ms[3]	1	RW	
	2	hv_lckmon_cnt_ms[2]	0	RW	
	1	hv_lckmon_cnt_ms[1]	1	RW	
	0	hv_lckmon_cnt_ms[0]	0	RW	
CDR State Machine Control		Reg 0x6A Channel	0x44		CDR State Machine Control
	7	INIT_CDR_SM_57	0	RW	At power-up, this register should be set to 0x00. See initialization set up
	6	INIT_CDR_SM_56	1	RW	
	5	INIT_CDR_SM_55	0	RW	
	4	INIT_CDR_SM_54	0	RW	
	3	INIT_CDR_SM_53	0	RW	
	2	INIT_CDR_SM_52	1	RW	
	1	INIT_CDR_SM_51	0	RW	
	0	INIT_CDR_SM_50	0	RW	
SMPTE_Rate_Enable		Reg 0xA0 Channel	0x1f		SMPTE_Data_Rate_Lock_Restriction
	7	Reserved	0	RW	1: Enable CDR Lock to 270 Mbps 0: Disable CDR Lock to 270 Mbps
	6	Reserved	0	RW	
	5	Reserved	0	RW	1: Enable CDR Lock to 1.485/1.4835 Gbps 0: Disable CDR Lock to 1.485/1.4835 Gbps
	4	dvb_enable	1	RW	
	3	hd_enable	1	RW	1: Enable CDR Lock to 2.97/2.967 Gbps 0: Disable CDR Lock to 2.97/2.967 Gbps
	2	3G_enable	1	RW	
	1	Reserved	1	RW	Reserved
	0	Reserved	1	RW	Reserved

5.4 Transmitter Registers

Table 8. Transmitter Registers

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
Out0_Mux_Select		Reg 0x1C Channel	0x18		OUT0 Mux Selection
	7	pdf_sel0_data_mux[2]	0	RW	When 0x09[5] = 1'b OUT0 Mux Selection can be controlled as follows: 000: Mute 001: 10 MHz Clock 010: Raw Data 100: Retimed Data Other Settings - Invalid
	6	pdf_sel0_data_mux[1]	0	RW	
	5	pdf_sel0_data_mux[0]	0	RW	
	4	vco_clk_sel	1	RW	When 0x09[5] = 1'b and 0x1E[[7:5] = 101'b OUT1 clock selection can be controlled as follows: 1: OUT1 puts out line rate clock 0: OUT1 puts out 10MHz clock
	3	mr_drv_out_ctrl[1]	1	RW	Controls both OUT0 and OUT1: 00: OUT0: Mute OUT1: Mute 01: OUT0: Locked Reclocked Data / Unlocked Raw Data OUT1: Locked Output Clock / Unlocked Mute 10: OUT0: Locked Reclocked Data / Unlocked RAW OUT1: Locked Reclocked Data / Unlocked Raw 11: OUT0: Forced Raw OUT1: Forced Raw
	2	mr_drv_out_ctrl[0]	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
OUT1_Mux_Select		Reg 0x1E Channel	0xE9		OUT1 Mux Selection
	7	pdf_sel_data_mux[2]	1	RW	When 0x09[5] = 1'b OUT0 Mux Selection can be controlled as follows: 111: Mute 101: 10MHz Clock if reg 0x1c[4]=0 and full rate clock if reg 0x1c[4] = 1 010: Full Rate Clock 001: Retimed Data 000: Raw Data Other Settings - Invalid
	6	pdf_sel_data_mux[1]	1	RW	
	5	pdf_sel_data_mux[0]	1	RW	
	4	Reserved	0	RW	
	3	Reserved	1	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	1	RW	

Table 8. Transmitter Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
OUT1 Invert		Reg 0x1F Channel	0x10		Invert OUT1 Polarity
	7	pdf_sel_inv_out1	0	RW	1: Inverts OUT1 polarity 0: OUT1 Normal polarity
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	1	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
OUT0_VOD		Reg 0x80 Channel	0x54		OUT0 VOD_PD
	7	drv_0_sel_vod[3]	0	RW	Controls OUTDriver 0 VOD Setting 0011: Nominal - 10% 0100: Nominal - 5% 0101: Nominal 800 mV 0110: Nominal + 5% 0111: Nominal + 10% Other Settings - Invalid
	6	drv_0_sel_vod[2]	1	RW	
	5	drv_0_sel_vod[1]	0	RW	
	4	drv_0_sel_vod[0]	1	RW	
	3	Reserved	0	RW	
	2	Reserved	1	RW	
	1	mr_drv_0_ov	0	RW	1: Enable 0x80[0] to override pin/sm control 0: Disable 0x80[0] to override pin/sm control
	0	sm_drv_0_PD	0	RW	1: Power down OUT0 0: OUT1 in normal operating mode
OUT1_VOD		Reg 0x84 Channel	0x04		OUT1 VOD Control
	7	Reserved	0	RW	
	6	drv_1_sel_vod[2]	0	RW	OUTDriver1 VOD Setting 000: 570 mV Differential(Diff) Peak to Peak(PP) 010: 730 mV(Diff PP) 100: 900 mV(Diff PP) 110: 1035 mV(Diff PP)
	5	drv_1_sel_vod[1]	0	RW	
	4	drv_1_sel_vod[0]	0	RW	
	3	Reserved	0	RW	
	2	drv_1_sel_scp	1	RW	1: Enables short circuit protection on OUT1 0: Disable short circuit protection on OUT1
	1	mr_drv_1_ov	0	RW	1: Enable 0x80[0] to override pin/sm control 0: Disable 0x80[0] to override pin/sm control
	0	sm_drv_1_PD	0	RW	1: Power down OUT1 driver 0: OUT1 in normal operating mode
OUT1_DE		Reg 0x85	0x00		OUT1 DE Control
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	

Table 8. Transmitter Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
	3	drv_1_dem_range	0	RW	Controls de-emphasis of 50 Ω Driver 0000: DE Disabled 0001: 0.2 dB 0010: 1.8 dB 0111: 11 dB
	2	drv_1_dem[2]	0	RW	
	1	drv_1_dem[1]	0	RW	
	0	drv_1_dem[0]	0	RW	

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3. *Regulatory Notices:*
 - 3.1 *United States*
 - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/llds/ti_ja/general/eStore/notice_02.page
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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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