Application Note

High-Speed PCB Layout for PCIe Gen 5

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ABSTRACT

This application note helps system designers implement best practices and understand PCB layout options when designing high-speed PCI Express (PCIe) platforms. This document is intended for audiences familiar with PCB manufacturing, layout, and design. A successful Gen5 x16 lane design requires a PCB layout with a mindset for optimization of crosstalk, return loss, and insertion loss.

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1 Introduction

Peripheral Component Interconnect Express (PCIe) was introduced over two decades ago to enable the growing demand for high bandwidth/speed data transfers. Each new generation for PCIe has effectively doubled the rate of transmission. The current generation, PCIe Gen5, transfers data at a rate of 32 GT/s. High speed interfaces such as PCIe introduced many challenges in regards to layout, including but not limited to traces, vias, reference planes, dielectrics, and so on. All of the factors mentioned previously have significant impacts at high data rates; thus, adhere to the following layout practices to overcome PCIe Gen5 layout challenges.

2 PCIe Gen3, Gen4, and Gen5 Loss Budget

PCIe Gen5 and lower rates use differential AC coupled transmission lines. Polarity inversion is allowed since NRZ data is used. There is on-chip termination that activates after the Rx detect process is asserted on both inputs and outputs to facilitate signal integrity. More importantly, PCIe Gen3 through Gen5 uses link training, allowing both TX and RX link equalization.

Before we get started discussing PCB layout guidelines, let's start with PCIe overall design considerations. Table 2-1 outlines the loss budget (dB) for PCIe Gen3 through Gen5, while Table 2-2 outlines the PCIe eye opening requirements for Gen3 through Gen5.

Table 2-1. PCIe Gen3 through Gen5 Loss Budget

Loss Breakdown	Gen3 (dB)	Gen4 (dB)	Gen5 (dB)
CPU Package	3.5	5	9.0
System Board Trace (9-inch trace with high-loss material)	13	14	16
CEM Connector	0.5	0.5	1.5
4" Add-In-Card	6.5	8.5	9.5
Total System Loss	23.5	28	36
Cross Talk Mitigation	Negligible	<2	4-5
Temp/Humidity Loss	-	-	2-3

Table 2-2. PCIe Gen3 through Gen5 Eye Opening

Eye Opening	Gen3	Gen4	Gen5
Extrapolated Eye Height after EQ	25 mV	15 ± 1.5mV	15 ± 1.5mV
Minimum Eye Width after EQ	0.3UI (37.5ps)	0.3UI (18.75 ± 0.55ps)	0.3UI (9.375 ± 0.5ps)

3 Minimum Eye Width

Minimum eye width and eye height is measured post-equalization before the 3-tap DFE blocks. This means at the output of the PCIe redriver, the eye opening at the needs to be equal or greater than the values presented in Table 2-2.

4 Cross Talk Mitigation

PCIe Gen5 cross talk needs to be mitigated, meaning there is a total channel loss that needs to be considered. We must allow at least 4 to 5 dB increased signal strength versus total system loss. This mitigation can be achieved by reducing differential signal loss insertion loss (SDD21) or improving cross talk. This 4 to 5 dB of signal strength improves the signal to noise ratio and thus improves the targeted BER (1E-12). To reduce the effect of cross-talk, maximize pair-to pair spacing, ground stitching, and the optimization of via anti-pads – more details about the listed topics are discussed in later paragraphs. Typically, it is advised to use closely coupled strip line to reduce the effect of cross-talk . However, vias and anti-pads need to be designed carefully. The DS320PR1601 TI EVM is designed using a co-planar GND reference waveguide, which reduces the effects of cross-talk.

5 Humidity and Temperature Insertion Loss

At higher temperature and humidity, insertion loss increases. The amount of loss depends on the operating data rate: At a higher data rate, loss increases. Additionally, this also depends on the board material. For example, Ultra Low Loss material has less loss across data rate versus standard loss. Therefore, some loss due to the electrical characteristics of the board material ought to be considered. Insertion loss is expected to be up to 8% higher at temperature for ultra low-loss materials such as Megtron 6, compared to nominal temperature, compared to higher loss materials such as FR4 where insertion loss is 11% higher at temperature compared to nominal.

6 Critical Signals

A primary concern when designing a system is accommodating and isolating high-speed signals. As high-speed signals are most likely to impact or be impacted by other signals, the signals must be laid out early (preferably first) in the PCB design process to make sure that the outlined routing rules can be followed.

Table 6-1 outlines the high-speed interface signals requiring the most attention when laying out a PCB that incorporates a Texas Instruments PCIe device

Table 6-1. Critical Signals

Signal Name	Description
PCIE_RXP	PCIe differential data pair, RX, positive
PCIE_RXN	PCIe differential data pair, RX, negative
PCIE_TXP	PCIe differential data pair, TX, positive
PCIE_TXN	PCIe differential data pair, TX, negative
REFCLKP/N	100MHz-Reference CLK

7 General High-Speed Signal Routing

High-speed PCB layout requires detailed attention to the signal path. Every element from PCB materials/building block, PCB layout, connectors, passive components, and so on. These elements have to be treated as RF elements capable of affecting signal characteristics.

8 PCB Grain and Fiber Weave Selection

When routing differential signals across common PCB materials, each trace experiences different dielectric constants and corresponding signal velocities due to the differences in static permittivity (ε_r) of the fiberglass weave (ε_r is approximately 6) and epoxy (ε_r is approximately 3) that comprise a PCB. Differences between ε_r and loss tangent (D_f) are caused by holes or openings within the fiber glass laminate. These differences cause resonance or anti-resonance in return loss or the insertion loss of the transmission media at different frequencies across the signal bandwidth.

A signal travels faster when ε_r is lower; therefore, an intra-pair skew can develop if a signal in a differential pair travels over a higher ratio of fiberglass or epoxy than the companion signal does. This intra-pair skew starts appearing on SDD12 and SDD22 at 2GHz and higher. This skew between the differential signals can significantly degrade the differential eye diagram as presented to the receiver, causing significant duty cycle distortion, AC common-mode voltage noise, and EMI issues. The extent of this problem will depend on the data rate, the length of the traces, the trace geometries, the type of fiberglass weave used, and the alignment of the traces to the weave pattern of a PCB. Problems from fiber weave alignment vary from board to board. This variance makes issues difficult to diagnose.

ε_r typically ranges from 2.5 to 4.5 and varies with frequency – decreases as frequency increases. D_f is a measurement of material power dissipation or the degree of signal attenuation and typically ranges from 0.02 to 0.001 for ultra-low loss materials. Smaller values of D_f result in lower signal attenuation, thus a low D_f is desirable for high speed applications such as PCIe.

Figure 8-1 and Figure 8-2 show the two most common methods to minimize the impact of PCB fiber weave in a board design. The goal of each method is to ensure that both signals of the differential pair will share a relatively common across the length of the pair routing.

The entirety of the signaling image plane is rotated 10° to 35° in relation to the underlying PCB fiber weave. The PCB manufacturer can affect this rotation without making changes to the PCB layout database as shown in Figure 8-1.

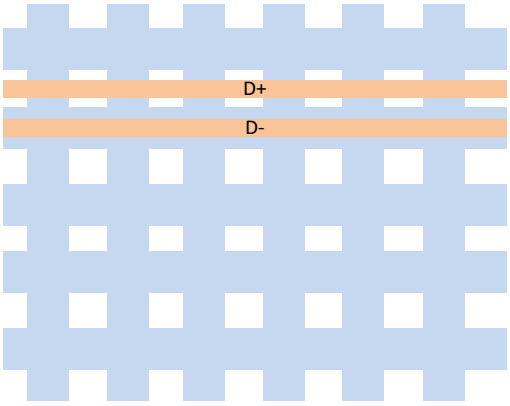

Figure 8-1. Rotation of the PCB Image

The high-speed differential signals are routed in a zig-zag fashion across the PCB as shown in Figure 8-2

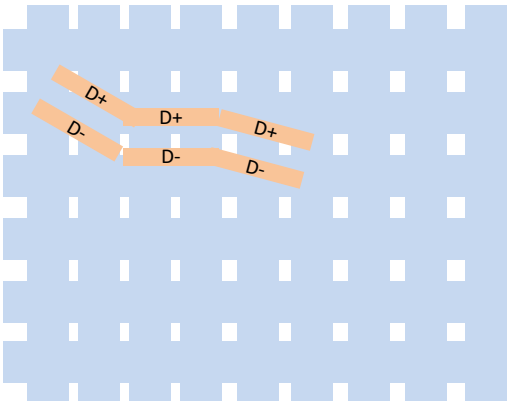

Figure 8-2. Zig-Zag Routing

Because the ratio of fiberglass to epoxy is the primary contributor to the ε_r disparity, choose a PCB style with a tighter weave, less epoxy, and greater ε_r uniformity across longer trace lengths. Before sending the design out for fabrication, specify a PCB style that can best accommodate high-speed signals.

9 PCB Material Loss Budget

The PCB material plays a large role in achieving optimum signal integrity. Table 9-1 shows insertion loss – SDD21 – of 1 inch of different board materials using different dielectric constants and loss tangents. Loss tangent (D_f) or Dissipation Factor is a measure of signal attenuation as a signal propagates through a transmission line. This attenuation is due to the electromagnetic wave absorption in the dielectric material and is referred to as dielectric loss. As frequency increases, the dielectric loss also increases proportionally.

Common material choices for high-speed signal layers are Panasonic Megtron 6, Roger, and GETEK. TI has successfully utilized Panasonic Megtron 6 for a variety of high-speed board designs.

Table 9-1. 1" Trace Loss Over Frequency for Various PCB Materials

Material Name	ε_r (Dielectric Constant)	D_f (Loss Tangent)	1" SDD21 at 8GHz(dB)	1" SDD21 at 16GHz(dB)
Megtron 6	3.4	0.002	0.189	0.336
Roger	3.48	0.0037	0.251	0.411
GETEK	4.1	0.011	0.548	1.017
Nelco 4000-6	4.0	0.012	0.578	1.078
FR4	4.4	0.014	0.686	1.289
Tetra Functional FR4	4.1	0.022	0.961	1.844

Total insertion loss is calculated as follows:

$$\frac{31.6}{Diff\ Impedance \times (W+T)} \times \left(\sqrt{f} + 2.32\sqrt{\varepsilon_r} \times D_f \times f\right) \quad (1)$$

Z_o is calculated as follows:

$$Z_o = \left(\frac{87}{\sqrt{\varepsilon_r + 1.41}}\right) \times LN\left(\frac{5.98 \times H}{0.8 \times W + T}\right) \quad (2)$$

Note: Z_o is designed to equal 85 Ω differential impedance, given this is the requirement for PCIe add-in-card applications.

- f = frequency (GHz)
- ε_r = Dielectric Constant of material
- D_f = Loss tangent of material
- W = Trace Width (mils)
- T = Trace thickness (mils)
- D = Trace edge-to-edge spacing (mils)
- H = Distance to nearest reference plane (mils)

PCB loss is a fraction of the total channel loss; additional loss due to the device package, vias, connectors, and so on and also have to be considered. When there are multiple vias, reference plane changes, and connectors, the channel frequency response becomes complex. Each time the signal travels through a via, connector, or hits a package with similar parasitic, these affect signal reflections and loss differently. A complex multi-tap DFE must be utilized to track these changes and equalize the signal correctly. To summarize, it is best to minimize the number of vias, connectors, and optimize landing pads of the ASIC.

For high speed PCB layout design, low loss material such as Megtron 6 is used on just the top and bottom layers – where high-speed signals are routed. Please note, other than cost, using low loss materials typically causes a longer PCB fabrication time. Additionally, it can take a longer amount time to acquire lower loss PCB materials since these might not be widely used.

10 High-Speed Signal Trace Impedance

As with all high-speed signals, keep total trace length for signal pairs to a minimum. The PCIe specification requires 70 to 100 Ω differential impedance. To interoperate with different root complexes and end points, Add-In-Cards require 85 Ω differential impedance. This requirement does not apply to vias, AC coupling capacitor pads, connectors, or cables. However, care needs to be taken to minimize impedance discontinuity.

Unlike high-speed differential signals for different PCIe lanes, the differential 100 MHz reference clock target impedance is 100 Ω. Additionally, the maximum allowable Random Jitter RMS is 200 fs. This is crucial in meeting the PCIe Gen5 link EQ validation test requirements.

11 High-Speed Signal Trace Length Matching

Trace length matching between different lanes or pairs is not required. An embedded clock within each differential pair allows for different differential trace length. However, there is a limit to prevent ASIC buffer over-flow. Typically, there can be up to 1 inch of difference, but this depends on the data rate and PCB board material.

Intra-pair trace – the trace length of positive versus negative lead of the signal – has to be kept within 5 mils. This is done to minimize common mode noise. This becomes even more crucial to consider when vias are present in the signal path of a differential pair. Match the etch lengths of the relevant differential pair traces of each interface. The etch length of the differential pair groups do not need to match (that is, the length of the transmit pair does not need to match the length of the receive pair).

12 Differential Trace Routing Guidelines

When matching the intra-pair length of the high-speed signals, add serpentine routing to match the lengths as close to the mismatched ends as possible. For more details, see Figure 12-1.

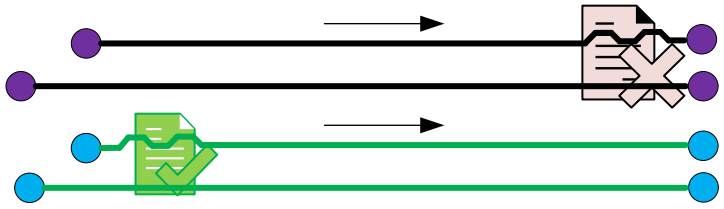

Figure 12-1. Length Matching

13 Differential-Inter-Pair Matching

The recommendation is to keep inter-pair length less than 6 inches. The PCIe root complex and end point provide enough buffering to handle this difference.

14 Intra-pair Length Matching

Positive and negative leads of the differential signal – L1/L2 length – needs to be within 5 mils. Note, if there is a need to compensate for intra-pair mismatch, this needs to be done right at the beginning of the differential trace segment where this occurs. If there is via involved, this needs to be done at the beginning of the differential trace segment. Otherwise, added common-mode noise can cause cross coupling and unneeded interference. For more details, see Figure 14-1.

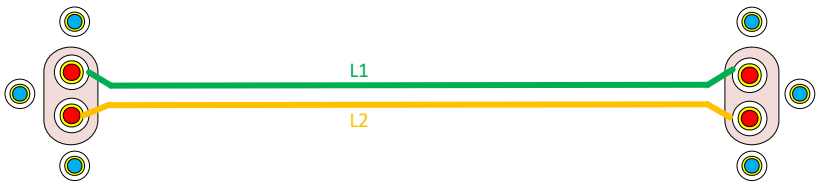

Figure 14-1. Intra-Pair Length Matching

15 Trace Bends

Bending traces need to be avoided mainly because trace bends can change trace width, create impedance mismatch, and create interference, for example. However, when a trace must be bent, use the rules outlined in the following sections.

16 Minimum Differential Trace-To-Trace Distance

The minimum differential trace-to-trace distance must be four times reference plane height (RPH). The PCIe Gen4 requirement is 4xRPH. This distance can prevent impedance change or common mode noise injection.

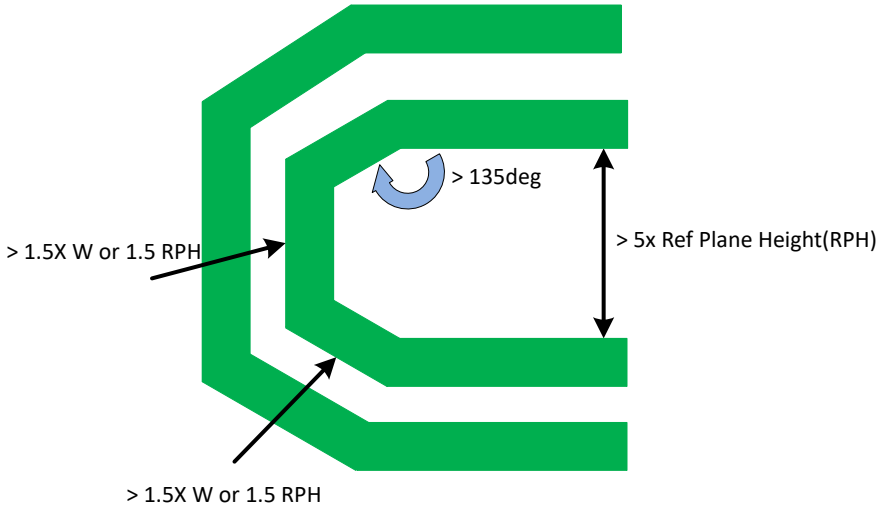

Figure 16-1. Shortest Trace Length Example

17 Serpentine Guidelines

Serpentine routing needs to be avoided when possible. However, if serpentine routing is needed, keep the following in mind:

- The difference in trace lengths for a differential pair changes geometry from closely coupled to loosely coupled for a length or 3xW or 3xRPH. As trace width increases, impedance drops. To compensate for the drop in impedance, increase trace width. This new trace width depends on the board geometry or board stack-up. Alternatively, if the board stack-up is known, the trace width can be calculated.
- The length of serpentine must be at least 3xW or 3xRPH – whichever is larger.

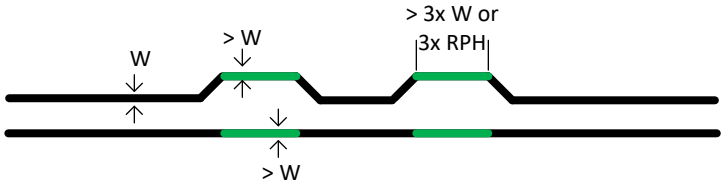

Figure 17-1. Serpentine Guidelines

18 High-Speed Differential Signal Quick Rules

- Do not place probe or test points on any high-speed differential signal.
- Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching power regulators, mounting holes, magnetic devices, edge of the board, or ICs that use or duplicate clock signals.
- After BGA breakout, keep high-speed differential signals clear of the PCIe device because high current transients produced during internal state transitions can be difficult to filter out.
- When possible, route high-speed differential pair signals on the top or bottom layer of the PCB with an adjacent GND layer.
- Make sure the high-speed differential signals are routed ≥ 5XW or 5XRPH – whichever is bigger - mils from the edge of the reference plane.

- Make sure the high-speed differential signals are routed at least 4XRPH away from voids in the reference plane. This rule does not apply where SMD pads on high-speed differential signals are voided.
- Maintain constant trace width after the PCIe device BGA escape to avoid impedance mismatches in the transmission lines.
- To improve cross talk, follow ground-signal-ground signal routing and route all high-speed differential pairs together symmetrically and parallel to each other. Deviating from this requirement occurs naturally during package escape and when routing to connector pins. Trace deviations must be as short as possible – otherwise this can require trace width compensation. HFSS simulation can optimize trace width.
- Crosstalk Between the Differential Signal Pairs: In devices that include multiple high-speed interfaces, avoiding crosstalk between various interfaces is important. To avoid crosstalk, make sure that each differential pair is not routed within 4-5 X RPH mils of another differential pair after package escape and before connector termination.

19 High-Speed Differential Pair Reference Plane

The entirety of any high-speed signal trace must maintain the same GND reference from origination to termination. If unable to maintain the same GND reference, via-stitch both GND planes together to make sure of continuous grounding and uniform impedance. Place stitching vias symmetrically within 50 mils (center-to-center, closer is better) of the signal transition vias.

For differential signals, the transmission line is formed by two traces and a reference plane. Good signal integrity depends on differential signals with controlled impedance. Controlled impedance is achieved by implementing optimized trace geometries and taking into account the dielectric constant and Loss Tangent of the board material you're working with. While the dielectric constant varies from board to board, the dielectric is constant within one board. Therefore, the impedance of a differential line is mostly dependent on the trace geometries and tolerances allowed at the PCB fab house. Impedance variance occurs based on the presence or absence of glass in a local portion of the PCB as noted earlier, but this poses issues at high speed (>3GHz Nyquist).

High-speed signals must be routed over a solid reference plane and not across a plane split or a void in the reference plane unless absolutely necessary. TI does not recommend high-speed signal references to power planes.

Routing across a plane split or a void in the reference plane forces return high-frequency current to flow around the split or void. This can result in the following conditions:

- Excess radiated emissions from an unbalanced current flow
- Delays in signal propagation due to increased series inductance
- Interference with adjacent signals
- Degraded signal integrity (that is, more jitter and reduced signal amplitude)

For examples of incorrect and correct plane void routing, see Figure 19-1 and Figure 19-2 for incorrect and correct trace routing, respectively.

Note, when a trace goes around the void, we need to make sure we have at least 4 times reference plane height to maintain target differential impedance.

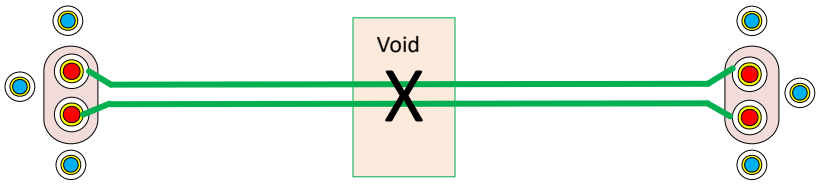

Figure 19-1. Incorrect Plane Void Routing

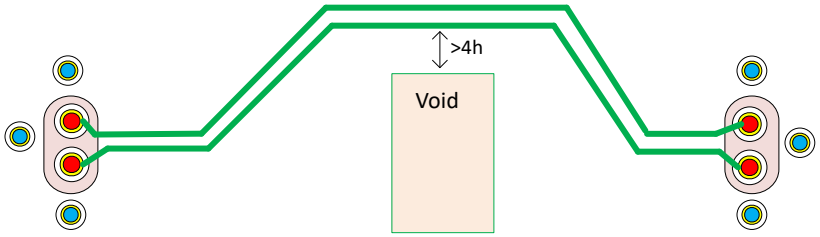

Figure 19-2. Correct Plane Voiding

If routing over a plane-split is completely unavoidable, place stitching capacitors across the split to provide a return path for the high-frequency current. Stitching capacitors minimize the current loop area and any impedance discontinuity created by crossing the split. The capacitors must be 1 µF or lower and placed as close as possible to the plane crossing. For examples of correct stitch capacitor placement, see Figure 19-3.

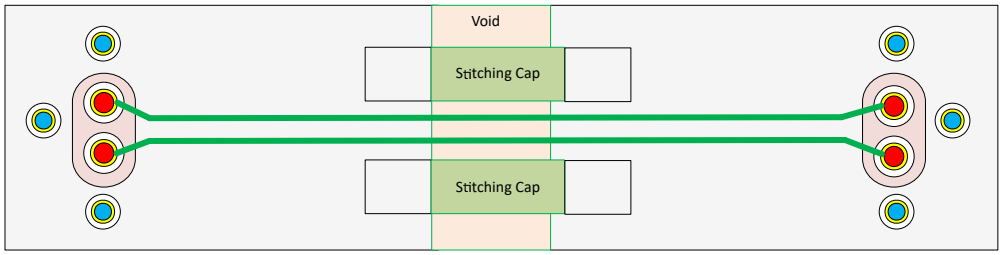

Figure 19-3. Stitching Capacitor over Plane Split

When planning a PCB stack-up, make sure that planes that do not reference each other are not overlapped because this produces unwanted capacitance between the overlapping areas. To see an example of how this capacitance can pass RF emissions from one plane to the other, see Figure 19-4.

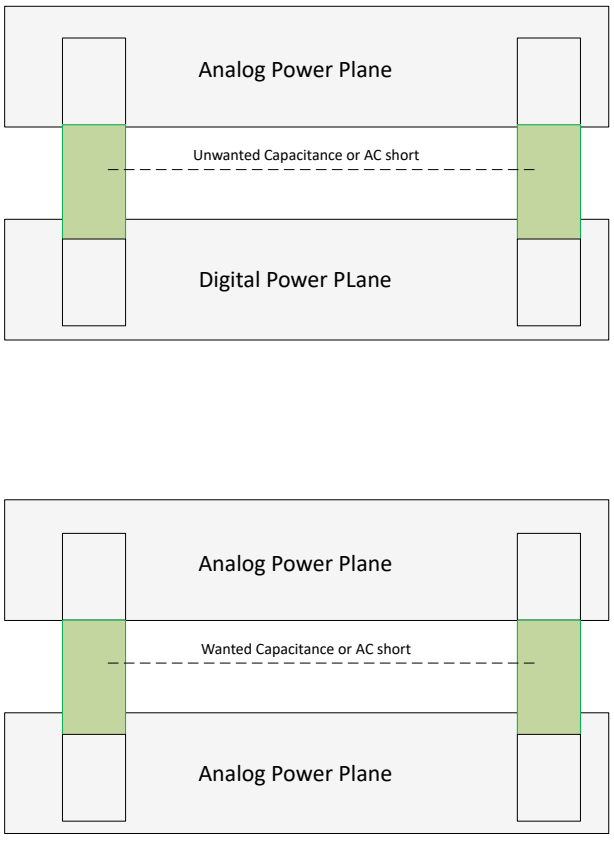

Figure 19-4. Passed Capacitance Examples

20 Via Staggering

When multiple vias are required, proper placement of the vias becomes important for current return path. Vias need to be *staggered* and not placed in a vertically- or horizontally- aligned fashion. The issue with aligned vias is that the current return path becomes blocked. The common analogy used as explanation is the river and logs story. If you have multiple logs aligned, suddenly the flow of water becomes impaired given the water will hit all logs at once. The same idea applies here, multiple aligned vias will impede the current return path.

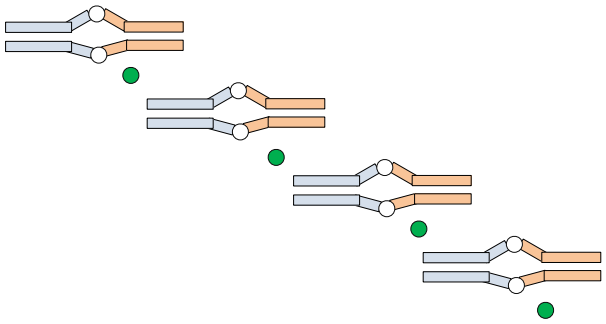

Figure 20-1. Staggered Vias (Recommended)

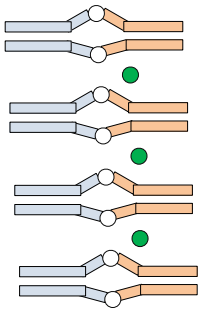

Figure 20-2. Non-Staggered Vias (Not Recommended)

21 Via Stubs

Proper care must be taken when considering high-speed signal trace and via placement on a PCB. TI recommends high-speed traces be placed on the top or bottom layer **only**. If vias are required, consider back drilling otherwise stub length can result in a reduction of the signal bandwidth.

22 Via Pads

When vias must be used, vias in pad are recommended versus vias in extended pads. Placing vias in an extended pad creates unwanted inductance which affects impedance. Via pads placed on unrouted layers must be removed otherwise via capacitance is reduced, which results in an impedance drop.

Figure 22-1. Via in Pad (Recommended)

Figure 22-2. Via in Extended Pad (Not Recommended)

23 Via Discontinuity Mitigation

A via presents a short section of change in geometry to a trace and can appear as a capacitive and or an inductive discontinuity. These discontinuities result in reflections and some degradation of a signal as it travels through the via. Reducing the overall via stub length to minimize the negative impacts of vias (and associated via stubs).

Because longer via stubs resonate at lower frequencies and increase insertion loss, keep via stubs as short as possible. In most cases, the stub portion of the via presents significantly more signal degradation than the signal portion of the via. Guidelines for vias are presented as follows:

1. PCIe Gen5 20/80% rise/fall time is 12 ps. To preserve this type of rise and fall time, approximately 29 GHz bandwidth (0.35/0.12(ns) rule) is required. At this bandwidth and using Megtron 6 (ε_r approximately 3.4), the resulting quarter wavelength is approximately 54 mils. This result means the stub has to be less than this length if back drilling is not implemented.
   a. This is the same reason why for a typical FR4 (ε_r approximately 4.2) PCB, the maximum stub length is approximately 51 mils.
2. For vias, follow the 10/20/40 drill/pad/anti-pad rule. See Figure 23-1
3. It is best to optimize anti-pad size by simulation – this is highly dependent on the board stack-up.
4. GND stitches around the anti-pad must be used – as many as possible to improve the current return path given the reference layer is changing. See Figure 23-1.
5. Closely coupled vias need to be used to optimize target impedance.
6. A short stub exhibits less or better reflection, but it can create more cross talk. Also, a long stub shows worse reflection but lower cross talk. During PCB simulation, cross talk versus reflection needs to be mitigated.
7. Consider GND flooding with very short GND stitches. This process prevents supply coupling capacitor via on pad.
8. If possible, use via-in-pad versus a traditional via to reduce the overall inductance of the pad. See Figure 22-1 for an example.
9. If using vias is necessary on a high-speed differential signal trace, make sure that the via count on each member of the differential pair is equal and that the vias are as equally spaced as possible. TI recommends placing vias as close as possible to the PCIe device.

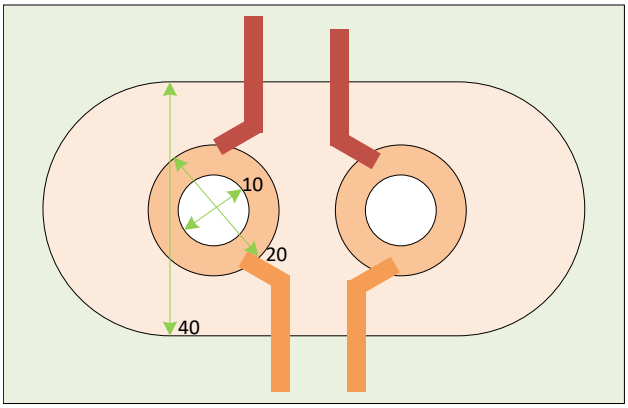

Figure 23-1. Pad Layout Example

24 Back-Drill Stubs

Back-drilling is a PCB manufacturing process in which the undesired conductive plating in the stub section of a via is removed. To back-drill, use a drill bit slightly larger in diameter than the drill bit used to create the original via hole. When via transitions result in stubs longer than 15 mils, back-drill the resulting stubs to reduce insertion losses and to make sure that they do not resonate.

25 AC Coupling Capacitors Placement

To prevent ground bounce and isolate common-mode voltage, PCIe TX must use AC coupling capacitors. The AC coupling capacitor value can range from 75 nF to 220 nF. Given 220 nF provides more DC content, this value

is typically used. Placement of the AC coupling capacitor causes an impedance change and thus can cause jitter if placed improperly.

26 AC Coupling Capacitor Physical Placement

If there is a chip to chip connection, the capacitor needs to be placed as close to the RX as possible. If there is a chip to a connector connection – CEM or PCIe edge finger – it is advised to place the capacitor as close to the edge finger or connector as possible.

It is also important to examine the effects of a void under the AC coupling capacitor. For example, assume the smallest AC coupling capacitor is used (0201). The width of this pad is 12 mils. Given different board stack-ups, the trace width of a differential 85 Ω trace could vary between 5-7 mils. The 0201-capacitor pad is almost twice the trace width; therefore, there is an impedance drop due to this pad difference.

Secondly, the pad or height of the capacitor pad has some fringe effects as well. Given these insights, it is best to use the smallest capacitor size – as close to the trace width as possible. It is possible to smoothly transition from the trace to the capacitor pad; however, 3D HFSS simulation would provide the optimum geometry.

Table 26-1. Capacitor Code and Dimensions

Code		Length(l)		Width(w)		Height(h)	
Imperial	Metric	Inch	mm	Inch	mm	Inch	mm
0201	0603	0.024	0.6	0.012	0.3	0.01	0.25
0402	1005	0.04	1.0	0.02	0.5	0.014	0.35
0603	1608	0.06	1.55	0.03	0.85	0.018	0.45

To minimize the discontinuities associated with the placement of SMD components on the differential signal traces, TI recommends voiding the SMD mounting pads of the reference plane by 100%. The void around the pad of the AC coupling capacitor should be two layers deep. Figure 26-1 is an example of a reference plane voiding of surface mount devices. As noted, the void is actually larger than the AC coupling capacitor pad. This is to compensate for the fringe effect of the AC coupling capacitor height and or body.

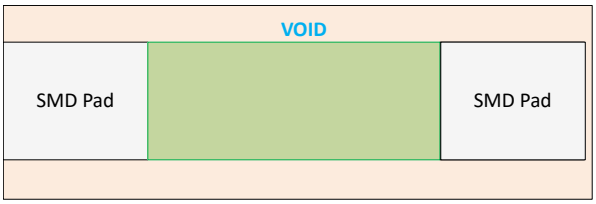

Figure 26-1. Reference Plane Void Example

27 Auxiliary Signal AC Match Termination

Unterminated pins create resonance and propagate cross talk. These resonances can couple to the high-speed lanes. Care needs be taken to AC terminate these signals. All auxiliary or unused signals must be terminated though a nominal 42.9 Ω Resistor in series with a 1.0 pF ± 20% Capacitor. This provides AC short preventing propagation of the resonance.

Table 27-1. List of Auxiliary PCIe Signals

Pin	Signal
X1 Add-In-Card	
B12	CLKREQ#
B17	PRSNT#
X4 Add-In-Card	
A19	MFG
A32	RSVD
B30	PWRBRK#
B31	PRSNT2#
X8 Add-In-Card	
A33	RSVD
B49	PRSNT2#
X16 Add-In-Card	
A50	RSVD
B81	PRSNT2#
B82	RSVD

Notes:

1. Each higher bifurcation requires previous settings. For example, X16 AIC, requires X8, X4, and X2 settings.
2. Logic to drive auxiliary signals can drive 1.0 pF and 42.9 Ω passive termination, refer to Figure 27-1. The combination of these R&C can produce close to 50 Ω termination at the 32 Gbps Nyquist frequency.
3. The trace impedance to drive the logic needs to be 50-Ω single ended.

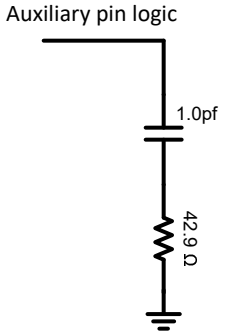

Figure 27-1. Auxiliary Pin Logic

28 Suggested PCB Stack-ups

TI recommends a PCB of at least six layers. Table 28-1 provides example PCB stack-ups.

Table 28-1. PCB Stack-up Examples

DS320PR1601EVM	Alternate 8-LAYER	Alternate 10-LAYER
High speed signal	Signal	Signal
Ground	Ground	Ground
Low speed signal	Signal	Signal
Power	Power	Power/Ground
Power	Power	Signal
Low speed signal	Signal	Signal
Ground	Ground	Power/Ground
High speed signal	Signal	Signal
		Ground
		Signal

Notes:

1. Route directly adjacent signal layers at a 90° offset to each other

The plane can be split depending on specific board considerations. Make sure that traces on adjacent planes do not cross splits.

29 Summary

At high data rates, components or elements within the signal path must be treated as RF elements. Parasitic due to these elements can introduce impedance mismatch, return loss degradation, common mode noise, cross talk, plus other interference sources. Additionally, temperature and humidity side effects must be considered. Using 3D HFSS PCB simulations and close examination of previous design can facilitate and provide a more deterministic approach to a high-speed PCB design.

30 References

1. Texas Instruments, DS320PR1601 32 Gbps 16 Lane PCIe 5.0, CXL 2.0 Linear Redriver, data sheet.

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