User's Guide
SNLA014A–September 1999–Revised June 2018

How to Map RGB Signals to LVDS/OpenLDI(OLDI) Displays

The purpose of this application note is to provide the data mapping to ensure interoperability between the LVDS (OpenLDI/OLDI) display interface and 18-bit or 24-bit LVDS SerDes (Serializer/Deserializer, or transmitter/receiver). These devices are also known as Channel-Link and FPD-Link devices.

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1 Introduction

The data mapping this document highlights is the JEIDA format (also known as Format 1), where the most significant bits (MSB) for an 18-bit application are mapped exactly the same as the most significant bits in the 24-bit application from the VGA controllers. Only 3 LVDS serialized data lines are required for an 18-bit SerDes application, while a 24-bit application uses 4 LVDS data lines. The additional least significant bits (LSB) in the 24-bit application are mapped to the 4th LVDS data line. This mapping format is shown in Figure 1.

However, the VESA format (also known as Format 2, where the MSB are mapped to the 4th LVDS data line) and any other format can also be used. This just requires re-mapping the bits to the correct pins, as shown in Figure 2.

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The tables in the following pages show the connections needed when using LVDS SerDes chipsets for flat panel display applications. Starting from the left, the outputs of the VGA are noted from LSB (less significant bit) to MSB (most significant bit). VGA controllers typically name the LSB as R0, B0, and G0. The MSB remains the same from the VGA controller pin definition, but 24-bit and 18-bit colors are named differently. This confuses the connections needed, so careful review of the following tables is recommended to ensure correct color bit mapping.

Although the JEIDA format is utilized for the mapping pinout in the tables in this document, the SerDes are not limited to this format. The most important thing is to ensure that whatever mapping is used is compatible with what the display expects.

In short, follow the below steps to correctly map to a display:

1. Identify the input application (e.g. single pixel or dual pixel)
2. Identify the RGB mapping format on the display datasheet (e.g. the image on the left of Figure 1)
3. Identify the pin number mapping on the SerDes datasheet (e.g. the image on the right of Figure 1)
4. Map the RGB signals to the appropriate pins

2 How to Read the Tables

The tables are read from left to right. From the left, the R0, G0 and B0 bits are the least significant bits (LSB) as defined by the VGA controllers. These signals should be connected to the input data pins of the transmitters (i.e., color bit R0 in an 18-bit application must be connected to Txin0 or R10, depending on the transmitter being used). The output signals of the receiver are mirror images of the input signals to the transmitter. The DS90C387/DS90CF388 are capable of supporting single pixel, dual pixel, or single-in/dual-out pixel modes. Determine the mode to be used, and then review the corresponding table. Specific part numbers like the DS90C387 and DS90C385 are used as examples in this document, but the procedure is the same for every LVDS SerDes device. Consult the mapping diagrams (e.g. Figure 1) on the individual datasheets to map the pins to the correct bits.

3 Single Pixel per Clock Input Application

Table 1. Single Pixel per Clock Input Application

VGA — TFT Data Signal		Transmitter Input Data Pin			Receiver Output Data Pin			TFT Panel Data Signal	
24-bit	18-bit	24-bit Tx (C385)	18-bit Tx (C365)	48-bit Tx (C387)	24-bit Rx (CF384A)	18-bit Rx (CF364A)	48-bit Rx (CF388)	18-bit	24-bit
R0 (LSB)		Txin27		R16	Rxout27		R16		R0
R1		Txin5		R17	Rxout5		R17		R1
R2	R0	Txin0	Txin0	R10	Rxout0	Rxout0	R10	R0	R2
R3	R1	Txin1	Txin1	R11	Rxout1	Rxout1	R11	R1	R3
R4	R2	Txin2	Txin2	R12	Rxout2	Rxout2	R12	R2	R4
R5	R3	Txin3	Txin3	R13	Rxout3	Rxout3	R13	R3	R5
R6	R4	Txin4	Txin4	R14	Rxout4	Rxout4	R14	R4	R6
R7 (MSB)	R5	Txin6	Txin5	R15	Rxout6	Rxout5	R15	R5	R7
G0 (LSB)		Txin10		G16	Rxout10		G16		G0
G1		Txin11		G17	Rxout11		G17		G1
G2	G0	Txin7	Txin6	G10	Rxout7	Rxout6	G10	G0	G2
G3	G1	Txin8	Txin7	G11	Rxout8	Rxout7	G11	G1	G3
G4	G2	Txin9	Txin8	G12	Rxout9	Rxout8	G12	G2	G4
G5	G3	Txin12	Txin9	G13	Rxout12	Rxout9	G13	G3	G5
G6	G4	Txin13	Txin10	G14	Rxout13	Rxout10	G14	G4	G6
G7 (MSB)	G5	Txin14	Txin11	G15	Rxout14	Rxout11	G15	G5	G7
B0 (LSB)		Txin16		B16	Rxout16		B16		B0
B1		Txin17		B17	Rxout17		B17		B1

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Table 1. Single Pixel per Clock Input Application (continued)

VGA — TFT Data Signal		Transmitter Input Data Pin			Receiver Output Data Pin			TFT Panel Data Signal	
24-bit	18-bit	24-bit Tx (C385)	18-bit Tx (C365)	48-bit Tx (C387)	24-bit Rx (CF384A)	18-bit Rx (CF364A)	48-bit Rx (CF388)	18-bit	24-bit
B2	B0	Txin15	Txin12	B10	Rxout15	Rxout12	B10	B0	B2
B3	B1	Txin18	Txin13	B11	Rxout18	Rxout13	B11	B1	B3
B4	B2	Txin19	Txin14	B12	Rxout19	Rxout14	B12	B2	B4
B5	B3	Txin20	Txin15	B13	Rxout20	Rxout15	B13	B3	B5
B6	B4	Txin21	Txin16	B14	Rxout21	Rxout16	B14	B4	B6
B7 (MSB)	B5	Txin22	Txin17	B15	Rxout22	Rxout17	B15	B5	B7

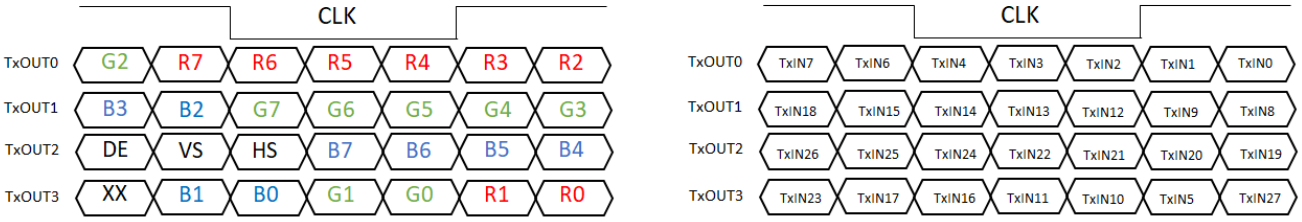

Figure 1. JEIDA/Format 1 Mapping for 24-bit, Single Pixel per Clock Input Applications

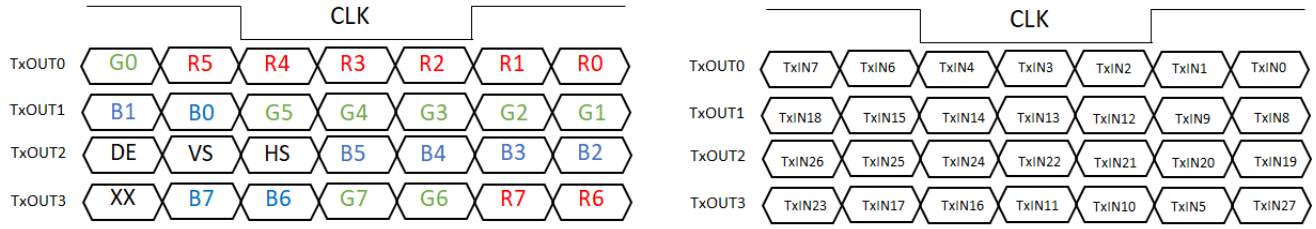

Figure 2. VESA/Format 2 Mapping for 24-bit, Single Pixel per Clock Input Applications

Figure 1 and Figure 2 illustrate JEIDA and VESA mapping and the corresponding pinout for 24-bit SerDes devices like the DS90C385 transmitter. “XX” is an extra general-purpose bit. You can choose to tie this input low if it will be unused, or you can send additional control information if necessary on this input.

The JEIDA format is very convenient for switching from 24-bits to 18-bits with 24-bit SerDes. When 24-bit SerDes is used in 18-bit applications, the LSB are dropped off. With the JEIDA format, the 4th LVDS data line (where RGB24[0:1] are) is ignored, and RGB18[0:5] maps to RGB24[2:7] without any user intervention. For example, what was previously R2 now becomes R0, and what was previously R7 now becomes R5. This can be seen in Figure 3 below.

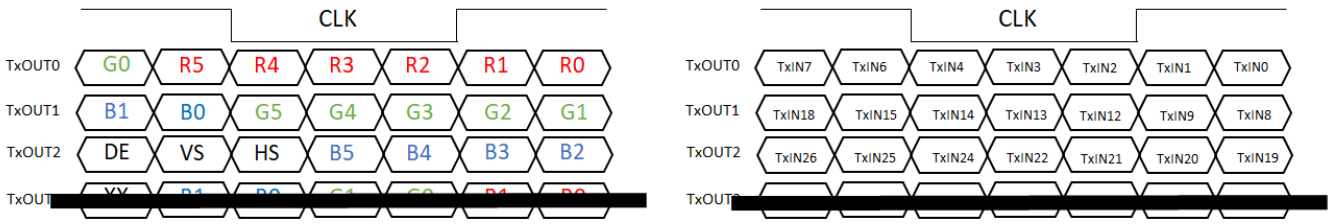

Figure 3. JEIDA/Format 1 Mapping for 24-bit Transmitters in 18-bit Applications

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4 Dual Pixel per Clock Input Application

Table 2. Dual Pixel per Clock Input Application

VGA — TFT Data Signal		Transmitter Input Data Pin			Receiver Output Data Pin			TFT Panel Data Signal	
48-bit	36-bit	24-bit 2Tx (C385)	18-bit 2Tx (C365)	48-bit 1Tx (C387)	24-bit 2Rx (CF384A)	18-bit 2Rx (CF364A)	48-bit 1Rx (CF388)	36-bit	48-bit
OR0 (LSB)		Txin27		R16	Rxout27		R16		OR0
OR1		Txin5		R17	Rxout5		R17		OR1
OR2	OR0	Txin0	Txin0	R10	Rxout0	Rxout0	R10	OR0	OR2
OR3	OR1	Txin1	Txin1	R11	Rxout1	Rxout1	R11	OR1	OR3
OR4	OR2	Txin2	Txin2	R12	Rxout2	Rxout2	R12	OR2	OR4
OR5	OR3	Txin3	Txin3	R13	Rxout3	Rxout3	R13	OR3	OR5
OR6	OR4	Txin4	Txin4	R14	Rxout4	Rxout4	R14	OR4	OR6
OR7 (MSB)	OR5	Txin6	Txin5	R15	Rxout6	Rxout5	R15	OR5	OR7
OG0 (LSB)		Txin10		G16	Rxout10		G16		OG0
OG1		Txin11		G17	Rxout11		G17		OG1
OG2	OG0	Txin7	Txin6	G10	Rxout7	Rxout6	G10	OG0	OG2
OG3	OG1	Txin8	Txin7	G11	Rxout8	Rxout7	G11	OG1	OG3
OG4	OG2	Txin9	Txin8	G12	Rxout9	Rxout8	G12	OG2	OG4
OG5	OG3	Txin12	Txin9	G13	Rxout12	Rxout9	G13	OG3	OG5
OG6	OG4	Txin13	Txin10	G14	Rxout13	Rxout10	G14	OG4	OG6
OG7 (MSB)	OG5	Txin14	Txin11	G15	Rxout14	Rxout11	G15	OG5	OG7
OB0 (LSB)		Txin16		B16	Rxout16		B16		OB0
OB1		Txin17		B17	Rxout17		B17		OB1
OB2	OB0	Txin15	Txin12	B10	Rxout15	Rxout12	B10	OB0	OB2
OB3	OB1	Txin18	Txin13	B11	Rxout18	Rxout13	B11	OB1	OB3
OB4	OB2	Txin19	Txin14	B12	Rxout19	Rxout14	B12	OB2	OB4
OB5	OB3	Txin20	Txin15	B13	Rxout20	Rxout15	B13	OB3	OB5
OB6	OB4	Txin21	Txin16	B14	Rxout21	Rxout16	B14	OB4	OB6
OB7 (MSB)	OB5	Txin22	Txin17	B15	Rxout22	Rxout17	B15	OB5	OB7
ER0 (LSB)		Txin27		R26	Rxout27		R26		ER0
ER1		Txin5		R27	Rxout5		R27		ER1
ER2	ER0	Txin0	Txin0	R20	Rxout0	Rxout0	R20	ER0	ER2
ER3	ER1	Txin1	Txin1	R21	Rxout1	Rxout1	R21	ER1	ER3
ER4	ER2	Txin2	Txin2	R22	Rxout2	Rxout2	R22	ER2	ER4
ER5	ER3	Txin3	Txin3	R23	Rxout3	Rxout3	R23	ER3	ER5
ER6	ER4	Txin4	Txin4	R24	Rxout4	Rxout4	R24	ER4	ER6
ER7 (MSB)	ER5	Txin6	Txin5	R25	Rxout6	Rxout5	R25	ER5	ER7
EG0 (LSB)		Txin10		G26	Rxout10		G26		EG0
EG1		Txin11		G27	Rxout11		G27		EG1
EG2	EG0	Txin7	Txin6	G20	Rxout7	Rxout6	G20	EG0	EG2
EG3	EG1	Txin8	Txin7	G21	Rxout8	Rxout7	G21	EG1	EG3
EG4	EG2	Txin9	Txin8	G22	Rxout9	Rxout8	G22	EG2	EG4

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Table 2. Dual Pixel per Clock Input Application (continued)

VGA — TFT Data Signal		Transmitter Input Data Pin			Receiver Output Data Pin			TFT Panel Data Signal	
48-bit	36-bit	24-bit 2Tx (C385)	18-bit 2Tx (C365)	48-bit 1Tx (C387)	24-bit 2Rx (CF384A)	18-bit 2Rx (CF364A)	48-bit 1Rx (CF388)	36-bit	48-bit
EG5	EG3	Txin12	Txin9	G23	Rxout12	Rxout9	G23	EG3	EG5
EG6	EG4	Txin13	Txin10	G24	Rxout13	Rxout10	G24	EG4	EG6
EG7 (MSB)	EG5	Txin14	Txin11	G25	Rxout14	Rxout11	G25	EG5	EG7
EB0 (LSB)		Txin16		B26	Rxout16		B26		EB0
EB1		Txin17		B27	Rxout17		B27		EB1
EB2	EB0	Txin15	Txin12	B20	Rxout15	Rxout12	B20	EB0	EB2
EB3	EB1	Txin18	Txin13	B21	Rxout18	Rxout13	B21	EB1	EB3
EB4	EB2	Txin19	Txin14	B22	Rxout19	Rxout14	B22	EB2	EB4
EB5	EB3	Txin20	Txin15	B23	Rxout20	Rxout15	B23	EB3	EB5
EB6	EB4	Txin21	Txin16	B24	Rxout21	Rxout16	B24	EB4	EB6
EB7 (MSB)	EB5	Txin22	Txin17	B25	Rxout22	Rxout17	B25	EB5	EB7

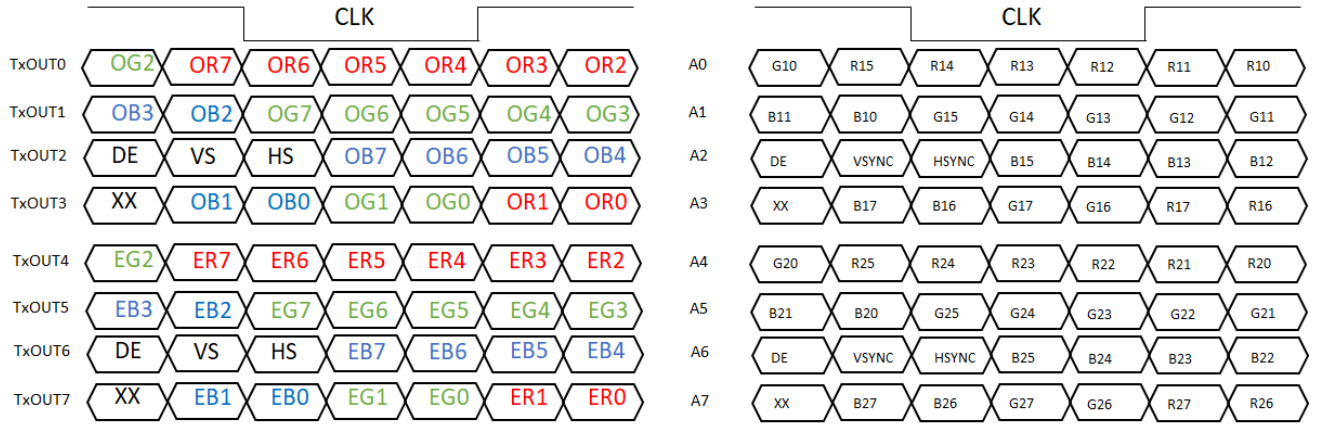

Figure 4. JEIDA/Format 1 Mapping for Dual Pixel per Clock Input Application

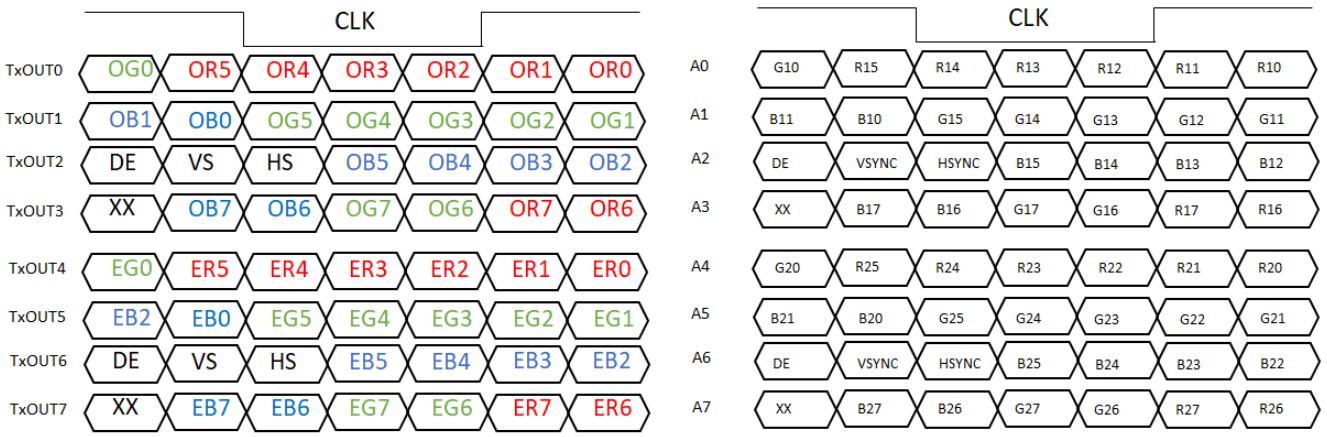

Figure 5. VESA/Format 2 Mapping for Dual Pixel per Clock Input Application

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Figure 4 and Figure 5 illustrate JEIDA and VESA mapping for 48-bit SerDes with the DS90C387 transmitter as an example. Two 24-bit SerDes can also be used for this application. In this case, the odd data would be sent to one SerDes and the even data would be sent to the other SerDes.

5 Single Pixel per Clock Input to Dual Pixel per Clock Output Application

Table 3 shows how the input signals (single pixel) are split into odd (first) and even (second) pixels (dual pixels). This is only supported with an even number of cycles during blanking (blanking occurs when DE = low). A single input is split into odd and even pixel data starting with the odd (first) pixel outputs (A0-A3). The next pixel goes to the even pixel outputs (A4-A7). The splitting of the data signal also starts with DE (data enable) transitioning from logic low to high, indicating active data.

Table 3. Single Pixel per Clock Input to Dual Pixel per Clock Output Application

VGA — TFT		Data Signal Input Data Pin	Output Data Pin	TFT Panel Data Signal	
24-bit	18-bit	48-bit 1Tx (C387)	48-bit 1Rx (CF388)	36-bit	48-bit
R0 (LSB)		R16	R16		OR0
R1		R17	R17		OR1
R2	R0	R10	R10	OR0	OR2
R3	R1	R11	R11	OR1	OR3
R4	R2	R12	R12	OR2	OR4
R5	R3	R13	R13	OR3	OR5
R6	R4	R14	R14	OR4	OR6
R7 (MSB)	R5	R15	R15	OR5	OR7
G0 (LSB)		G16	G16		OG0
G1		G17	G17		OG1
G2	G0	G10	G10	OG0	OG2
G3	G1	G11	G11	OG1	OG3
G4	G2	G12	G12	OG2	OG4
G5	G3	G13	G13	OG3	OG5
G6	G4	G14	G14	OG4	OG6
G7 (MSB)	G5	G15	G15	OG5	OG7
B0 (LSB)		B16	B16		OB0
B1		B17	B17		OB1
B2	B0	B10	B10	OB0	OB2
B3	B1	B11	B11	OB1	OB3
B4	B2	B12	B12	OB2	OB4
B5	B3	B13	B13	OB3	OB5
B6	B4	B14	B14	OB4	OB6
B7 (MSB)	B5	B15	B15	OB5	OB7
		R16	R26		ER0
		R17	R27		ER1
		R10	R20	ER0	ER2
		R11	R21	ER1	ER3
		R12	R22	ER2	ER4
		R13	R23	ER3	ER5
		R14	R24	ER4	ER6
		R15	R25	ER5	ER7
		G16	G26		EG0
		G17	G27		EG1
		G10	G20	EG0	EG2

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Table 3. Single Pixel per Clock Input to Dual Pixel per Clock Output Application (continued)

VGA — TFT		Data Signal Input Data Pin	Output Data Pin	TFT Panel Data Signal	
24-bit	18-bit	48-bit 1Tx (C387)	48-bit 1Rx (CF388)	36-bit	48-bit
		G11	G21	EG1	EG3
		G12	G22	EG2	EG4
		G13	G23	EG3	EG5
		G14	G24	EG4	EG6
		G15	G25	EG5	EG7
		B16	B26		EB0
		B17	B27		EB1
		B10	B20	EB0	EB2
		B11	B21	EB1	EB3
		B12	B22	EB2	EB4
		B13	B23	EB3	EB5
		B14	B24	EB4	EB6
		B15	B25	EB5	EB7

6 TFT Control Data Signal and CLK

Table 4 shows the mapping of the control signals (DE, HSYNC, VSYNC) for SerDes chipsets.

Table 4. TFT Control Data Signal and CLK

VGA — TFT Data Signal	Input Data Pin			Output Data Pin			TFT Panel Data Signal	
	24-bit Tx (C385)	18-bit Tx (C365)	48-bit Tx (C387)	24-bit Rx (CF384A)	18-bit Rx (CF364A)	48-bit Rx (CF388)	18/36-bit	24/48-bit
HSYNC	Txin24	Txin18	HSYNC	Rxout24	Rxout18	HSYNC	HSYNC	
VSYNC	Txin25	Txin19	VSYNC	Rxout25	Rxout19	VSYNC	VSYNC	
DEN	Txin26	Txin20	DE	Rxout26	Rxout20	DE	DEN	
CLK	TxCLKin	TxCLKin	CLKIN	TxCLKout	TxCLKout	CLKOUT	CLK	

7 Conclusion

Using the recommended color mapping, interoperability is obtained between the LVDS display interface and 18-bit or 24-bit LVDS SerDes devices. It is also possible to directly interface a 24-bit VGA to an 18-bit panel as the additional LSB color bits are mapped to separate LVDS data lines.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 1999) to A Revision **Page**

- Formatted the user guide to TI's latest documentation standard 1
- Changed the *Introduction* section 1
- Color-coded the *Single Pixel per Clock Input Application* and *Dual Pixel per Clock Input Application* gentables for the user 2
- Updated the VGA TFT Data Signal and TFT Panel Data Signal bit names for the 36-bit and 48-bit applications listed in the *Dual Pixel per Clock Input Application* table 4
- Updated the TFT Panel Data Signal bit names for the 36-bit and 48-bit applications listed in the *Single Pixel per Clock Input to Dual Pixel per Clock Output Application* table 6
- Changed the *Conclusion* section 7

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