User's Guide

LMK1D1208 Low-Additive Jitter, Eight LVDS Outputs Clock Buffer Evaluation Board

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ABSTRACT

The LMK1D1208 is a high-performance, low additive jitter LVDS clock buffer with two universal inputs, eight LVDS outputs and an input enable pin.

This evaluation module (EVM) is designed to demonstrate the electrical performance of the LMK1D1208. Throughout this document, the acronym EVM and the phrases evaluation module and evaluation board are synonymous with the LMK1D1208EVM.

The LMK1D1208EVM is equipped with 50- SMA connectors and impedance-controlled 50- microstrip transmission lines for best performance.

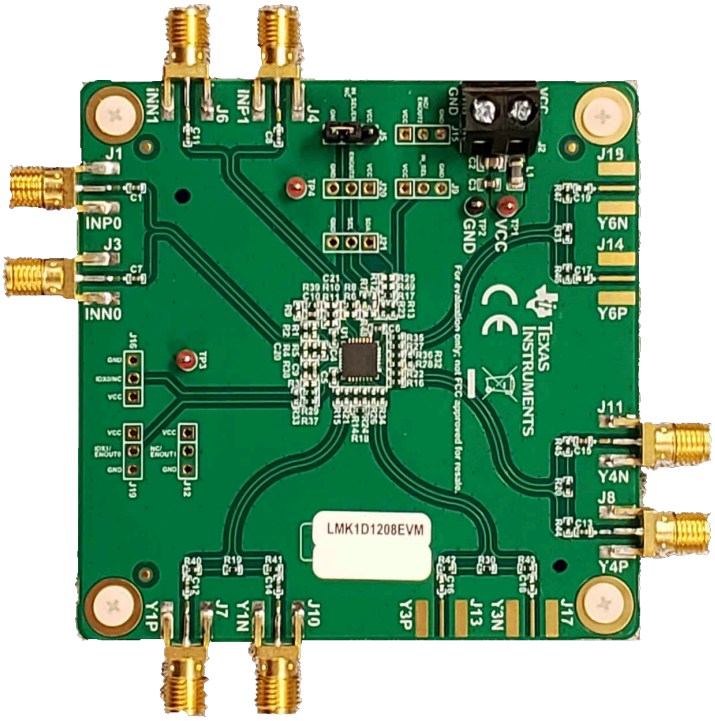

Figure 1-1. LMK1D1208 Evaluation Board

Table of Contents

Trademarks

1 Features

- Easy-to-use evaluation board to fan out low-phase noise clocks
- Simple, fast device configuration and setup
- Control pin(s) configurable through jumpers
- Single supply input powered at either 1.8 V, 2.5 V, or 3.3 V
- Differential or single-ended input clocks accepted
- EVM supports four differential LVDS outputs. Both output banks are available for testing

2 General Description

The LMK1D1208 is a high-performance, low-additive jitter clock buffer. This has two universal input buffers that support differential clock inputs which can be selected by the control pin. The device also features on-chip bias generators that can provide LVDS common-mode voltage for AC-coupled differential clock inputs.

The evaluation module (EVM) is designed to demonstrate the electrical performance of the LMK1D1208. This fully assembled and factory-tested evaluation board allows complete validation of device functionalities. For optimum performance, the board is equipped with SMA connectors and well-controlled, 50-Ω impedance microstrip transmission lines.

3 Signal Path and Control Circuitry

The LMK1D1208 supports single-ended inputs up to 250 MHz and differential inputs up to 2 GHz. Each device provides up to eight LVDS outputs operating at the input frequency.

For more information, see the *LMK1D1208 Low Additive Jitter LVDS Buffer* data sheet (SNAS815) for details.

4 Getting Started

The EVM has self-explanatory labeling and offers almost the same naming convention as used in the data sheets. The ***bold italic*** text in this document follow the same spelling as the actual labeling on the EVM board. The EVM can be used with differential inputs by default or with single-ended inputs after board modification.

5 Power Supply Connection

TP1 and TP2 can be used as optional test points.

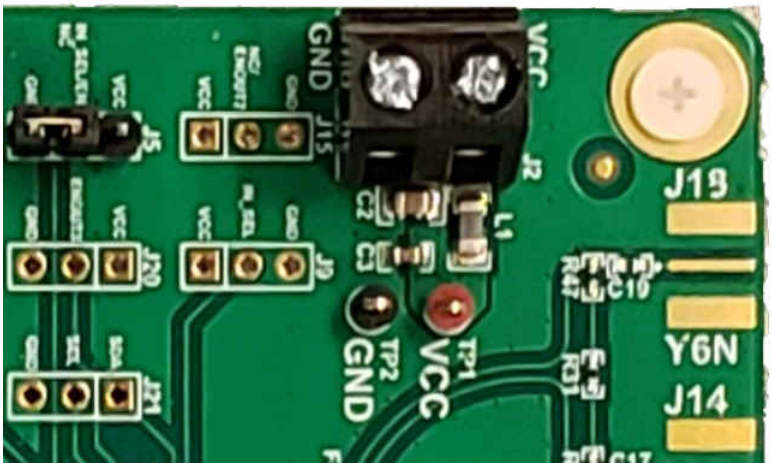

Figure 5-1. Power Block Connection

Connect the power supply source to the contact header labeled ***VCC*** (***JC2-1 or TP1***), and connect the ground of the power supply source to ***GND*** (***JC2-2 or TP2***). The decoupling capacitors and ferrite bead isolate the EVM power from the power pins of the device.

A supply voltage of 1.71 V to 3.465 V can be used for this EVM.

6 Input Clock Selection

The LMK1D1208 can receive either a differential or single-ended clock as clock input. The default board configuration is for a differential signal at both device inputs. The inputs can be applied through the SMAs, ***J1, J3*** or ***J4, J6***. These inputs are AC-coupled to the device. The common-mode voltage is provided by the device on-chip bias generator (V_{AC_REF}) pins.

LMK1D1208: Either of the two input clocks can be selected using the jumper ***J5***. When ***J5*** is connecting ***IN_SEL*** to ***GND***, ***IN0*** is selected. When ***J5*** is connecting ***IN_SEL*** to ***VDD***, ***IN1*** is selected.

6.1 Differential Input

Differential Input is configured by default.

6.2 Configuring Single-Ended Input

Single-ended input must be configured by replacing or removing passive components on the board. Follow Table 6-1 for proper configuration of single-ended input.

Table 6-1. Single-Ended Configurations by Bias Voltage

BIAS VOLTAGE TO INx_N (V)	INPUT TO INx_P (V)	INPUT	REMOVE BIASING RESISTOR	REMOVE COMMON-MODE RESISTOR	REPLACE WITH 0-Ω RESISTOR	REPLACE WITH 100-Ω RESISTOR
0.9	1.8 (LVCMOS)	IN0_N	R2 R4	R38	C1	N/A
		IN0_P			C7	N/A
0.9	1.8 (LVCMOS)	IN1_N	R8 R10	R39	C8	N/A
		IN1_P			C11	N/A
1.25	2.5 (LVCMOS)	IN0_N	R4	R38	R3 C1, C7	R1 R2
		IN0_P				
1.25	2.5 (LVCMOS)	IN1_N	R10	R39	R9 C8, C11	R6 R8
		IN1_P				
1.65	3.3 (LVCMOS)	IN0_N	R4	R38	R3 C1, C7	R1 R2
		IN0_P				
1.65	3.3 (LVCMOS)	IN1_N	R10	R39	R9 C8, C11	R6 R8
		IN1_P				

7 Output Clock

The LMK1D1208 generates up to eight LVDS outputs, and two outputs are available by default on the EVM (OUT1 and OUT4) through the following SMAs: ***J7*** and ***J10*** for OUT1; ***J8*** and ***J11*** for OUT4. The LVDS outputs are AC-coupled to their respective SMAs. Each output pair has an option of 100-Ω termination on the board (***R19*** and ***R20*** – populated).

8 EVM Board Schematic

Figure 8-1 shows the printed-circuit board (PCB) schematic.

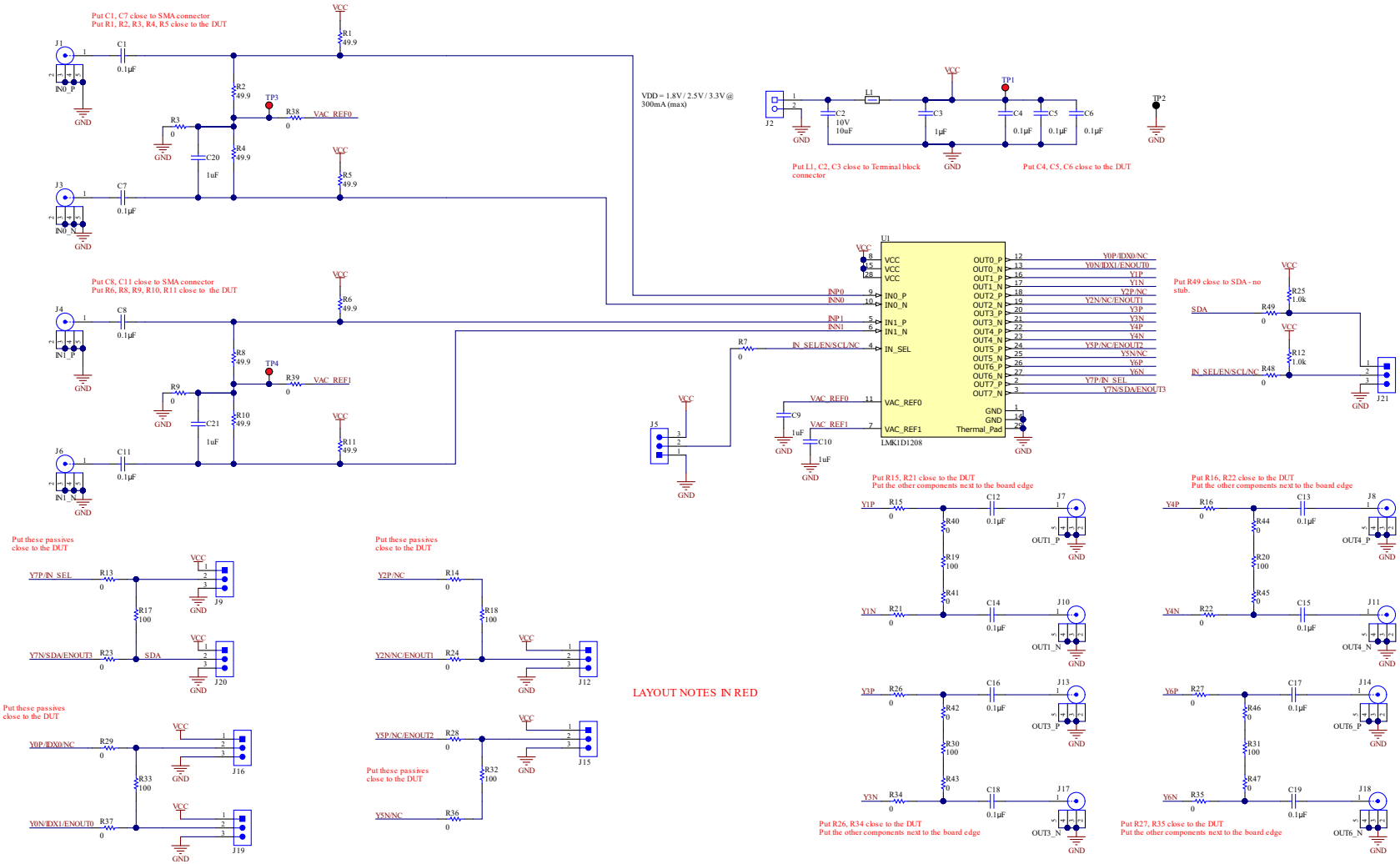

Figure 8-1. LMK1D1208EVM Schematic

9 REACH Compliance

REACH Compliance

In compliance with the Article 33 provision of the EU REACH regulation we are notifying you that this EVM includes component(s) containing at least one Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are:

Component Manufacturer	Component type	Component part number	SVHC Substance	SVHC CAS (when available)
Molex	5.08 Pitch Eurostyle Vertical Fixed Mount PCB Terminal Block, 2 Circuits	039544-3002	Lead	7439-92-1

10 Bill of Materials

Table 10-1. Bill of Materials

QUANTITY	VALUE	DESIGNATOR	PACKAGE REFERENCE	DESCRIPTION	MANUFACTURER	PART NUMBER
11	0.1uF	C1, C4, C5, C6, C7, C8, C11, C12, C13, C14, C15	0402	CAP, CERM, 0.1 µF, 10 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0402	Kemet	C0402C104K8RACAUTO
1	10uF	C2	0805	CAP, CERM, 10 uF, 10 V, +/- 10%, X5R, 0805	Kemet	C0805C106K8PACTU
1	1uF	C3	0603	CAP, CERM, 1 µF, 10 V,+/- 5%, X7R, AEC-Q200 Grade 1, 0603	Kemet	C0603X105J8RAC7867
2	1uF	C9, C10	0402	CAP, CERM, 1 uF, 6.3 V, +/- 20%, X7R, 0402	MuRata	GRM155R70J105MA12D
4	4-40 x 0.25"	H1, H2, H3, H4	Screw	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH
4	4-40 x 0.5"	H5, H6, H7, H8	Standoff	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C
8		J1, J3, J4, J6, J7, J8, J10, J11	SMA Connector	CONN SMA JACK STR EDGE MNT	RF Solutions Ltd.	CON-SMA-EDGE-S
1	5.08mm, 2x1	J2	Terminal Block	Terminal Block, 5.08mm, 2x1, TH	Molex	039544-3002
1	100mil, 3x1	J5	Header	Header, 100mil, 3x1, Gold, TH	Sullins Connector Solutions	PBC03SAAN
1	50 ohm	L1	1206	Ferrite Bead, 50 ohm @ 100 MHz, 12 A, 1206	MuRata	BLM31SN500SZ1L
1	0.650" x 0.200"	LBL1	PCB Label	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10
4	49.9	R2, R4, R8, R10	0402	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	Panasonic	ERJ-2RKF49R9X
27	0	R7, R13, R14, R15, R16, R21, R22, R23, R24, R26, R27, R28, R29, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47	0402	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04020000Z0ED
8	100	R17, R18, R19, R20, R30, R31, R32, R33	0402	RES, 100, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0402	Vishay/Beyschlag	MCS0402MD1000BE100
1	1x2	SH1	Shunt	Shunt, 100mil, Gold plated, Black	Samtec	SNT-100-BK-G
3	Red	TP1, TP3, TP4	Testpoint	Test Point, Miniature, Red, TH	Keystone	5000

Table 10-1. Bill of Materials (continued)

QUANTITY	VALUE	DESIGNATOR	PACKAGE REFERENCE	DESCRIPTION	MANUFACTURER	PART NUMBER
1	Black	TP2	Testpoint	Test Point, Miniature, Black, TH	Keystone	5001
1		U1	VQFN28	2:8 Low Additive Jitter LVDS Buffer	Texas Instruments	LMK1D1208

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