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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Audio
- Amplifiers: Op Amps
- Low-Power RF
- General Interest

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Clock jitter analyzed in the time domain, Part 3

By Thomas Neu
Systems and Applications Engineer

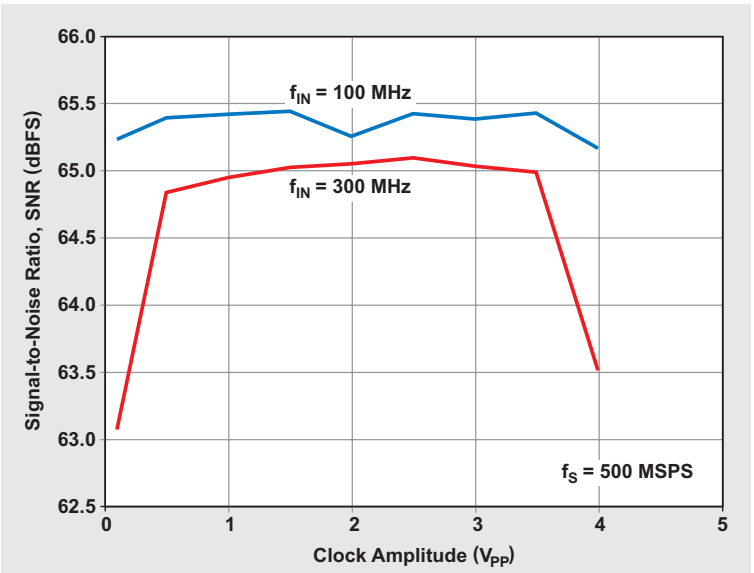
Introduction

Part 1 of this three-part article series focused on how to accurately estimate jitter from a clock source and combine it with the aperture jitter of an ADC.[1] In Part 2, that combined jitter was used to calculate the ADC's signal-to-noise ratio (SNR), which was then compared against actual measurements.[2] This article, Part 3, shows how to further increase the SNR of the ADC by improving the ADC's aperture jitter, with a focus on optimizing the slew rate of the clock signal.

As shown in Parts 1 and 2, a bandpass filter on the clock signal is a key component for achieving an ADC's data-sheet SNR values. The far-end phase noise of the clock signal adds a substantial amount to the total jitter of the clock signal, causing the SNR to degrade even faster at higher input frequencies.

Unfortunately, there are two major disadvantages associated with the bandpass filter. The first is that it not only removes the clock signal's far-end phase noise, it also eliminates the higher-order odd harmonics of the fundamental clock frequency, turning a square wave into a sine wave. These odd harmonics (third, fifth, etc.) are essential for achieving a fast slew rate to minimize the ADC's aperture jitter. The second disadvantage of the bandpass filter, depending on topology and order, is that it has some loss associated with it that can typically range anywhere from 1 to 9 dB. This loss is equivalent to attenuating the clock amplitude and thus reducing the slew rate of the clock signal even further.

Figure 20. SNR versus clock amplitude versus input frequency (from ADS54RF63 data sheet)

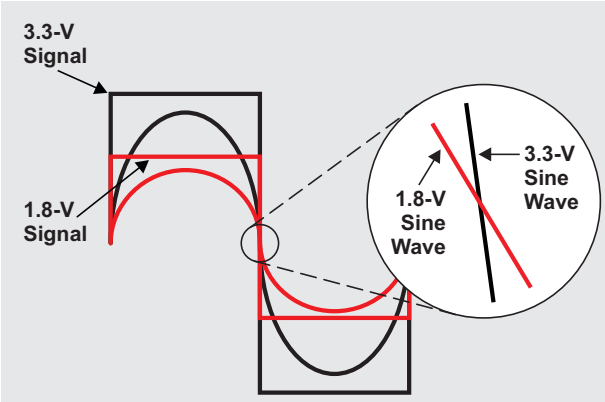


The slew rate's impact on an ADC's SNR performance is often shown in the ADC's data sheet as SNR plotted versus clock amplitude, as in Figure 20. This figure, taken from the Texas Instruments (TI) ADS54RF63 data sheet,[3] shows that the larger the clock's amplitude is, the larger its slew rate will be. Figure 20 also demonstrates that, as expected, the SNR sensitivity to the clock's slew rate increases as the input frequency, f_{IN}, increases. However, the plot also indicates that overdriving the clock input too much may actually cause clipping or damage inside the ADC, negatively impacting the SNR.

In an effort to lower the intrinsic noise and reduce the power consumption, manufacturers produce clock-distribution ICs with smaller process nodes and consequently lower power-supply rails. For example, it is much more difficult to generate a fast-slew-rate clock signal from a 1.8-V device than from a 3.3-V device; and the loss from the bandpass filter only makes this deficiency worse (see Figure 21).

The remainder of this article focuses on two practical ways to maximize the slew rate of the filtered clock signal in real applications by trying to "restore" the removed clock harmonics. Essentially, the clock edges need to be

Figure 21. Bandpass-filter input and output with 1.8-V and 3.3-V logic



squared up again, and the signal swing needs to be increased as much as possible to compensate for the loss from the bandpass filter (BPF). Both tasks can be accomplished by increasing the signal gain through either an active or a passive circuit (see Figure 22). Both options have advantages and disadvantages, all of which will be discussed next along with the key considerations for making a selection.

Using a low-noise amplifier for active gain

System designers often don't want to use active gain because it adds noise to the system and consumes extra power. However, in some cases it may be the only option, as (for example) when the design uses a high clock frequency that exceeds the bandwidth of the step-up transformer.

There are several parameters the system designer needs to consider when selecting the amplifier:

Bandwidth specification—There are a lot of RF amplifiers available, but very few extend down to intermediate frequencies (<250 to 500 MHz). The noise figure of standard CMOS amplifiers isn't low enough to be considered (<2 dB), so the best practice is to choose an RF amplifier. The amplifier's usable bandwidth needs to be wide enough to include at least the third and preferably the fifth harmonic of the fundamental clock frequency. Therefore, an amplifier for a 122.88-MHz clock needs to cover at least 368.64 MHz, and for a 500-MHz clock at least 1.5 GHz.

Noise figure—To minimize the additional noise contribution of the low-noise amplifier (LNA), its noise figure

Figure 22. Addition of circuitry to boost slew rate

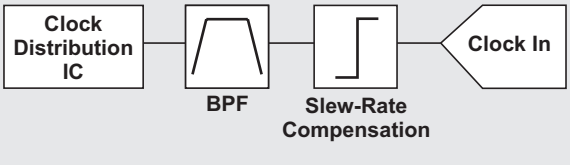
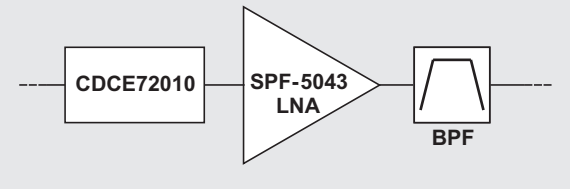
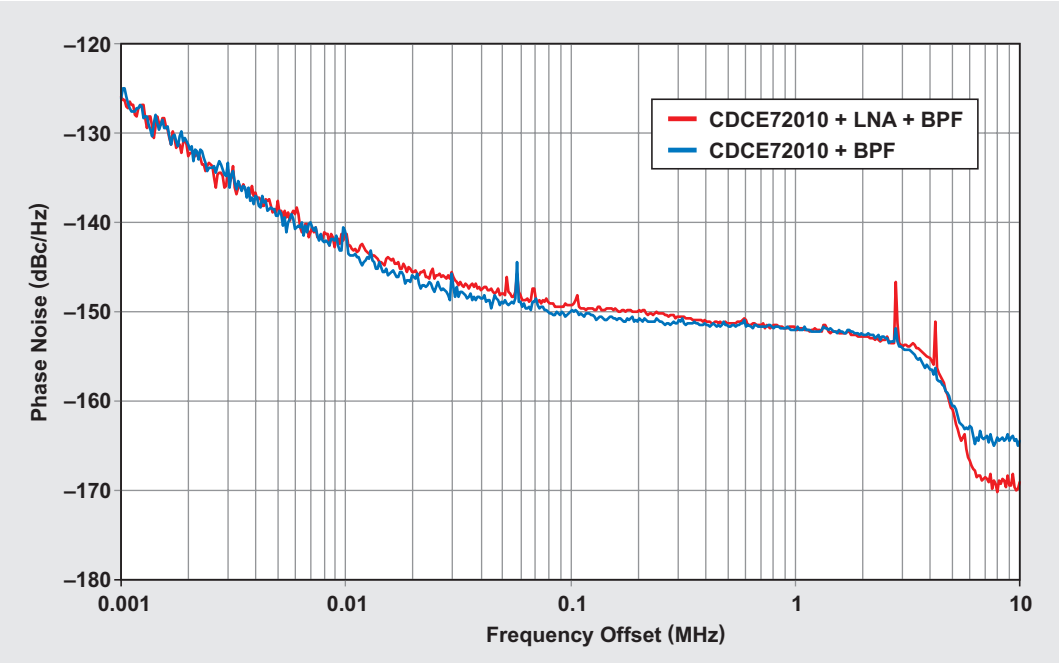


Figure 23. Low-power LNA compensates for BPF losses



should be at least 2 dB or better. Most LNAs, even with low noise figures, add broadband noise to the clock signal. Hence the LNA should be placed between the clock-distribution device and the bandpass filter (BPF) (see Figure 23) to limit the amount of extra noise (see Figure 24). (The TI CDCE72010 used for Figures 23 and 24 is the clock synchronizer used in the examples in Part 2 of this

Figure 24. LNA slightly degrades clock signal's phase noise inside BPF's pass band



article series.) Better noise figures typically require more power consumption, which may set some practical limits to the amplifier search.

P1dB compression point—The P1dB compression point essentially defines the maximum possible output swing. To achieve a clock signal of about 2 V_{PP}, the P1dB needs to be at least 10 dBm.

Voltage rail—The voltage rail of the amplifier can be used to avoid exceeding the maximum voltage rating of the ADC's clock pins. However, for maximum performance, a new voltage rail may be necessary, adding cost and board space to the system.

Stability—A low-loss LC bandpass filter has a high reactance. RF LNAs are designed to ideally drive a resistive 50-Ω load, so driving a reactance may cause instability or distortion with additional unwanted spurs, which may require a matching network.

Gain—Even though the LNA is operated with high gain (>10 to 12 dB) similar to a comparator, the research in conjunction with this article showed that pure comparators are not suitable for this function. They add too much noise to the output signal, and most often their slew rate is not fast enough.

Part 2 described the example of the CDCE72010 clock synchronizer driving the TI ADS54RF63 and ADS5483 ADCs with a sampling frequency of 122.88 MSPS. The SPF-5043 LNA from RF Micro Devices was evaluated as a suitable amplifier for this example (see Figure 23). In an effort to keep the additional power consumption from the LNA to a minimum, the amplifier was operated from a 3.3-V supply and the quiescent current was measured at about 41 mA, or a power consumption of about 131 mW.

The SPF-5043 data sheet lists the following specifications:

- Usable bandwidth extends down to 100 MHz
- Noise figure = 0.6 dB
- P1dB = ~19 dBm
- Gain = ~22 dB

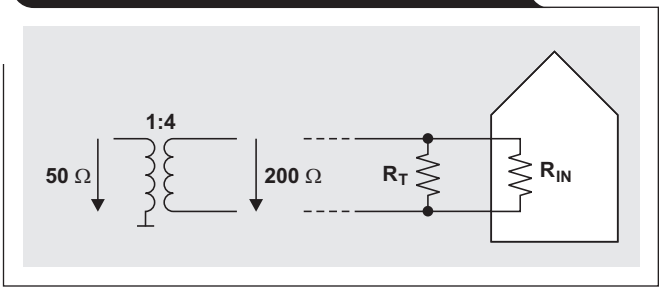
Even though the LNA's noise figure is really low, the SNR performance was better when the LNA was placed before the bandpass filter instead of following it.

The maximum output voltage of the SPF-5043 is limited by the 3.3-V voltage rail. However, when a step-up transformer is used to convert the signal from single-ended to differential, additional measures may be necessary to avoid exceeding the maximum voltage rating of the ADC's clock inputs.

Using a step-up transformer for passive gain

The easiest way to improve the slew rate of the clock signal is by means of a step-up transformer. Since it is a passive component, it doesn't add extra noise or increase power consumption. In power-sensitive or portable applications, a transformer-based solution may be the only practical choice; and oftentimes a transformer may already be used in the clock path to convert a clock input from single-ended to differential. However, there are some applications where a step-up transformer is not practical and the following parameters need to be considered:

Figure 25. Step-up transformer changes input impedance

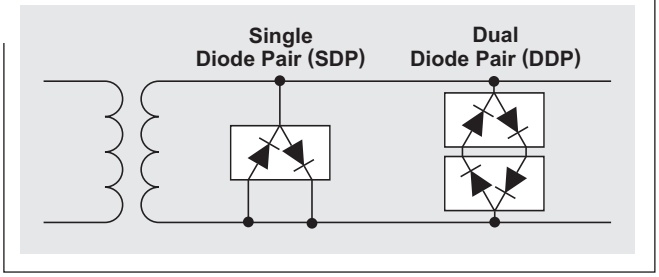


Bandwidth requirement—Transformers themselves have the frequency response of a bandpass filter. The magnetic coupling between input and output gets weaker as the frequency gets close to DC, and at higher frequencies the transformer parasitics such as inner-winding capacitance and leakage inductance are starting to dominate. The pass-band bandwidth of off-the-shelf transformers is typically less than that of a wideband LNA such as the SPF-5043, and the upper frequency limit decreases as the step-up ratio increases (1:8 versus 1:4).

Impedance transformation and transformer impedance ratio—Besides increasing the output voltage, the step-up transformer also changes the input impedance. For example, a transformer with a 1:4 impedance ratio changes a 50-Ω source into a 200-Ω source impedance (see Figure 25). Therefore, the ADC clock's input impedance needs to be considered when the transformer impedance ratio is selected, because it is in parallel with the clock's input termination (R_T). For example, if the ADC clock's input impedance is only 200 to 300 Ω, then a 1:8 step-up transformer—even without any termination—would present a 25- to 40-Ω load to the clock source. This is a significant load that may keep the clock source from generating as high a swing because it can't source enough output current.

Maximum voltage swing—The step-up transformer can easily generate output voltages larger than 5 V, quickly exceeding the maximum voltage ratings of the ADC's clock input. A 5-V converter typically has a maximum input voltage of about 5.5 V, while a 3.3-V converter may tolerate a maximum of only about 3.6 V. Exceeding the maximum voltage rating of the ADC reduces its life span and may even result in catastrophic failure due to electrical overstress. Although the clock input typically is protected with ESD diodes, it is not good practice to rely solely on them. A better alternative for protecting against electrical overstress may be to employ external clipping diodes.

Figure 26. Using clipping diodes to protect ADC inputs



Using Schottky clipping diodes

Using clipping diodes is a common way to protect the data converter's inputs from exceeding the maximum voltage rating. Because low-capacitance Schottky diodes, such as the HSMS-2812 from Avago Technologies, can maintain fast slew rates, they are well-suited for RF and high-speed applications. The HSMS-2812 has a forward voltage of 410 mV. Using a pair of anti-parallel diodes (see Figure 26) creates a differential clipping voltage of ±410 mV (820 mV_{PP}). For ADCs that require a higher clock amplitude, two pairs of anti-parallel diodes can be placed back-to-back, doubling the clipping voltage to ±820 mV (1.64 V_{PP}).

Figure 27 shows the filtered LVCMOS output of the CDCE72010 that results when a 1:4 transformer is used with and without a single diode pair (SDP). Also shown is the output for when a 1:8 transformer is used with an SDP or a back-to-back dual diode pair (DDP). It can be seen that with the 1:4 transformer, the SDP reduces the sine-wave amplitude from about 1.6 to 0.9 V_{PP}. However, the clipped output waveform no longer resembles a pure sine wave but looks instead like a square wave.

It is interesting to note that when the SDP configuration is used, there doesn't seem to be an amplitude difference between using the 1:4 or the 1:8 transformer, although the waveform for the latter appears to have a slightly faster slew rate. For the DDP configuration with the 1:8 transformer, the output amplitude is about 1.6 V_{PP} with a little better slew rate around the zero crossing point.

Figure 27. Clock signal with different transformer and clipping-diode configurations

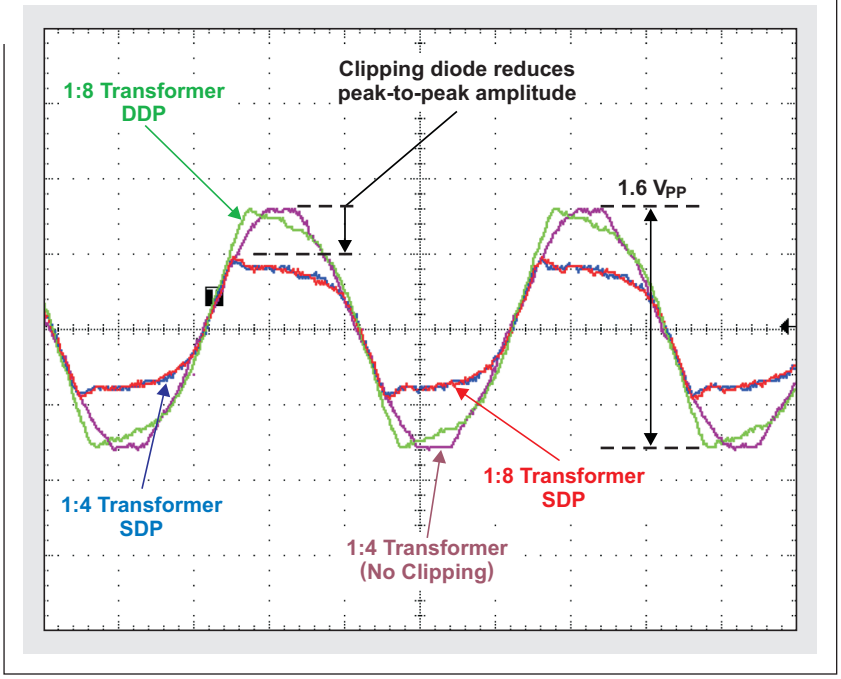
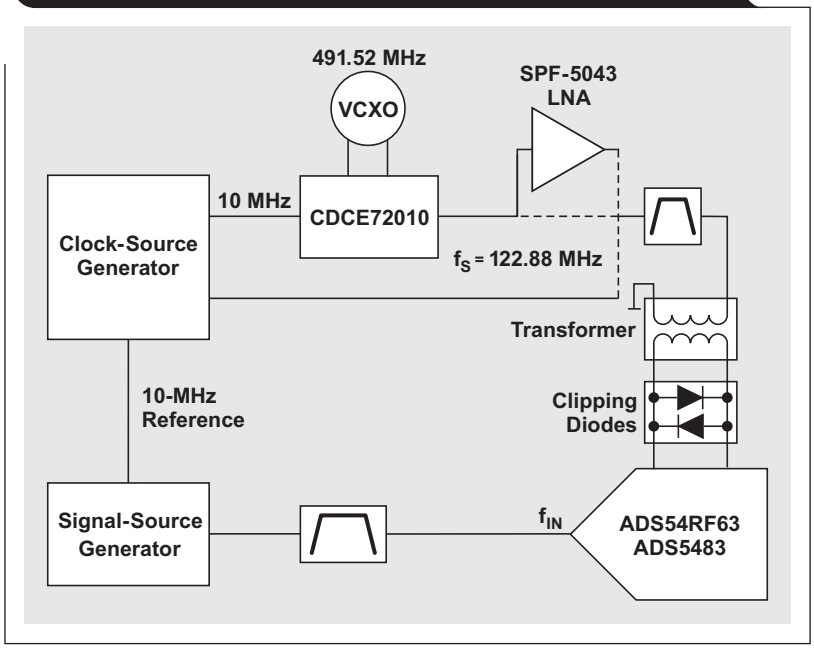


Figure 28. Setup for testing different active- and passive-gain circuits



SNR measurements

An investigation was conducted to see whether the ADC's aperture degradation due to the external clock's slew-rate limitation could be improved. Different configurations using step-up transformers, an SPF-5043 LNA, and clipping diodes were tested to maximize the ADC's SNR when a realistic clocking solution such as the CDCE72010 was used (see Figure 28) rather than a low-jitter clock-source generator.

As highlighted in Part 2 of this article series, the filtered LVCMOS output of the CDCE72010 has about 90 fs of clock jitter, while the clock-source generator has only about 35 fs. Although the clock-jitter difference prevents the CDCE72010 from ever achieving the same SNR as when the clock-source generator is used, the goal was to find a configuration to reduce the resulting SNR gap as much as possible. The ADS54RF63 ADC was used with a sampling frequency (f_S) of 122.88 MSPS and an input frequency (f_{IN}) of 1.0 GHz. The ADS5483 ADC was also used, with the same value for f_S but with an f_{IN} of 100 MHz.

The following different parameters were examined:

- Use of an LNA to boost the output voltage and slew rate of the CDCE72010
- Step-up transformers with ratios of 1:1, 4:1, 8:1, and 16:1 (Coilcraft WBC series and Mini-Circuits ADT series)
- Avago's HSMS-2812 clipping diodes—either SDPs or back-to-back DDPs in anti-parallel configuration

Measurements for ADS54RF63

The default configuration for the ADS54RF63 evaluation module (ADS54RF63EVM) used a Coilcraft WBC4-1 step-up transformer, and the baseline SNR was about 60.7 dBFS when the low-jitter clock-source generator was used. If the CDCE72010 with the LVCMOS output was used as the clock source instead, the SNR dropped to 57.8 dBFS. However, with only about 90 fs of clock jitter, an SNR better than about 60 dBFS should theoretically be attainable, so there was room for at least a 2.2-dB improvement.

Figure 29. Measured SNR of different clock-input configurations using ADS54RF63 with f_S = 122.88 MSPS and f_{IN} = 1 GHz

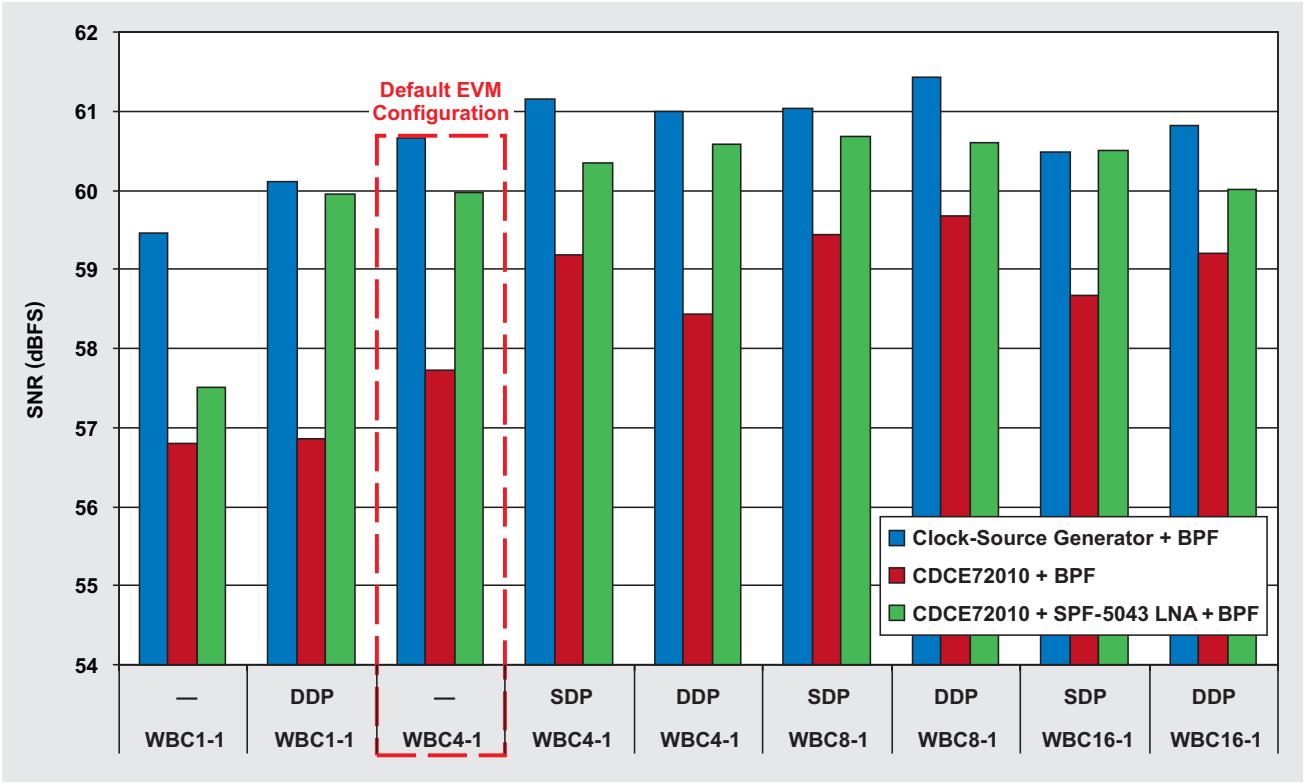
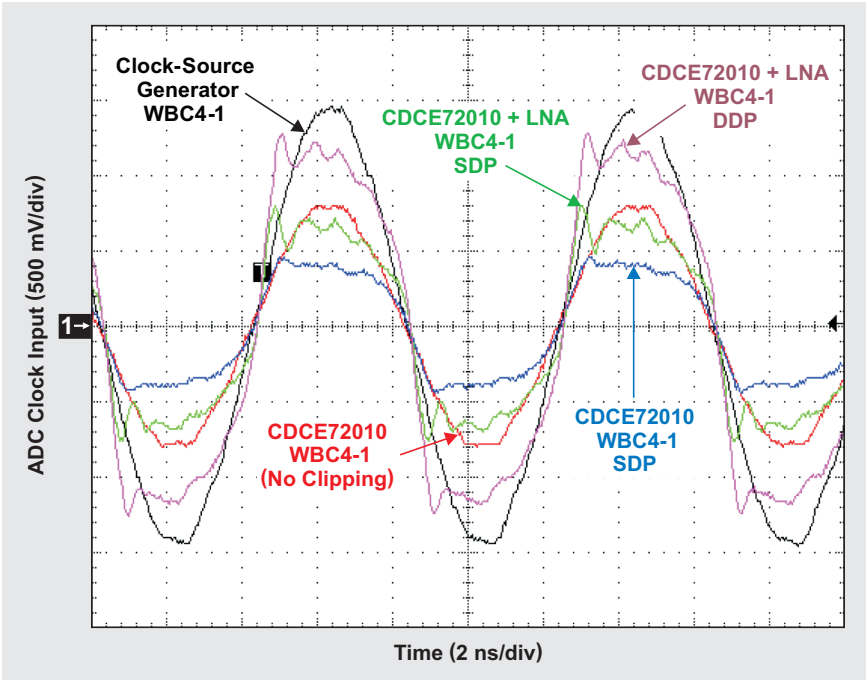


Figure 29 shows the different EVM clock-input configurations along with the measured SNR values of the ADS54RF63. It can be seen that the clipping diodes alone seemed to improve the SNR with the default WBC4-1 step-up transformer, while the addition of the SPF-5043 LNA provided a big boost in SNR. Using the single-diode-pair (SDP) configuration along with the WBC4-1 transformer and the LNA improved the SNR to about 60.4 dBFS, which was a 2.6-dB improvement! Using a purely passive solution, the WBC8-1 transformer with an SDP and no LNA, yielded an SNR of about 59.5 dBFS, very close to the 60-dBFS target.

Figure 30 shows a comparison of the clock-input waveforms that occurred with different configurations. The low-jitter clock-source generator combined with the WBC4-1 step-up transformer provided a very large slew rate. Figure 30 shows that the filtered output of the CDCE72010 had

Figure 30. Input waveforms with different clock-source and clipping-diode configurations



a smaller peak-to-peak amplitude and thus a slower slew rate, which negatively impacted the ADC's aperture jitter. Adding the SDP to that configuration seemed to slightly improve the slew rate around the zero crossing point, which also manifested itself as improved SNR performance. Adding the high-gain LNA to the CDCE72010 output sent a much larger signal with a much larger slew rate to the clipping diodes. This resulted in an even faster transition through the zero crossing point, which in turn further improved the aperture jitter of the ADC. The dual-diode-pair (DDP) configuration seemed to improve the slew rate immediately before the zero crossing point a little bit. However, Figure 30 also shows that if the CDCE72010 with the WBC4-1 transformer were used without the LNA, the output voltage might be too low to fully trigger the clipping event. The measurement results in Figure 29 show better SNR performance with the WBC8-1 step-up transformer and DDPs.

Measurements for ADS5483

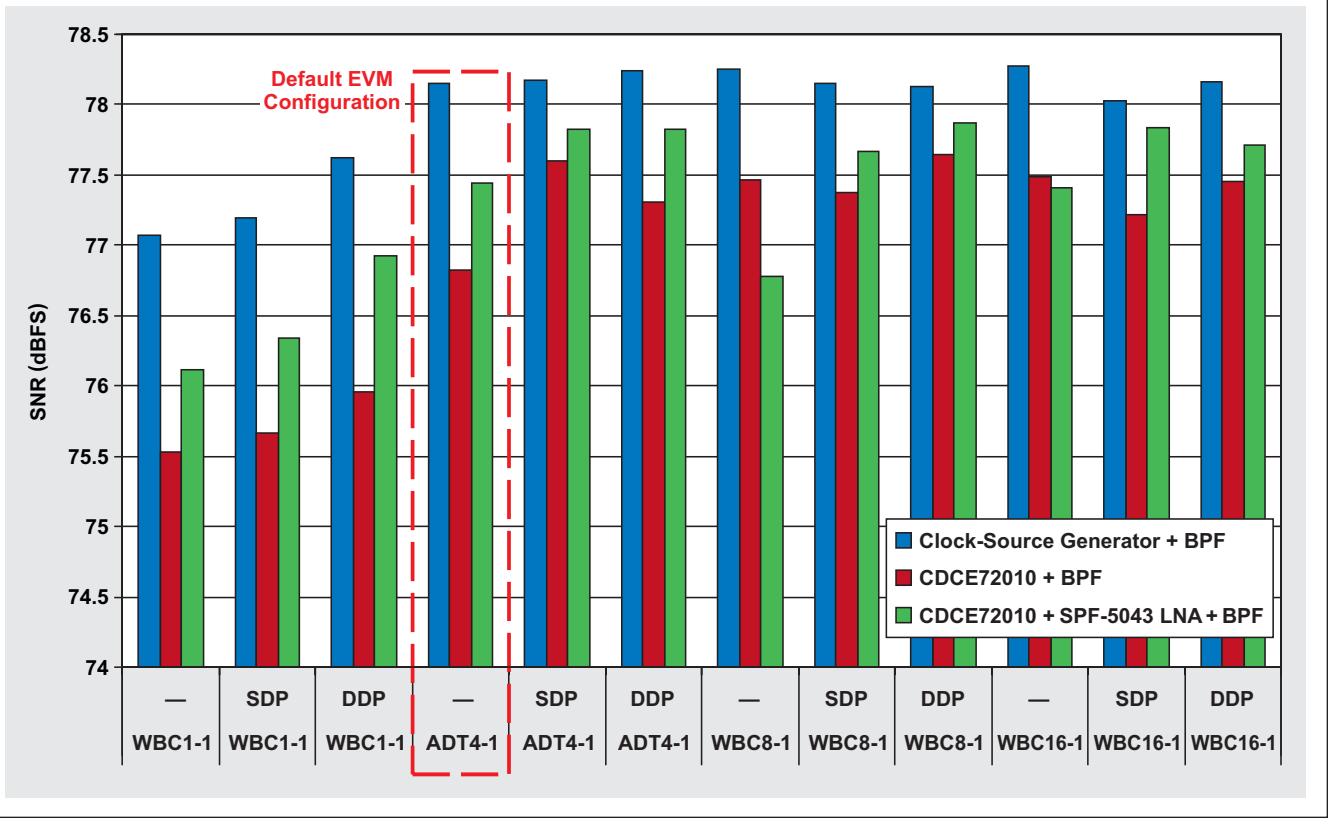
The ADS5483EVM employed a Mini-Circuits ADT4-1WT step-up transformer on the clock input. The baseline SNR with a low-jitter clock source was measured at 78.2 dBFS, while the CDCE72010 output yielded an SNR of about 76.8 dBFS. The CDCE72010 with a clock jitter of about 90 fs should provide an SNR of about 77.6 dBFS, which would be an improvement of almost 1 dB.

The measured SNR values of the ADS5483 with the various EVM clock-input configurations are illustrated in Figure 31. Adding the SDP to the ADT4-1WT transformer provided enough boost to the slew rate for the SNR with the CDCE72010 to improve by almost 1 dB to the 77.6-dBFS target. A larger step-up ratio didn't seem to add any further benefit. Adding the LNA in addition to the ADT4-1WT boosted the SNR to about 77.8 dBFS. It should be noted as well that a lower clock amplitude (WBC1-1) significantly degraded the SNR, as expected.

Conclusion

As explained in Parts 1 and 2 of this article series, the ADC's aperture jitter is not fixed but dependent on the clock-input slew rate. While the bandpass filter is necessary to minimize the clock jitter as much as possible, it also reduces the clock's slew rate by filtering out the higher-order harmonics. This article has shown practical ways (using either active or passive gain) to improve the slew rate of an existing clocking solution with a bandpass filter, thus improving the ADC's SNR by several decibels. The SNR measurements have shown that improving the slew rate of the clock signal makes the ADC's SNR match the predicted SNR for a given amount of clock jitter.

Figure 31. Measured SNR of different clock-input configurations using ADS5483 with f_S = 122.88 MSPS and f_{IN} = 100 MHz



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3. "12-bit, 500-/550-MSPS analog-to-digital converters," ADS5463/54RF63 Data Sheet	slas515

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How delta-sigma ADCs work, Part 1

By Bonnie Baker
Signal Integrity Engineer

Analog techniques have dominated signal processing for years, but digital techniques are slowly encroaching into this domain. The design of delta-sigma (ΔΣ) analog-to-digital converters (ADCs) is approximately three-quarters digital and one-quarter analog. ΔΣ ADCs are now ideal for converting analog signals over a wide range of frequencies, from DC to several megahertz. Basically, these converters consist of an oversampling modulator followed by a digital/decimation filter that together produce a high-resolution data-stream output. This two-part article will look closely at the ΔΣ ADC's core. Part 1 will explore the basic topology and function of the ΔΣ modulator, and Part 2 will explore the basic topology and function of the digital/decimation filter module.

ΔΣ converters: An overview

The rudimentary ΔΣ converter is a 1-bit sampling system. An analog signal applied to the input of the converter needs to be relatively slow so the converter can sample it multiple times, a technique known as oversampling. The sampling rate is hundreds of times faster than the digital results at the output ports. Each individual sample is accumulated over time and "averaged" with the other input-signal samples through the digital/decimation filter.

The ΔΣ converter's primary internal cells are the ΔΣ modulator and the digital/decimation filter. The internal ΔΣ modulator shown in Figure 1 coarsely samples the input signal at a very high rate into a 1-bit stream. The digital/decimation filter then takes this sampled data and converts it into a high-resolution, slower digital code. While most converters have one sample rate, the ΔΣ converter has two—the input sampling rate ($\mathbf{f_S}$) and the output data rate ($\mathbf{f_D}$).

The ΔΣ modulator

The ΔΣ modulator is the heart of the ΔΣ ADC. It is responsible for digitizing the analog input signal and reducing noise at lower frequencies. In this stage, the architecture implements a function called noise shaping that pushes low-frequency noise up to higher frequencies where it is outside the band of interest. Noise shaping is one of the reasons that ΔΣ converters are well-suited for low-frequency, high-accuracy measurements.

The input signal to the ΔΣ modulator is a time-varying analog voltage. With the earlier ΔΣ ADCs, this input-voltage signal was primarily for audio applications where AC signals were important. Now that attention has turned to precision applications, conversion rates include DC signals. This discussion will use a single cycle of a sine wave for illustration.

Figure 1. Block diagram of ΔΣ ADC

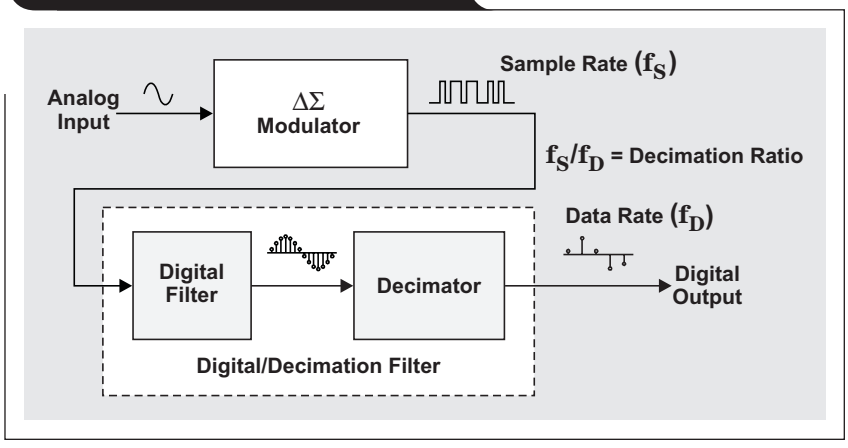


Figure 2. Input signal to the ΔΣ modulator

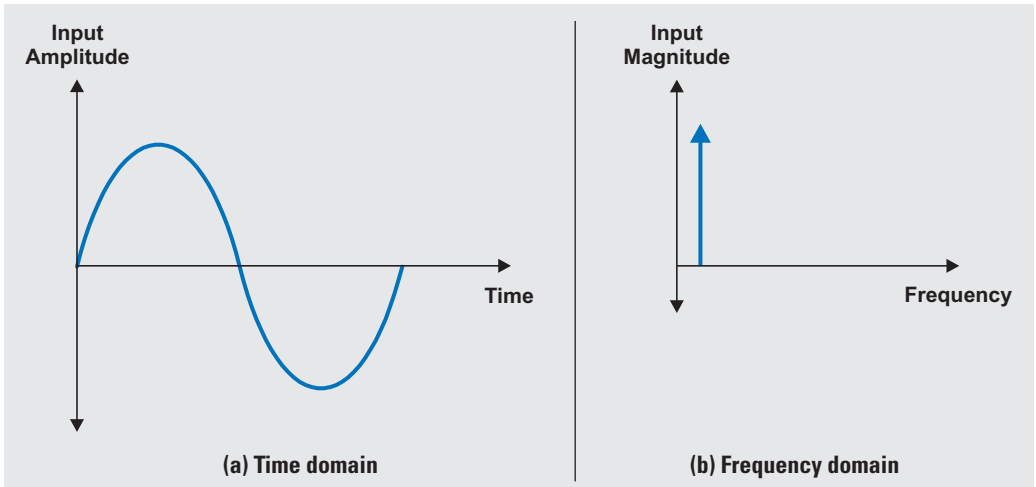


Figure 2a shows a single cycle of a sine wave for the input of a ΔΣ modulator. This single cycle has voltage amplitude that changes with time. Figure 2b shows a frequency-domain representation of the time-domain signal in Figure 2a. The curve in Figure 2b represents the continuous sine wave in Figure 2a and appears as a straight line or a spur.

There are two ways to look at the ΔΣ modulator—in the time domain (Figure 3) or in the frequency domain (Figure 4). The time-domain block diagram in Figure 3 shows the mechanics of a first-order ΔΣ modulator. The modulator converts the analog input signal to a high-speed, single-bit, modulated pulse wave. More importantly, the frequency analysis in Figure 4 shows how the modulator affects the noise in the system and facilitates the production of a higher-resolution result.

The ΔΣ modulator shown in Figure 3 acquires many samples of the input signal to produce a stream of 1-bit codes. The system clock implements the sampling speed, $\mathbf{f_S}$, in conjunction with the modulator's 1-bit comparator. In this manner, the quantizing action of the ΔΣ modulator is produced at a high sample rate that is equal to that of the system clock. Like all quantizers, the ΔΣ modulator produces a stream of digital values that represent the voltage of the input, in this case a 1-bit stream. As a result, the ratio of the number of ones to zeros represents the input analog voltage. Unlike most quantizers, the ΔΣ modulator includes an integrator, which has the effect of shaping the quantization noise to higher frequencies. Consequently, the noise spectrum at the output of the modulator is not flat.

In the time domain, the analog input voltage and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage at $\mathbf{x_2}$. This voltage is presented to the integrator, whose output progresses in a negative or positive direction. The slope and direction of the signal at $\mathbf{x_3}$ is dependent on the sign and magnitude of the voltage at $\mathbf{x_2}$. At the time the voltage at $\mathbf{x_3}$ equals the comparator reference voltage, the output of the comparator switches from negative to positive, or positive to negative,

Figure 3. First-order ΔΣ modulator in the time domain

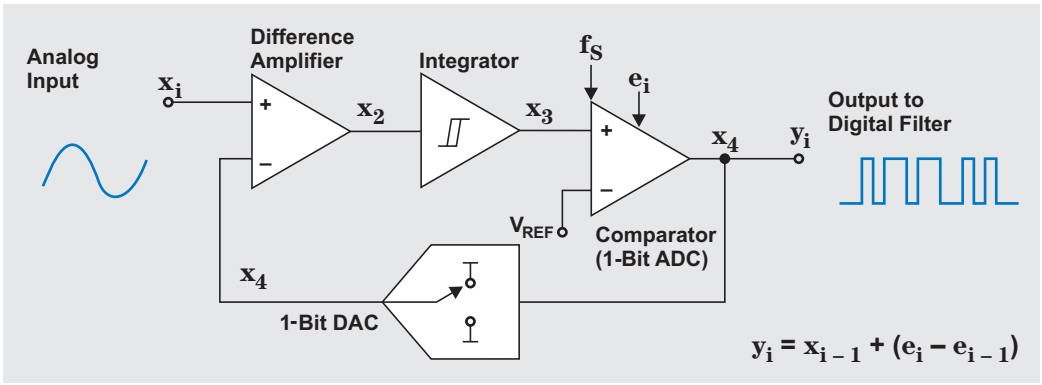
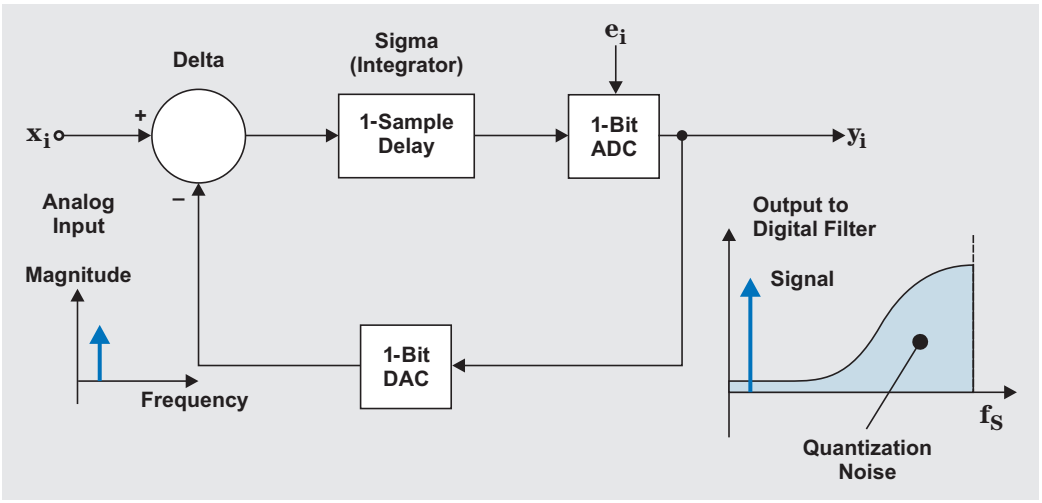


Figure 4. First-order ΔΣ modulator in the frequency domain



depending on its original state. The output value of the comparator, $\mathbf{x_4}$, is clocked back into the 1-bit DAC, as well as clocked out to the digital filter stage, $\mathbf{y_i}$. At the time that the output of the comparator switches from high to low or vice versa, the 1-bit DAC responds by changing the analog output voltage of the difference amplifier. This creates a different output voltage at $\mathbf{x_2}$, causing the integrator to progress in the opposite direction. This time-domain output signal is a pulse-wave representation of the input signal at the sampling rate ($\mathbf{f_S}$). If the output pulse train is averaged, it equals the value of the input signal.

The discrete-time block diagram in Figure 3 also shows the time-domain transfer function. In the time domain, the 1-bit ADC digitizes the signal to a coarse, 1-bit output code that produces the quantization noise of the converter. The output of the modulator is equal to the input plus the quantization noise, $\mathbf{e_i - e_{i-1}}$. As this formula shows, the quantization noise is the difference between the current quantization error ($\mathbf{e_i}$) and the previous quantization error ($\mathbf{e_{i-1}}$). Figure 4 illustrates the frequency location of this quantization noise.

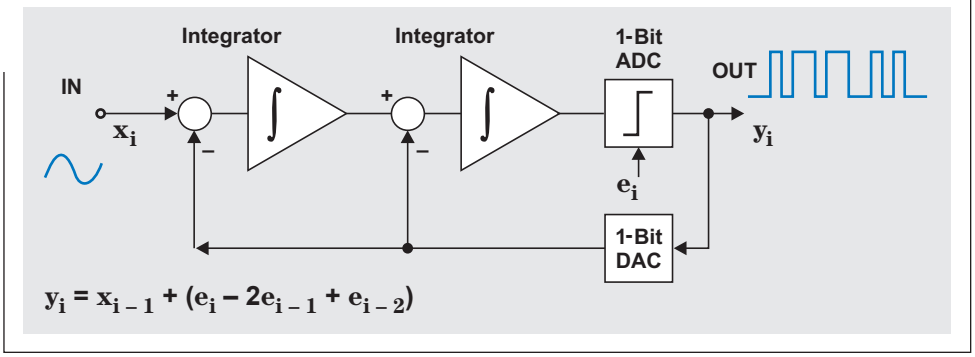
Figure 4 also shows that the combination of the integrator and sampling strategy implements a noise-shaping filter on the digital output code. In the frequency domain, the time-domain output pulses appear as the input signal (or spur) and shaped noise. The noise characteristics in Figure 4 are the key to understanding the modulator's frequency operation and the ability of the ΔΣ ADC to achieve such high resolution.

The noise in the modulator is moved out to higher frequencies. Figure 4 shows that the quantization noise for a first-order modulator starts low at zero hertz, rises rapidly, and then levels off at a maximum value at the modulator's sampling frequency ($\mathbf{f_S}$).

Using a circuit that integrates twice instead of just once is a great way to lower the modulator's in-band quantization noise. Figure 5 shows a 1-bit, second-order modulator that has two integrators instead of one. With this second-order modulator example, the noise term depends on not just the previous error but the previous two errors.

Some of the disadvantages of the second- or multi-order modulators include increased complexity, multiple loops,

Figure 5. Block diagram of a second-order ΔΣ modulator



and increased design difficulty. However, most ΔΣ modulators are higher-order, like the one in Figure 5. For instance, Texas Instruments ΔΣ converters include second- through sixth-order modulators.

Multi-order modulators shape the quantization noise to even higher frequencies than do the lower-order modulators. In Figure 6, the highest line at the frequency $\mathbf{f_S}$ shows the third-order modulator's noise response. Note that this modulator's output is very noisy all the way out at its sampling frequency of $\mathbf{f_S}$. However, down at lower frequencies, below $\mathbf{f_D}$ and near the input-signal spur, the third-order modulator is very quiet. $\mathbf{f_D}$ is the conversion frequency of the digital/decimation filter. Selecting a value for $\mathbf{f_D}$ will be discussed in Part 2 of this article series.

Modulators: The first half of the story

The modulator of the ΔΣ ADC successfully reduces low-frequency noise during the conversion process. However, the high-frequency noise is a problem and is undesirable in the final output of the converter. Part 2 of this article series will discuss how to get rid of this noise with a low-pass digital/decimation filter.

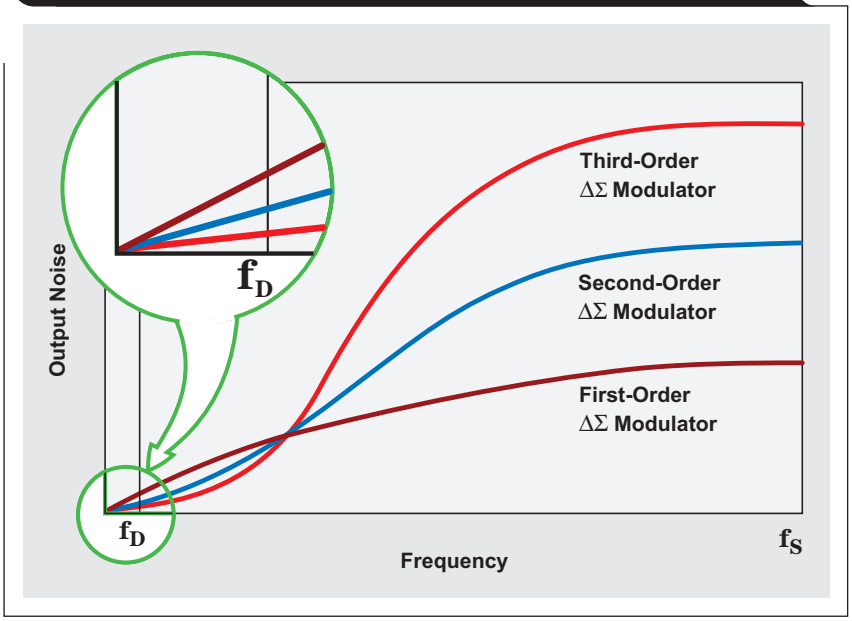
References

1. R. Jacob Baker, *CMOS: Mixed-Signal Circuit Design*, Vol. II. John Wiley & Sons, 2002.
2. Texas Instruments, *Nuts and Bolts of the Delta-Sigma Video Tutorial* [Online]. Available: http://focus.ti.com/docs/training/catalog/events/event.jhtml?sku=WEB408001

Related Web site

dataconverter.ti.com

Figure 6. ΔΣ modulator noise shaping versus modulator order with a sampling frequency of $\mathbf{f_S}$



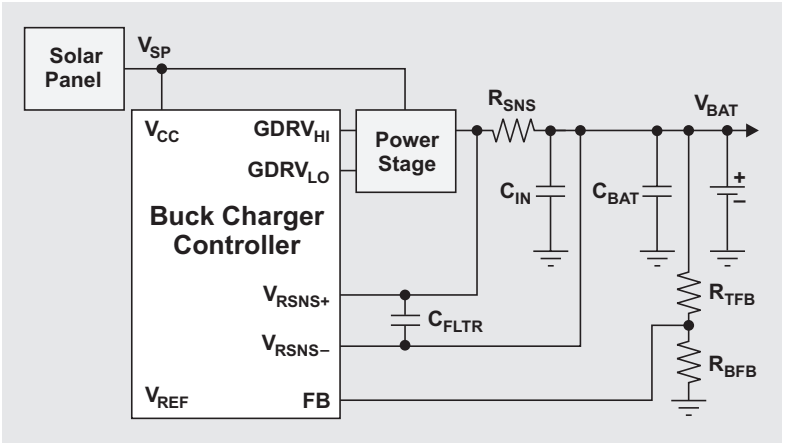
A boost-topology battery charger powered from a solar panel

By Jeff Falin, *Power Applications Engineer,*
and Wang Li, *Battery Power Applications Engineer*

Introduction

Solar charging of batteries has recently become very popular. A solar cell's typical voltage is 0.7 V. Many panels have eight cells in series and are therefore capable of producing 5.6 V at most. This voltage is adequate for charging a single Li-ion battery, such as that used in cell phones, to 4.2 V with a buck or step-down charger. However, using the same panel to charge a multicell Li-ion battery like that used in laptop computers requires a boost or step-up charger. Most chargers currently on the market are based on a buck or step-down topology and therefore require their input voltage to be higher than the battery's fully charged voltage. However, it is possible to modify a buck battery charger into a boost or step-up battery charger. This article identifies the key concerns in implementing such a modification and provides a design example that uses the Texas Instruments (TI) bq24650 solar battery charger.

Figure 1. Block diagram of solar-powered battery charger

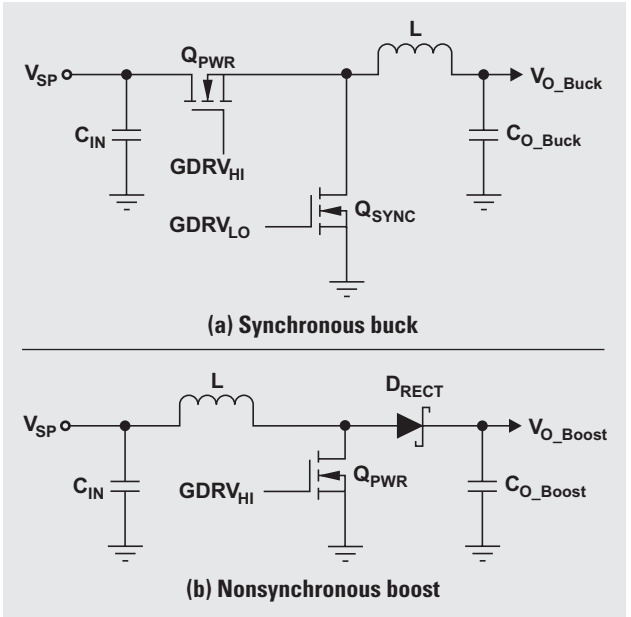


The buck power stage versus the boost power stage

Figure 1 shows a simplified block diagram of a solar-powered battery charger. The charger-controller IC monitors the charging current through a current-sense resistor (R_{SNS}) and the battery voltage (V_{BAT}) through the feedback resistors (R_{TFB} and R_{BFB}). The IC also adjusts the output of the power stage in order to meet the charging parameters. If the input source voltage (V_{SP}) will always be higher than the maximum battery voltage, a buck power stage can be used. If V_{SP} will always be lower than the maximum battery voltage, a boost power stage is required.

Figure 2 shows a synchronous buck power stage and a nonsynchronous boost power stage. Both use the high-side gate drive ($GDRV_{HI}$) to drive the power FET (Q_{PWR}). However, a buck controller cannot be easily configured to drive a synchronous rectifying switch for a boost converter; so Q_{SYNC} is replaced by diode D_{RECT}, and the low-side gate drive ($GDRV_{LO}$) is not used. A buck converter also provides continuous inductor current that is filtered by capacitors C_{IN} and C_{BAT} (see Figure 1) regardless of which switch is on. Unlike the buck converter, the boost converter uses Q_{PWR} only to charge the inductor. During this time the output capacitor must supply the battery-charge current. When D_{RECT} turns on, the now charged inductor provides both the output-capacitor and the battery-charging currents. Therefore, the boost converter's output-voltage ripple

Figure 2. Power-stage topologies



will always be higher than that of a buck converter that uses the same inductor and output capacitance and the same output power. This ripple can cause inaccurate current measurement across the current-sense resistor. Compared to the buck power stage shown in Figure 1, the boost power stage will require a larger sense-voltage filter capacitor (C_{FLTR}) and a larger output capacitance (C_{BAT}).

Limiting precharge current when $V_{BAT} << V_{SP}$

The boost power stage's rectifying diode provides a DC current path from V_{SP} to the battery when the controller is not switching. With a deeply discharged battery, the battery voltage could be below the solar panel's output voltage, causing the charger controller to stop switching and no longer regulate the battery-charging current. Therefore, a current-limiting resistor ($R_{Precharge}$) in series with the diode (see Figure 3) is required to limit the charge current to a lower, precharging current value. Once the battery voltage reaches V_{SP}, the controller begins switching, and $R_{Precharge}$ can be shorted out with a FET (Q_{Short}) to allow the controller to provide higher charge currents. Figure 3 shows how $R_{Precharge}$ can be used with Q_{Short} and a comparator to implement this functionality.

$R_{Precharge}$ is sized to give the maximum recommended precharge current for the battery at the solar panel's maximum power-point voltage (V_{SP_MPP}). Q_{Short} is sized to accommodate the maximum battery voltage ($V_{BAT(max)}$) and the maximum charge current ($I_{CHRG(max)}$). The comparator feedback resistor (R_{HYS}) provides hysteresis. Therefore, resistor dividers are needed on the sensed-voltage inputs to the comparator.

Ensuring operation when $V_{BAT} > V_{SP}$ or when $V_{BAT} < V_{BATSHT}$

A buck charger expects the battery voltage to always be less than the charger's input voltage. In fact, many chargers have a feature that puts the charger into sleep mode if V_{BAT} is greater than V_{SP}. Alternatively, if V_{BAT} falls below a certain threshold (V_{BATSHT}), the IC may assume the battery is shorted and enter protection mode. If the voltages at the current-sense pins (V_{RSNS+} and V_{RSNS-}) are used to determine the battery's state, the sensed voltages will need to be level shifted to avoid a false detection of a shorted output. Figure 4 shows how to use an instrumentation amplifier, configured as a current-shunt monitor, to level shift the current information sensed across R_{SNS}. This circuit lowers the DC set point of the sensed voltages enough that the IC will not enter sleep mode but keeps the voltages high enough that the IC does not enter short-circuit-protection mode. If the charger does not have its own reference voltage (V_{REF}), an external reference IC can be used.

Figure 3. Precharge circuitry

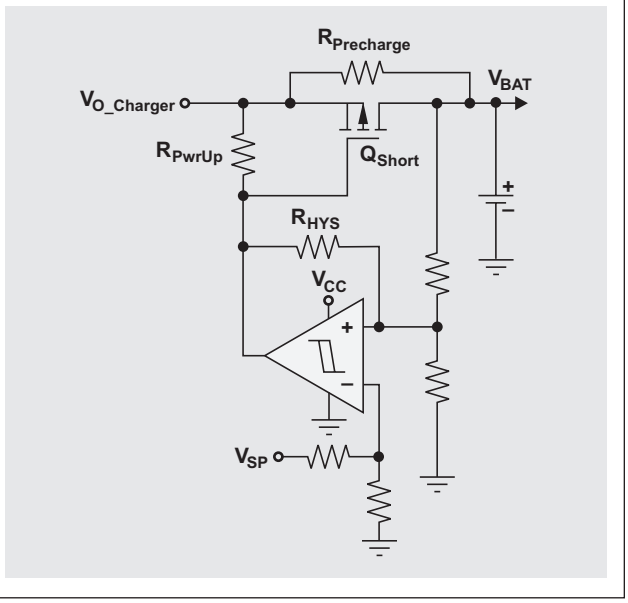
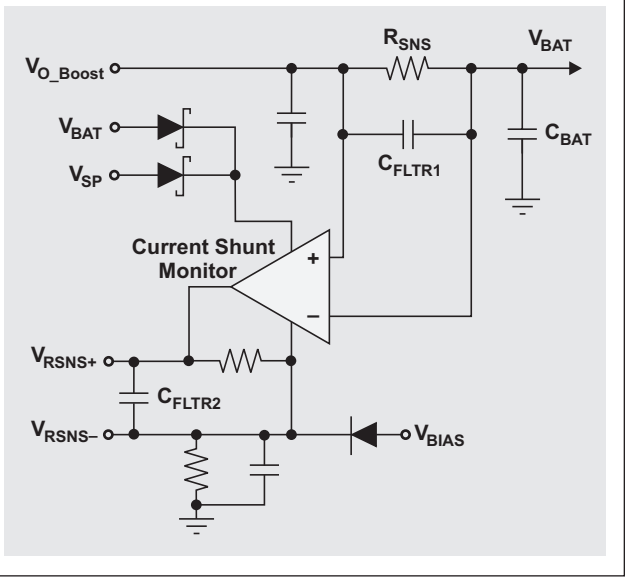


Figure 4. Current-sensing circuit with level shifting



Computing the maximum charge current

A boost charger's maximum charge current is a function of its available input power. A simple way to estimate the maximum charge current is to first estimate the input-to-output efficiency, $P_{OUT}/P_{IN} = \eta_{est}$, where η_{est} is an estimate of the boost charger's efficiency in similar operating conditions. The following equation can then be used to estimate the maximum charge current at a specific battery voltage:

$$I_{CHRG(max)} = \frac{V_{SP\_MPP} \times I_{SP\_MPP} \times \eta_{est}}{V_{BAT}},$$

where V_{SP_MPP} is the solar panel's maximum power-point voltage, and I_{SP_MPP} is the solar panel's maximum power-point current.

R_{SNS} should be sized to provide $I_{CHRG(max)}$. Q_{PWR} has a voltage rating slightly higher than $V_{SP(max)}$, and Q_{PWR} and L1 have current ratings equal to at least I_{SP_MPP}. The charger's control circuitry that manages input voltage and current will adjust the charge current to keep the charger operating at the solar panel's maximum power point. Charge controllers such as the bq24650 perform the same function with maximum-power-point tracking (MPPT).

Design example using the bq24650

Table 1 maps the functional pin names from Figure 1 to the corresponding bq24650 pin names in Figure 5. Figure 5 shows TI's bq24650 charger controller configured to charge a 12.6-V, 3-cell Li-ion battery from a 5-V solar panel. The maximum charge current is limited to 1.2 A. The power n-channel FET (Q1) and rectifying diode (D1) are sized by using standard design guidelines for boost converters. The inductor (L1) and output capacitors (C3 and C4) are sized to reduce inductor-current ripple and the resulting output-voltage ripple. R18 is used to slow down the fast turn-on of Q1. Also, the controller's PH pin is grounded to help provide the boosted output voltage. To prevent the output of the current-shunt monitor (U2) from loading the SRP pin, a unity-gain buffer (U3) is necessary.

Table 1. Cross-reference for controller pin names

FIGURE 1 CONTROLLER PIN NAME	bq24650 PIN NAME
$GDRV_{HI}$	HIDRV
$GDRV_{LO}$	LODRV
V_{RSNS+}	SRP
V_{RSNS-}	SRN
FB	VFB

Figure 5. The bq24650 configured as a boost charger

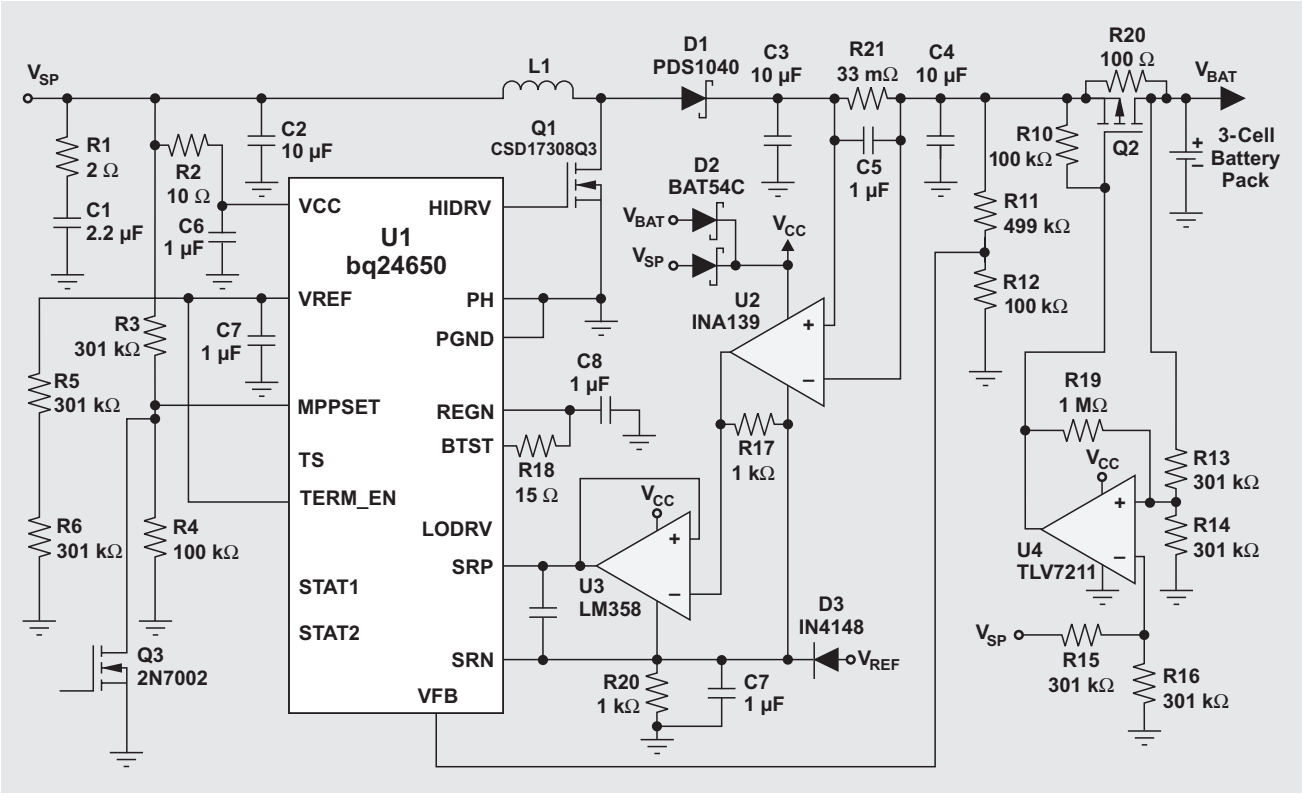
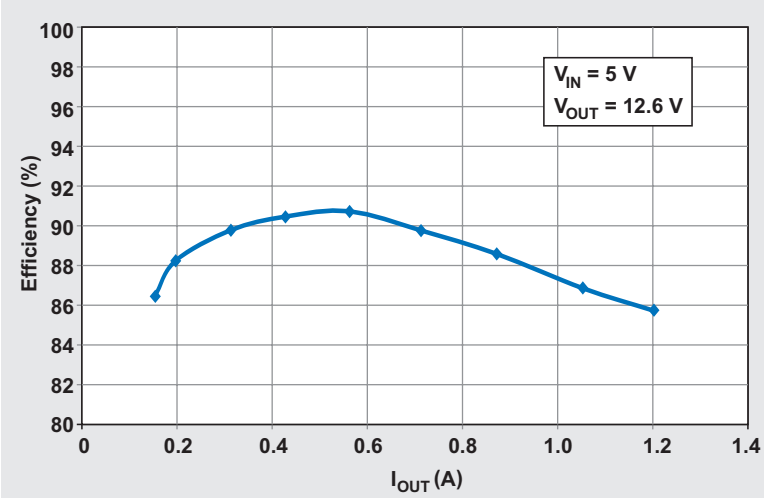


Figure 6 shows the efficiency of the charger in Figure 5. Although the bq24650 is internally compensated as a buck charger, its small-signal control loop is stable over a wide operating range when the IC is operating as a boost charger (see Figure 7). When using the bq24650 with different power-stage inductors and capacitors, the designer is responsible for confirming loop stability.

Figure 6. Efficiency of boost charger in Figure 5



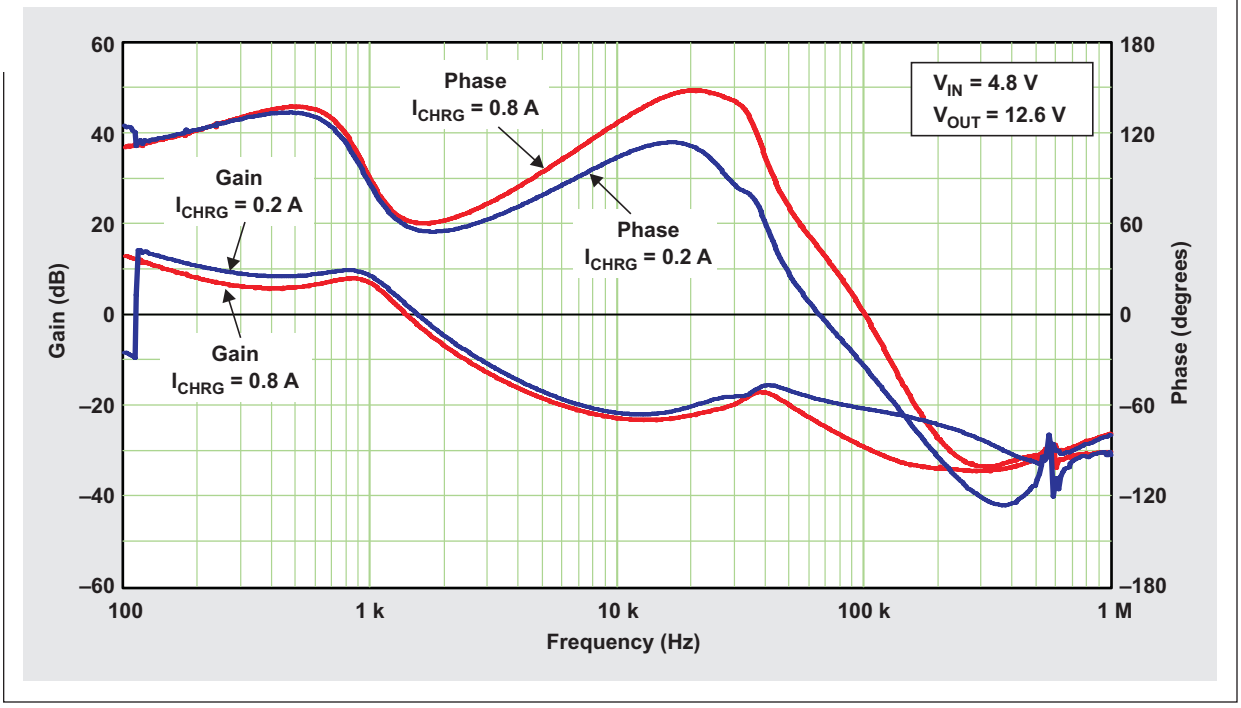
Conclusion

The demand for step-up battery chargers is growing, especially as the demand for charging from solar panels grows. Following the guidelines presented in this article, a designer can convert the bq24650 buck charger into a boost charger. When converting a different buck charger into a boost charger, the designer is responsible for understanding how that charger operates in order to determine which additional circuitry is necessary as well as to confirm stable operation.

Related Web sites

power.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with bq24650, CSD17308Q3, INA139, LM358, or TLV7211

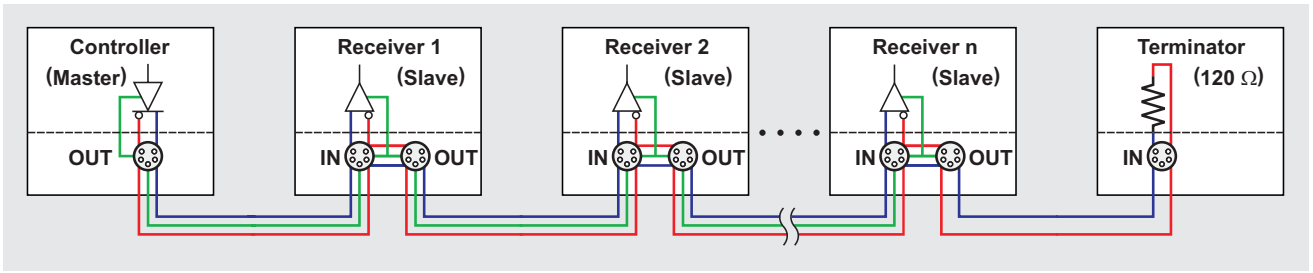
Figure 7. Bode plot of gain and phase with an open feedback loop



Isolated RS-485 transceivers support DMX512 stage lighting and special-effects applications

By Thomas Kugelstadt
Senior Applications Engineer

Figure 1. Daisy-chained topology of DMX512 network



Stage lighting and special-effects applications in modern theaters, opera houses, sports arenas, and concert halls utilize complex data-transmission networks. These networks, often reaching distances of up to 1200 m, provide communication between several hundreds of network nodes that control dimmers, moving lights, fog machines, and other special-effects equipment.

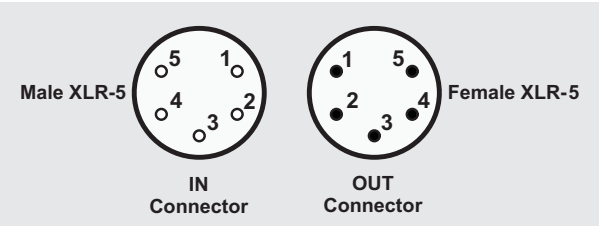
The first standard ensuring reliable intercommunication for these applications was known as DMX512 and was originally developed in 1986 by the United States Institute for Theatre Technology (USITT) Engineering Commission. In 1998, the Entertainment Services and Technology Association (ESTA) took over maintenance of this standard. A revised version was approved by the American National Standards Institute (ANSI) in 2004. The standard was revised again in 2008 and is now officially known as ANSI E1.11-2008, entitled *Entertainment Technology—USITT DMX512-A—Asynchronous Serial Digital Data Transmission Standard for Controlling Lighting Equipment and Accessories,* or DMX512-A in short.

Topology

A DMX512 network utilizes a multidrop topology similar to RS-422, where a single controller (master node) sends repetitive control data to multiple receivers (slave nodes). Within the network, all nodes are connected through daisy-chaining; that is, each slave node has an IN connector as well as an OUT connector. The controller, which has only an OUT connector, connects to the IN connector of the first slave. The OUT connector of the first slave connects to the IN connector of the next slave, and so on (see Figure 1). The OUT connector of the last slave in the chain connects to a 100-Ω or 120-Ω terminator plug.

So that the ingoing and outgoing data signals of a DMX512 port can be distinguished, the IN connectors are male XLR-5, and the OUT connectors are female XLR-5 (see Figure 2).

Figure 2. DMX512 standard connectors



Protocol

A DMX512 controller transmits packets of asynchronous serial data at 250 kbps (see Figure 3). A data packet starts with a break (logic low) and is followed by a mark (logic high), a sequence known as mark-after-break (MAB). Following MAB is a time slot consisting of a start bit, eight data bits, and two stop bits. The entire packet consists of a maximum of 513 time slots, 512 of which are actual data slots. The first slot, known as the start code, specifies the type of data in the packet.

Physical layer

The DMX512-A standard specifies EIA-485 as the network's physical layer, thus allowing for a maximum common-mode loading of up to 32 unit loads and a maximum bus length of 1200 m. Network wiring typically consists of twisted-pair cable with a characteristic impedance of either 120 Ω for RS-485 cable or 100 Ω for CAT5 cable, with a termination resistor of equal impedance at the end of the bus.

In addition to EIA-485, DMX512-A recommends earth-grounded transmitter ports and isolated receiver ports to avoid the formation of disruptive ground loops (see Figure 4).

Furthermore, DMX512-A makes provisions for enhanced-functionality (EF) topologies that enable the use of responders. The responders are receiving nodes that can return status information to the controller. The two EF topologies most often applied are EF1 and EF2. EF1 provides a half-duplex link between the DMX512 network's controller and responders. EF2 provides a full-duplex link between the network nodes. In both cases, the I/O port of responders, falling under the category of receiving devices, must have isolated transmit and receive ports.

Full-duplex RS-485 transceivers are the devices best suited for these applications because simple rewiring of the A,B and Y,Z bus terminals can accommodate not only the receiver-only configuration in standard DMX512 systems but also the half- and full-duplex configurations used respectively in EF1 and EF2 systems.

Legacy receiver designs often used a non-isolated transceiver in combination with opto-isolators. However, the mold compound in these isolators, basically representing the dielectric between the light-emitting diode and the receiving photo transistor, absorbed moisture over time, reducing the long-term stability of the isolation barrier.

A further drawback of legacy designs was the use of an isolated power supply that was required to provide the

Figure 3. DMX512 packet timing

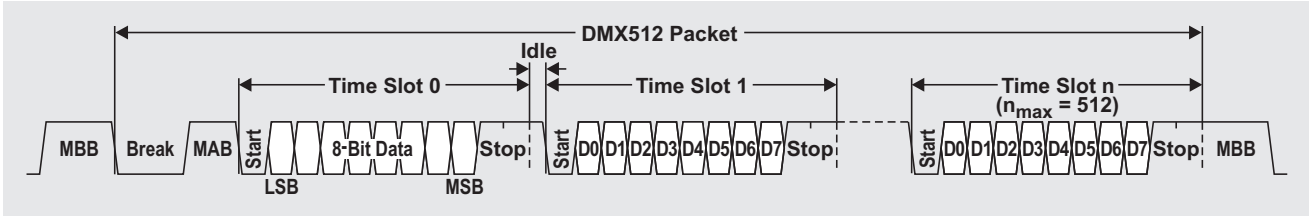
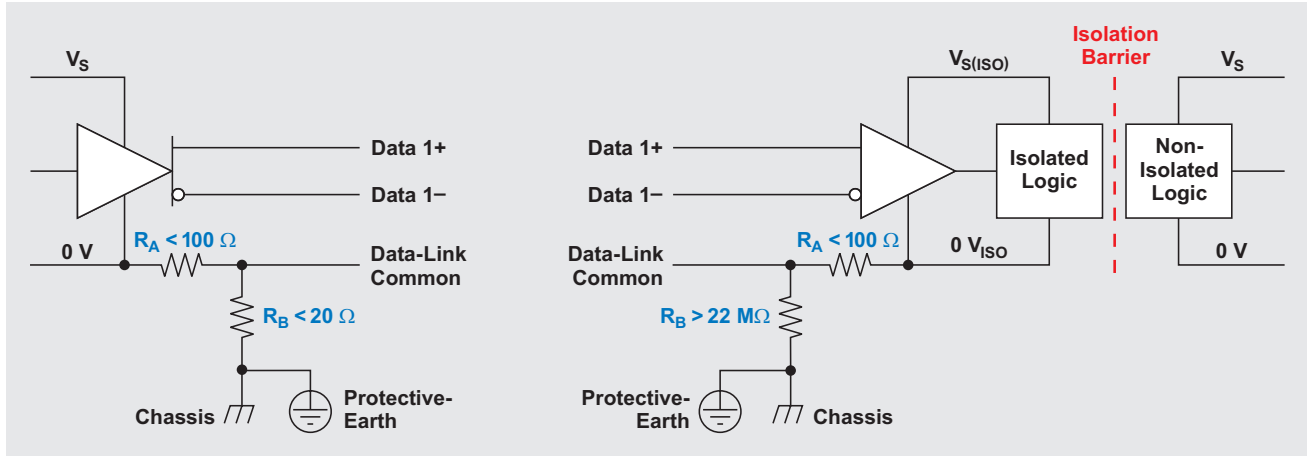


Figure 4. Ground-referenced transmitter and isolated receiver



supply voltage across the isolation barrier. Bulky DC/DC-converter modules were often applied whose cost exceeded that of all the signal-path components—including the transceiver, isolators, and UARTs—by up to 300%.

With the recent introduction of digital capacitive-isolation technology, the issue of long-term reliability has been solved. The isolation barrier, consisting of small, high-voltage capacitors in the range of 120 fF, uses silicon dioxide (SiO_2) as the isolation dielectric. SiO_2 is one of the hardest isolation materials with little moisture absorption, thus providing extremely high, long-term reliability and long life.

Furthermore, the new Texas Instruments (TI) family of isolated RS-485 transceivers possesses integrated transformer drivers that drastically simplify the design of the isolated power supply. The on-chip transformer driver is basically a free-running oscillator with a typical frequency, f_{OSC}, of 400 kHz. This oscillator drives two powerful output transistors, which in turn drive an external center-tapped transformer in a push-pull configuration. The relative high frequency allows for the use of small transformers that enable an overall small-form-factor design.

Figure 5 shows a complete solution for a responder circuit that complies with DMX512-A. As an isolated, 3.3-V, low-power transceiver, TI's ISO35T provides RS-485-compliant bus signals with a 1.5-V minimum and a 2-V typical differential output voltage at full differential and common-mode loading. The device's maximum data rate of 1 Mbps satisfies the 250-kbps requirement of DMX512-A, and the longer rise and fall times of 200 ns ensure low electromagnetic interference.

Here the incoming control data from the DMX512 bus is signal-conditioned by the input comparator and sent across the isolation barrier towards the receiver output. Output data at the R terminal enters the UART interface of TI's MSP430F2132, a low-power microcontroller. The microcontroller converts the UART data into a synchronous, high-speed serial data stream to feed an eight-channel, high-voltage-output digital-to-analog converter (DAC). TI's DAC7718 allows for bipolar outputs of up to ±16.5 V and unipolar outputs of up to 33 V.

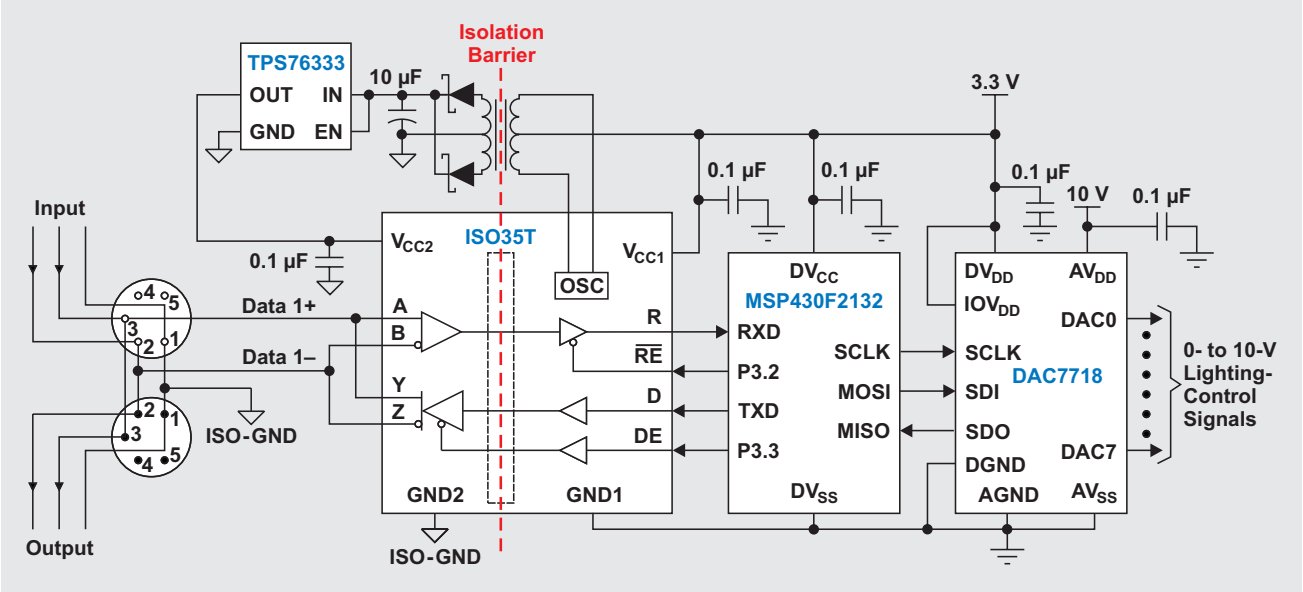
Because stage special-effects equipment uses unipolar control voltages in the range of 0 to 10 V, the DAC7718 is an ideal analog interface for this type of application, enabling the control of up to eight light dimmers per network node.

The remaining node circuitry, including the DAC, the microcontroller, and the transceiver, operates from a single 3.3-V supply. The 3.3-V low-dropout regulator (TI's TPS76333) on the isolated side provides up to 150 mA of output current along with overcurrent limiting and thermal protection.

Related Web sites

interface.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with DAC7718, ISO35T, ISO1176T, ISO3086T, MSP430F2132, or TPS76333

Figure 5. Isolated DMX512 responder node



Industrial data-acquisition interfaces with digital isolators

By Thomas Kugelstadt
Senior Applications Engineer

Galvanic isolation has become the mantra in the industrial engineering community as legal regulations call for its implementation in industrial system designs. Galvanic isolation allows for the exchange of information and power between two communicating points while preventing actual current flow at the same time.

Galvanic isolation has two main benefits. First, it protects people and equipment from potentially dangerous current and voltage surges. Second, it prevents the unintentional design of ground loops, whose noise would otherwise interfere with signals from data links and other interconnections.

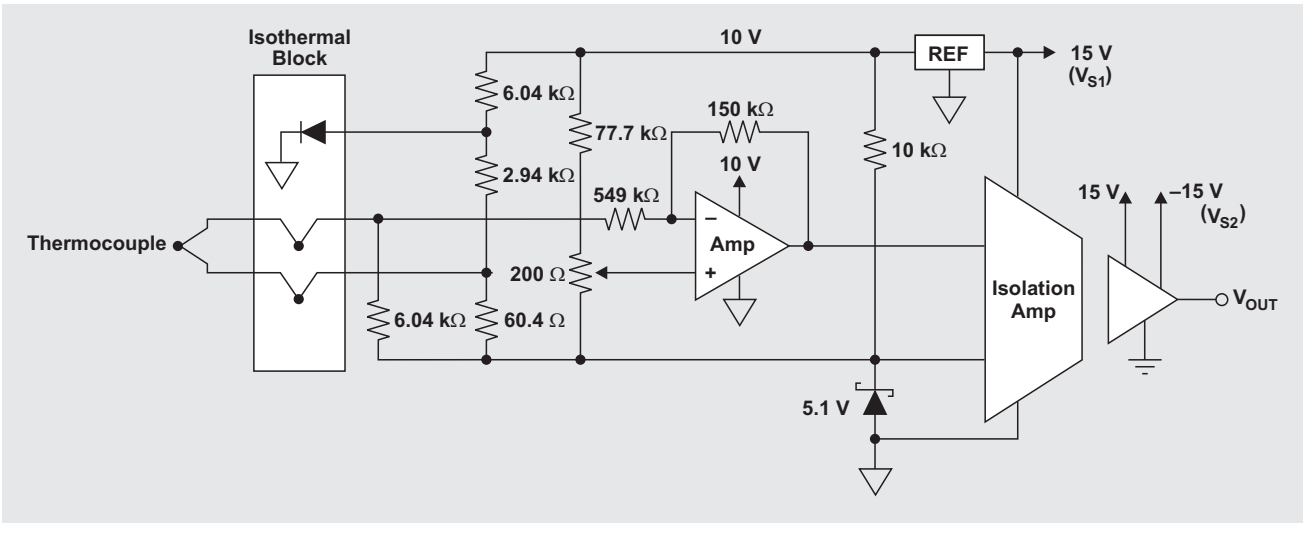
Legacy designs of analog I/O, instrumentation, motion-control, and other sensor interfaces often used single-channel isolation amplifiers to separate the sensor circuitry in the harsh environment of the factory floor from the signal-processing stage in the noise-free control-room environment. Advancements in technology and design have led to new space- and power-saving digital isolators whose multichannel capability permits equipment designs with smaller form factors. This article explains both types of isolators and their operational principles. Application examples are also provided.

Legacy isolation designs

A classic example of a legacy design using an isolation amplifier is the single-channel, isolated temperature-measurement circuit in Figure 1. Here a thermocouple converts the measured temperature into a low-voltage DC output. The following resistor-diode network conditions the input signal by providing operating-point biasing, compensating for temperature drift, and boosting the input sufficiently to match the input-voltage range of the isolation amplifier.

The isolation amplifier is a precision amplifier that uses duty-cycle modulation (DCM) to transmit the input signal across a capacitive isolation barrier. DCM ensures immunity to varying barrier characteristics while maintaining signal integrity. This results in high reliability and good common-mode transient immunity.

Figure 1. Isolated temperature measurement



Inside the device, the input and output sections are galvanically isolated by two matched capacitors (see Figure 2). The input section converts the input voltage, V_{IN}, into an input current, I_{IN}, via an input resistor, R_{IN}. Configured as an integrator, amplifier A1 integrates the difference between I_{IN} and the current source until the input threshold of the following comparator is exceeded. Together, the comparator and the sense amplifier, AS1, force the current source to switch at the frequency of the internal 500-kHz oscillator. The resulting drive signal into the capacitive barrier is a complementary, duty-cycle-modulated square wave.

The output section demodulates the signal from the isolation barrier through a balanced low-pass filtering. Sense amplifier AS2 detects signal transitions across the barrier and drives a switched current source into integrator A2. This stage balances the duty-cycle-modulated current against the feedback current through R_F, thus yielding an average value of V_{OUT} equal to V_{IN}. The sample-and-hold (S/H) amplifiers in the feedback loop remove undesired voltage ripples inherent in the demodulation process.

Isolation amplifiers, while highly accurate and reliable, have several technological drawbacks. These amplifiers possess a low input-signal bandwidth no greater than 50 kHz. Their requirement for a minimum power supply of ±4 V does not support modern low-voltage designs. Their expensive manufacturing process requires the separate fabrication of input and output chips, laser trimming for precise circuit matching, and final assembly of both chips together with the isolation capacitors into one package.

Modern isolation designs

Modern data-acquisition designs use analog-to-digital converters (ADCs) whose inputs are multiplexed into a single-channel conditioning path (see Figure 3). A programmable gain amplifier (PGA) boosts the weak input

Figure 2. Inside the isolation amplifier

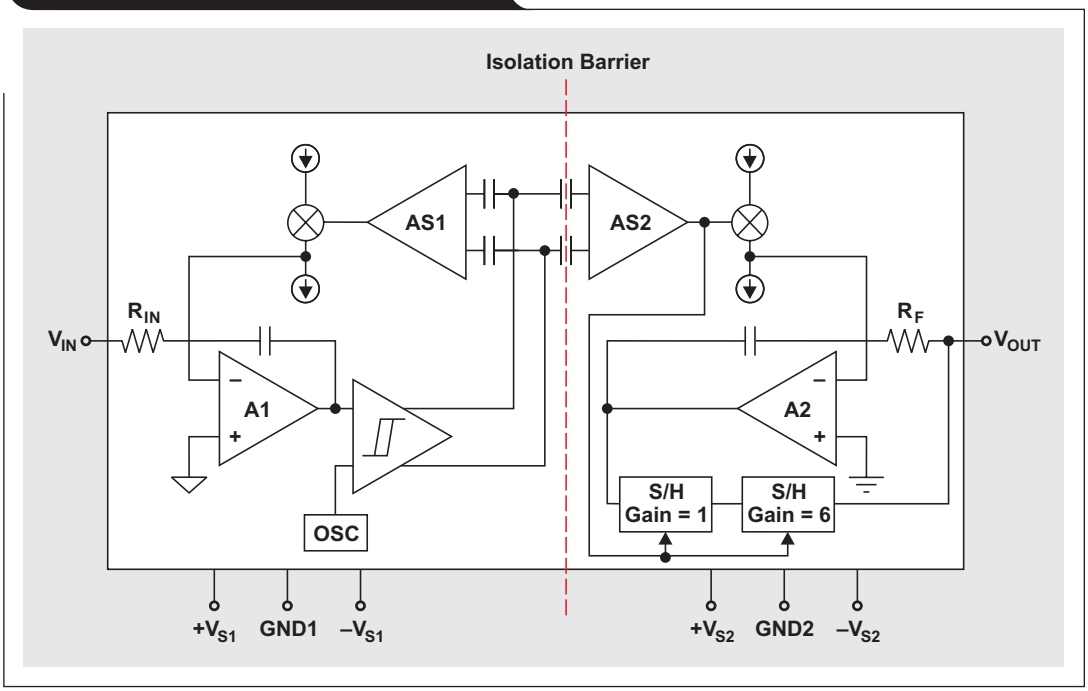
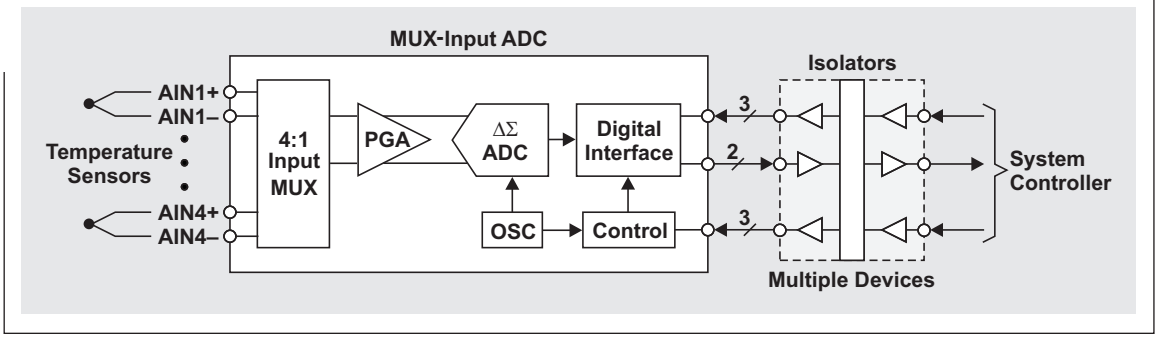


Figure 3. Isolated data-acquisition system



signal, and the converter applies delta-sigma modulation to the signal to convert it to a digital data stream. The digital-conversion results are then transmitted across the digital isolator to a system controller for further processing in the digital domain.

Digital isolators can possess various isolation barriers that use magnetic, optoelectric, or capacitive isolation technologies. The isolator in Figure 4 is based on a capacitive isolation-barrier technique. The device consists of two parallel data channels, a high-speed AC channel with a bandwidth ranging from 100 kbps up to 150 Mbps, and a low-speed DC channel covering the range from 100 kbps down to DC.

Inside the isolator, a single-ended input signal entering the AC channel is converted into a balanced signal through inverting and non-inverting input buffers. RC networks then differentiate the signal into transients, and comparators convert the transients into short pulses. A final flip-flop then converts these pulses into an output signal that is identical in phase and shape to the original input signal.

A decision logic (DCL) in the form of a watchdog timer measures the durations between signal transients. If the duration between two consecutive transients exceeds the maximum time window (as in the case of a low-frequency signal), the output multiplexer is switched from the high-speed AC to the low-speed DC channel.

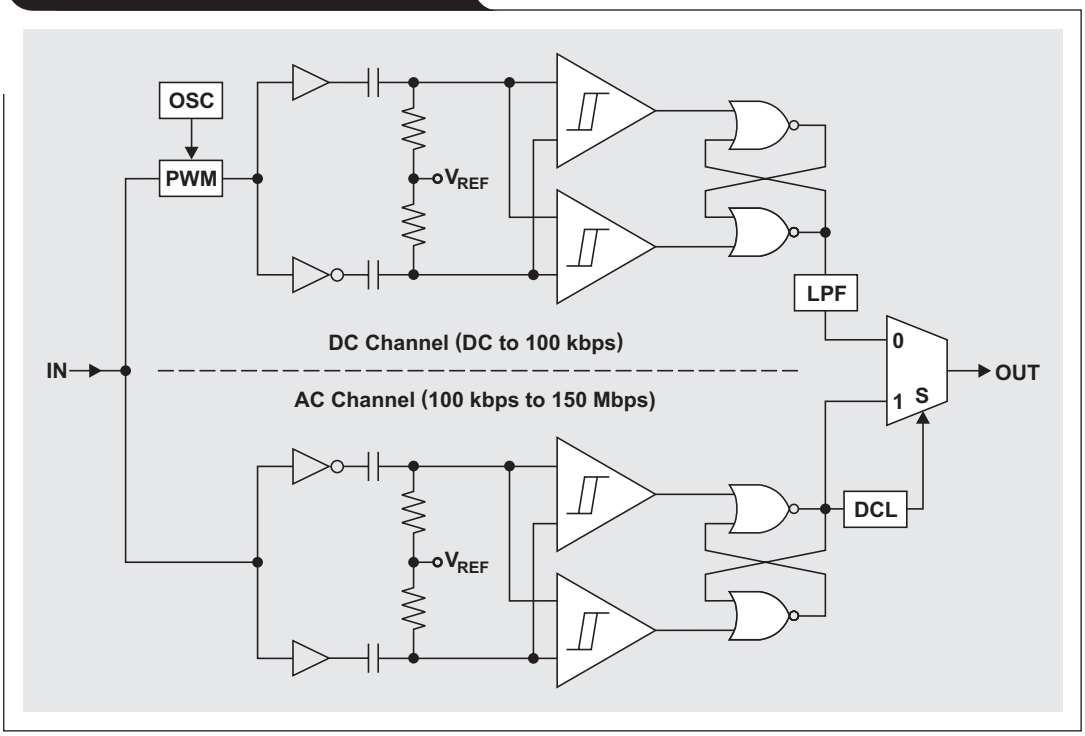
Because low-speed signals lack sufficient transitions to easily cross the tiny isolation capacitors, the carrier frequency of an internal oscillator is applied to them via a pulse-width modulator (PWM). Past the barrier, a low-pass filter (LPF) removes the high-frequency content from the actual data prior to passing it on to the output multiplexer.

Industrial applications

The two most common applications for industrial data-acquisition systems are in process control and factory automation. Process-control systems typically detect or measure multiple physical quantities, such as temperature and pressure, within one system, while factory automation usually monitors one physical quantity across multiple systems. Consequently, the configuration of data converters used in each application differs significantly. Process-control systems addressing a wide range of sensor and transducer types require a wide range of parametric settings for gain, sampling rate, measurement repetition, and impedance buffering. In strong contrast, factory automation often gets along with monitoring multiple sensors of the same type, thus requiring only a minimum number of parametric settings.

Because the number of parametric settings impacts the isolation efforts and the associated costs of the digital-interface design, it is important to distinguish between

Figure 4. Digital capacitive isolator



process control and factory automation. Two typical designs of a data-acquisition system are shown in Figures 5 and 6 to illustrate the difference.

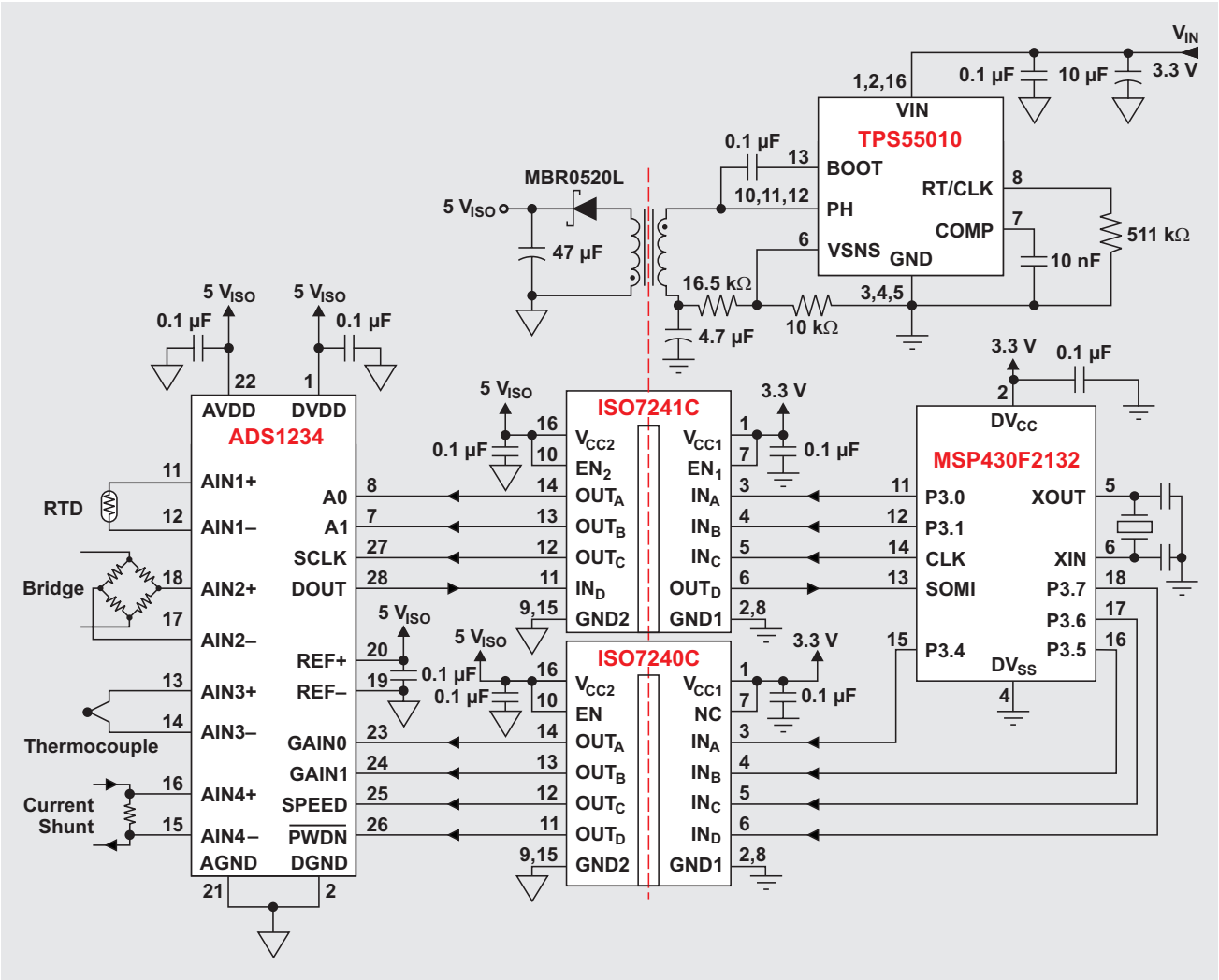
In the Figure 5 configuration, a variety of sensors measure different quantities such as temperature, pressure, and current. Various gain settings maximize the input dynamic range of the ADC for each sensor. Switching between sampling rates might be necessary to match the rate of change at certain input channels. An optional power-down feature preserves ADC power when measurements are not performed. This high versatility necessitates up to eight isolated control channels.

By contrast, in the Figure 6 configuration, four thermocouples of the same type measure the temperatures of different types of equipment continuously. While this design uses the same ADC as in Figure 5, the uniform sensor characteristics allow the settings for gain and sample rate to be fixed and the power-down feature to be disabled. This system configuration drastically reduces isolation requirements because there are only four lines for data and control.

Conclusion

Isolation amplifiers are out, and digital isolators are in. To save design time and board space and to keep the cost of materials down, it is imperative to understand the system requirements before deciding what type of isolator to use.

Figure 5. Isolated data-acquisition system for process control



References

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Document Title **TI Lit. #**

1. Thomas Kugelstadt, "Designing with digital isolators," *Analog Applications Journal* (2Q 2009) slyt335
2. Thomas Kugelstadt, "Magnetic-field immunity of digital capacitive isolators," *Analog Applications Journal* (3Q 2010) slyt381

Related Web sites

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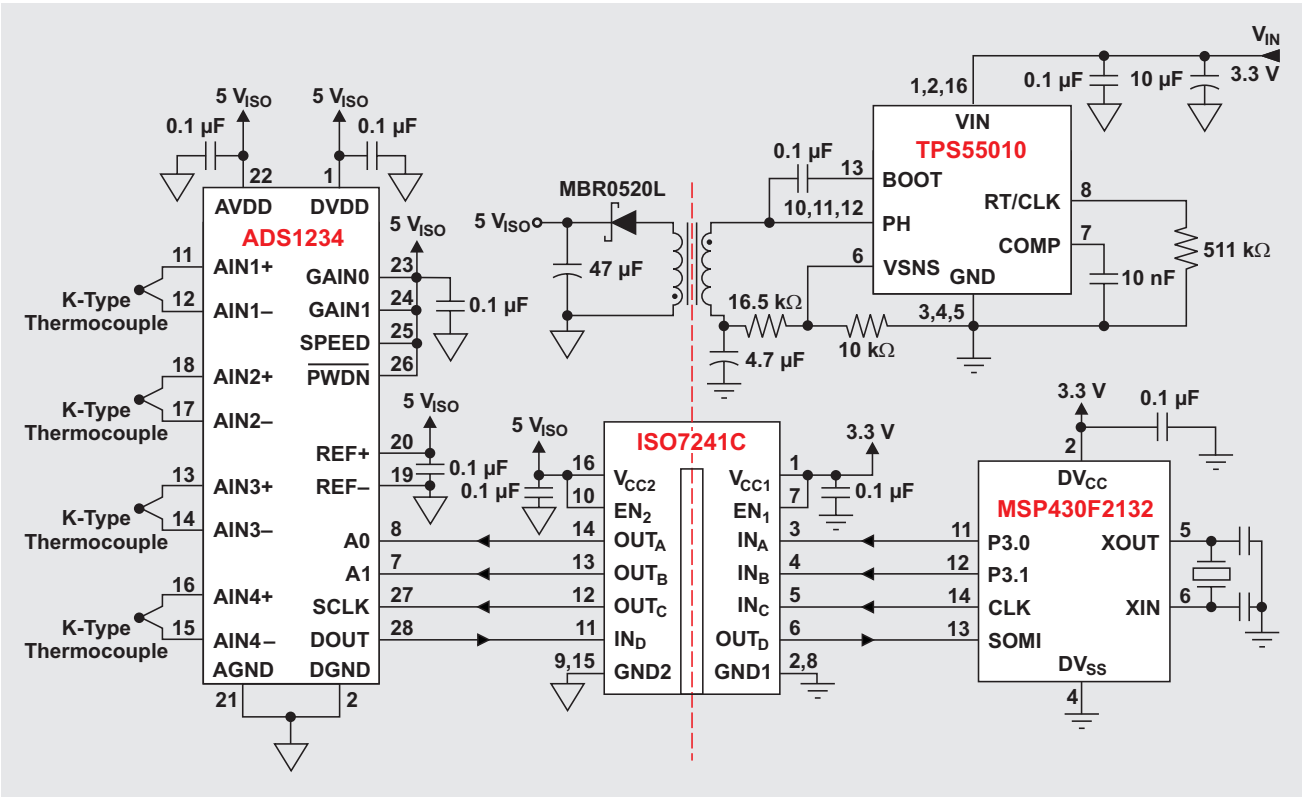
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with ADS1234, ISO7240C, ISO7241C, MSP430F2132, or TPS55010

Figure 6. Isolated data-acquisition system in factory automation



Converting single-ended video to differential video in single-supply systems

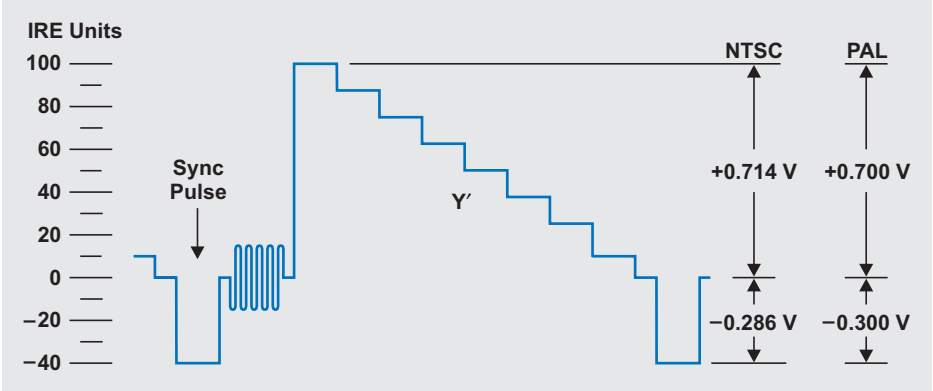
By Jim Karki
Member, Technical Staff, High-Performance Analog

Introduction

Video signals are commonly encoded, decoded, and processed as single-ended, but it is often desirable to convert them to differential for transmission over cables. A good example is a security system where cameras are placed in various locations and the video feeds are routed back to a central location for observation and storage.

Because of its inherent resistance to noise, differential transmission has been used for many years in telephone lines and professional audio. Assuming noise is coupled equally into the differential transmission line(s), it shows up at the receiver as a common-mode signal that is rejected.

Figure 1. SD composite video baseband signal (CVBS) showing grayscale



With single-supply devices becoming more and more common these days, it is nice to design the line-drive circuit to be single-supply as well. In single-supply systems, the signal levels are shifted to fit within the supply voltage, and the bias levels need to be accounted for so as not to cause unwanted offsets in the output. These tasks are aside from the normal ones like setting gains, choosing the type of line termination, and allowing for adequate bandwidth and slew rate.

Single-ended-output operational amplifiers or fully differential amplifiers (FDAs) can be used to convert single-ended video signals to differential. The purpose of this article is to show how to use an FDA to convert single-ended video signals to differential to drive a Cat 5 cable with double termination in a single-supply system. It is assumed that the reader is familiar with FDA concepts and use. For more information on FDA fundamentals, please see Reference 1.

Typical video parameters

Figure 1 shows a composite video baseband signal (CVBS) showing grayscale that is often used with standard-definition (SD) video. SD video characteristics typically follow the analog-signal standards established for the NTSC or PAL television broadcast systems. The total peak-to-peak output voltage is specified to be 140 IRE = 1 V_{PP}, with only the sync and luminance (Y′) where the sync pulse is negative. With chrominance information added, a fully modulated composite video signal is about 1.23 V_{PP}. To support the negative pulse, split-supply ($\pm V_S$) operational amplifiers can be used, or AC coupling where the DC levels are restored at the receiver. Using a split supply or AC coupling requires more components and is more costly. DC coupling can lower cost, but moving to DC-coupled signals that support a single supply requires level shifting the signal. For example, the data sheet of the Texas Instruments (TI) TMS320DM368 video processor specifies video-buffer output voltages ranging from 0.35 V to 1.35 V with a 75-Ω load. In this way, a 1-V_{PP} video signal can be supported with a shift in bias level and is acceptable in consumer video.

Other higher-definition video formats like enhanced-definition (ED) and high-definition (HD) do not encode as much different information into one line as SD. They use multiple lines with signals of varying duration and transition speed depending on the video content and specification.

So video signals are pulse-oriented by nature, and amplifiers and transmission media need to have excellent pulse characteristics to properly reproduce them. Because of this, it is standard practice to use double termination of the transmission line. In double termination, the amplifier driving the line is designed to have the same output impedance as the characteristic line impedance, and the receiver is designed to have the same input impedance as the characteristic line impedance. With this configuration, reflections from pulse edges are minimized and the best signal integrity is maintained. Since operational amplifiers are ideally voltage sources, their outputs have very low impedance (near 0 Ω), and matching the output impedance

is easily done by adding a series output resistor. This output resistor, in conjunction with the input impedance of the receiver, gives a 6-dB loss that is inherent in double termination. To make up for the loss, it is common practice for video buffers to be designed to have a gain of 2 V/V (6 dB) so the overall gain from video source to load is 1 V/V (0 dB).

Category 5 (Cat 5) cabling is very common and used widely for computer local-area networks (LANs), but it is also used to carry other signals such as telephone, video, and audio. Most Cat 5 cables are low-cost and unshielded and use a twisted-pair design with differential signaling for noise rejection. The nominal characteristic impedance of Cat 5 cable is 100 Ω.

Circuit analysis

Proposed circuit #1

A first proposed circuit for converting a single-ended video signal from a single-supply video source like the TMS320DM368 to drive a differential line might be as shown in Figure 2. The function of the various elements is as follows:

V_{S+} is the power supply to the amplifier; and the negative supply input, V_{S-}, is grounded.

V_{IN} is the input from the TMS320DM368 video source, ranging from 0.35 V to 1.35 V.

R_G and R_F are the main gain-setting resistors for the amplifier. For a gain of 2 V/V, $R_F = 2R_G$.

V_{OUT+} and V_{OUT-} are the differential output signals from the FDA. They are 180° out of phase and are level shifted to the common-mode output voltage, V_{OCM}.

The two R_O resistors are selected to match the characteristic line impedance, Z_O. For $Z_O = 100\ \Omega$, $R_O = 50\ \Omega$.

R_L is the resistor selected to match Z_O. For $Z_O = 100\ \Omega$, $R_L = 100\ \Omega$.

At first look the circuit in Figure 2 might appear to be acceptable, but closer inspection shows it needs some work. This circuit does not provide a 75-Ω load for the TMS320DM368 video buffer, so the buffer output voltages will not be correct. When driven from a video source like the TMS320DM368, whose video-buffer output range is 0.35 V to 1.35 V, the output signals from this circuit will have a differential offset equal to the common-mode voltage of the video signal times the gain and will be level shifted to V_{OCM}. Calculations show that the Figure 2 circuit output will have a 1.7-V differential offset. To correct the offset, R_G on the undriven side of the FDA must be split and biased to make a Thevenin equivalent of R_G on the driven side of the FDA. The Thevenin-equivalent input voltage equals the common-mode voltage from the video source; i.e., $V_{TH} = V_{IN\_CM}$.

Figure 2. Proposed circuit #1 for converting single-ended video signals to differential

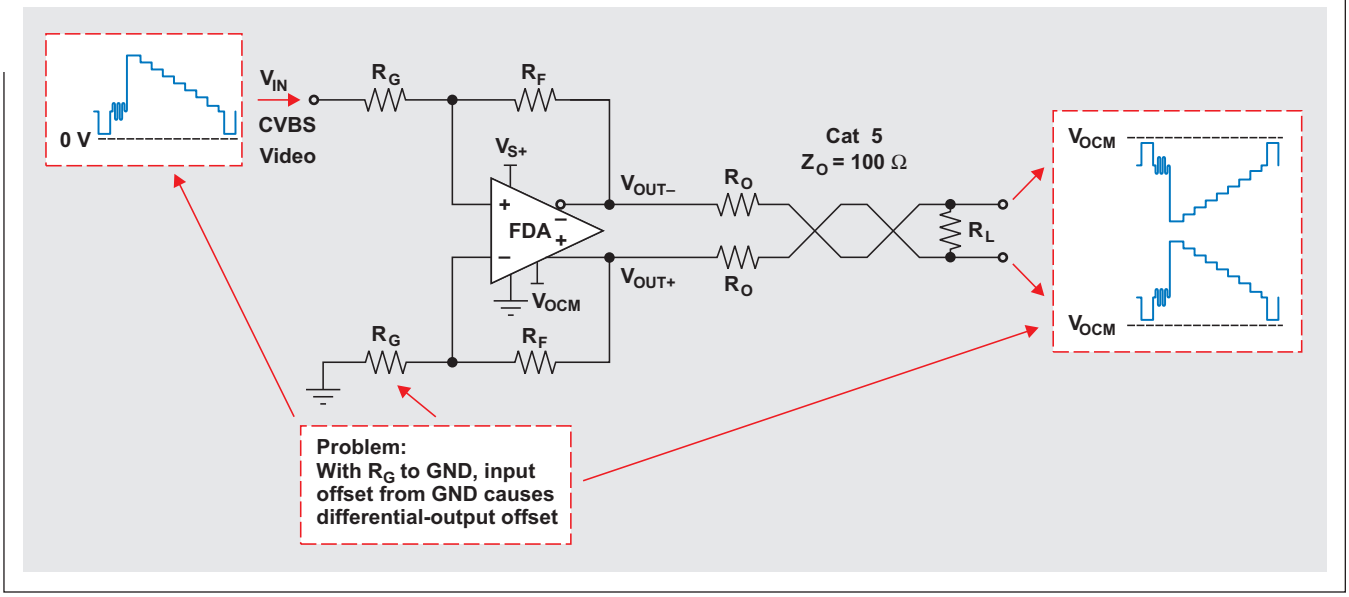
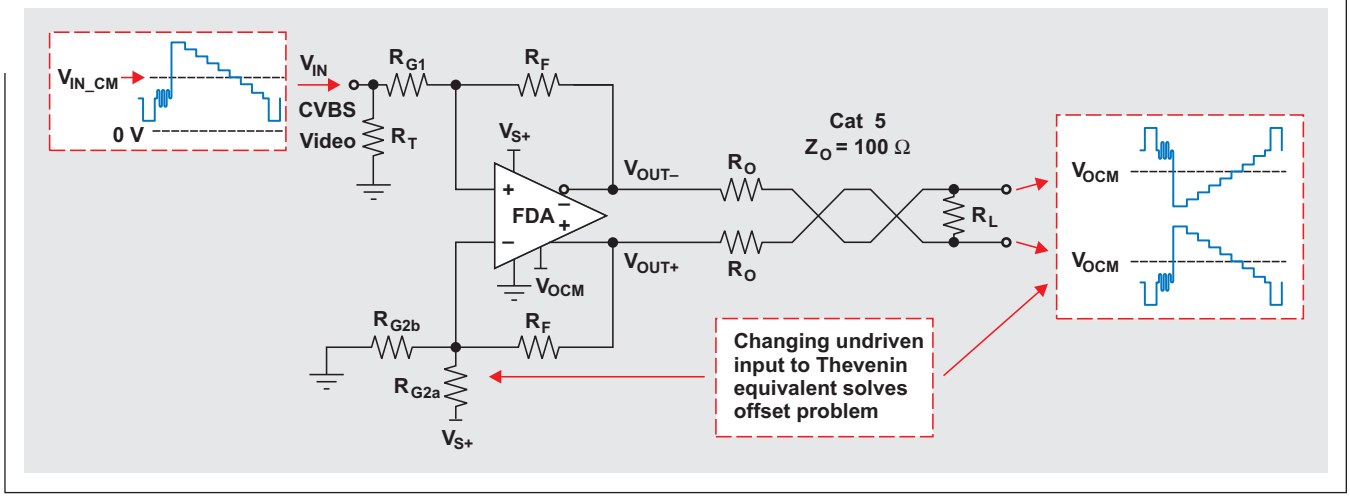


Figure 3. Proposed circuit #2 with corrected differential-output offset



Proposed circuit #2

A second proposed circuit for converting a single-ended video signal from a single-supply video source like the TMS320DM368 to drive a differential line is shown in Figure 3. In this version, the circuit is improved to correct the offset in circuit #1 by adding R_T for a 75-Ω input termination and changing R_G on the undriven side of the FDA to be the Thevenin equivalent of the driven side, with $V_{TH} = V_{IN\_CM}$. The function of the components is the same as before, with R_G on the undriven side replaced by R_{G2a} and R_{G2b}. An analysis and a simulation of circuit #2 follow.

Analysis of circuit #2

For analysis of circuit #2 in Figure 3, it is assumed that the FDA is an ideal amplifier with infinite gain and no offset. One goal of the design is to make the undriven side of the FDA a Thevenin equivalent of the driven side. This is working backwards from the normal way to use the theorem, converting the simpler form of the driven side to a more complex circuit on the undriven side.

The first step is to set the parallel sum, $R_{G2a} \parallel R_{G2b} = R_{TH}$, where $R_{TH} = R_{G1} + R_S \parallel R_T$. This can be written in equation form as

$$R_{TH} = R_{G1} + \frac{R_S \times R_T}{R_S + R_T}. \quad (1)$$

R_S equals 75 Ω and is the output impedance of the TMS320DM368 video buffer. R_T equals 82.5 Ω and is the resistance required to make the input impedance of the amplifier circuit equal 75 Ω. For detailed information on how to select R_T and R_{G1} for proper termination and gain, see Reference 2.

The second step is to set $V_{TH} = V_{IN\_CM}$, where

$$V_{IN\_CM} = \frac{V_{IN(min)} + V_{IN(max)}}{2}. \quad (2)$$

The required V_{TH} is easy to analyze by using Figure 4 and is calculated by

$$V_{TH} = V_{S+} \times \frac{R_{G2b}}{R_{G2a} + R_{G2b}}. \quad (3)$$

For completeness before going on, assuming the device has been set up per the foregoing, the gain from single-ended input to differential output is set by

$$G = \frac{V_{OUT\pm}}{V_{IN}} = 2 \times \frac{R_F}{R_{TH}} \times \frac{R_T}{R_S + R_T}. \quad (4)$$

Each single-ended output is half the differential output and is level shifted to V_{OCM}:

$$V_{OUT+} = V_{IN} \times \frac{R_F}{R_{TH}} \times \frac{R_T}{R_S + R_T} + V_{OCM}$$

$$V_{OUT-} = -V_{IN} \times \frac{R_F}{R_{TH}} \times \frac{R_T}{R_S + R_T} + V_{OCM}$$

Figure 4. Thevenin equivalent (V_{TH}) analysis diagram

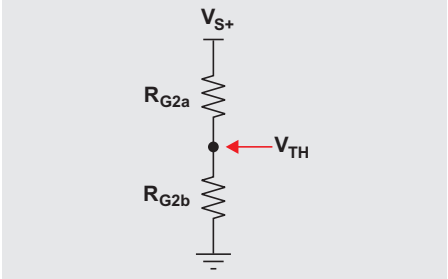
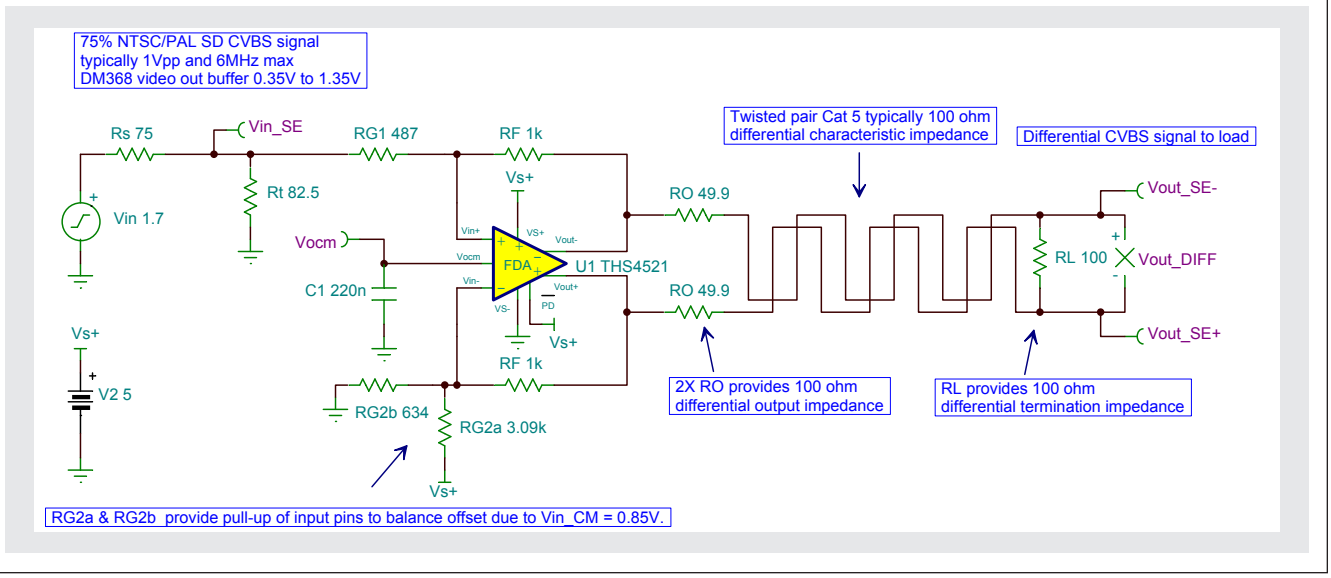


Figure 5. TINA-TI™ example circuit



To find the unique values of R_{G2a} and R_{G2b} that will satisfy the design, Equations 1 and 3 need to be rearranged and solved simultaneously. One approach yields

$$R_{G2a} = R_{TH} \times \frac{V_{S+}}{V_{TH}}. \quad \textbf{(5)}$$

This value can then be used to find

$$R_{G2b} = \frac{R_{G2a} \times R_{TH}}{R_{G2a} - R_{TH}}. \quad \textbf{(6)}$$

Calculation example for circuit #2

For this example of how to use circuit #2, it is assumed that the input signal is from the TMS320DM368, with a signal output range of 0.35 V to 1.35 V. Cat 5 cable is used, so R_O = 50 Ω and R_L = 100 Ω for double termination. The TI THS4521, an FDA with a single +5-V supply, was chosen for this example.

The THS4521 data sheet recommends that R_F be equal to 1 kΩ. To provide 75-Ω input termination and a value for G of 2 V/V (6 dB), R_{G1} can be set at 487 Ω and R_T at 82.5 Ω per Reference 2. These values can be used in the following equations to calculate the remaining resistor values.

Using Equation 1:

$$R_{TH} = R_{G1} + \frac{R_S \times R_T}{R_S + R_T} = 487\ \Omega + \frac{75\ \Omega \times 82.5\ \Omega}{75\ \Omega + 82.5\ \Omega} = 526\ \Omega$$

Using Equation 2:

$$V_{IN\_CM} = \frac{V_{IN(min)} + V_{IN(max)}}{2} = \frac{0.35\ V + 1.35\ V}{2} = 0.85\ V$$

Using Equation 5:

$$R_{G2a} = R_{TH} \times \frac{V_{S+}}{V_{TH}} = 526\ \Omega \times \frac{5\ V}{0.85\ V} = 3096\ \Omega$$

Using Equation 6:

$$R_{G2b} = \frac{R_{G2a} \times R_{TH}}{R_{G2a} - R_{TH}} = \frac{3096\ \Omega \times 526\ \Omega}{3096\ \Omega - 526\ \Omega} = 634\ \Omega$$

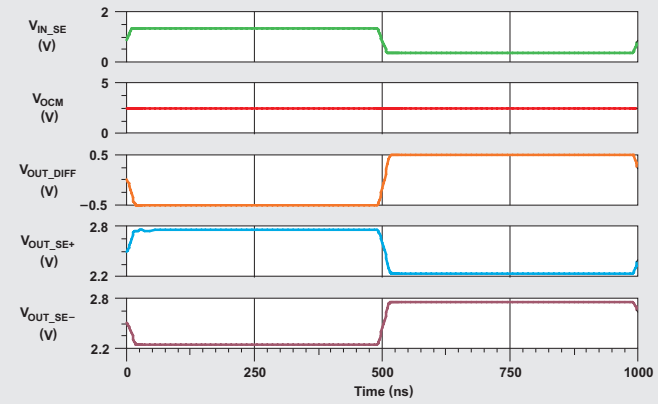
The nearest standard 1% values, 3.09 kΩ and 634 Ω, are used in the following simulation.

Simulation with TINA-TI™ software

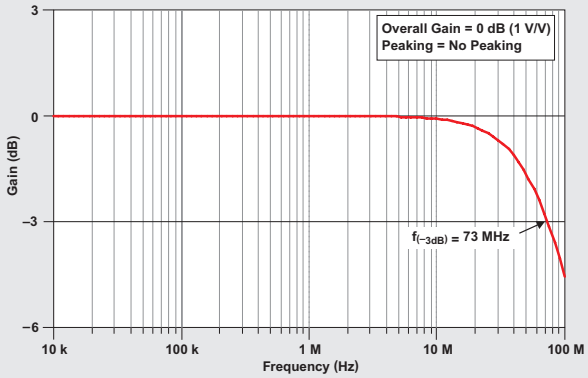
It is always a good idea to simulate a proposed circuit to catch errors and verify that any assumptions are valid. Figures 5 and 6 show the result of a transient and frequency analysis performed with TINA-TI™ software. The simulation shows no unwanted offsets in the transient response with the output level shifted to V_{OCM} = 2.5 V, and the AC frequency response shows that gain to the load is 1 V/V (0 dB) as desired.

To see the TINA-TI simulation of this circuit, go to http://www.ti.com/lit/zip/slyt427 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). If you have the TINA-TI software installed, you can open the file THS4521_SE_to_DIFF_for_Cat5_video_drive.TSC to view the example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

Figure 6. TINA-TI™ simulation results of example circuit



(a) Transient simulation with a 1-MHz square wave and V_{IN_SE} = 0.35 to 1.35 V



(b) Simulation of AC frequency response from V_{IN_SE} to V_{OUT_DIFF}

Conclusion

The THS4521 is an excellent choice for converting standard-definition (SD) or enhanced-definition (ED) video signals from single-ended to differential in single-supply applications. Table 1 shows the most stringent NTSC and PAL video-buffer requirements of SD and ED versus THS4521 specifications. The THS4521 meets them all.

The THS4521 is capable of working for this application with a supply as low as +2.5 V. This, along with its low quiescent current and power-down capability, makes it ideal for remote, portable, and battery-powered devices.

Table 1. NTSC/PAL SD/ED video-buffer requirements versus THS4521 specifications

SPECIFICATION	0.1-dB BANDWIDTH (MHz)	SLEW RATE (V/µs)
NTSC/PAL CVBS Video	6	38
NTSC/PAL ED Video	12	53
THS4521 (V_S = 3.3 V)	20	420

References

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Document Title	**TI Lit. #**
1. James Karki, "Fully-differential amplifiers," Application Report	sloa054d
2. Jim Karki, "Input impedance matching with fully differential amplifiers," *Analog Applications Journal* (4Q 2008)	slyt310

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/THS4521
www.ti.com/sc/device/TMS320DM368

TINA-TI example:
www.ti.com/lit/zip/slyt427

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www.ti.com/tina-ti

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