Current balancing in four-pair, high-power PoE applications

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Introduction

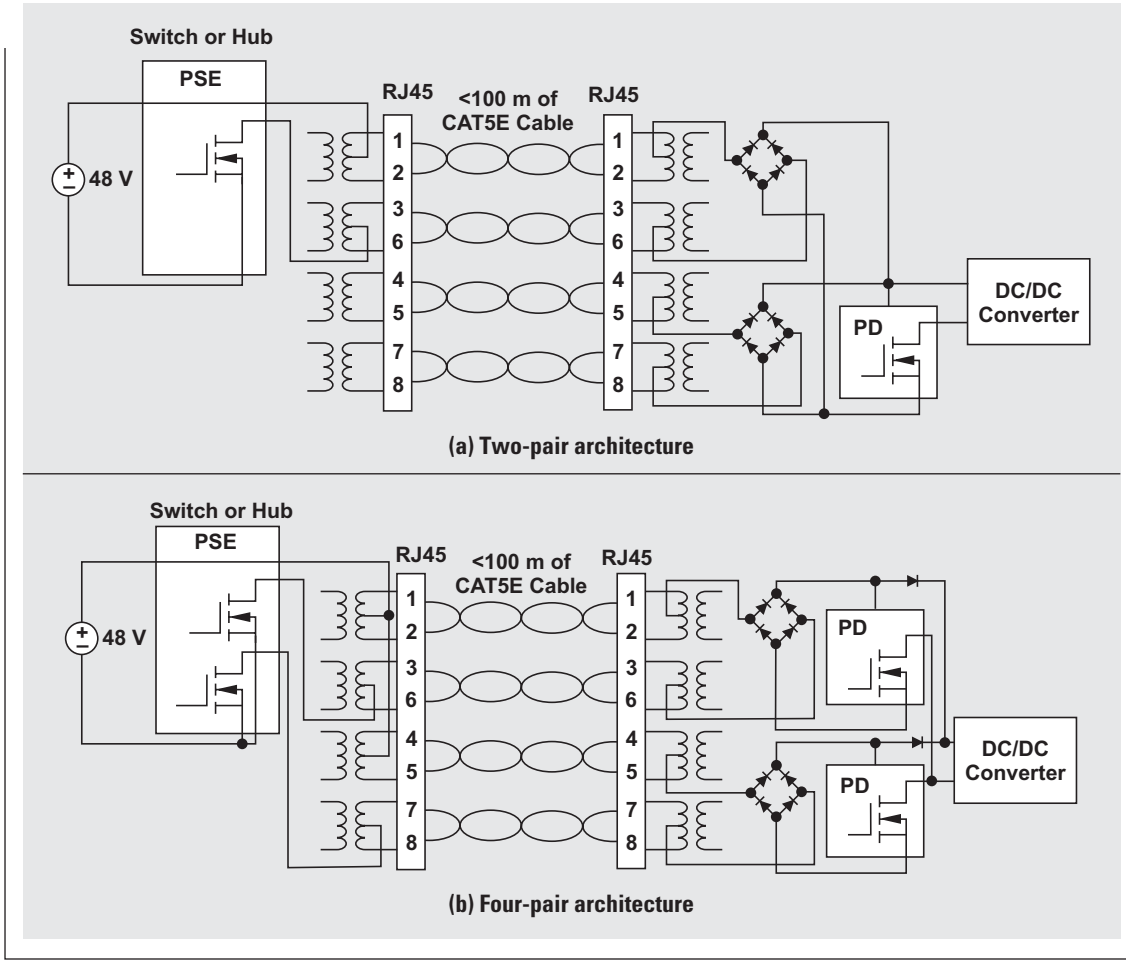
Power-over-Ethernet (PoE) parameters are specified by IEEE 802.3-2005 clause 33, which defines both the allowable architectures and the maximum deliverable power for a PoE system.[1] The present standard mandates a two-pair architecture allowing a maximum of 12.95 W at the end of the cable. As end equipment becomes more complex, it requires more power and architectures more flexible than the IEEE standard allows. This article describes a unique current-balancing technique that uses a four-pair architecture to deliver up to 50-W to the end equipment.

Review of PoE two-pair/four-pair architectures

An end-to-end PoE solution typically comprises a power source, referred to as "power sourcing equipment" (PSE), and end equipment, referred to as the "powered device" (PD). The PSE may be standalone or embedded in a router or switch. Most Ethernet cable used today is Category 5E (CAT5E) cable composed of four unshielded twisted pairs of copper.

Figure 1 shows the possible architectures that can be used to deliver power over CAT5E cable. The architecture in Figure 1a delivers power to the PD from the PSE in a single loop over two pairs of the CAT5E cable. The IEEE

Figure 1. Two possible architectures for power delivery to the PD



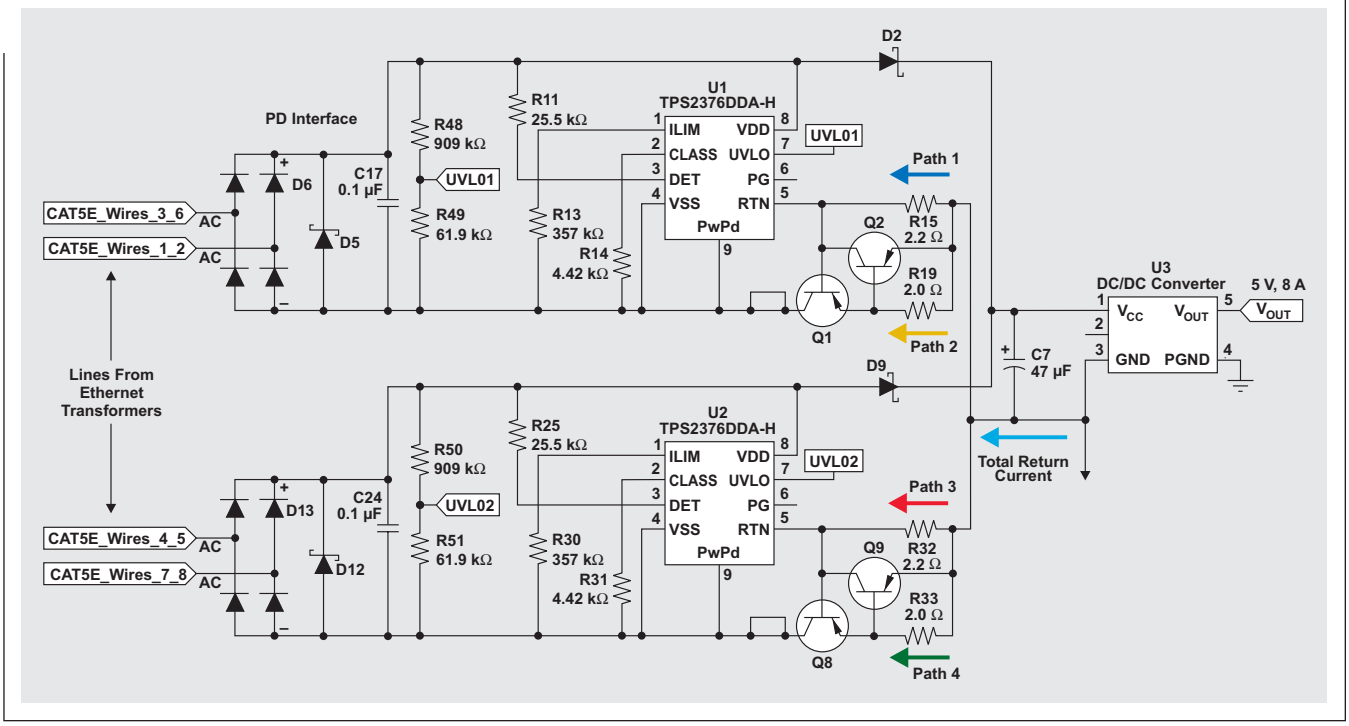
standard specifies that power may be delivered in a single loop over either of the two pairs but not over all four pairs simultaneously. Using two current loops over all four pairs, the architecture in Figure 1b increases the available power delivered to the input of the PD. The main advantage of the four-pair architecture is the increased number of conductors which decreases power loss and increases total power to the end equipment. The main disadvantages are the added cost and the increased complexity needed to ensure that the current is balanced between the two current loops.

In the four-pair architecture, both current loops feed a single DC/DC converter. If the impedances of each loop were identical, current balancing would be unnecessary and each loop would provide half of the needed input current to the DC/DC converter. However, mismatches in the wires, connectors, and components will naturally cause one loop to carry more current than the other. To ensure reliability, the series components in each current loop must be designed to handle the worst-case imbalance while maintaining data transmission. A larger imbalance implies an oversized (and thus more costly) design. Maximum power delivery can be obtained by balancing the current between the line pairs so that each path operates just below its current limit. The following design example and analysis show how the worst-case imbalance can be determined and minimized.

Design example with current-booster circuit

In a four-pair architecture, the detection and classification functions of the PD must be performed on each two-pair current loop, which necessitates the need for two PD controllers. In the design example that follows, two TPS2376-H controllers are used as the PD input source to the DC/DC power supply[2] (see Figure 2). The DC/DC power supply uses a UCC3809-2 in a single-switch flyback

Figure 2. Design example of four-pair architecture with current-booster circuit



topology to provide an isolated 5 V at 8 A to the load.

Table 1 shows the predetermined design specifications used for this design example. It is assumed that an available PSE will supply a regulated voltage between 51 and 57 V that is capable of sourcing up to 800 mA for each current loop consisting of two pairs of the CAT5E cable. A reasonable assumption for the loop impedance of each two-pair loop (maximum length of 100 m) is 12.5 Ω. The CAT5E cable will connect to the PD interface and input to the DC/DC converter that will provide an isolated 5 V at 8 A to the load. For simplicity and emphasis on the PD interface, the DC/DC power supply is shown in Figure 2 as a simple black box.

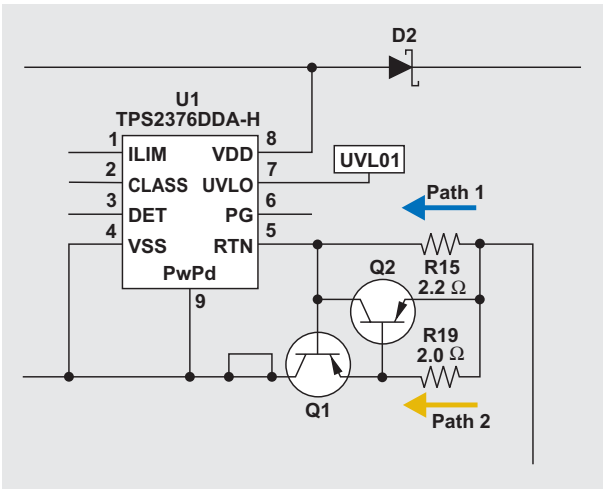
Assuming that the DC/DC converter is ~85% efficient, approximately 47 W of input power is needed. Depending on the CAT5E cable length and the PSE voltage, an input current between 0.825 and 1.2 A is required to meet the input-power specification.

The current limit of the TPS2376-H is listed in Table 1 because it is imperative that the current in either of the two current loops not exceed this value during operation to avoid unwanted shutdown. Because the minimum current limit of the TPS2376-H is 625 mA, the current-booster circuitry in Figure 3 was introduced to gain the full potential of the allowable 800 mA of input current per two-pair loop. In reality, the current is not boosted—it is merely shunted around the TPS2376-H. Figure 3 shows how the current-booster circuit works for one of the current loops. As the return current into pin 5 (RTN) on the TPS2376-H increases, the voltage drop across R15 increases, lowering the voltage between base and emitter sufficiently to turn on transistor Q1. Current through R15 will turn on Q1 when $V_{R15} > 0.7$ V. This allows Q1 to conduct and shunt a portion of the return current around the TPS2376-H. Q2 provides protection for Q1 during short-circuit and transient conditions by clamping the base of Q1 to its collector and forcing it off. Q2 will turn on when $V_{R19} > 0.7$ V, shunting some of the Q1 base current and eventually turning it off if the current continues to increase. For a more detailed explanation of this circuit, please see Reference 3.

Table 1. Design specifications

	MIN	TYP	MAX
PSE Voltage (V)	51	—	57
Impedance per Two Pairs (Ω)	—	12.5	—
Input Current per Two Pairs (A)	—	—	0.800
V_{OUT} (V)	4.95	5	5.05
I_{OUT} (A)	—	—	8.0
DC/DC Output Power to Load (W)	—	—	40
DC/DC Input Power (W)	—	—	47
DC/DC Efficiency (%)	—	85	—
DC/DC Input Current (A)	0.825	—	1.200
Current Limit (A) (TPS2376-H)	0.625	0.765	0.900

Figure 3. Current-booster circuit for one current loop



Modeling the four-pair architecture within PSPICE

To ensure that the design will current share appropriately, it is necessary to model the four-pair architecture within a simulation tool such as PSPICE. The key elements that need to be modeled are the sources of impedance in series with each current loop; i.e., the diode bridge, the CAT5E cable resistance, and the series resistances of the TPS2376-H pass FETs and booster circuitry. Table 2 correlates the actual schematic in Figure 2 with the PSPICE simulation schematic in Figure 4.

The simulation models the PSE as an ideal DC voltage source, the DC/DC power supply as an ideal DC current source, and the CAT5E cable and PD interface as the four current paths. The color-coded paths in Figure 4 correspond to those shown in Figure 2. Modeling the PSE as an ideal voltage source and the DC/DC power supply as an ideal DC current source are reasonable assumptions that simplify the simulation significantly and allow the analysis to focus on the current balancing of the CAT5E and PD circuitry.

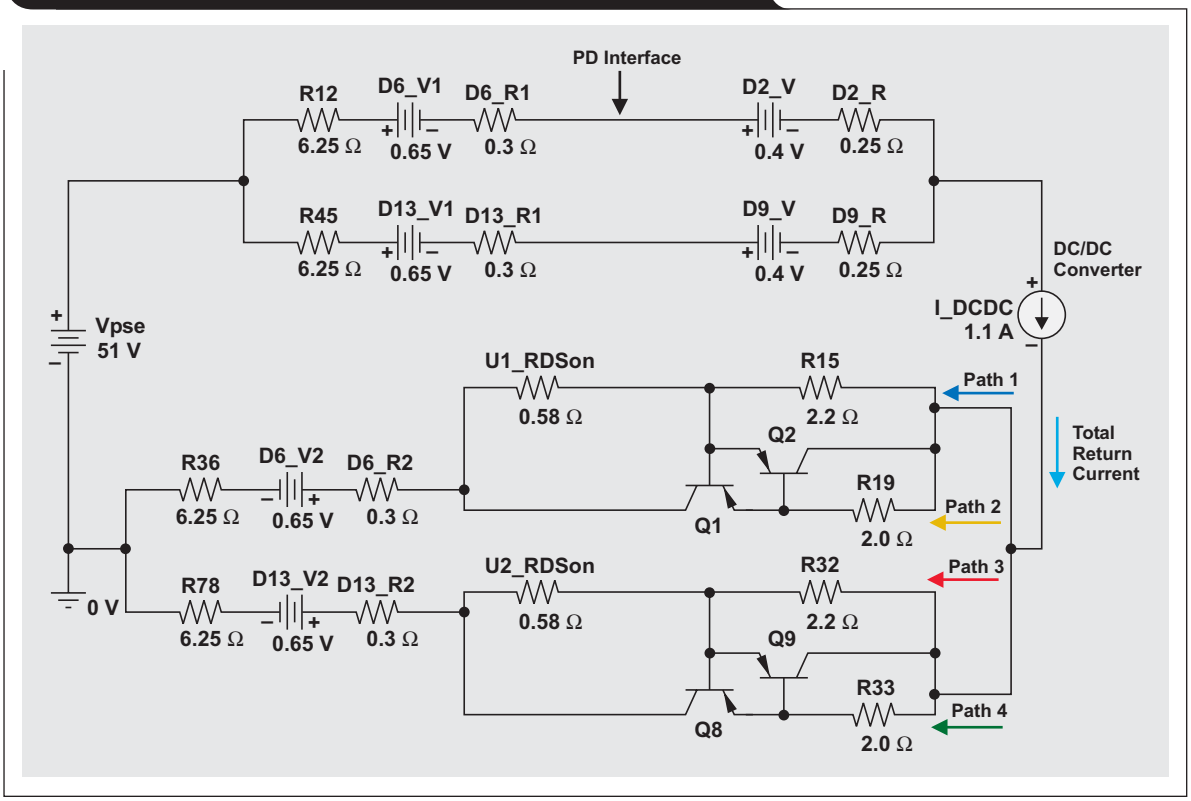
As stated earlier, in an ideal circuit the current would be equal in each current path because each path contains the same components. However, imbalances do arise because of variations in diode forward voltage drops, cable resistance, and pass FET on resistances. PSPICE allows for examination of the ideal case where matched components are used and the current in each current loop is balanced. The simulation is made by sweeping the current in the DC current source, I_DCDC, and recording the current in each of the two current loops and the power delivered to the DC current source. The power delivered to the DC current source represents the input power to the DC/DC converter. (If the efficiency of the DC/DC power supply is known, it can be multiplied by the input power to calculate the actual power to the load.) Within each current loop, it is important to make sure that the current through the pass FET of each TPS2376-H device is less than the 625-mA current-limit threshold and that the total current in either current loop does not exceed 800 mA.

A second variable that must be considered is the length of the CAT5E cable. The IEEE standard allows for a

Table 2. Modeling of four-pair architecture

ACTUAL SCHEMATIC (Figure 2)	PSPICE SIMULATION SCHEMATIC (Figure 4)
U1	U1_RDSon (pass FET on resistance)
U2	U2_RDSon (pass FET on resistance)
D6	D6_V1, D6_V2, D6_R1, D6_R2
D13	D13_V1, D13_V2, D13_R1, D13_R2
D2	D2_V, D2_R
D9	D9_V, D9_R
CAT5E cable resistance	R12, R45, R36, R78
PSE input voltage	Vpse
DC/DC power supply	I_DCDC
Q1, Q2, Q8, Q9, R15, R19, R32, R33	Q1, Q2, Q8, Q9, R15, R19, R32, R33

Figure 4. Balanced PSPICE circuit for load-share simulation



maximum of 100 m of Ethernet cable between the PD and PSE.[1] Figure 5 shows the simulation results for the corner areas of 100 m and 1 m of cable length when the model cable resistances (R12, R45, R36, R78) are modified. All simulations are done at the minimum PSE voltage of 51 V because input current is highest at this condition.

The simulation results confirm that when matched, the current loops will load share identically as Path 1 overlaps Path 3 and Path 2 overlaps Path 4. As input power increases above 25 W, the current-booster circuitry begins turning on and a portion of the current in each current loop is shunted around the TPS2376-H. The largest current handled by either TPS2376-H device is ~465 mA when the input power to the DC/DC power supply is 48 W and 100 m of cable connects the PD to the PSE. The largest current in either of the two-pair current loops is 599 mA (465 mA + 134 mA). This simulation result is acceptable because the maximum TPS2376-H current is less than the 625-mA current limit and the maximum current in either of the two-pair current loops is less than 800 mA.

Understanding sources of loop-impedance mismatch

To ensure reliable performance, it is important to understand the sources of loop-impedance mismatch so that worst-case imbalances can be entered into the simulation and analyzed. The simulation circuit in Figure 6 takes into account maximum variations in diode forward voltage, 1% resistor tolerances, and maximum pass FET on-resistance tolerances. Also, the maximum cable length resistance tolerance of 3% was used in accordance with the IEEE standard.

Figure 5. PSPICE simulation of balanced current sharing

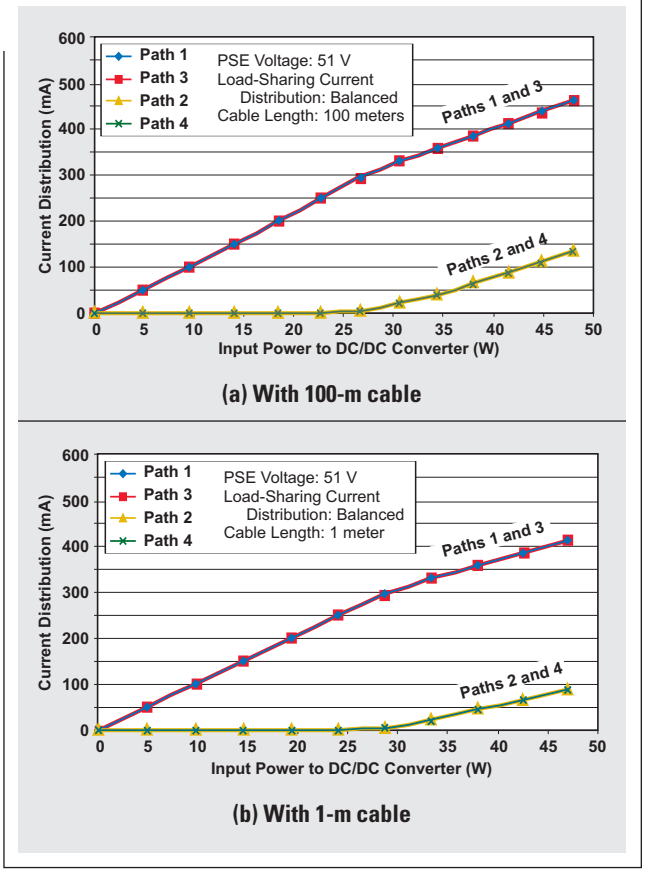
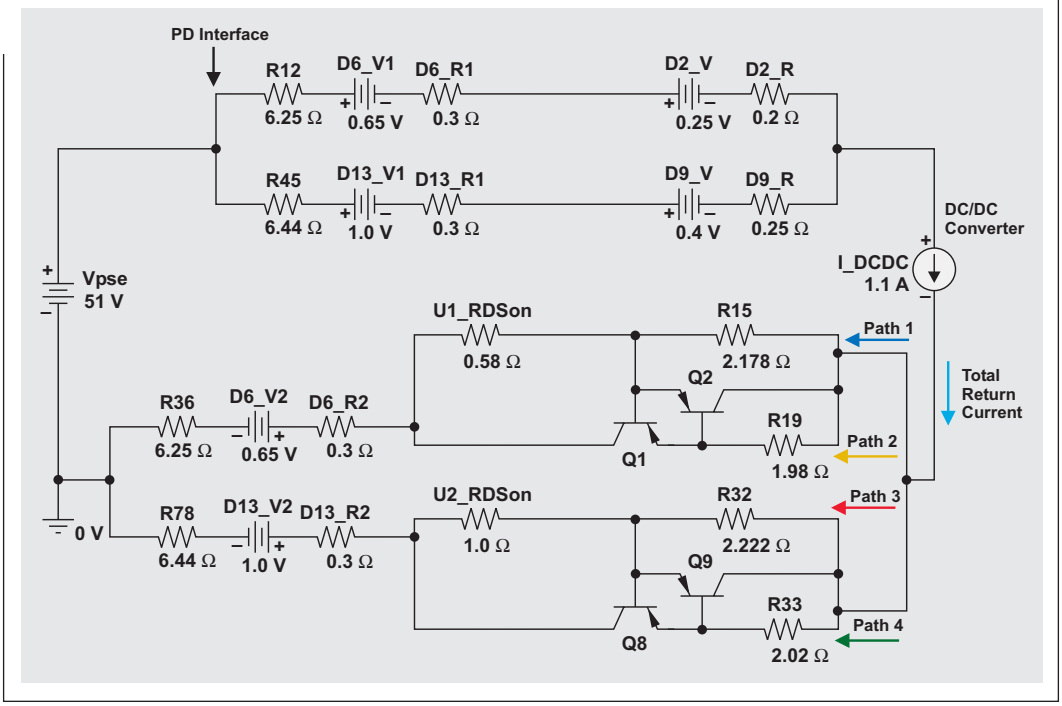


Figure 6. Unbalanced PSPICE circuit for load-share simulation



The values were adjusted so that all impedance mismatches were in one current loop, allowing for the largest imbalance. The four-pair architecture simulation previously discussed was run a second time to determine the extent of current imbalance in each current pair.

Figure 7 shows that the largest current through either of the TPS2376-H devices is 488 mA with a 100-m cable and 498 mA with a 1-m cable. The largest current available (in this example, Path 1 plus Path 2) is 640 mA with a 100-m cable and 660 mA with a 1-m cable. Because the worst-case current imbalance exceeds neither 625 mA through the TPS2376-H nor 800 mA in one current loop, the design remains within the original design specification.

Board-level results

To verify that the simulations are accurate, an evaluation board was built and tested. Figure 8 shows the current in each of the current loops when measured in an ideal lab setting at 25°C ambient temperature. These board-level results demonstrate a current imbalance through each TPS2376-H of only 10 mA (2.1%) with a 100-m cable and 1 mA (0.2%) with a 1-m cable.

To emulate worst-case conditions, the evaluation board was retested with a diode and resistor in series with the return path of the R78 current loop (Paths 3 and 4). The forward voltage drop of the diode (0.7 V) and an additional 0.5-Ω resistance were added to compensate for worst-case

Figure 7. PSPICE simulation of unbalanced current sharing

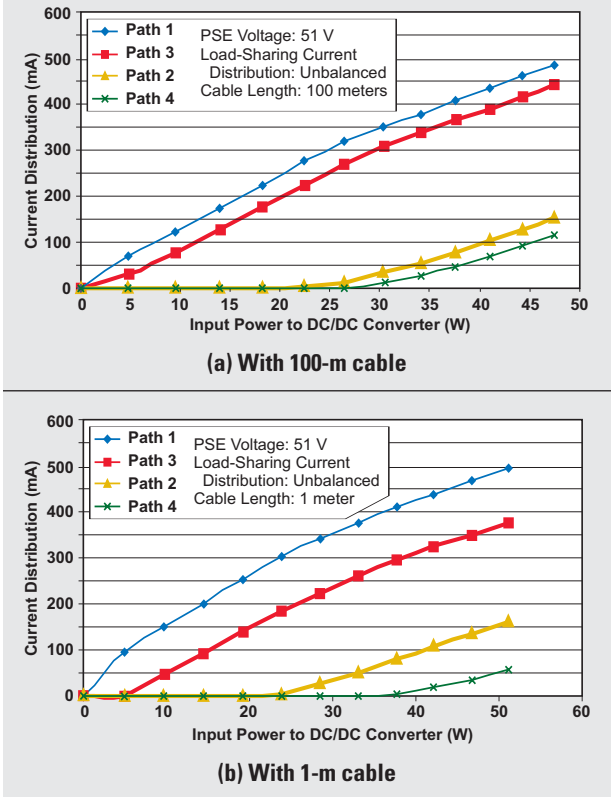
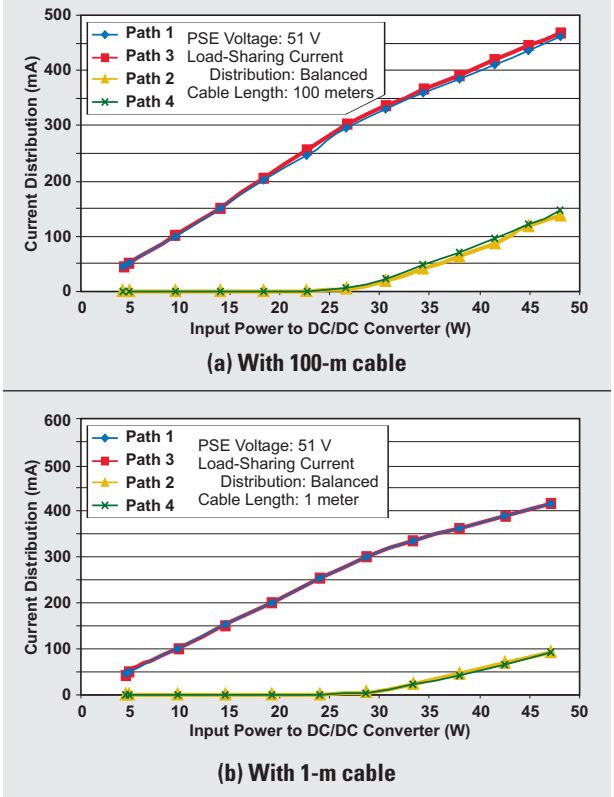


Figure 8. Board-level test results of balanced current sharing



diode forward voltage variations and system resistance tolerances. This permitted a reasonable board-level test to be conducted to measure actual current-loop imbalances.

Figure 9 shows that the largest current through either of the TPS2376-H devices is 488 mA with a 100-m cable and 484 mA with a 1-m cable. The largest current available (in this example, Path 1 plus Path 2) is 648 mA with a 100-m cable and 640 mA with a 1-m cable. Because the worst-case current imbalance exceeds neither 625 mA through the TPS2376-H nor 800 mA in one current loop, the design remains within the original design specification.

Conclusion

Overall, both simulation and board-level results confirm that the current-booster circuit will meet the initial design requirements for current balancing by keeping the return current through each TPS2376-H under its minimum current limit and under the maximum current allowable in the CAT5E Ethernet cable. The addition of the current-booster circuit improves the current balancing between the two current loops so that the wire, connector, and component tolerances do not cause the design to fall out of the design specifications.

References

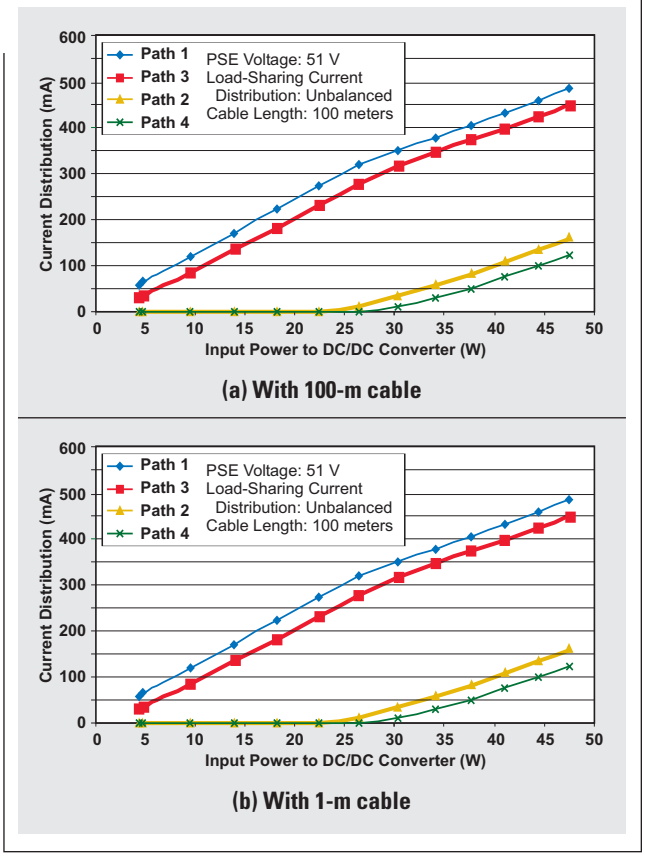
For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. IEEE 802.3 standard, http://standards.ieee.org/getieee802/802.3.html	—
2. "IEEE 802.3af PoE High Power PD Controller," TPS2376-H Datasheet	slvs646
3. Martin Patoka, "High-Power PoE PD Using TPS2375/77-1," Application Report	slva225

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS2376-H
www.ti.com/sc/device/UCC3809-2

Figure 9. Board-level test results of unbalanced current sharing



(a) With 100-m cable

(b) With 1-m cable

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